Investigations on Electronic Behavior and Stability Issues of Zinc Oxide (ZnO) based Thin-Film Transistors (TFTs)

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CERTIFICATE

This is to certify that the thesis entitled **"Investigations on Electronic Behavior and Stability Issues of Zinc Oxide (ZnO) based Thin-Film Transistors (TFTs)"** submitted by **Kavindra Kandpal,** ID. No**. 2014PHXF0601P** for award of Ph.D. of the Institute embodies original work done by him under my supervision.

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Kavindra Kandpal

Dedicated

to

My Son Devansh

ABSTRACT

As research in the area of new materials for display technology has been intensifying, a different class of semiconducting materials, i.e. oxide semiconductors, is emerging as an alternative. Among the known oxide semiconductors, Zinc Oxide (ZnO) has attracted interest for thin-film-transistor (TFT) applications because of its high transparency, nontoxicity and high electron mobility. ZnO intrinsically is an n–type semiconductor mainly due to oxygen vacancies and metal interstitial. ZnO thin films have been investigated for TFT applications such as, pixel driving and switching circuit in active-matrix display panels (AMOLEDs, AMLCDs). The operation characteristic of TFTs, however, critically depends on the physical and structural properties of the deposited ZnO film, the gate dielectric, quality of ZnO and gate dielectric interface.

To analyze physical and structural properties of the film, this thesis reports the room temperature deposition of ZnO film of different thicknesses using RF magnetron sputtering technique. For TFT applications, room temperature deposition is highly desirable as it can support wide range of substrate material. Structural and surface morphological characterization were done using X-ray Diffraction (XRD), Field Emission Scanning Electron Microscope (FESEM) and Atomic Force Microscopy (AFM) techniques, while resistivity measurement was done using Four-Probe method. ZnO films were deposited using ZnO ceramic target and Zn metallic target. In both cases, the nature of deposited film was polycrystalline and it is found that crystallinity and grain size improve with the increase in film thickness. RF magnetron sputtering with Zn metallic target provides cost effectiveness for large coating area as it results in faster deposition rate (1-1.1 Å/s) than RF magnetron sputter deposition using ZnO target (0.6-0.7Å/s). However, the ideal stoichiometry and strong *c*-axis oriented phase of hexagonal wurtzite structure of ZnO was observed when deposition is carried out using ZnO target. For ZnO deposition with Zn metallic target, XRD analysis of 100 nm and 200 nm thick

films show dominant cubic phase of ZnO along with small presence of ZnO_2, while, XRD analysis of 800 nm thick film confirms strong *c*-axis growth of wurtzite ZnO. ZnO film deposited using Zn metallic target shows higher sheet resistance ($10^{10} - 10^{11}$ Ω/□) than the ZnO film deposited using ZnO target ($10^{7} - 10^{8}$ Ω/□), which indicates that Zn metallic target deposited films were more oxygen rich.

To address the high threshold voltage and high leakage in ZnO based TFTs, a detailed investigation on high−κ dielectrics for low operating voltage and low leakage Zinc Oxide thin film transistor (ZnO TFT) was carried out using three material selection methodologies namely Ashby, Technique for Order Preference by Similarity to Ideal Solution (TOPSIS) and VlseKriterijumska Optimizacija I Kompromisno Resenjein in Serbian (VIKOR). Various material properties such as dielectric constant, conduction band offset to ZnO, band-gap and temperature coefficient mismatch of high−κ dielectric to ZnO are investigated to find out the most promising gate dielectric material. The analysis concludes that Lanthanum oxide (La_2O_3) is the most promising gate dielectric material closely followed by Hafnium oxide (HfO_2) and Zirconium oxide (ZrO_2) for ZnO based thin film transistor. The results obtained show a good agreement among Ashby's, TOPSIS and VIKOR approaches.

ZnO based TFT operates in accumulation mode. In ZnO based TFT, the threshold voltage has remained ambiguous due to existence of grain boundary traps in polycrystalline semiconducting channel. This thesis also provides analytical relationship of threshold voltage with grain boundary trap density by assuming grain boundary as continuous one dimensional line charge. The analysis concludes that for higher density of grain boundary traps, threshold voltage increases, and its effect can be minimized by employing high−κ dielectric as a gate dielectric. Further, it discusses the effect of grain boundary dominated scattering on effective mobility and concludes that the thermionic emission dominated regime in ZnO based TFT is limited to low value of overdrive voltage.

To describe the electrical characteristic of ZnO based TFT, SPICE LEVEL-3 model, which is originally defined for metal oxide field effect transistor (MOSFET), is successfully adapted as a behavioral model for ZnO based TFT. Various performance

parameters like subthreshold slope, on-to-off ratio, threshold voltage and effective mobility are described in detail. Finally, to investigate the threshold voltage instability in ZnO based TFT, fabrication of MIS-C (metal-insulator-semiconductor capacitor) structure using ZrO_2 gate dielectric is reported. ZnO based TFT exhibits counter clockwise hysteresis due to existence of oxygen vacancies in the gate dielectric which may be originated during ZnO sputtering.

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LIST OF SYMBOLS

T	Absolute temperature
D_G	Average grain size
R_a	Average roughness
E_g	Band-gap
k_B	Boltzmann constant
L	Channel length
T_0	Characteristic temperature
v_c	Collection velocity
ΔE_c	Conduction band offset
N^*	Critical concentration
J	Current density
$g(E)$	Density of states
N_c	Density of states of electron in conduction band
κ_{ox}	Dielectric constant of oxide
$\|\psi\|$	Difference of threshold voltage and flat band voltage of ZnO TFT
N	Dopant concentration
I_{DS}	Drain current
V_{DS}	Drain to source voltage
μ_{poly}	Effective grain dominated mobility in polycrystalline channel
m^*	Effective mass
μ_{eff}	Effective mobility
E	Electric field
χ	Electron affinity
n	Electron concentration

m_0	Electron rest mass
q	Electronic charge
ε_∞	Electronic part of dielectric constant
$D_{GB}(E)$	Energy dependent acceptor type DOS
E_f	Equilibrium Fermi level
S*	Euclidean distance from ideal solution
S^-	Euclidean distance from worst case solution
μ_{FE}	Field effect mobility
f	Figure of merit
β	Full width half maxima
F	Functional parameter (Ashby)
J_{GL}	Gate leakage current density
V_{GS}	Gate to source voltage
μ_{GB}	Grain boundary scattering dominated mobility
N_t	Grain boundary trap density
A*	Ideal solution (TOPSIS)
D_{it}	Interface state density
N_{it}	Interface trap charge density
Q_i	i^{th} alternative of VIKOR
G_i	Maximum group utility
ϕ_{ms}	Metal-semiconductor work function difference
R_i	Minimum regret of the opponent
$\mu_{GB\parallel}$	Mobility due to longitudinal grain boundaries
$\mu_{GB\perp}$	Mobility due to transverse grain boundaries
A^-	Negative ideal solution (TOPSIS)
N_G	Number of grains in polycrystalline channel
I_{on}/ I_{off}	On-to-off ratio
C_{ox}	Oxide capacitance per unit area

t_{acc}	Physical extent of accumulation layer in ZnO channel
ϕ_b	Potential barrier
C_i	Relative closeness of ith alternative from ideal solution
ε_r	Relative permittivity
ρ	Resistivity
A^*	Richardson constant
R_q	Root mean square roughness
μ_{sat}	Saturation mobility
S	Schottky barrier pinning factor
R_s	Sheet resistance
D_{GB}	Size of grain boundary
μ_s	Surface mobility
V_T	Threshold voltage
ΔV_T	Threshold voltage shift
g_m	Transconductance
V_{ox}	Voltage dropped across oxide
σ	Weight of maximum group utility
D_d	Width of depletion region
W	Width of the TFT

LIST OF ABBREVIATIONS

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
AMLCD	Active-Matrix Liquid Crystal Displays
AMOLED	Active-Matrix Organic Light Emitting Diodes
ATSC	Advance Television System Committee
BJT	Bipolar Junction Transistor
BLO	Backside Lift Off
BUV	Back Side Ultraviolet
CAD	Computer-Aided Design
CBO	Conduction Band Offset
CMOS	Complementary Metal Oxide Semiconductor
CNL	Charge Neutrality Level
C–V	Capacitance – Voltage
DOS	Density of States
EOT	Equivalent Oxide Thickness
FESEM	Field Emission Scanning Electron Microscopy
FET	Field-Effect Transistor
FN	Fowler Nordheim
FPD	Flat Panel Display
GB	Grain Boundary
HDTV	High-Definition Television
a–Si:H	Hydrogenated Amorphous Silicon
IC	Integrated Circuit
ITO	Indium Tin Oxide
I–V	Current – Voltage

LOCOS	Local Oxidation of Silicon
LTPS	Low Temperature Polysilicon
MADM	Multi- Attribute Decision Making
MBE	Molecular Beam Epitaxy
MCDM	Multi-Criteria Decision Making
MFP	Mean Free Path
MIS-C	Metal-Insulator-Semiconductor-Capacitor
MOCVD	Metal-Organic Chemical Vapor Deposition
MODM	Multi-Objective Decision Making
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
Δ |TEC|	Mismatch in thermal expansion Coefficient
MTR	Multiple-Trapping and Release
NBTI	Negative-Bias Temperature Instability
OTFT	Organic Thin Film Transistor
PBTI	Positive-Bias Temperature Instability
PLD	Pulsed Laser Deposition
Poly-Si	Polycrystalline Silicon
QVGA	Quarter Video Graphics Array
RCA	Radio Corporation of America
RF	Radio Frequency
SPICE	Simulation Program with Integrated Circuit Emphasis
SS	Subthreshold Slope
TCO	Transparent Conductive Oxide
TFT	Thin Film Transistor
TOPSIS	Technique for Order Preference by Similarity to Ideal Solution
TTFT	Transparent-Thin Film Transistor
VIKOR	VlseKriterijumska Optimizacija I Kompromisno Resenje in Serbian
XPS	X-Ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction

CHAPTER - 1

INTRODUCTION

1.1 Evolution of Thin Film Transistor (TFT) Technology

The evolution history of metal-oxide-semiconductor field-effect transistor (MOSFET) and TFTs are almost similar. In 1930, the concept of field effect transistor (FET) was introduced by J. E. Lilienfield [1]. On his patent "method and apparatus for controlling electric currents", he proposed a three terminal structure using copper-sulfide semiconducting layer deposited over glass substrate and aluminium foil as a gate, but oxide was absent in this structure. Later in 1935, Oskar Heil in his British patent [2] gave a description of modulation in resistance of semiconducting layer placed between two electrodes via capacitive coupling from a third electrode. However, the concept of FET took time to commercialize because it needed sophisticated fabrication techniques for reliable and reproducible device behaviour. TFTs are also essentially a kind of field effect transistor, where the modulation in current at deposited semiconducting thin film is achieved by varying vertical electric field using gate electrode.

In early days, compound semiconductors like CdSe or CdS received lot of interest for TFT applications because of their high mobility (40 $cm^2V^{-1}s^{-1}$) [3], [4]. But, because of limitation of fabrication technology, mass production of these TFTs were not realized. Meanwhile, due to the evolution of silicon technology (BJT and MOSFET), the focus shifted to developing silicon based integrated circuits (ICs) which offers enhanced performance, high reliability, reproducibility and high packing density. However, IC technology needs single crystal silicon as a substrate which is very costly and undergoes

high temperature processing. Researchers find this as a motivation and tried to look other cheaper options available for channel and substrate material, and technology to fabricate cheaper TFT in low thermal budget. So, different materials (*a*–Si:H, poly–Si, oxide semiconductors and organic material) were proposed and used to fabricate TFTs.

In 1968, Boesen and Jacobs proposed lithium (Li) doped ZnO semiconducting material as a channel layer to realize insulated gate FET structure [5]. The fabricated structure resulted in depletion type FET with $V_T = –8$ V. In 1979, one major breakthrough came as hydrogenated amorphous silicon (*a*–Si:H) TFT was fabricated in glass substrate using PECVD (Plasma Enhanced Chemical Vapour Deposition) with silicon nitride (Si_3N_4) as a gate dielectric [6]. However, the mobility of this TFT was too low to drive the pixel of OLED display. Besides this, *a*–Si:H exhibits photoconductive properties and, hence, leakage due to visible light exposure becomes a major concern. Even then, in early days, *a*–Si:H TFTs were used in LCD display for mass production due to its cost effectiveness and compatibility with existing IC technology. Later, the researchers addressed the issue of extreme low mobility (~1 $cm^2V^{-1}s^{-1}$) of *a*–Si:H TFTs and developed a method of depositing poly–Si in glass substrate which was able to obtain a mobility value as high as 360 $cm^2V^{-1}s^{-1}$ [7]. However, this process requires very high temperature (~ 600 ^{0}C) anneal for re-crystallization. Not only that, due to polycrystalline nature of deposited film, it also suffers from grain boundary scattering.

In late 1990s, a new class of TFTs named as OTFT (organic thin film transistor) was introduced. Organic thin film deposition is advantageous as it need low thermal budget and does not require costly vacuum equipment. Organic films can be easily spin coated or printed on the substrate at the room temperature. The main challenge with the OTFT is poor mobility. Though some of the OTFTs have been demonstrated for high field mobility [8], high mobility OTFT often requires a large operating voltage, that results in power consuming display panels. Later major breakthrough came as, R. L. Hoffman *et al.* demonstrated the new generation transparent TFT (TTFT) using ZnO as a channel [9]. This TFT showed an optical transmission of 75% in the visible portion of the electromagnetic spectrum. The C–V (capacitance–voltage) measurement indicated *n*–type, enhancement-mode TFT with excellent on-to-off ratio (I_{on}/ I_{off}) of 10^7, high

threshold voltage (10 – 20 V) and decent field effect mobility (μ_{eff} = 0.3 to 2.5 $cm^2V^{-1}s^{-1}$). In last decade, various breakthroughs came in ZnO based TFT technology which include low threshold voltage, improved field effect mobility and room temperature deposition. Fig. 1.1 shows the timeline of TFT technology development, using different channel materials prior to the year 2003.

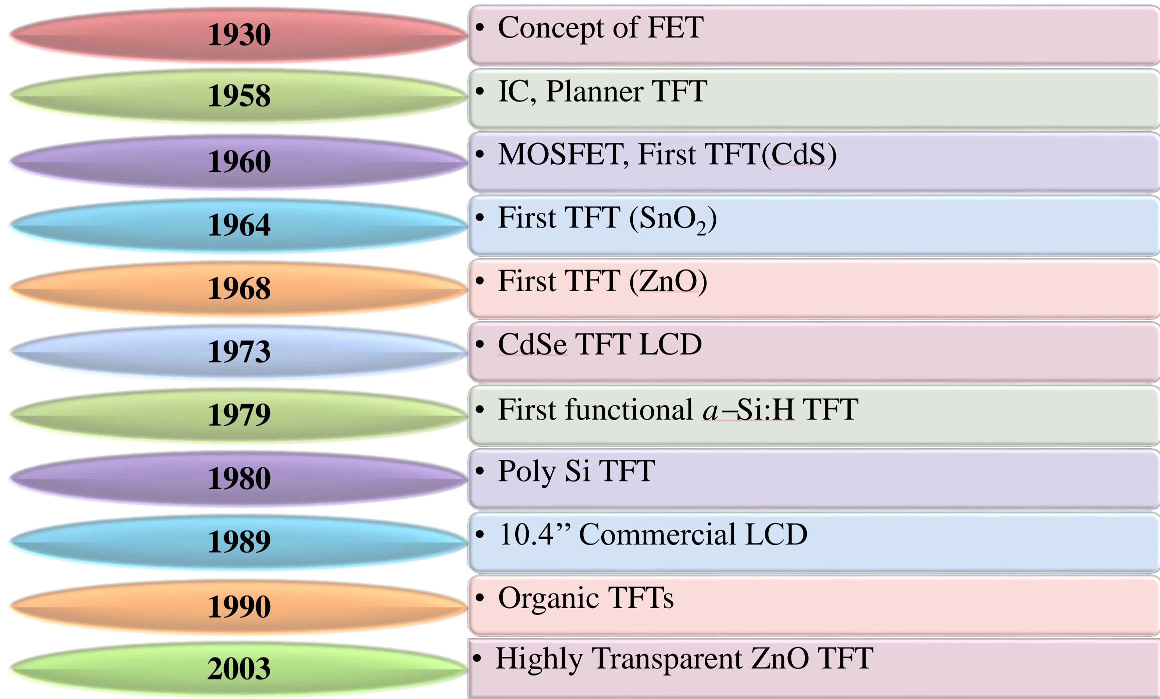

Fig. 1.1 Timeline of TFT technology development (prior to next generation ZnO TFT)

In last decade, TFT technology has been experiencing rapid transition from *a*–Si:H and polysilicon based TFT to ZnO based TFT, and because of this transition, transparent TFT has become a reality. Over the years, advancement in TFT technology has become a driving force of human civilization. The consumers which were earlier passive are now connected to each other through various electronic gadgets like laptops, tablets, phablets and smart phones due to advancement in large area electronics. TFTs are commonly used as a pixel addressing element and as a driving transistor in active matrix liquid crystal display (AMLCD) and active matrix organic light emitting diode (AMOLED) display panels [10]–[13]. Fig. 1.2 shows the use of TFT as a switching transistor (T_1) and driving transistor (T_2) in a typical pixel circuit.

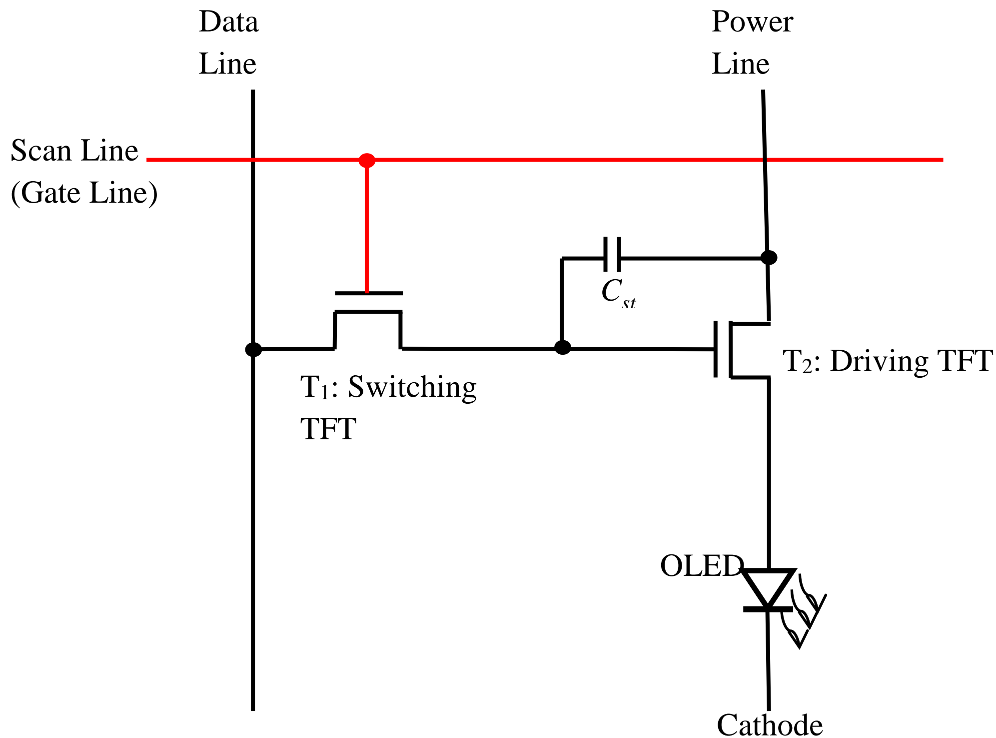

Fig. 1.2 Typical two TFT, OLED pixel driver circuit

Although, the display technologies like LCD were available for over last six decades, they were unable to compete with well-established CRT technology. In the last decade, the scenario has changed drastically due to rapid development of AMOLED and AMLCD based devices together with Micro Electro Mechanical System (MEMS) technology (especially smart phones and tablets). According to the IHS *Display Long-Term Demand Forecast Tracker*, the worldwide revenue of the TFT LCD improved from about $1 billion in 1989 to near $131.4 billion in 2014. In the same span, the technology has seen transition from *a*–Si:H TFT to ZnO based TFT. The main producers expanded from Japan to the surrounding Asia Pacific countries, such as South Korea, Taiwan, and China. Some of the key players in the zinc oxide based TFT market are Sharp Corporation (Japan), Sony Corporation (Japan), Apple Inc. (U.S.), LG Electronics (South Korea), Asus (Taiwan), AU Optronics (Japan), Samsung Group (South Korea), and Fujitsu (Japan).

1.2 ZnO TFT

In ZnO TFTs, ZnO is used as a semiconducting channel layer as it possesses high mobility and high optical transparency in visible spectrum. ZnO based TFTs provide several advantages over *a*–Si:H based TFT. First, ZnO can be grown as a crystalline material at relatively lower deposition temperature. Second, it can be deposited on various substrates made up of silicon, plastic, amorphous glasses [14] which make it possible to realize a total transparent ZnO based TFT. Moreover, because of its wide band gap, the characteristics of ZnO do not degrade in the exposure of visible light. Finally, ZnO thin film can achieve considerably higher mobility than *a*–Si:H (~12 $cm^2V^{-1}s^{-1}$, compared to 1 $cm^2V^{-1}s^{-1}$ for *a*–Si:H produced in similar conditions) [15].

ZnO TFT typically consists of ZnO channel, gate dielectric and three electrodes namely source, drain and gate. Depending upon the position of source and drain with respect to the channel, one can define TFT structures as coplanar or staggered. In coplanar structure, source and drain are on the same side with respect to channel, while in staggered structure source and drain are on the opposite side with respect to channel. Inside these, bottom-gate and top-gate structures exist depending on whether the gate electrode is on bottom or top of the structure [16]. Fig. 1.3 shows a schematic view of one of the most popular topology of ZnO TFT i.e. staggered bottom-gate ZnO TFT.

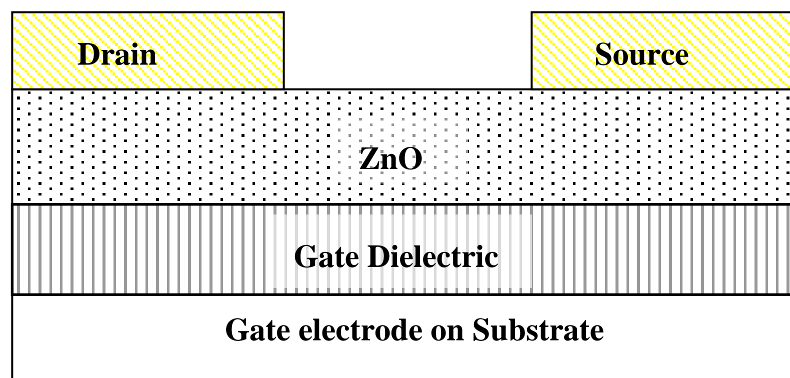

Fig. 1.3 Schematic view of bottom-gate ZnO TFT

The operation of a TFT is similar to that of MOSFET i.e. for gate to source voltage (V_{GS}) greater than threshold voltage (V_T), electron flows from source to drain through the ZnO semiconductor. However, important difference exists in TFT and MOSFET, as TFT uses cheaper substrate material like glass or plastic as a substrate whereas, MOS uses the single crystal silicon as a substrate, which accounts for higher electrical performance of MOSFET over TFT. In MOSFET, the substrate material itself serves as a channel layer whereas, in TFTs deposited semiconducting film on the substrate is used as a channel layer. Moreover, MOSFET fabrication process temperature usually exceeds 1000 ^{0}C whereas the thermal budget associated in fabrication of TFT is quite less, as it is limited by softening point of substrate. In MOSFET, at source and drain the p−n junctions are present however; in oxide TFT they are not present. Another important difference between MOSFET and TFT exist in terms of conduction mechanism. In MOSFET, current conduction is achieved after formation of an inversion layer close to the interface between semiconductor and gate dielectric while in TFT, it is achieved by formation of an accumulation layer.

In order to study the performance of ZnO based TFT, it is essential to know about the figures of merit of the device. These figures of merit are extracted from static characteristics of the TFT and are discussed in the following section.

1.3 TFT Performance Parameters

Performance of TFT is defined mainly by following figures of merit:

a. On-to-off ratio (I_{on}/ I_{off})

b. Threshold voltage (V_T)

c. Subthreshold slope (*SS*)

d. Mobility (μ).

These performance parameters are extracted from the output and transfer characteristic of TFT. Fig. 1.4 shows typical transfer characteristic (I_{DS}-V_{GS}) of low operating voltage ZnO TFT, where drain to source current (I_{DS}) is plotted in logarithmic axis.

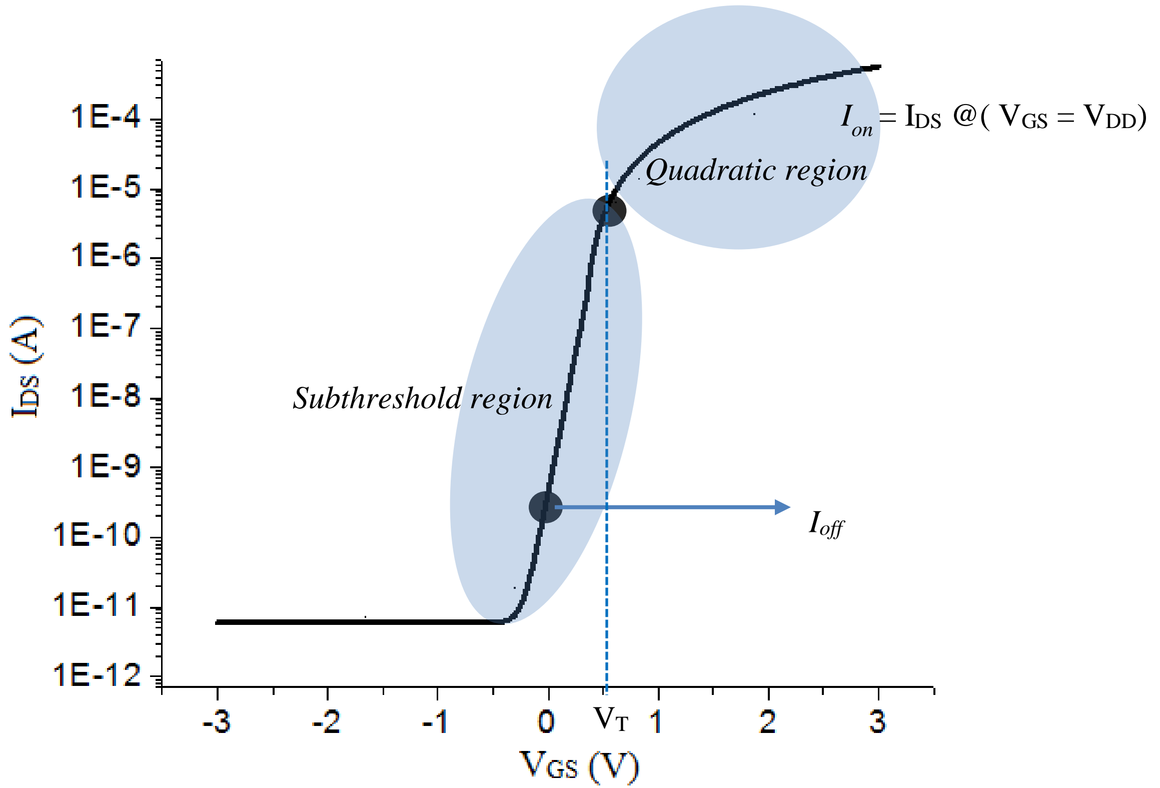

Fig. 1.4 Typical transfer characteristic of low voltage ZnO based TFT

I_{off} of a TFT is defined as the source to drain subthreshold leakage current and is measured when gate to source voltage (V_{GS}) is equal to 0 V and drain to source voltage (V_{DS}) is equal to supply voltage [17]. I_{off} determines the standby or off-state power consumption of TFT panels and its minimum value is generally given by the gate leakage current or noise level of the measurement equipment. In TFT, the on-current (I_{on}) is defined as current in saturation region when both V_{DS} and V_{GS} are equal to supply voltage. A high value of I_{on} ensures fast switching speed of a TFT. Hence, I_{on}/ I_{off} is an important performance metric of ZnO TFT, and needs to be kept as high as possible for the low power, high speed TFT applications.

Threshold voltage (V_T) in ZnO TFT corresponds to the value of gate to source voltage which can form an accumulation layer close to semiconductor dielectric interface, between the source and drain terminal. For n–type TFT, if $V_T > 0$ V then, the device is known as enhancement type device; else, depletion mode device. Usually enhancement

type device is preferred as no V_{GS} is required to turn off the transistor thereby minimizing power dissipation. However, in oxide TFTs exact estimation of threshold voltage is difficult due to structural disorder of semiconducting channel.

Another important performance parameter of a TFT is subthreshold slope (SS) (sometimes called as inverse subthreshold slope or subthreshold swing) which is a measure of necessary gate to source (V_{GS}) required to increase drain current (I_{DS}) by one decade. A smaller value of SS results in low power consumption and higher speed. SS is defined as inverse of maximum slope of transfer characteristic [16].

$$SS = \left(\frac{d \log(I_{DS})}{dV_{GS}} \Big| \max \right)^{-1} \qquad \ldots(1.1)$$

Mobility is related with the efficiency of carrier transport in a semiconductor. It affects directly the drain current and operating frequency of the TFT. In polycrystalline ZnO film, mobility is affected by several scattering mechanism like scattering at the grain boundaries, lattice vibration and ionized impurities. Moreover, since the motion of carriers is constrained to narrow region close to semiconductor dielectric interface, additional source of scattering like columbic scattering due to dielectric charge is also present. Gate field perpendicular to the channel also has a significant effect on mobility. In TFTs, mobility can be extracted from the transfer or output characteristics in several ways [18].

One way is to define mobility as effective mobility (μ_{eff}). If C_{ox} is gate dielectric capacitance per unit area and W/L is aspect ratio of the transistor then μ_{eff} can be defined in terms of conductance $(g_{ds} = \partial I_{DS} / \partial V_{DS})$ in deep triode region (low value of V_{DS}) as:

$$\mu_{eff} = \frac{g_{ds}}{C_{ox}(V_{GS} - V_T)(W / L)} \qquad \ldots(1.2)$$

The calculation of μ_{eff} includes the effect of V_{GS} on mobility. However, to compute μ_{eff} it is required to have exact value of threshold voltage V_T. Moreover, calculation of μ_{eff} is also sensitive to contact resistance due to low value of V_{DS}. An alternative way of defining mobility is by defining field effect mobility (μ_{FE}) in terms of transconductance $(g_m = \partial I_{DS} / \partial V_{GS})$ for low value of V_{DS}, and is expressed as:

$$\mu_{FE} = \frac{g_m}{C_{ox} V_{DS} (W / L)} \quad \ldots(1.3)$$

μ_{FE} is the most widely used parameter as it does not require the value of V_T and the derivative of transfer characteristic can be easily obtained. Similarly, mobility in saturation region (μ_{sat}) can be extracted from the graph of square root of drain current ($\sqrt{I_{DS}}$) vs. gate to source voltage, as:

$$\mu_{sat} = \frac{\left(\frac{d(\sqrt{I_{DS}})}{dV_G} \right)^2}{\frac{1}{2} C_{ox} \frac{W}{L}} \quad \ldots(1.4)$$

Table 1.1, illustrates the comparative analysis of various TFT. It is clear from the table that poly – Si TFT offers highest mobility. But, its performance is affected by high leakage current and very slow response (high value of SS). On the other hand, ZnO TFT offers decent field effect mobility, excellent on-to-off ratio (I_{on}/ I_{off}) and fast response. But, it suffers from the requirement of high threshold voltage (V_T). However, this can be lowered by the incorporation of high−κ dielectric as a gate dielectric and this will be discussed in detail, in chapter-4.

Table 1.1 Comparative analysis of various TFTs

Performance parameters	***a*-Si:H TFT** [19]	**Poly−Si TFT** [20]	**Organic TFT** [21]	**ZnO TFT** [22]
μ_{FE} ($cm^2V^{-1}s^{-1}$)	0.8	37	0.02	20
I_{on}/I_{off}	10^7	10^5	10^6	10^9
V_T (V)	4.5	3.4	0.7	6
SS (V/ dec)	0.5	1.10	0.17	0.14

1.4 Research Motivation and Objectives

The rate of progress of TFT technology has been quite commendable. Industry R&D activities have been aiming at improving the throughput, cost and yield of ZnO TFTs. As mentioned earlier, TFTs performance highly depends upon the ZnO film quality and its interface with the gate dielectric. ZnO based TFT provide several advantages over its *a*–Si based counterpart. However, inspite of its huge potential, in the flat panel display (FPD) market, it carries a significant number of challanges.

I. The room temperature deposition of high quality and highly uniform ZnO film is extremely important as it supports wide range of substrates including glass, plastic and silicon. At the same time, it is also important to analyze the structural and electrical properties of ZnO film, as it determines the TFT behavior.

II. ZnO TFTs primarily suffer from high threshold voltage, compared to nc–Si, poly–Si and *a*–Si-H TFT. e.g. ZnO TFT with Si_3N_4 or SiO_2 gate dielectric exhibits a very high value of threshold voltage (10 – 20 V) [23]. However, high–κ dielectric can be used as a gate dielectric to reduce threshold voltage. But, the selection of high–κ dielectric is not straightforward, e.g. dielectrics having very high dielectric constant may not have good conduction band offset to ZnO, and a high value of band offset is needed for low leakage ZnO TFT. Other criteria, which are very critical while selecting potential gate dielectric are band-gap of dielectric material (should be as high as possible), its thermodynamic stability and quality of interface. Usually dielectrics which have high value of band-gap possess low value of dielectric constant and vice versa. So clearly there is a trade- off among various material indices for selection of gate dielectric.

III. Academic research in many institutions has helped in developing the device models for the oxide TFT performance and the associated technical issues. But, each of these models has their own conditions of validity and also has limited range of applicability. In principle, ZnO TFT operates in accumulation mode as opposed to inversion mode. In accumulation mode TFTs, the threshold voltage has remained ambiguous due to existence of grain boundary traps in polycrystalline semiconducting channel. In these grain boundary traps, the carriers get trapped and due to this a very

limited number of carriers remains available in extended states at room temperature. Hence, a model for threshold voltage needs to be developed, which can introduce the effect of grain boundary trap state density in threshold voltage.

IV. All kinds of TFTs (*a*–Si:H, poly–Si, organic, oxide) suffer from threshold voltage instablity and need significant attention for improved and reliable performance. These devices can be commercially used in AMOLED and AMLCD applications successfully, only if, the reliabliy and reproducibility can be assured. The interface of ZnO with gate dielectric is very critical and needs to be optimized so that the interface state density (D_{it}) can be minimized. The ZnO – dielectric interface is also very crucial to determine subthreshold behavior of device.

V. Moreover, as most of the design engineers need computer aided design (CAD) tools compaitable SPICE models for the design of large area FPDs, it is needed to develop either a new TFT SPICE model or need to adapt existing SPICE model effectively. Though, HSPICE LEVEL–40 is customized for TFTs but its use is covered by a license [24]. This limits its adoption in early development phase of TFT technology. Adapting existing SPICE model for ZnO TFT application is a good idea but, it needs a detailed investigation so that in simulation, behaviour of ZnO based TFT can be produced with the least possible error compared to experimental characteristic.

Thus, to address the above mentioned challenges in ZnO based TFT, the following objectives of this thesis are formulated:

I. To deposit and analyze the structural and electrical properties of ZnO films.

II. To identify most suitable gate dielectric material for low threshold voltage and low leakage ZnO based TFT using material selection methodologies.

III. To develop analytical model for mobility and threshold voltage including the effect of structural disorder in channel layer.

IV. To adapt existing SPICE model for behavioral modeling of ZnO based TFT and its validation with experimental work.

V. To investigate threshold voltage instability present in ZnO based TFT using current – voltage (I–V) or capacitance – voltage (C–V) characteristics.

1.5 Thesis Organization

Chapter 1 provides an overview of TFT in general and ZnO TFT in particular. It compares TFT with conventional MOSFET and discusses the TFT performance parameters and its structure. Comparative analysis of various TFTs (*a*–Si:H, poly–Si, organic and ZnO based TFT) is done. Finally, it provides research motivation and objective of the thesis.

Chapter 2 deals with a comprehensive literature review on ZnO based TFT. It describes ZnO properties as a semiconductor and provides fabrication flow of transparent ZnO TFT. It also discusses the technological challenges on ZnO based TFT like high threshold voltage, and provides the review of transport mechanisms in ZnO based TFT. It wraps up the discussion with electrical instability in ZnO based TFTs.

Chapter 3 discusses deposition and characterization of ZnO films deposited at room temperature using RF magnetron sputtering. Two different sputtering targets, ZnO ceramic target and Zn metallic target were used for the deposition. Both types of film were well studied using structural and electrical characterization. Additionally, this chapter also provides film thickness dependent study on structural and electrical properties.

Chapter 4 presents the investigations on high–κ dielectrics for low operating voltage and low leakage ZnO TFT using three material selection methodologies namely *Ashby's approach*, *Technique for Order Preference by Similarity to Ideal Solution* (TOPSIS) and *VlseKriterijumska Optimizacija I Kompromisno Resenjein in Serbian* (VIKOR). Various material properties such as dielectric constant, conduction band offset to ZnO, band-gap and temperature coefficient mismatch of high–κ to ZnO are investigated to find out the most promising gate dielectric material.

Chapter 5 formulates an analytical model of threshold voltage as a function of grain boundary trap density, by assuming grain boundary as continuous one dimensional line charge. In the process, it discusses the thermionic emission dominated mobility model in detail. It is followed by adaption of SPICE LEVEL-3 model for ZnO based TFT and its validation. Finally, it investigates the origin of threshold voltage instability in ZnO based TFT using C–V or I–V characteristics and discusses its impact on TFT performance.

Chapter 6 summarizes the outcomes of this research and provides suggestions for future work and research direction related to the area of ZnO based TFTs.

Appendix sections **A.1** – **A.4** discuss the fabrication and characterization of ZnO / ZrO_2 metal-insulator-semiconductor-capacitor (MIS-C) structure. The characterization includes high frequency C-V analysis, I-V analysis and interface state density (D_{it}) measurement.

CHAPTER - 2

ZnO BASED TFT: LITERATURE REVIEW

2.1 Recent Development in ZnO based TFT Technology

This section reports recent development in ZnO based TFT technology. Fig. 2.1 shows major development of new generation ZnO TFT technology. In 2006, Liu *et al.* fabricated a high performance ZnO TFT on a glass substrate using RF magnetron sputtering [25]. In the same year, Park *et al.* successfully demonstrated 2.15 inch AM-OLED panel driven by ZnO -TFT in which ZnO thin film was deposited by ALD (Atomic layer deposition) technique [26]. Chiang *et al.* [27] fabricated transparent TFTs with a new set of oxide semiconductor, zinc tin oxide which is composed of heavy metal cations. The channel layer was deposited via RF magnetron sputtering and the result shows that the post – deposition annealing affects mobility and threshold voltage of device. A mobility of 50 $cm^2V^{-1}s^{-1}$ and a drain current on-to-off ratio (I_{on}/I_{off})) greater than 10^7 was obtained [27]. Kwon *et al.* [28], fabricated a Ga_2O_3–In_2O_3–ZnO (GIZO) TFT with bottom gate topology to drive 4–*in* QVGA AMOLED display. In 2014, Ma *et al.* [29] proposed high breakdown voltage ZnO TFT using ZrO_2 as the high–κ gate dielectric with ALD deposition technique and a thermal budget less than 130 ^{0}C. A 5 nm thin layer of ZrO_2 was used as gate dielectric; this transistor showed enhancement type operation with gate bias voltage less than 2 V due to high–κ dielectric.

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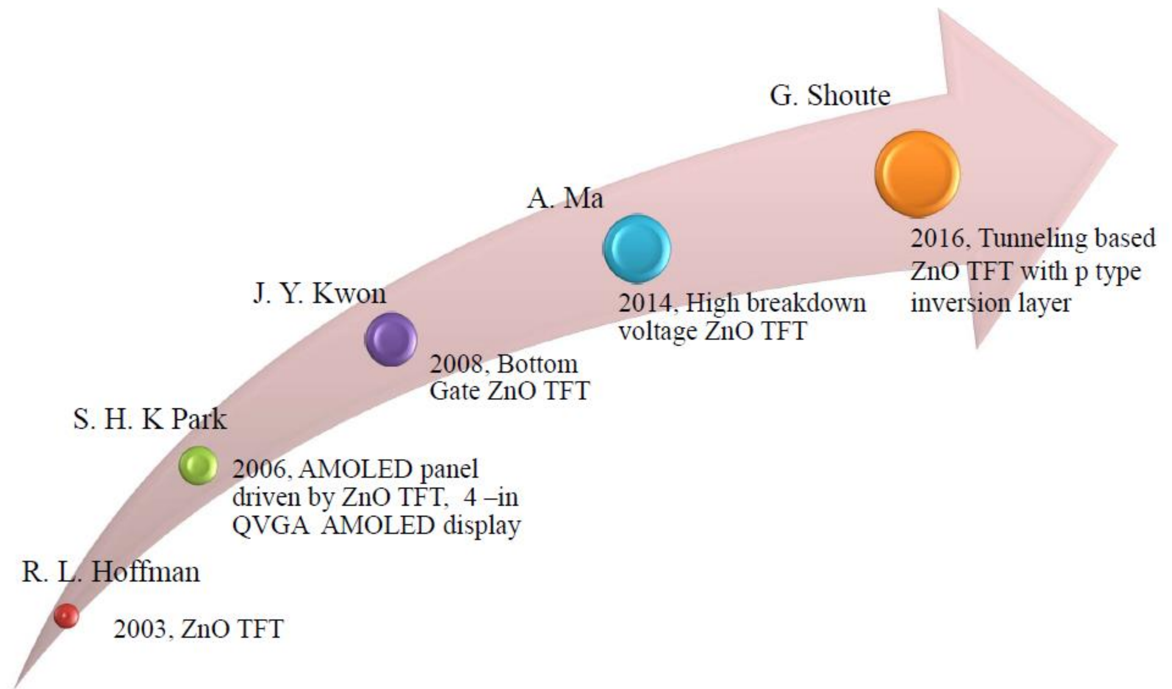


Fig. 2.1 Major development in ZnO TFT technology

In past few years, various efforts have been done for improving the device performance of ZnO TFT. In 2014, to overcome the growing demand of enhanced mobility of TFT for OLED application, Song *et al.* [30] proposed a methodology to fabricate high mobility ZnO- graphene hybrid TFT. It combines the advantage of graphene with extremely high mobility and ZnO film with high on-to-off ratio. Graphene was synthesized using thermal CVD and a 25-mm-thick Cu foil was used as a catalytic substrate for graphene growth. A dilute ZnO solution was spin-coated onto the graphene/SiO_2/Si substrate. Hybrid TFT exhibited ambipolar behavior, high on-to-off ratio of 10^5, and very high mobility of 329.7 ± 16.9 $cm^2V^{-1}s^{-1}$. The ambipolar behavior of the hybrid (ZnO/Graphene) TFT could be due to the superimposed density of states (DOS) involving the donor states in the wide band-gap of ZnO thin films and the linear dispersion of monolayer graphene. In 2015, Lee *et al.* [31] investigated thin film of zinc oxynitride (ZnON) a glassy composite of ZnO, ZnO_xN_y and Zn_3N_2 for high mobility TFTs. Fabrication of ZnON thin film involves an anion control strategy based on the substitution of oxygen with nitrogen in ZnO by adopting the argon plasma process. The

channel mobility of ZnON TFT was extracted to be 138 $cm^2V^{-1}s^{-1}$. The STEM image of ZnON material shows uniform contrast throughout the entire thin film, and this uniformity is the root cause of enhanced mobility in ZnON thin film [31]

Another major issue with TFTs are their sensitivity towards threshold voltage shift. A prolonged use or operation under excess bias can cause increased temperature of display device, which in turn, can cause significant shift in threshold voltage of pixel- TFTs. To increase the immunity of TFTs over gate bias stress, Nayak *et al.* [32] in 2015, investigated a highly stable ZnO TFT using ZnO/HfO_2 multilayer channel structure. Inserting ultra-thin HfO_2 layers between ZnO films greatly improve gate- bias stress stability compared to TFT with a single layer of ZnO. The thin HfO_2 layer acts as a passivation layer which prevents the adsorption of water and oxygen molecules in ZnO film hence improves the gate-bias stress stability of ZnO TFT [32].

Oxide semiconductors TFT have been mainly limited to n−type electronic applications because of the lack of availability of p−type oxide semiconductor. Researchers from University of Alberta, in 2016, investigated the ZnO semiconductor that is able to sustain a strong p–type inversion layer using ultra-thin high–κ dielectric constant barrier when sourced with a p–type material [33]. A ZnO film of 25 nm was deposited on a p–type (100) silicon wafer and a 4 nm thick HfO_2 high–κ oxide layer was deployed as gate insulator. The presence of ultra-thin high–κ insulator reveals the presence of enhanced tunnel current of electrons from the metal (Al/ Au), through the barrier, into ZnO. The resulting performance of this device (HfO_2/n-ZnO/p-Si) exhibited the highest reported current (63 mA/mm), and transconductance densities (56 mS/mm).

2.2 Fabrication of Bottom Gate ZnO TFT

For the fabrication of TFT, typically, glass is used as a substrate material. From 1990 to 2010, glass substrate size has been constantly enlarged i.e. up to 2.88 × 3.15 m, thus supported the large area electronics. This also corresponds to almost 6 pieces of 65 - inch TFT array patterned over the glass substrate. For fabricating top gated TFT, one can follow similar mask steps as used in MOSFET. However, for TFT isolation one doesn't need the device isolation techniques like LOCOS and trench isolation as the substrate itself is insulator. Further, in TFT fabrication the semiconducting layer and dielectric is deposited on substrate.

To fabricate, bottom gate staggered ZnO TFT, back side ultraviolet (BUV) exposure is preferred. Geng *et al.* proposed a self aligned process (where gate is defined first and with respect to gate source and drain are defined) involving BUV and five photo mask [34]. Self aligned process provides immunity to mask alignment errors. Fan *et al.* fabricated the bottom gate staggered ZnO TFT using two- mask process and backside-lift-off (BLO) scheme [35] shown in Fig. 2.2. Step – 1 shows, a Ti layer is deposited onto a glass substrate by using thermal evaporation and then it is patterned by the first photo-mask and defines the gate electrode. Step – 2 involves the deposition of gate dielectric layer and it is followed by the deposition of ZnO thin layer using RF sputtering. Step – 3 involves lithography, where the patterned gate serves as a mask for back – side UV exposure. In Step – 4, the development of photoresist is done and after the development photoresist remains over the unexposed portion. Step – 5 involves deposition of indium tin oxide (ITO) for source and drain. Step – 6 involves lift-off process and uses photoresist as sacrificial layer. Following the BLO the second photo-mask were used to define the channel width and contact region.

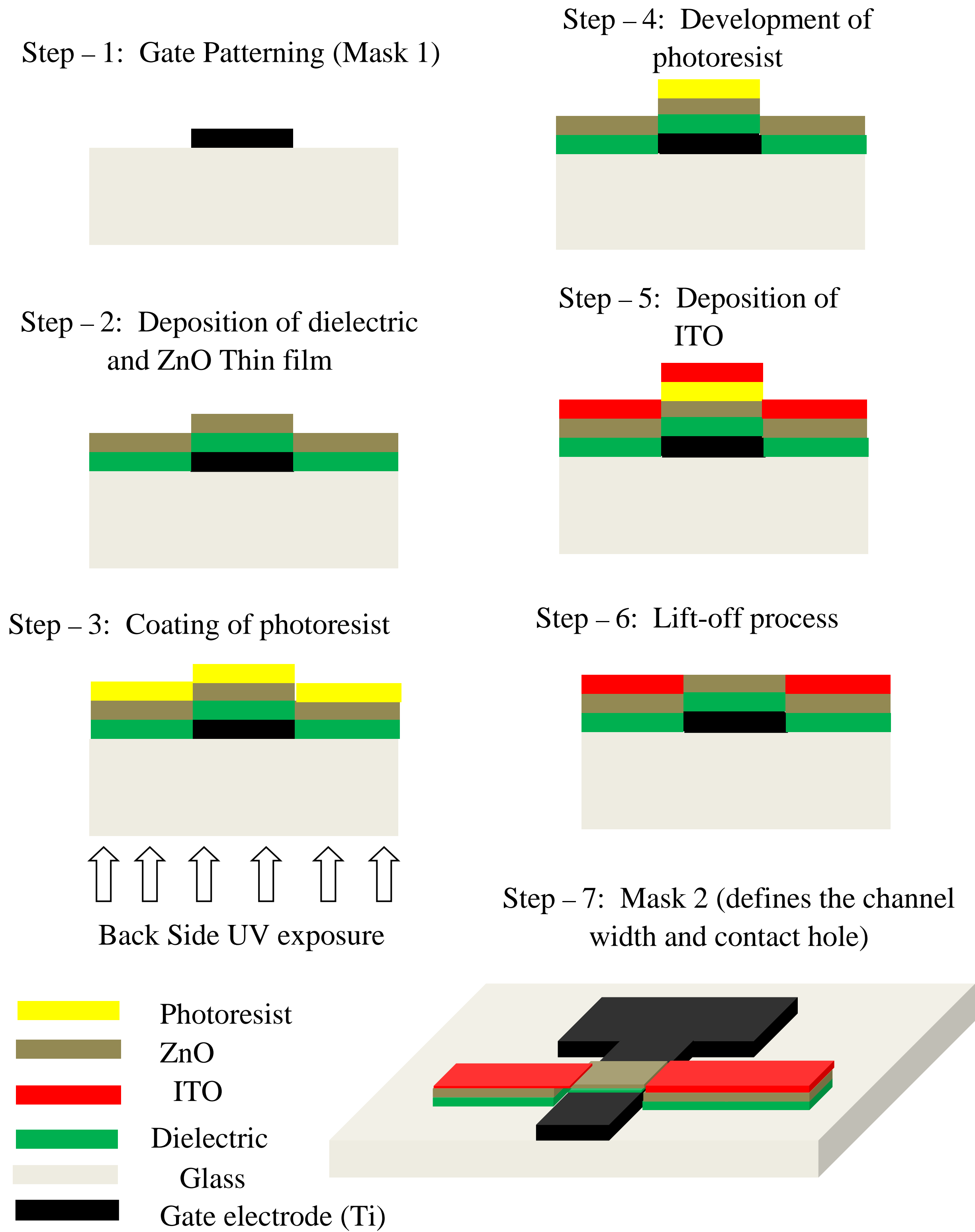


Fig. 2.2 Two-mask process flow of bottom gate ZnO TFTs with self-aligned structure

The performance of ZnO based TFT greatly depends upon structural and electrical properties of ZnO films. Similarly, choice of gate dielectric is highly important as it determine operating voltage and gate leakage of TFT. The next subsections discuss about, ZnO as a semiconductor and various gate dielectrics for ZnO TFT.

2.2.1 ZnO Semiconductor

ZnO is a wide band-gap (3.4 eV), *II-VI* compound semiconductor, having a wurtzite structure (most stable) with lattice spacing a = 0.325 nm and c = 0.521 nm [14], [15]. The crystal structure of ZnO material is shown in Fig. 2.3. The zinc (Zn) atoms are tetrahedrally co-ordinated to four oxygen atoms, with the oxygen atom occupying the octahedral sites. Intrinsically, ZnO is an n–type semiconductor primarily due to presence of intrinsic native defects (oxygen vacancies and Zn interstitials). Hydrogen is considered as main cause of n–type doping in undoped ZnO. The Zn interstitials acts like a shallow donor which constitutes the donor level just below the bottom of conduction band, while the oxygen vacancies act like a deep donor.

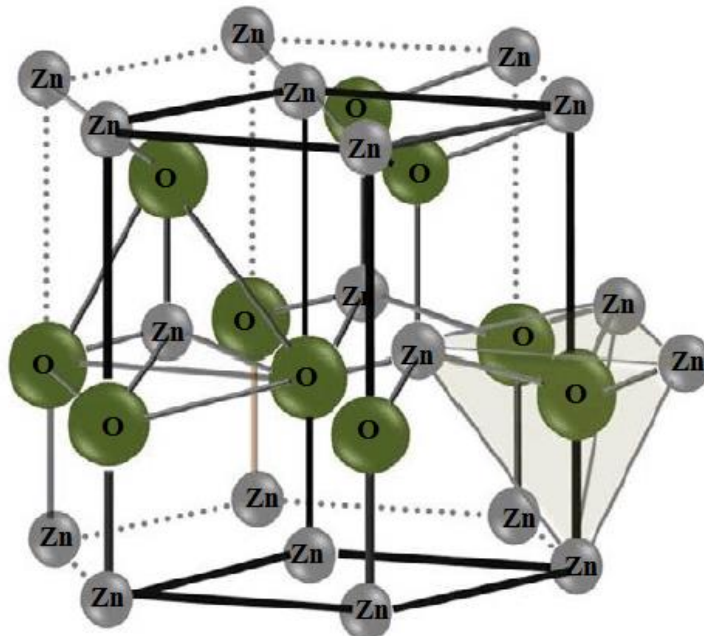


Fig. 2.3 ZnO crystal structure

Table 2.1 lists various material parameters of ZnO semiconductor [36]. ZnO is promised to be an attractive material for numerous applications in electronics, photonics, sensing and acoustic [37]. The primary applications of ZnO lie in the area of Transparent TFT owing to its high conductivity and high optical transparency and in the area of photonics as an optical emitter due to its high exciton binding energy (~ 60 meV). Another promising area of ZnO is acoustic wave devices mainly due to its large electrochemical coupling along *c* axis. One emerging application area of ZnO is its possible use as a transparent conductive oxide (TCO). As the world is facing the shortage of the growing demand of indium for ITO, ZnO is promised to be the alternate TCO because of its good conductivity, excellent surface smoothness, low deposition temperature, high optical transparency and good etching chemistry [37]. A great deal of research is being carried out in ZnO nanostructures like ZnO nanowires, nanobelts and their integration with mainstream semiconductor like Si, GaAs and GaN. High crystalline quality and good charge carrier property are the main reason driving its use as nanoscale devices [Photodetectors, Lasers, Surface acoustic wave device (SAW)].

Table 2.1 Material parameters of ZnO

Parameter	Value
Density	5.606 gcm^{-3}
Stable phase @ 300K	Wurtzite
Melting point	1975^0 C
Band-gap (E_g) @ 300K	3.4 eV
Relative permittivity of ZnO (ε_r)	8.12
Refractive Index	2.008
Hall mobility (μ_H)	150 $cm^2V^{-1}s^{-1}$
Electron affinity (χ)	4.6 eV
Charge neutrality level (CNL) from vacuum level	3.27 eV
Exciton binding energy	60 meV
Effective mass of electron in conduction band	0.318 m_o
Effective mass of holes in valence band	0.5 m_o

where m_o is electron rest mass.

ZnO semiconductor is commonly doped with group III elements like aluminum (Al), gallium (Ga) and indium (In) to make it n–type. However, obtaining a stable p–type behavior in ZnO semiconductor is still a challenge. To achieve the projection of thin film technology by Nikki asia [38] such as, CMOS ICs using oxide TFT, one need stable p–type ZnO semiconductor so that CMOS realization (where both n–type and p–type FET are present) will be possible. p–type ZnO can also facilitate the material for light emitting devices emitting in UV region because of its high exciton energy. Though researchers have achieved limited success in obtaining stable and reproducible p–type ZnO, the widespread fabrication of ZnO homojunction p–n junction LED is still a challenge. To obtain reliable p–type ZnO, one needs to minimize the high donor defect density. Researchers have used N_2 for the same purpose, in which N_2 passivate the interface trap formed by oxygen vacancies. A very low p–type dopant concentration was obtained (~ 10^{16} cm^{-3}) [39]. If wide band gap semiconductor like ZnO are doped with high dose of acceptor impurities, it can results in localization of carriers, thereby unable to modulate the conductivity of ZnO film. A polycrystalline ZnO doped with 10% Mg and 2% P were used to fabricate the enhancement type ZnO TFT [40]. Mg doping increases the band gap of semiconductor therefore increase the activation energy for the donor like defects, hence compensating n–type doping.

It was reported that ZnO thin films can be grown by various growth technique like RF sputtering [41], metal organic CVD [42], molecular beam epitaxy (MBE) [43], and pulsed laser deposition [44]. The various methods for fabricating ZnO TFTs and reported electrical characteristics are summarized in Table 2.2. From the list of parameters mentioned in the table, mobility and on-to-off ratio is hugely impacted by film quality and hence fabrication technology and its controlling parameters. However, the threshold voltage is mainly influenced by the dielectric constant and thickness of gate dielectric. RF sputtering is the mostly used fabrication technology for ZnO TFT due to its room temperature processing as it enables compatibility with wide variety of substrate. The only disadvantage in this process is use of high vacuum equipment.

Table 2.2 Performance characteristics of ZnO based TFTs with various fabrication techniques

Deposition method	References	Max. Processing temperature (^oC)	Mobility ($cm^2V^{-1}s^{-1}$)	on-to-off ratio (I_{on} / I_{off})	Threshold Voltage (V)
RF sputtering	[45], [46]	R.T.	16.3 – 20	6.4×10^4 – 2×10^5	2.8 – 21
PLD	[40], [47]	500 – 600	2.3– 5.32	10^4 – 1.5×10^8	1.2 – 3
Sol- gel	[23]	700	0.2	10^7	10 – 20
ALD	[48]	150	6.7	9.5×10^7	4.7
Spray pyrolysis	[49]	400	54	10^7	----

2.2.2 Gate Dielectric

The performance and stability of ZnO TFT hugely depends upon the deposited gate dielectric. ZnO based TFT suffers from high threshold voltage requirement. However, high–κ gate dielectric can solve this problem easily. To achieve effective coupling between gate electrode and semiconductor surface, one needs either high–κ dielectric or needs thin gate dielectric layer. However, a thin dielectric layer can lead to considerable amount of gate leakage, hence the use of high–κ dielectric is the only choice after a certain limit of dielectric layer thickness. Moreover, most of the display applications need high current driving capacity of driver TFT to drive the OLED pixel. Hence, one needs higher oxide capacitance (C_{ox}), as current is directly proportional to C_{ox} and this can be achieved effectively by high–κ dielectric. Most of the high–κ dielectrics faces mainly two issues: first, high–κ dielectric usually have lower band gap which leads to low breakdown voltage and second, they exhibit polycrystalline structure and a rough surface which results in less reliability and degraded interface quality. In literature ZnO interface is studied with various high–κ dielectrics such as: HfO_2, ZrO_2, La_2O_3, Y_2O_3 and $BaTiO_3$

[50]–[53]. All these dielectrics have their own merits and demerits over others when used in ZnO TFTs, e.g. $BaTiO_3$ has a very high value of permittivity (κ = 2000) but has a very poor value of conduction band offset (– 0.45 eV). On the other hand, Al_2O_3 has very low value of permittivity (κ = 9) but has a very good value of conduction band offset to ZnO (3.3 eV). Other criteria, which are very critical while selecting gate dielectric, are band-gap of dielectric material and its thermodynamic stability.

2.3 Transport Model of ZnO TFT

The adequate knowledge of transport mechanism through ZnO semiconductor is essentially required to analyze the electrical behavior of ZnO TFT. In ZnO polycrystalline channel, one needs to understand the current conduction mechanism through grain and grain boundaries. The two most popular models that explain the transport mechanism are: *Hossain's model* and *Multiple Trap and Release model* (MTR model). These models are presented in next subsections.

2.3.1 Hossain Model

Hossain *et al.* [36], proposed model for current conduction in ZnO TFTs by assuming the defects in crystallite and the ZnO gate dielectric are localized in grain boundaries (GBs), with a peak density at the mid gap. The value of characteristic decay energy of Gaussian distribution constant E_1 and E_2 of the defects in the GB are assumed material constant [36]. The polycrystalline thin film of ZnO is defined by equally spaced GBs parallel to ZnO film thickness and perpendicular to direction of carriers. The GB is modeled as a thin layer having acceptor and donor type states with Gaussian distribution as:

$$N_{ga}(E) = N_{ta} \exp\left\{-[(E_{1a} - E)/E_{2a}]^2\right\} \quad \text{…(2.1)}$$

$$N_{gd}(E) = N_{td} \exp\left\{-[(E - E_{1d})/E_{2d}]^2\right\} \quad \text{…(2.2)}$$

where *a*, *d*, *g* stands for acceptor like states, donor like states and Gaussian distribution. E and $N_g(E)$ are the trap energy inside the band gap and corresponding

density of defect states respectively. N_t is the total density of trap states. According to this model, the Poisson's equations, to define the potential profile across the ZnO Channel and in GBs can be written as:

$$\frac{\partial^2 V}{\partial x^2} = -\frac{q(n - p - N_d^+)}{\varepsilon_{ZnO}} \qquad \text{for crystallite region…(2.3)}$$

$$\frac{\partial^2 V}{\partial x^2} = -\frac{q(n - p - N_d^+)}{\varepsilon_{ZnO}} + \frac{q(n_a - n_d)}{\varepsilon_{ZnO}} \qquad \text{for GB region…(2.4)}$$

where *n, p*, are electron and hole density respectively, N_d^+ is ionized shallow donor density and the $(n_a - n_d)$ are the net negative charge in GB. These charges are responsible for depletion of neighboring electrons from the GB. The resulting barrier of height ϕ_b (Fig. 2.4) is the main obstacle for the carriers to transport through ZnO channel.

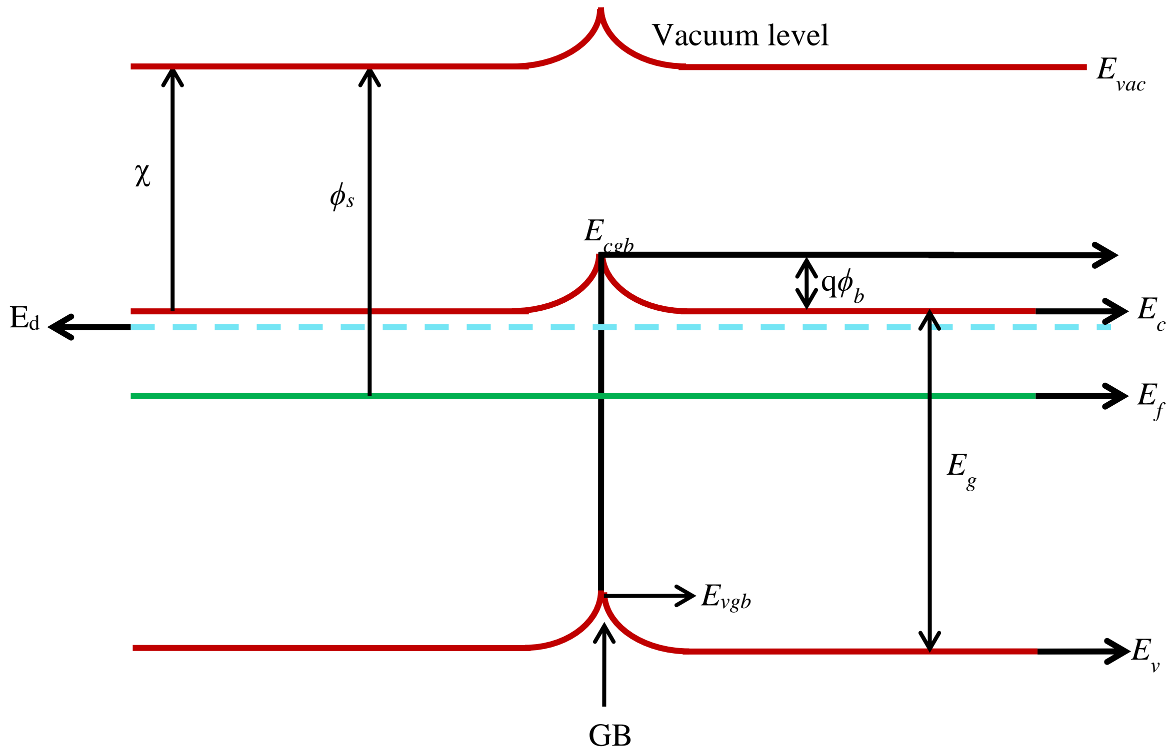


Fig. 2.4 Energy band diagram of ZnO channel in the presence of grain boundary

Mainly, two different transport mechanisms are utilized for the defect free grain region and GB. Drift and diffusion mechanism are responsible for the current conduction through grain while thermionic emission is utilized for current conduction over grain boundaries. If applied field across the channel is $\vec{E}$ then electron current density $\vec{J}$ equation for the defect free region can be written as:

$$\vec{J} = qn\mu\vec{E} + qD\nabla n \qquad \ldots(2.5)$$

where q, n, μ, D, and ∇n are the electron charge, electron concentration, mobility, diffusion coefficient and electron concentration gradient respectively. Electron current density in the GB of barrier of height ϕ_b due to thermionic process can be written as [36]:

$$\vec{J}_{gb} = A^{*}T^{2}\frac{n}{Nc}\exp\left(-\frac{q\phi_b}{k_B T}\right) \qquad \ldots(2.6)$$

where N_c is the density of states for electron in conduction band, A^* is the electron Richardson constant, T is the absolute temperature, k_B is Boltzmann's constant and n is electron density which is given as: $n = N_c \exp[-(E_c - E_f)/k_B T]$ where E_f is equilibrium Fermi level and E_c is the energy of conduction band. This model is used to calculate the potential profile for single grain boundary and multiple grain boundaries for ZnO TFT. However, this model has several limitations such as**,** it considers current through grain boundary only due to thermionic process, and ignore the impact of drain to source voltage on barrier height, which can surpass the barrier for certain V_{DS} and the mechanism of carrier transport will be governed by drift and diffusion.

2.3.2 Multiple- Trapping and Release (MTR) Model

Torricelli *et al.* [54], proposed the multiple-trapping-and-release (MTR)-transport model to describe the transport mechanism in ZnO TFTs. At low disorder levels, the localized states are mainly at the band edges and as the disorder increases the localized states move further into bands. This physical scenario is described conventionally by density of states (DOS). The MTR model formulates density of states for acceptor like states with respect to conduction band edge (E_c) using double exponential DOS given by

$g(E)$ as:

$$g(E) = N_{deep} \exp\left(\frac{E - E_c}{k_B T_{deep}}\right) + N_{tail} \exp\left(\frac{E - E_c}{k_B T_{tail}}\right) \qquad \ldots(2.7)$$

where, T_{deep} and T_{tail} are characteristic temperature of deep and tail states whereas, N_{deep} and N_{tail} are deep and tail states at the conduction band edge respectively. In ZnO the shallow states arises from metal interstitials and deep states arises mainly from oxygen vacancies. The shallow traps in ZnO introduce a distribution of localized energy levels over the valance band edge and under the conduction band edge.

Fig. 2.5 illustrates the MTR model, a charge carrier (shown as filled circle) from the conduction band (CB) is trapped into localized site in the gap, after thermal excitation it can be free to move or return to extended state. In MTR model, the very first assumption for the release mechanism is that trapped carriers are activated by thermal excitation. It also assumes that charge carriers near a trap site are trapped instantaneously with a probability close to one. The carriers in extended states are responsible for charge transport. The MTR model is also being successfully used to explain transport in *a*–Si and poly–Si with small sized grains.

MTR model was used to define transport properties of ZnO TFT deposited by spray pyrolysis, over wide range of temperatures, biasing condition and at different channel lengths. It is observed that ZnO TFTs field-effect mobility (μ_{eff}) increases with carrier concentration and is temperature activated. Transport properties are strongly influenced by the tail states, extended in a wide range of energy in the band-gap of ZnO.

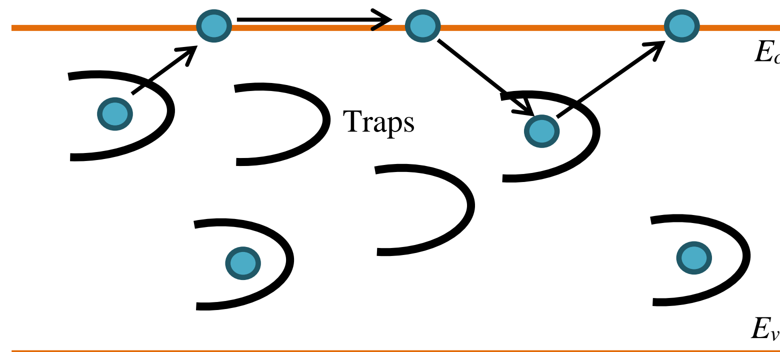


Fig. 2.5 Multiple- tapping and release mechanism

2.3.3 Other Device Models

The performance of ZnO TFT is largely influenced by trap densities and grain boundaries at the interface. GBs act like a trap centers and induce a barrier, which in turn reduces mobility in the channel. M. Kimura [55], in his model assumed, uniformly distributed trap centers in the ZnO film. Their study clarifies that the main reason of trap densities is the presence of donor like trap states which originates from Zn antisites and Zn interstitial. These defects can be minimized with optimization of deposition techniques and with proper choice of underneath surface. Kawasaki *et al.* [56], presented a model considering the grain boundary effects in the ZnO nanocrystalline (nc) thin film. The significant differences between device modeling of the nc–ZnO TFT and the poly–Si TFT can be pointed out as:

1) In nanocrystalline ZnO thin film, the developed depletion region around closely spaced grain boundaries overlaps to make potential profiles in the film different from that of poly-Si thin film.
2) Due to probable existence of deep level traps in GBs and wide band-gap (E_g) of ZnO, the GB barrier height modulation with applied gate bias for ZnO TFTs will be different from that of poly-Si TFTs.

Hai-Xia *et al.*[57], reported a model for the density of states (DOS) and carrier transport in a poly–ZnO TFT. The GB was modeled as a thin semiconductor layer with defect states parallel to the transverse electric field, with the assumption that the regions on both sides of the GBs were completely defect-free. The DOS, $g(E)$ was described as a combination of four components; a) an acceptor–like exponential band tail function, b) a donor–like exponential band tail function c) an acceptor–like Gaussian deep state function, and d) donor–like Gaussian deep state function.

2.4 Electrical Instability in ZnO based TFT

ZnO based TFTs are recognized as one of the potential candidates for next-generation active addressing devices (a TFT array to switch on or off pixels) for flat panel display (FPD), therefore many research groups are focusing on improving ZnO – dielectric

interface. A change in threshold voltage largely influences the life of an AMLCD display as a shift can cause insufficient driving current to the pixel which in turn results in a dark pixel. Lesser the shift better is TFT. TFTs are sensitive to threshold voltage shift when subjected to voltage stress and illumination stress. In dielectric and the dielectric semiconductor interface, four types of charges exist, namely fixed oxide charge, mobile ion charge, trapped oxide charge and interface trap charge. Fixed oxide charge and trapped charge cause the capacitance-voltage (C–V) characteristic of transistor to have translational shift. Mobile ion charges (Na^+ and K^+) are responsible for hysteresis in C–V characteristic as these charges are pushed away in positive bias sweep and pulled back in negative bias sweep. For positive ions, the hysteresis is counter clockwise. Oxide charges are the charge trapped in oxide sites; usually carrier excited from semiconductor into the dielectric is main reason of it. Oxide charges results in shift of C–V profile and are main contributor to unstable device. The interface trap charges are present at dielectric – channel interface and limits the transconductance (g_m) and switching speed of TFT. Moreover, extreme value of interface trap charge density can also results in Fermi level pinning.

Prolonged operation under electrical stress is also responsible for threshold voltage instability. Under electrical stress tunneling of electron or holes, into and through a gate dielectric can cause "defects" to be generated within the dielectric layer and/or at ZnO – dielectric interface. Higher the electrical stress more will be the probability of defect creation. These defects can take form of electron traps, hole traps, interface states, trapped electron and trapped holes [17]. These trap centers determine time dependent behavior of the threshold voltage and tunneling current. As shown in Fig. 2.6, when positive bias is applied at the gate electrode, accumulated electron can undergoes Fowler –Nordheim tunneling (process 1) or trap assisted tunneling (process 2). However, if dielectric is thin enough, direct tunneling will also be present. As electrons tunnel through gate dielectric then there is a probability that some of the electrons gets trapped in these defect sites. These occupied states now modify the dielectric electric field. Electric field near to anode (gate) is increased, while field near to cathode (channel) is decreased. In other words, trapped electrons in defect sites partially screen the applied

electric field so that the net gate voltage appears to be smaller. The condition become worse when hole generation, injection and trapping also takes place. In this process electron goes through FN tunneling and then travels through conduction band of dielectric, and if the voltage drop across gate dielectric is more than the band-gap of gate-dielectric, then electron can gain enough energy to cause impact ionization. These generated holes can be trapped in gate dielectric.

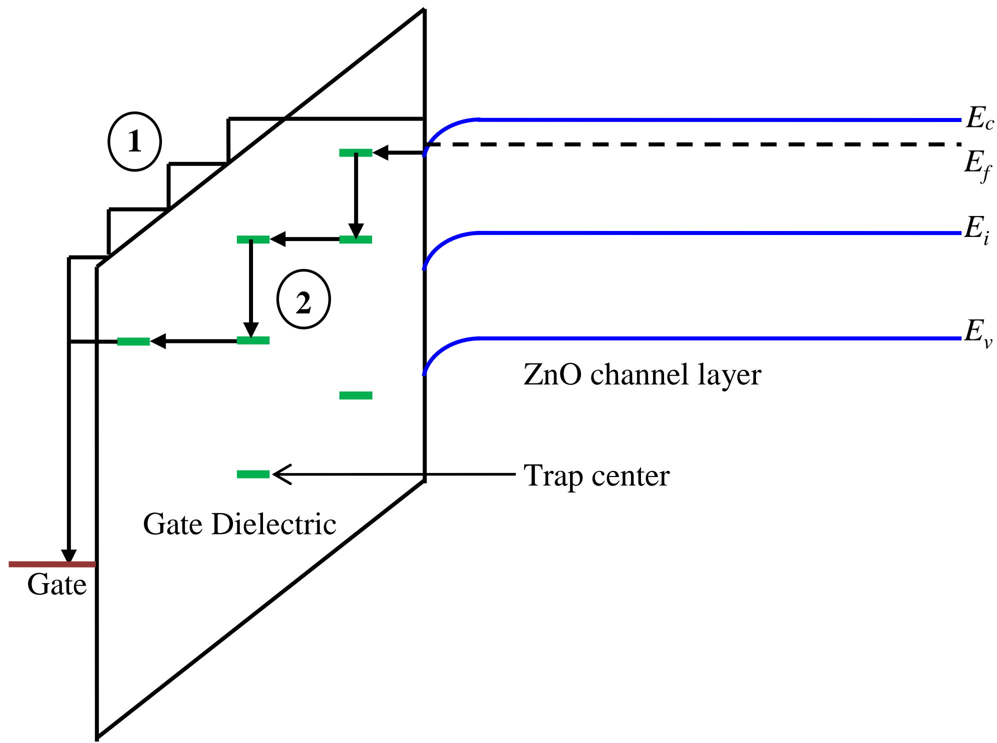


Fig. 2.6 Band diagram of metal gate dielectric/ZnO interface when positive voltage is applied at the gate. Process 1: Fowler –Nordheim Tunneling, Process 2: Trap assisted tunneling.

J. M. Lee *et al.* [58] investigated the drain current in the indium, gallium doped ZnO TFT under positive bias stress. The gate bias was swept from –5 to 15 V in positive direction. It was observed that, the shape of transfer curve was more or less constant while, the location of intercept was different which implies threshold voltage was affected. Slope of curve remains unchanged, which implies that subthreshold slope and mobility remains unaffected. Trapped electrons in gate dielectric screens the gate voltage hence effectively threshold voltage increases. The time dependence of V_T under positive stress can be fitted to an empirical stretched exponential relation [58]:

$$\Delta V_T = \Delta V_{To}\left\{1 - \exp[-(t/\tau)^{\beta}]\right\} \qquad \ldots(2.8)$$

where ΔV_{To} is value of ΔV_T at infinite time, and is a function of stress voltage. β is stretched exponential exponent and τ is characteristic trapping time of carriers and is given by

$$\tau = \tau_o \exp(E_\tau / k_B T) \qquad \ldots(2.9)$$

where τo is thermal pre-factor, E_τ is the average effective barrier, that electrons in ZnO semiconductor channel need to overcome before they can enter at the gate dielectric.

Fig. 2.7 shows the time dependency of threshold voltage shift using the stretched exponential equation for $\beta = 0.42$ and $\tau = 2 \times 10^4$ [58]. β and τ does not depends upon the bias stress voltage but, ΔV_{To} increases with stress voltage. Extensive Bias-Temperature-Stress (BTS) studies have been carried out on ZnO TFT to track the threshold voltage (V_T), field effect mobility (μ_{eff}), subthreshold slope (SS), grain boundary trap creation over time.

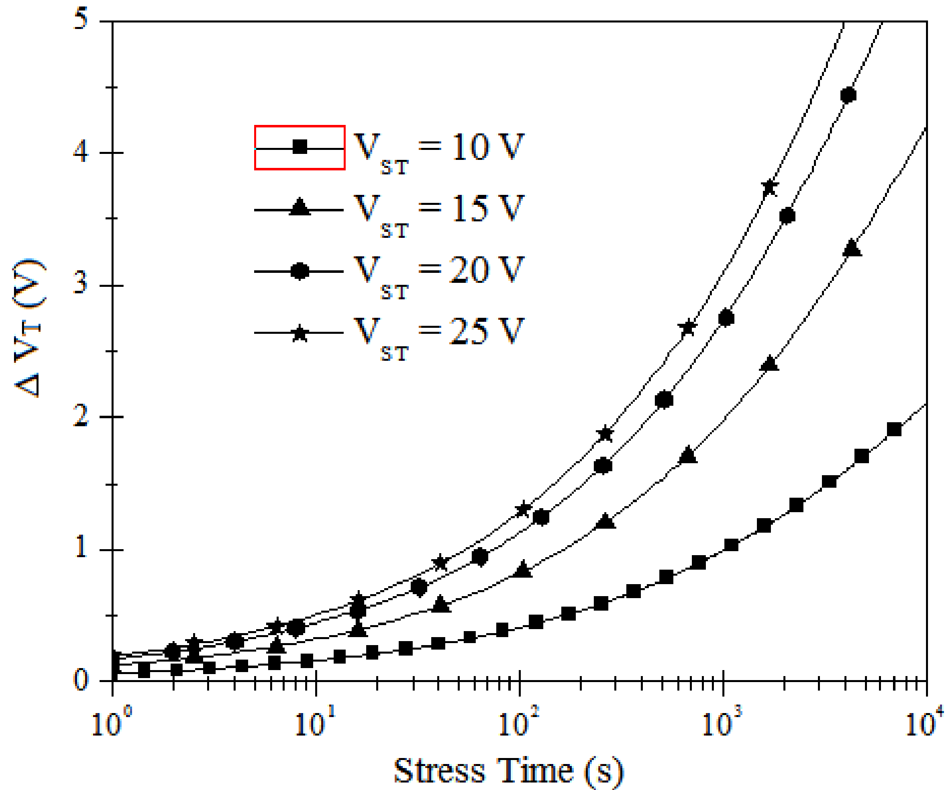


Fig. 2.7 Time dependence of threshold voltage shift under different gate bias stress

All the TFT devices (*a*–Si, Poly–Si, and Oxide) suffer from threshold voltage shift; however, a smart change in device topology can reduce this phenomenon. Yun *et al.* [59], fabricated dual-gate and bottom gate ZnO TFTs without any additional processes and analyzed their threshold voltage variation under a negative gate bias stress (NBS). The dual-gate device shows superior electrical performance, in terms of SS and I_{on}/I_{off}. NBS of $V_{GS} = -20$ V with $V_{DS} = 0$ was applied, which resulted in negative threshold voltage (V_T) shift. After applying voltage stress for 1000 s in dual–gate ZnO TFT, the V_T shift was 0.60 V, while in a bottom-gate ZnO TFT, the V_T shift was 2.52 V. The stress immunity of the dual–gate device was result of modulation in field distribution or potential profile in the ZnO channel due to addition of another gate [59].

D. Gupta *et al.* [60], investigated the stress – recovery characteristic of ZnO TFTs under gate bias and current-stress conditions. At room temperature, a characteristics time of $1.6 \times 10^3 - 3.6 \times 10^3$ s during stress and $7.7 \times 10^3 - 15.7 \times 10^3$ s during recovery was obtained by following a stretched exponential model under all gate voltage bias and current conditions. The device simulation indicates that threshold voltage shift ΔV_T is mainly caused by the increase in acceptor like defects of the DOS in the ZnO channel layer. W. S. Choi [61], studied the effect of threshold voltage shift on TFT scaling. Result shows that the device scaling influences the threshold voltage and subthreshold slope as: a decrease in the active layer thickness results in an increase in threshold voltage, while the subthreshold slope decreases. Siddiqui *et al.* [62], investigated the effect on performance parameter of TFT under illumination stress. Under illumination, the ZnO TFT show an increase in off current, subthreshold slope and negative shift in threshold voltage. Initially mobility was observed to increase for certain time t_{pk} and start decreasing after t_{pk}.

In order to have reliable TFT operation, researchers need to identify the process which can produce near perfect ZnO – dielectric interface and techniques to limit the negative and positive bias temperature instability (NBTI and PBTI).

2.5 Conclusion

This chapter presented a comprehensive review on ZnO based TFTs. It discussed transport models of ZnO based TFT and explained the effect of grain boundaries, trap densities and threshold voltage shift on the performance of ZnO TFT. In the process, this chapter highlighted the challenges like requirement of stable p−type ZnO semiconductor for various electronic applications and high value of ZnO mobility to meet growing demand of HD-LED TV (High Definition LED TV). At the same time it addressed the need of high–κ dielectrics for low leakage and low threshold voltage in ZnO TFTs.

Based on literature review, it was found that current research across the globe in the area of ZnO based TFT, focuses on low threshold voltage and high-mobility ZnO based TFT for power efficient and high performance TFT panels. It was also noted that the threshold voltage instability limits the device performance and affects the reliability of a device. This originates because of interface charge in ZnO−dielectric system and due to defects on gate dielectric called trap centres. It was also explained that selection of high–κ dielectric for low gate leakage and low threshold voltage is not straight forward. Hence, a detailed investigation is needed for selecting the gate dielectric.

CHAPTER - 3

DEPOSITION AND CHARACTERIZATION OF ZnO FILM

3.1 Introduction

The operational characteristic of TFTs critically depends upon the physical and structural properties of the deposited ZnO film. Hence, it is required to deposit highly uniform, high quality ZnO film at the room temperature. In the recent past, various ZnO thin film deposition techniques were reported which include, metal organic chemical vapor deposition (MOCVD), pulsed laser deposition (PLD), RF magnetron sputtering, thermal evaporation, sol gel and spray pyrolysis [23], [42], [46], [63]. Out of these, first three deposition techniques deliver highly transparent and low resistive film with good crystallinity [64]. MOCVD is used for industrial purposes, however, requires higher substrate temperature (> 150 ºC) which limits its application in TFTs. The room temperature deposition is highly important as it supports wide range of substrates including glass, plastic and silicon. PLD is another versatile technique but gives a very low deposition rate which limits its application for large coating area. RF sputtering is the mostly preferred technique for large area coating as it supports room temperature deposition and possesses good deposition rate.

Fortunato *et al.* [46] fabricated ZnO TFT with high mobility undoped ZnO thin film. For the RF power density of 5 Wcm^{-2}, the 100 nm thick film was close to being

Part of this chapter, in its current form has been published as "Study of structural and electrical properties of ZnO thin film for thin-film transistor (TFT) applications" in *Journal of Materials Science: Materials in Electronics*, Springer, vol. 28, pp. 16013-16020, 2017.

stoichiometric with fewer structural defects and possesses resistivity of 10^8 Ω-cm. It was shown that the modulation in resistivity can be achieved either by doping of the group III elements such as aluminum (Al), boron (B), gallium (Ga) and indium (In) or by annealing treatment and process optimization in controlled atmosphere. Further, for a range of RF power density (2-10 Wcm^{-2}), the resistivity was modulated from 10^{-1} to 10^8 Ω-cm. Jeong *et al.* [65] deposited high resistivity (6×10^{14} Ω-cm) undoped 500 nm thick ZnO film using reactive RF magnetron sputtering with a sputtering pressure of 10 mTorr and RF power of 180 W. However, film doped with Al impurity shows improved resistivity of the order of 10^{-4} Ω-cm for a possible use as transparent conductive oxide. D D Han *et al.* [66] reported the influence of RF sputtering power on resistivity of undoped ZnO thin film deposited at room temperature. They were able to achieve resistivity values 2.17 kΩ-cm to 198 kΩ-cm for 1 μm thick ZnO film for a range of RF sputtering power (90 W – 140 W).

This work presents room temperature deposition of high crystalline quality of ZnO films for TFT application using ZnO ceramic and Zn metallic target. RF sputtering process was optimized for both the cases, for high crystallinity and improved resistivity ZnO thin films. Results of this work are very significant as improved resistivity and high crystallinity ZnO thin film was deposited at room temperature which make it ideal for TFT applications.

This chapter is organised in the following order: Section 3.2 gives an brief overview of RF sputtering technique. Section 3.3 discusses ZnO film deposition using ZnO target and characterization of deposited films, while Section 3.4 discusses ZnO film depositon using Zn metallic target and deposited film characterization. The characterization of ZnO films involves identification of crystal structure and surface morphology of deposited ZnO films using various characterization techniques including X-ray diffractometer (XRD), X-ray photoelectron spectroscopy (XPS), atomic force microscopy (AFM), and field emission scanning electron microscopy (FE-SEM). It also discusses about the resistivity measurement using four-probe method. Finally, Section 3.4 provides the conclusion of this chapter.

3.2 RF Magnetron Sputtering

RF magnetron sputtering has emerged as an alternative to other vacuum coating techniques such as e-beam evaporation and thermal evaporation. RF magnetron sputtering offers many advantages over other vacuum and non-vacuum process for ZnO thin film deposition. This includes room temperature deposition, high deposition rate, high purity films, extremely good adhesion of films, excellent step coverage and small features, easy control of growth parameters and ease of sputtering and automation [67]. Fig. 3.1 shows the schematic representation of RF sputtering system.

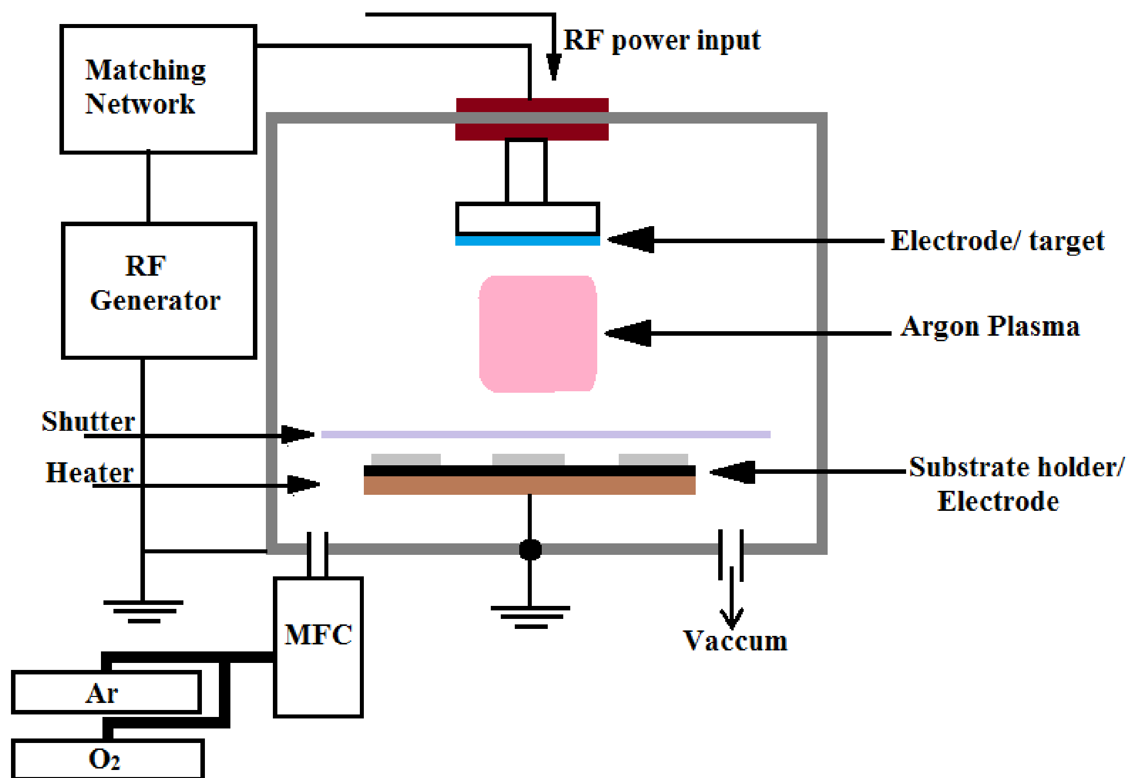


Fig. 3.1 Schematic diagram of RF sputtering technique for thin film deposition

Sputtering is the process whereby atoms of a material (known as target) are ejected by the bombardment of high-energy particles. The bombardment is done by positive ions derived from an electrical discharge in a gas (Ar). To obtain useful coating of ZnO using sputtering, couple of criteria needed to be satisfied. First, Ar+ ions of sufficient energy must be created and directed towards the surface of ZnO/ Zn target to eject atoms from the material. In this regard magnetron sputter process can help as, magnetic confinement of the Ar^+ plasma near the target allows increase in sputter current, thereby increase in deposition rate. Second, ejected atoms must be able to move without any hindrance towards the sample to be coated. To achieve this, a high vacuum is required to maintain high ion energies and to prevent frequent atom- gas collisions after ejection from the target. In sputtering, the average distance that atoms can travel without colliding with gas atoms is defined as mean free path (MFP). MFP increases with decrease in pressure. For transparent ZnO based semiconducting film, most crucial point is control of phase composition and stoichiometry. Usually Zn metallic target and ZnO ceramic target are used for sputtering. Zn metallic target based deposition provides faster deposition rate than ZnO ceramic target, but it needs advance process control techniques for precise control of reactive process while, ceramic target sputtering possesses more robust process as stoichiometry depends on the target stoichiometry up to certain extent [64].

3.3 RF Sputtered Deposition of ZnO Film Using ZnO Target

This section describes ZnO film deposition using ZnO ceramic target and characterization of deposited ZnO films of different thicknesses (100 nm and 200 nm) to study the thickness dependent effect on structural and electrical properties.

3.3.1 Experimental

A 4” diameter, n–type silicon <100> wafer of thickness 525± 25 µm was used as a substrate for the deposition. Prior to deposition, Si substrate was cleaned using standard RCA-1 and RCA-2 standard process. RCA-1 (a solution of $NH_4OH/H_2O_2/ H_2O$ in ratio of 1:1:5) was used to strip organic and metallic contamination while RCA-2 (a solution of

HCl/ H_2O_2/ H_2O in ratio of 1:1:6) was used to remove alkali ions contamination [68]. To measure the resistivity of ZnO thin film using four probe measurement method, the semiconducting Si substrate needed to be isolated so that the resistivity of silicon wafer doesn't affect the measurement. Hence a small thickness of SiO_2 is grown thermally over Si substrate before the deposition of ZnO. RF sputtered ZnO thin film of thicknesses 100 nm and 200 nm were deposited over Si substrate at room temperature using 99.9 % pure ZnO target. As the RF sputtering involves high vacuum, initially a base pressure of 4 mTorr was achieved in the vacuum chamber, then, through the mass flow controller (MFC) the flow rate of oxygen and argon was kept at 5 sccm and 20 sccm respectively. At the beginning of deposition a shutter delay of 120 seconds was provided in order to ensure a contamination-free chamber. During the deposition a pressure of 28 mTorr and RF power of 50 W was maintained which resulted in a deposition rate of 0.6- 0.7 Å/s.

3.3.2 Structural and Surface Morphological Characterization

The crystal structure and surface morphology of the deposited thin film were characterized using X-ray diffractometer (PANalytical X'pert Pro), X-ray photoelectron spectroscopy (Omicron Nanotechnology ESCAPlus), atomic force microscopy (Burker Multimode Scanning probe Microscope), and field emission scanning electron microscopy (Nova Nano FE-SEM 450 model).

Fig. 3.2 shows XRD spectra of ZnO thin film of thickness 100 nm and 200 nm. Both the films show strong c-axis orientation and hexagonal phase of deposited ZnO. However, relative intensity of (002) phase with respect to (110) phase and (103) phase is much greater in 200 nm thick ZnO film than 100 nm thick ZnO film, thereby giving it better crystallinity compared to 100 nm thick ZnO film. It indicates that crystallinity improves with an increase of film thickness. For 200 nm thick ZnO film, the dominating (002) diffraction peak occurs at an angle $2\theta = 34.4058^o$. The XRD spectra also give information about various structural parameters like grain size, defect density, lattice parameters, residual stress and lattice strain. Average grain size (D_G) of 200 nm thick ZnO film for (002) crystallographic plane was computed using Scherrer's formula [69]:

$$D_G = \frac{0.94\lambda}{\beta \cos\theta} \quad \ldots(3.1)$$

where λ is X-ray wavelength and β is full width half maxima (FWHM) in radian. For this work, λ and β were taken 1.54 Å and 0.3838° respectively, which results in a grain size of 22.63 nm. The lattice parameters (a, b, c) can be calculated using eq. (3.2) and eq. (3.3) [70].

$$a = b = \frac{\lambda}{\sqrt{3}\sin\theta} \quad \ldots(3.2)$$

$$c = \frac{\lambda}{\sin\theta} \quad \ldots(3.3)$$

The values of $a = b$, c are found to be 3.0074 and 5.209 respectively which shows a good agreement with standard JCPDS (Joint Committee on Powder Diffraction Standards) data (PDF #01-075-7917($a_o = b_o = 3.253$, $c_o = 5.211$)).

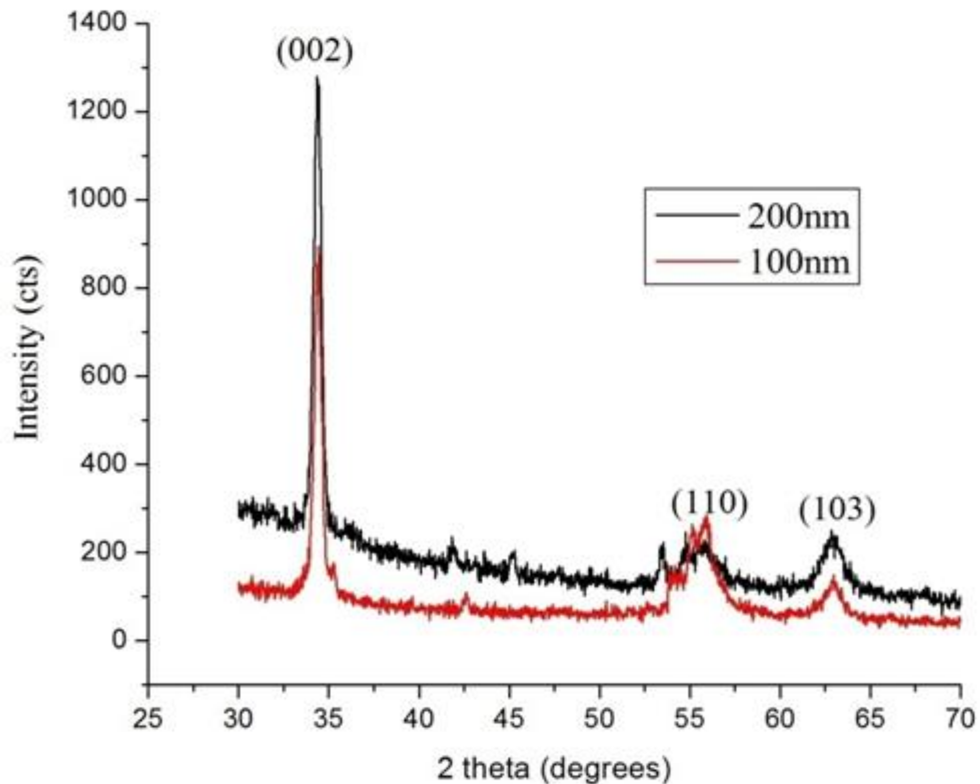


Fig. 3.2 XRD spectra of ZnO thin film of 100 nm and 200 nm thickness

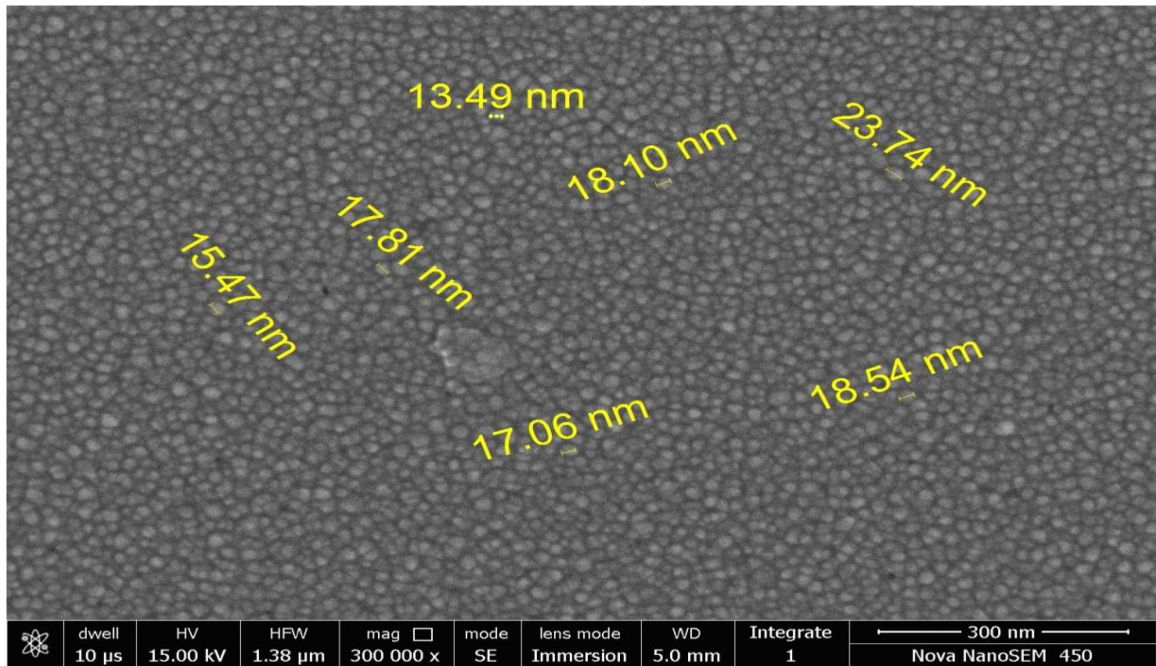
From the XRD spectra, other structural properties like dislocation density can be estimated, which is defined as dislocations per unit volume and is given by inverse of square of grain size [71]. In this case it comes out to be 1.95×10^{-3} nm^{-2}. Smaller value of dislocation density attributes to better crystallization of the thin film. Moreover, lattice strain and residual stress are calculated using eq. (3.4) and (3.5) and found to be 5.401×10^{-3} and -134 GPa respectively. A negative sign for residual stress signifies that the nature of stress is compressive.

$$\text{Lattice strain } = \frac{\beta}{\tan\theta} \qquad \ldots(3.4)$$

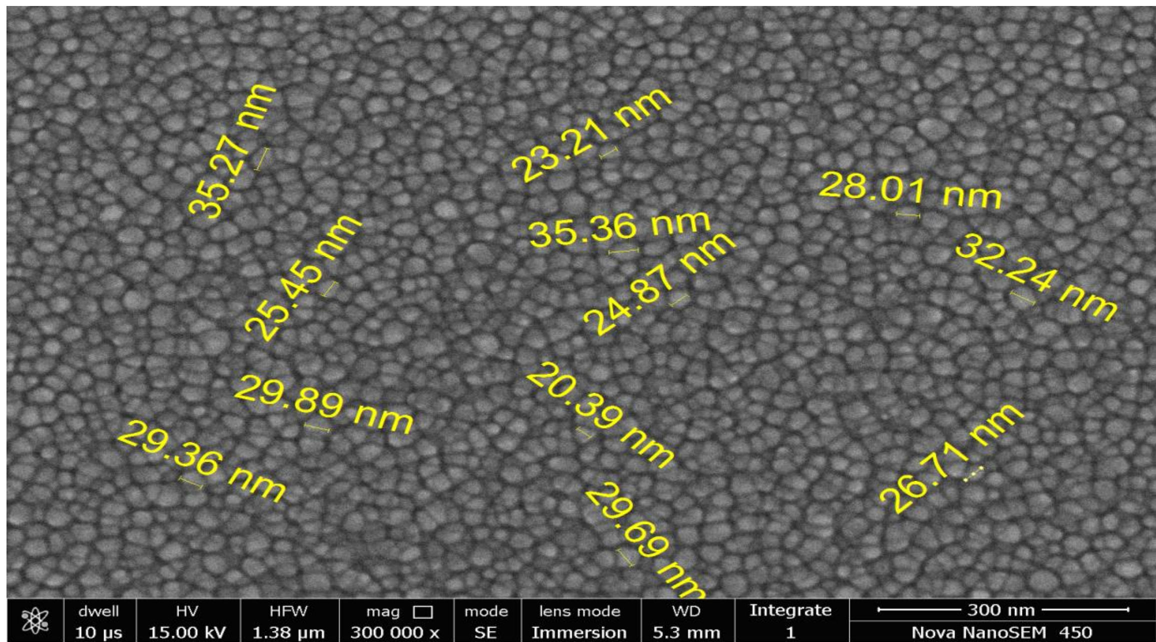
$$\text{Residual stress } = -233\frac{(c-c_o)}{c_o}[GPa] \qquad \ldots(3.5)$$

Fig. 3.3 shows the SEM image of 100 nm and 200 nm thick ZnO films at 300k X magnification. Micrograph image illustrates grain size of 13 nm to 24 nm for 100 nm thick film and 20 nm to 35 nm for 200 nm thick film. This further validates the polycrystalline nature of thin film and also validates that increase in deposited film thickness improves the crystallinity and hence the grain size.

X-ray photoelectron spectroscopy (XPS) is done to confirm presence of zinc and oxygen content in the deposited film. XPS measurement was carried using Al Kα (characteristic energy 1486.7 eV, 300 W power) monochromatic Al radiation. Further, the energy scale of spectrometer was calibrated with C 1s (284 eV). Fig. 3.4 shows measured XPS survey spectra (0-1100 eV) intensity versus binding energy. Absence of contamination is evident from the spectra, which shows only emissions from Zn and O. The core level spectra of O 1s orbital main peak is centered at the lower binding energy of 530.10 eV is attributed to the O^{2-} ions on hexagonal Zn^{2+} ion array, which confirms ZnO chemical state [72]. Moreover, Zn LMM auger peak, is used to identify the chemical stage of Zn species, as single auger transition, involves three electrons and auger peak centered at 498 eV is attributed to ZnO bonds [73].



(a)



(b)

Fig. 3.3 SEM micrograph image of (a) 100 nm thick ZnO film (b) 200 nm thick ZnO film

To measure surface smoothness, AFM imaging is done for 100 nm and 200 nm thick ZnO films. Three dimensional AFM image of surface topography demonstrates surface roughness of the deposited thin film in a scanning area of 1μm × 1μm as shown in Fig. 3.5 and Fig. 3.6. Topographic imaging is done using tapping mode, here the AFM cantilever is oscillated near its resonant frequency and the ultra-sharp probe tip comes in contact with sample during part of oscillation cycle.

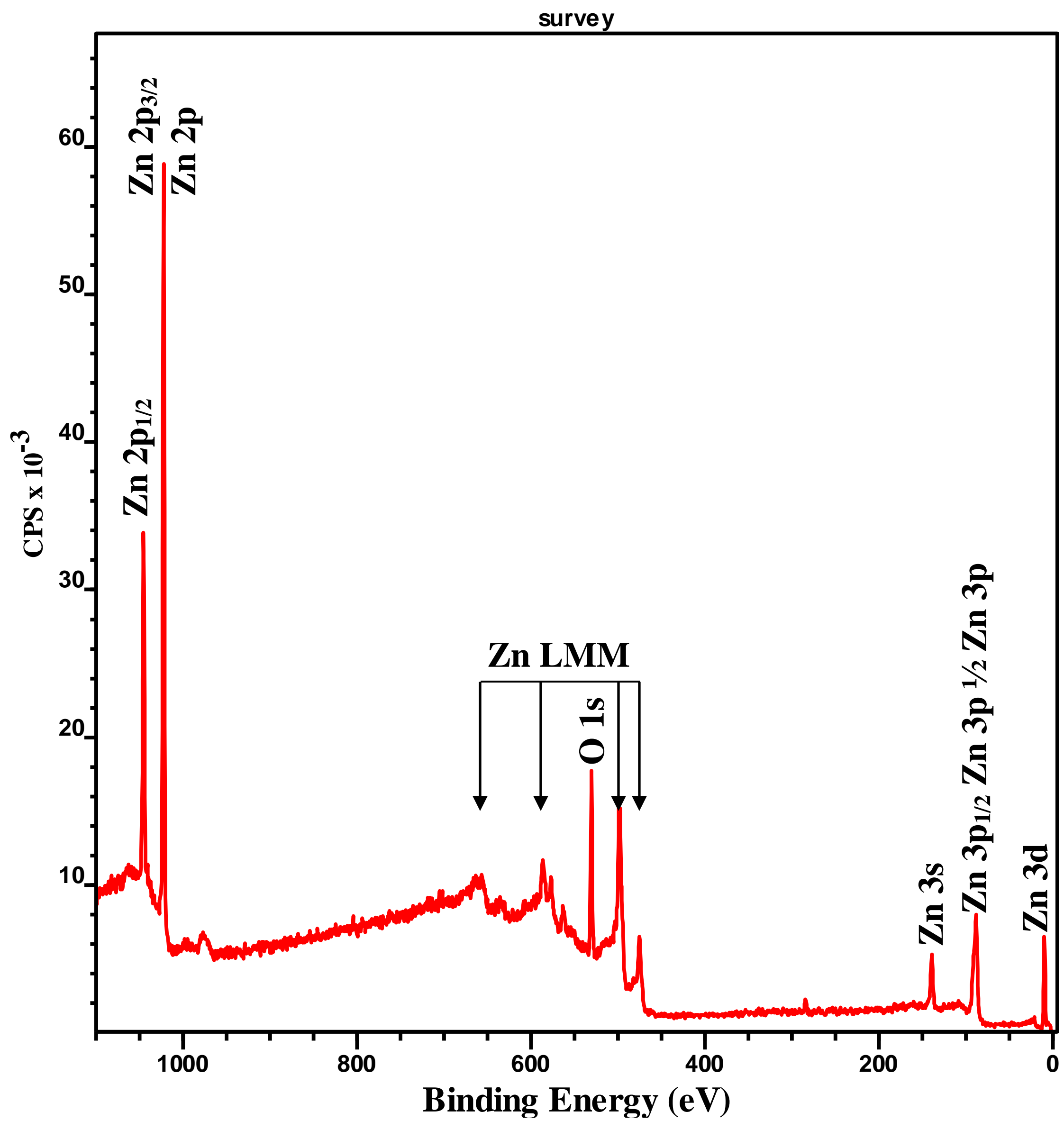
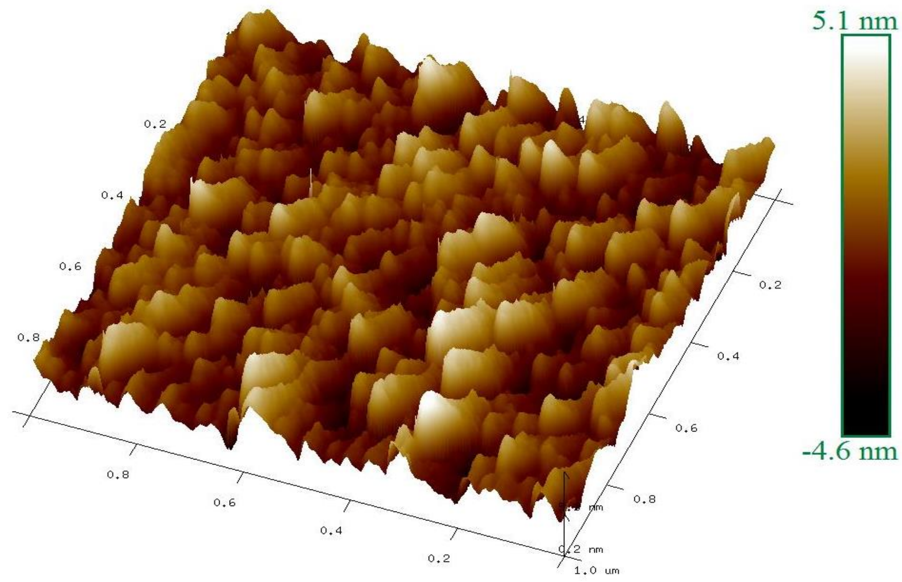
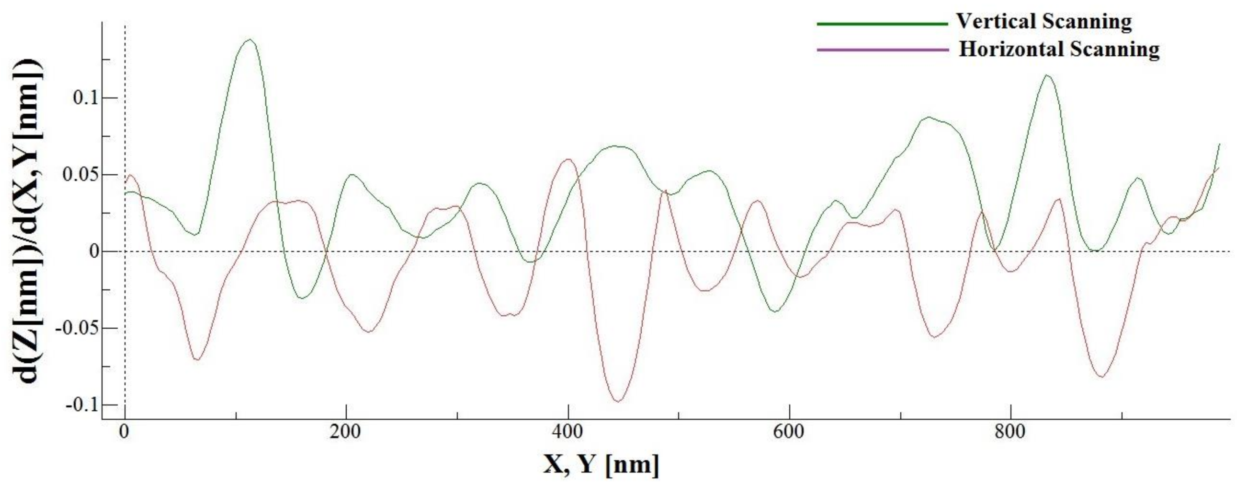


Fig. 3.4 Surface elemental survey scan XPS spectrum of ZnO film

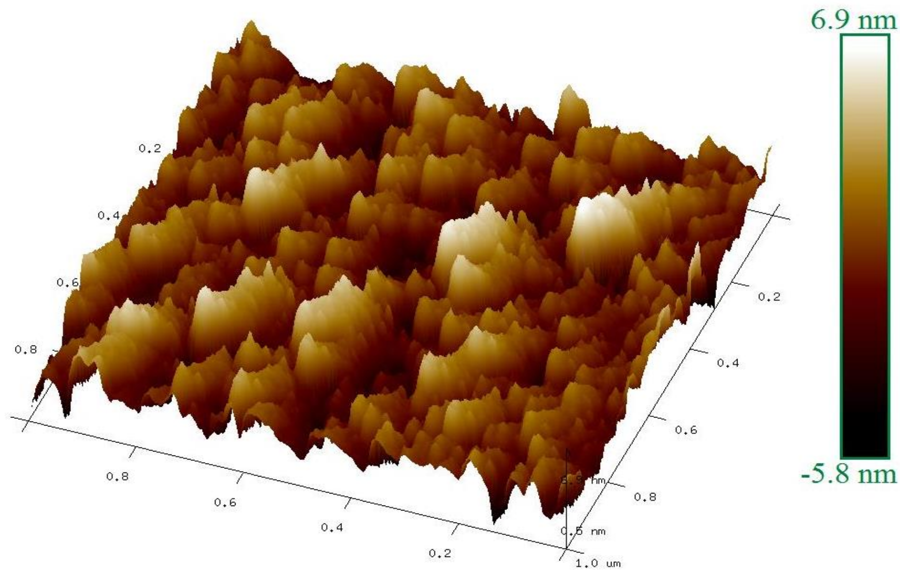


(a)

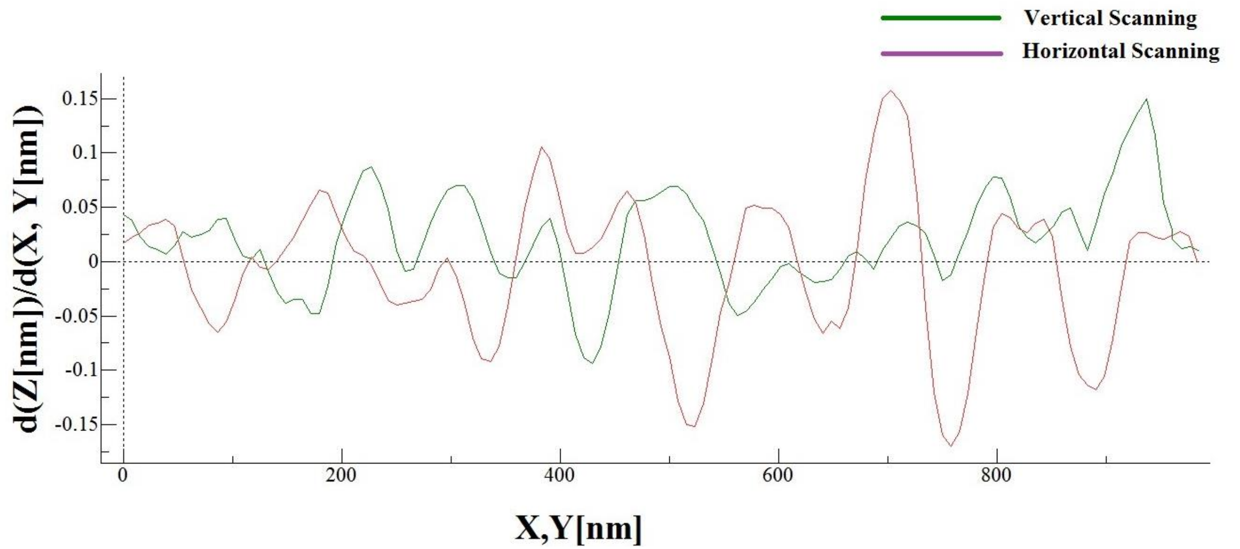


(b)

Fig. 3.5 (a) Three – dimensional AFM image of 100 nm thick ZnO film, (b) (*dz/d(x,y)*) of 100 nm thick ZnO film for a scan area of 1 µm × 1 µm



(a)



(b)

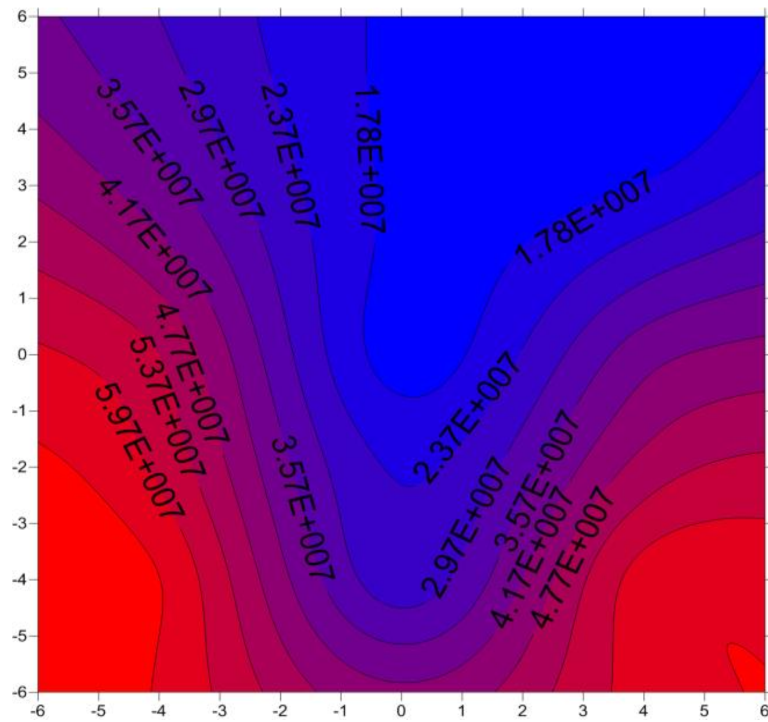
Fig. 3.6 (a) Three – dimensional AFM image of 200 nm thick ZnO film (b) (*dz/d(x,y)*) of 200 nm thick ZnO film for a scan area of 1 μm × 1 μm

For 100 nm thick film, average roughness (R_a) (deviation in height from mean) and root mean square roughness (R_q) was 1.09 nm and 1.37 nm respectively. However, for 200 nm thick film R_a and R_q were 1.41 nm and 1.79 nm respectively. The AFM results clearly demonstrate good surface morphology of deposited ZnO thin film. However, there is a slight increase in surface roughness of 200 nm thick ZnO film over 100 nm thick ZnO film. Fig. 3.5 (b) and Fig. 3.6 (b) shows $dz/d(x,y)$ profile vs. horizontal (x axis), vertical (y axis) scanning, where z is height (thickness) of the film. Along the vertical or horizontal scanning the derivative of height (thickness) with respect to scanning distance ($dz/d(x,y)$) can give a fair idea about the step coverage and it is found to be -0.20 to 0.18 nm/nm in the scanning area 1μm × 1μm.

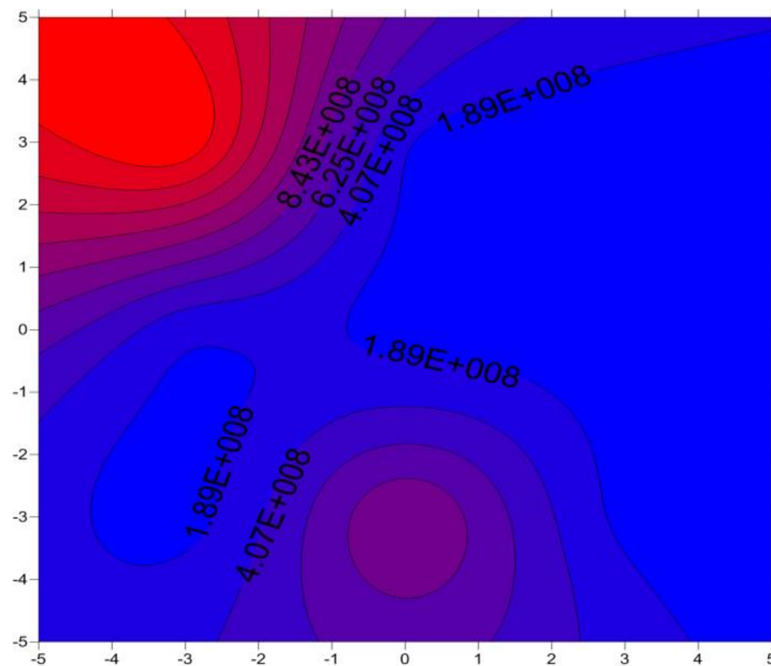
3.3.3 Resistivity Measurement

Signatone Quad Pro controller system was used to measure resistivity of undoped polycrystalline ZnO thin film. This setup provides an accuracy of more than 1 % in standard range and uses four probe method. Spacing between each probe was 0.0625 inches and probe tip was made up of tungsten carbide. The resistivities of rectangular sample of 100 nm and 200 nm thick undoped ZnO film were measured in 10 different places in a sample. A current of 10^{-9} mA was injected through outer two probes and corresponding voltage drop was measured across the inner two probes. Fig. 3.7 shows the contour map demonstrating sheet resistance throughout the rectangular sample of 100 nm and 200 nm thick ZnO film.

Average sheet resistance (R_s) of 100 nm thick film is found to be 4.47×10^8 Ω/□ whereas, for 200 nm thick ZnO film it is 3.62×10^7 Ω/□. This clearly indicates that because of improved crystallinity of 200 nm thick film, the sheet resistance is improved. Given the sheet resistance of ZnO film, resistivity (ρ) can be obtained using: $\rho = R_s$ x t_{ZnO}. where, t_{ZnO} is the thickness of ZnO thin film. Using this relation, resistivity of 100 nm thick ZnO film is found to be 4.470 kΩ-cm, while the resistivity of 200 nm thick ZnO film decreases to 0.724 kΩ-cm. Moreover, resistivity of the RF-sputtered undoped ZnO thin film is much better than other reported films deposited using RF sputtering[46], [65].



(a)



(b)

Fig. 3.7 Sheet resistance contour map of (a) 200 nm thick ZnO film, (b) 100 nm thick ZnO film, where blue to red region shows an increase in sheet resistance

3.4 RF Sputtered Deposition of ZnO Film Using Zn Metallic Target

This section describes ZnO film deposition using Zn metallic target and characterization of deposited ZnO films. Fig. 3.8 shows the reactive magnetron sputtering unit used for deposition of ZnO films. Initially 100 nm and 200 nm thick ZnO film were deposited and it was found that the hexagonal phase of ZnO was totally absent in 100 nm thick film, while in 200 nm thick film a small presence of hexagonal phase was obtained. It gave us a clear indication that for thicker film the hexagonal phase can be obtained without any annealing treatment. Hence, an 800 nm thick ZnO film was also deposited and characterized to confirm hexagonal phase (wurtzite structure) of ZnO for thicker film. Following sections provide detail of experimental procedure and characterization.

3.4.1 Experimental

A 3” diameter, p−type silicon <100> wafer of thickness 350 μm was used as a substrate for the deposition. Prior to deposition, Si substrate was cleaned using standard RCA-1 and RCA-2 standard process similar to the process used in section 3.3.1. Small thickness (1 μm) of SiO_2 is then thermally grown over silicon to isolate the semiconducting Si substrate so that the resistivity of silicon wafer doesn’t affect the ZnO film resistivity measurement. RF sputtered ZnO thin film of thicknesses 100 nm, 200 nm and 800 nm were deposited over SiO_2 layer at room temperature using 99.99 % pure metallic Zn target. RF sputtering involves high vacuum, hence a base pressure of 2×10^{-7} Torr was achieved in the chamber, and then through mass flow controller (MFC), the flow rate of argon and oxygen was kept at 20 sccm and 30 sccm respectively [11]. At the beginning of deposition, a shutter delay of 300 seconds was provided for target pre-cleaning and pure ZnO deposition. During the deposition, a pressure of 20 mTorr and RF power of 400 W was maintained which resulted in a deposition rate of 1.0- 1.1 Å/s.

Fig. 3.8 Reactive magnetron sputtering unit in CSIR- CEERI Pilani

3.4.2 Structural and Surface Morphological Characterization

Fig. 3.9 shows XRD pattern of ZnO thin film of thickness 100 nm, 200 nm and 800 nm. For 100 nm and 200 nm thick films, XRD result shows cubic phase of ZnO which has hardly been reported in literature with Si/ SiO_2 substrate. As the deposition was done using reactive process with Zn metallic target, it results in different phases for ZnO film for lower thicknesses. Deposition using Zn metallic target gives cost effectiveness and increased deposition rate compared to ZnO target, but needs precise control of reactive process [64]. The dominant diffraction peak at 44.54^0 corresponds to (102) cubic phase (a = 4.53 Å) of ZnO [74], [75]. A small presence of ZnO_2 (200) also being observed at $2\theta = 38.3^0$ [76].

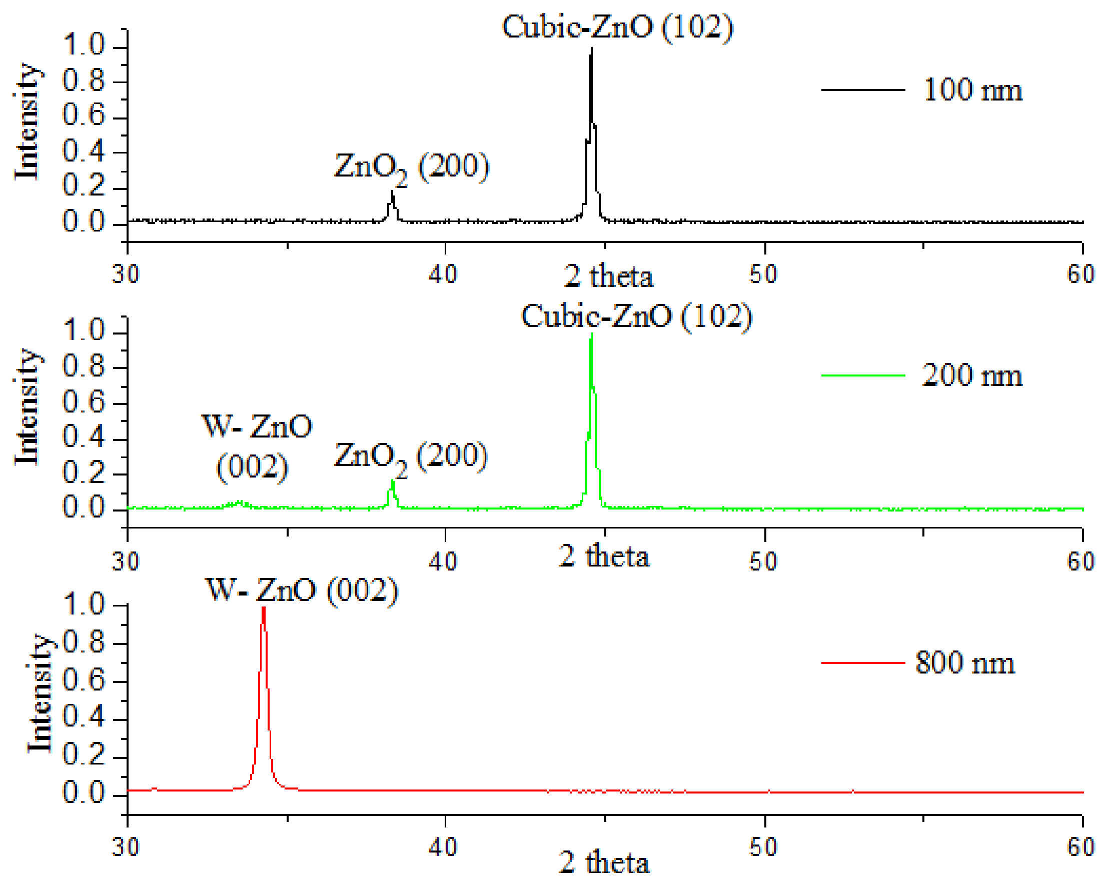


Fig. 3.9 XRD spectra of ZnO thin film of 100, 200, 800 nm thickness

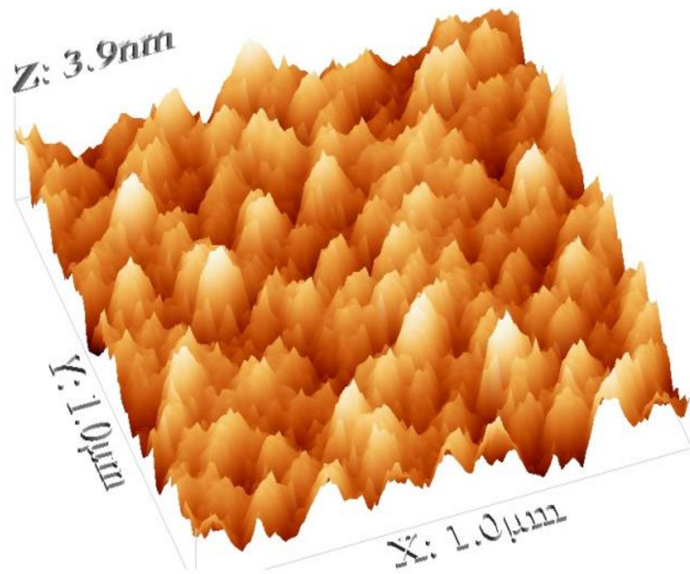
From the XRD spectra it is clear that in 100 nm thick ZnO film, wurtzite phase is completely absent while, for 200 nm thick film small presence of wurtzite phase of ZnO at 34^0 is observed. In 800 nm thick film however, the cubic phase is totally absent and only a strong c axis orientated hexagonal wurtzite phase is present at $2\theta = 34.28^0$ (good agreement with standard JCPDS data PDF #01-075-7917, $a = b = 3.25$ Å, $c = 5.21$ Å). Theoretically it is found that, the total energy of cubic phase of ZnO is more than hexagonal phase of ZnO by 50 – 150 meV/ atom [77]. More exposure to RF power during the deposition of 800 nm thick film could be a reason of absence of cubic phase. Further, the crystallinity of film also improves with increase in thickness, as one can see only a single peak is present for 800 nm thick ZnO film.

To measure surface smoothness, AFM imaging is done for 100 nm, 200 nm and 800 nm thick ZnO films. Two dimensional (2-D) and three dimensional (3-D) AFM image of surface topography to demonstrate surface roughness of the deposited film in a scanning area of 1 µm × 1 µm is shown in Fig. 3.10 – Fig. 3.12. The results obtained from AFM are tabulated in Table 3.1.

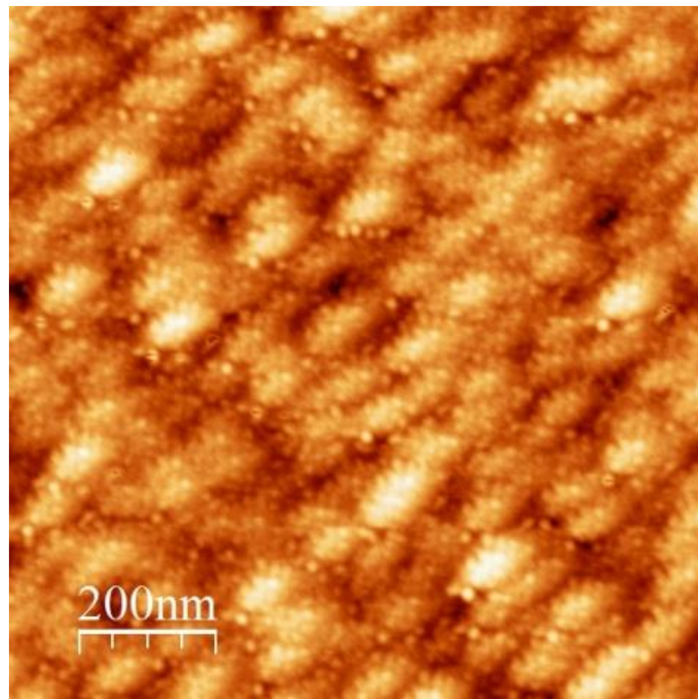
Table 3.1 Summary of AFM results for different thicknesses ZnO films

Film thickness	Average roughness (R_a)	RMS roughness (R_q)	Average grain size (D_G)
100 nm	1.78 nm	0.449 nm	25 nm
200 nm	2.72 nm	0.831 nm	40 nm
800 nm	10.79 nm	3.017 nm	96 nm

AFM results confirm the high quality step coverage with minimal surface roughness. A clear increase in surface roughness in 800 nm thick ZnO film is attributed to its wurtzite structure and increased grain size. The root mean square roughness (R_q) of cubic ZnO layer (100 nm and 200 nm thick films) is suppressed drastically due to the lesser growth rate than wurtzite, hence better surface smoothness.

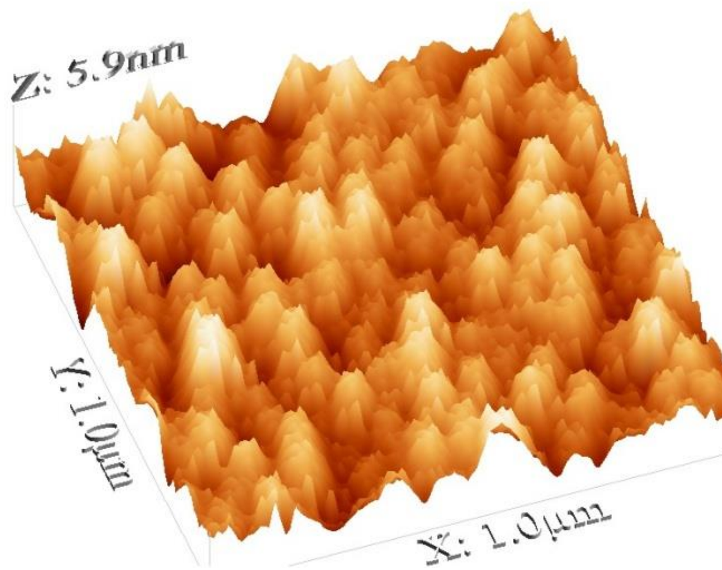


(a)

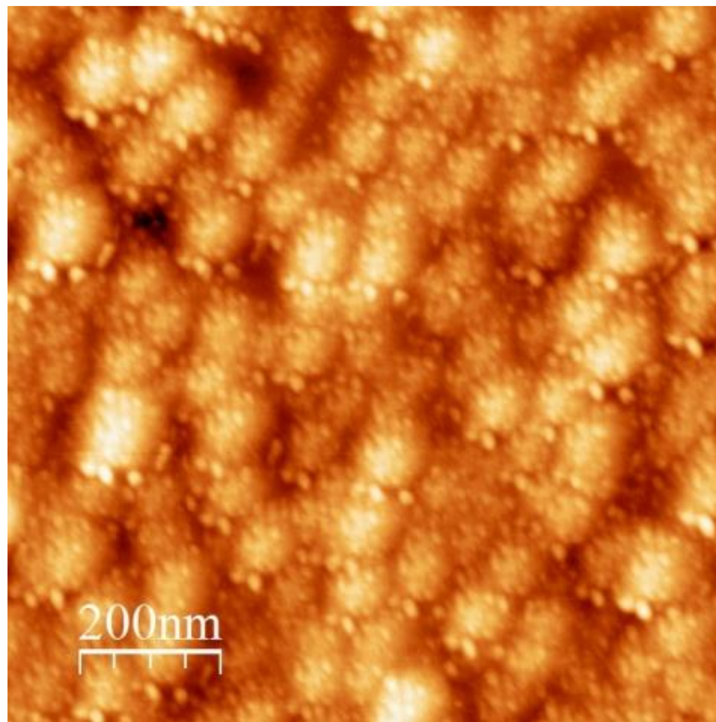


(b)

Fig. 3.10 (a) 3-D and (b) 2-D AFM image of 100 nm thick ZnO film

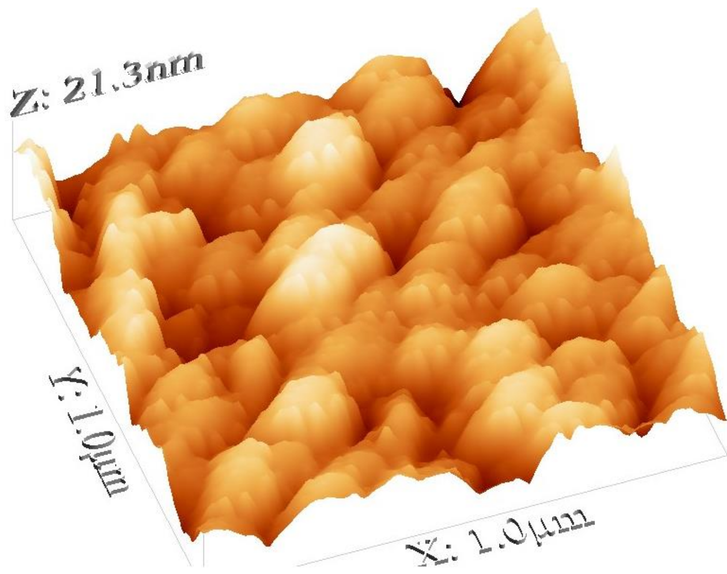


(a)

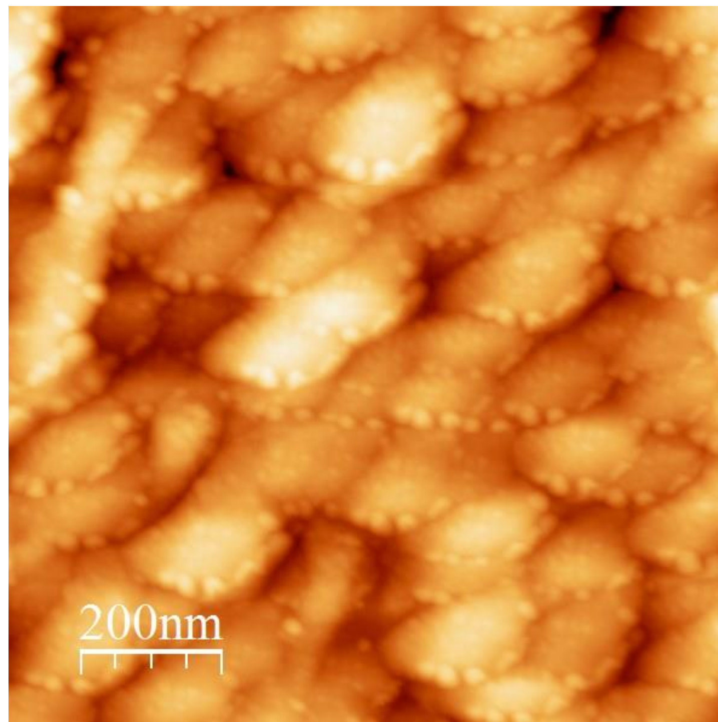


(b)

Fig. 3.11 (a) 3-D and (b) 2-D AFM image of 200 nm thick ZnO film



(a)



(b)

Fig. 3.12 (a) 3-D and (b) 2-D AFM image of 800 nm thick ZnO film

3.4.3 Resistivity Measurement

Signatone Quad Pro controller system as described in section 3.3.3, was used to measure resistivity of undoped polycrystalline ZnO thin film. Fig. 3.13 - Fig. 3.15 shows the sheet resistance contour of 100 nm, 200 nm and 800 nm thick ZnO sample. The sheet resistance (R_s) of undoped 100 nm and 200 nm samples is found approximately 7×10^{11} Ω/□, while the sheet resistance of undoped 800 nm ZnO thin film shows almost 10 time reduction to 6.025×10^{10} Ω/□, due to improved grain size and crystallinity. The resistivity (ρ) of ZnO film can be obtained from sheet resistance. This gives the resistivity of undoped 100 nm, 200 nm and 800 nm thick ZnO film as 7 MΩ-cm, 14 MΩ-cm, 4.82 MΩ-cm respectively. Likewise in other semiconductors, modulation in resistivity can be achieved either by doping of the group III elements or by annealing treatment [65], [75].

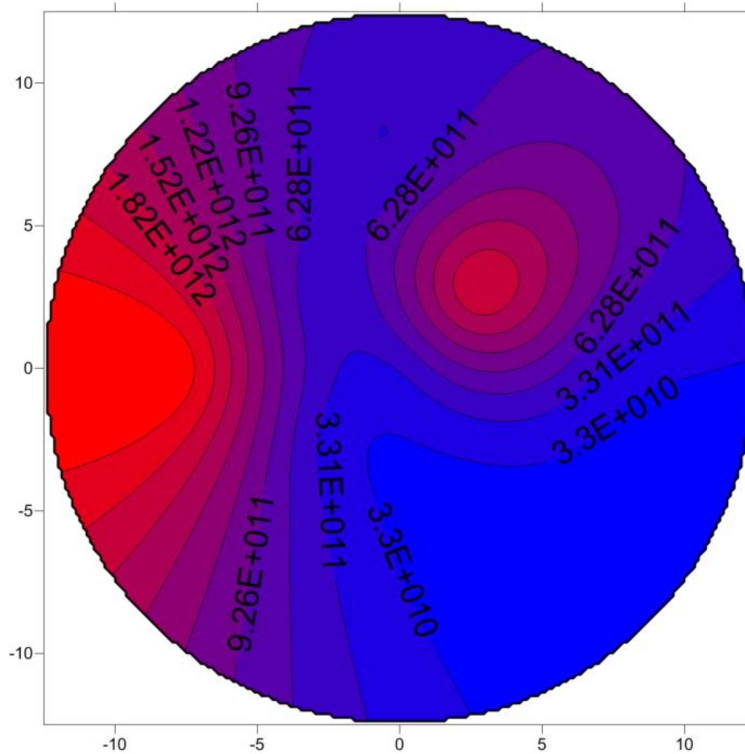


Fig. 3.13 Sheet resistance contour map of 100 nm thick ZnO circular sample

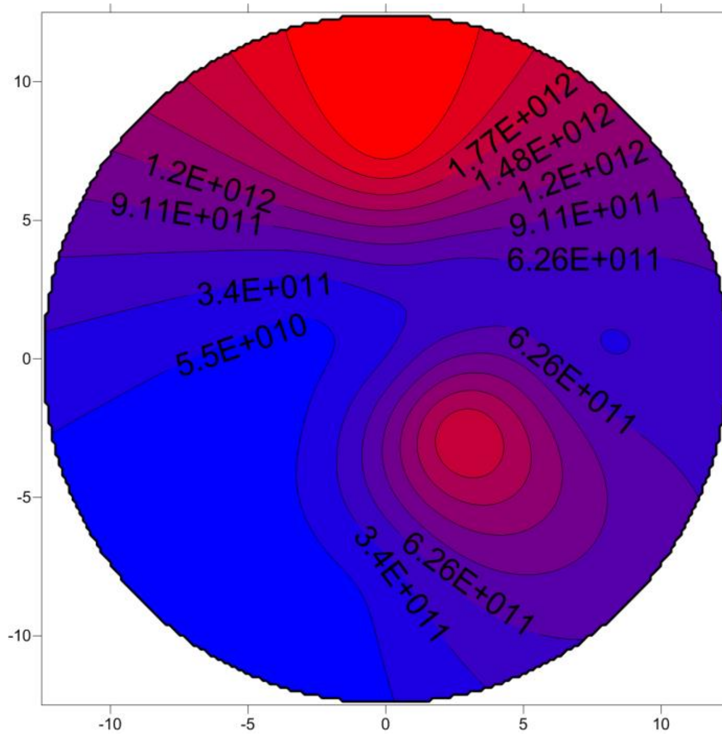


Fig. 3.14 Sheet resistance contour map of 200 nm thick ZnO circular sample

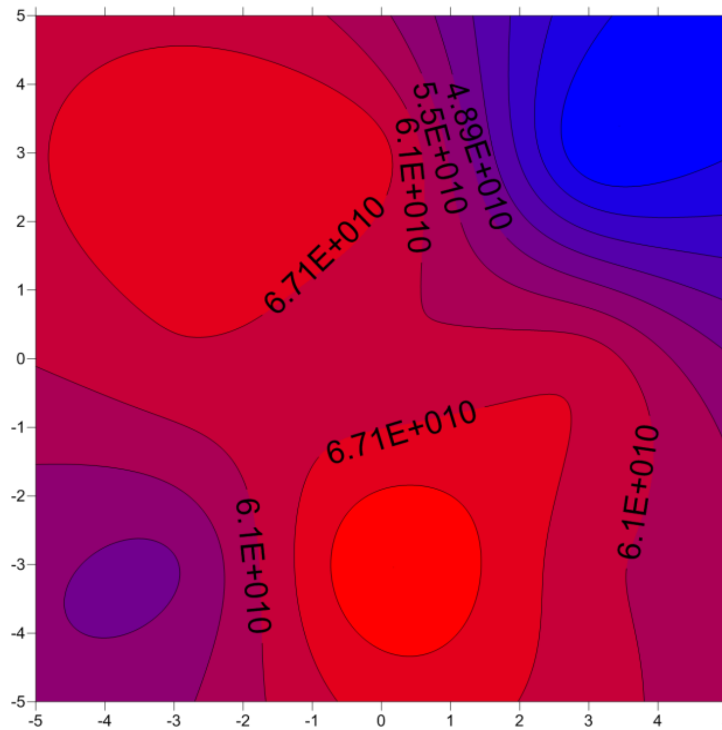


Fig. 3.15 Sheet resistance contour map of 800 nm thick ZnO circular sample

3.5 Conclusion

This chapter has reported preparation and characterization of polycrystalline ZnO film deposited at room temperature for the fabrication of TFT and provided thickness dependent study of ZnO film. ZnO films were deposited using ZnO ceramic target and Zn metallic target.

When **ZnO is deposited using ZnO target**, XRD analysis of deposited film confirms good crystallinity and strong c-axis orientation (wurtzite structure). Moreover, XRD results also confirm the improvement in crystallinity with an increase in film thickness. FE-SEM results validate that the grain size increases with an increase in deposited ZnO thin film thickness which is also been well supported by XRD results as improved crystallinity results in bigger grain size. AFM results confirm the high quality step coverage of RF sputtered ZnO films and shows minimal surface roughness. Further, four-probe measurement of undoped ZnO films gives moderate resistivity of 4.47 kΩ-cm and 0.724 kΩ-cm for 100 nm and 200 nm thick ZnO film respectively.

When **ZnO is deposited using Zn metallic target**, XRD analysis of deposited film of different thickness confirms presence of cubic phase (zincblende structure) of ZnO and ZnO_2 in both 100 nm and 200 nm thick ZnO film. However, for 800 nm thick film only a single peak of W-ZnO was observed which shows improved crystallinity with increasing thickness. AFM results confirm the high quality step coverage of RF sputtered ZnO films and shows minimal surface roughness. Four probe measurement of undoped ZnO films also shows 10 time reduction in sheet resistance of 800 nm thick film than 100 or 200 nm thick film.

We conclude that the deposited ZnO film in either case is polycrystalline and grain size increases with deposited film thickness. ZnO can have either wurtzite structure of hexagonal phase or zincblende structure of cubic phase. Moreover, reactive RF magnetron sputtering with Zn metallic target provides cost effectiveness for large coating area over RF sputter deposition using ZnO ceramic target with an increased deposition rate (1-1.1 Å/s) than 0.6-0.7Å/s. However, the ideal stoichiometry was observed when deposition is carried out using ZnO target. ZnO deposition with Zn metallic target

employs reactive process, hence control in phase and stoichiometry is not easy and due to this, for lower thickness of deposited film (XRD results of 100 nm, 200 nm thick ZnO) presence of cubic phase of ZnO and ZnO_2 were visible. The Zn metallic target deposited films were more oxygen rich; thereby results in higher sheet resistance than ZnO ceramic target deposited film. The highly crystalline films of different thicknesses deposited at room temperature in this work are highly suitable as a channel layer for the fabrication of TFT as it can support wide range of substrate material.

CHAPTER - 4

MATERIAL SELECTION FOR GATE DIELECTRIC

4.1 Introduction

The performance of a TFT fundamentally depends on the type of gate dielectric and the quality of dielectric − channel interface because of the current flows in the ZnO channel next to the interface. In recent years, researchers have focused on high−κ dielectric materials as an alternative to SiO_2 in highly scaled electronic devices [78]–[80]. However, despite the intensive work on high−κ dielectrics, the performance of the devices with high-κ dielectrics is still rather poorly analyzed compared to those with SiO_2 gate oxides. The use of high−κ gate dielectrics in ZnO based TFTs is becoming increasingly necessary, as scaled transistors lead to unacceptable levels of gate leakage current. As discussed in chapter-2, ZnO TFTs suffer from high value of threshold voltage compared to *a*–Si-H TFT. However, an increase in coupling of gate field to the channel layer can reduce the operating voltage of the transistor.

In bottom gate structure as shown in Fig. 1.3, ZnO thin film is deposited on the top of gate dielectric. For enhanced performance, ZnO interface with gate dielectric needs to be clean and free from defects and interface charges. According to the boundary condition, the transverse electric field density (D) should be continuous at the dielectric–ZnO interface as:

$$D_{oxide} = D_{ZnO} \quad \text{…(4.1)}$$

This chapter in its similar form has been published as "Investigations on High−κ dielectrics for low threshold voltage and low leakage Zinc Oxide Thin-Film Transistor" in Journal of Materials Science: Materials in Electronics, Springer, vol. 27, pp. 5972-5981, 2016.

In terms of electric field, eq. (4.1) can be written as,

$$\kappa_{ox}\varepsilon_0 E_{oxide} = \varepsilon_{r(ZnO)}\varepsilon_0 E_{ZnO} \qquad \ldots(4.2)$$

$$E_{ZnO} = \frac{\kappa_{ox}}{\varepsilon_{r(ZnO)}} E_{oxide} \qquad \ldots(4.3)$$

From the eq. (4.3) it is clear that the higher the dielectric constant of gate oxide, the higher would be the electric field in the ZnO, which will result in same amount of charge in the ZnO with less applied gate bias, resulting in a lower threshold voltage V_T.

In terms of the voltage, eq. (4.3) can be written as

$$E_{ZnO} = \frac{\kappa_{ox}}{\varepsilon_{r(ZnO)}} \frac{V_{ox}}{t_{ox}} \qquad \ldots(4.4)$$

From eq. (4.4), it is clear that a high electric field in the channel can be obtained either by reducing the gate dielectric thickness or by using a gate dielectric material with higher dielectric permittivity (high−κ gate dielectric). Both solutions increase the gate capacitance; however, high−κ material presents a more promising solution since it gives flexibility to use thicker high−κ gate dielectric to reduce leakage. Another term which is widely used in IC technology is equivalent oxide thickness (EOT). EOT is a measure of the scaling capability of high−κ dielectric compared to SiO_2 dielectric. The EOT of a high−κ dielectric is defined as, the thickness required by SiO_2 to achieve same voltage modulation effect or same equivalent capacitance density as of high−κ dielectric [81] and is given by eq. (4.5) as:

$$EOT = \frac{\kappa_{SiO_2}}{\kappa_{ox}} t_{ox} \qquad \ldots(4.5)$$

There are several advantages associated with high−κ gate dielectric in ZnO-TFTs. It allows use of a thicker dielectric layer, which leads to reduction in gate field at the ZnO-dielectric interface and consequently reduce the effect of gate bias stress on the threshold voltage V_T. The use of thicker high−κ dielectric layers also reduces gate leakage current without affecting the induced interface charge density. Moreover, high−κ dielectric also

enhances the driving capacity of TFT by increasing pixel driving current. However, a very large value of dielectric constant κ can lead to unfavorable large fringing field at source and drain region [82].

4.2 Material Selection Methodologies

The key performance parameters for selection of a potential gate dielectric require permittivity, band-gap and band alignment to ZnO. However, together with these parameters; film morphology, stability, interface quality, reliability and process compatibility are also important to further enhance the device performance [81]. As there are various high−κ dielectric that have been reported in fabrication of ZnO- TFT, where each dielectric is having its own advantages and limitations, so to find out the best possible alternative, one can use multi – criteria decision making (MCDM) approach [83] when there are more than one attribute. The MCDM approach is further subdivided into MODM (multi-objective decision making) and MADM (multi-attribute decision making). These approaches are well studied by many researchers in engineering regime [84]–[86]. The most popular material selection methodologies are Ashby's approach, *Technique for Order Preference by Similarity to Ideal Solution* (TOPSIS) and *VlseKriterijumska Optimizacija I Kompromisno Resenjein in Serbian* (VIKOR) [85]–[87]. This chapter describes material selection methodologies in detail and applies these methodologies to find out most promising dielectric for low leakage and low threshold voltage ZnO based TFTs, from the intrinsic properties of ZnO and dielectric material.

Ashby's approach is one of the most commonly used MODM approach as it optimizes alternatives based on the prioritized objectives. VIKOR and TOPSIS are MADM techniques and the alternatives are ranked on the basis of weighted attributes. Ashby approach is very easy when performance indices are less in number however, it does not generate ranking score. VIKOR and TOPSIS are widely used for a wide range of material selection problem which gives ranking solution. VIKOR and TOPSIS approaches differ in the fact that; VIKOR uses linear normalization method whereas TOPSIS uses vector normalization to convert different scales of various criteria into standard units [87]. TOPSIS method gives the solution by finding the shortest distance from the ideal solution

and longest distance from worst case solution whereas the VIKOR gives the compromise solution by determining least individual regret of the opponent and highest group utility of majority [86].

Flow chart shown in Fig. 4.1 illustrates the various steps that are used to find out the best gate dielectric for ZnO TFT. First step is to find out the possible dielectric candidates those form stable interface with ZnO. Lei H. Wen *et al.* [88] has studied ZnO – Al_2O_3 heterojunction, which is formed by Laser Molecular Beam epitaxy (LMBE). Y. K. Moon e*t al.* [50] studied ZnO TFT using La_2O_3 gate dielectric, where La_2O_3 was deposited using electron cyclotron resonance-atomic layer deposition (ECR-ALD). Moreover, the ZnO and $BaTiO_3$ interface was studied and band offsets was measured by C. H. Jia *et al.* [51]. Similarly all the other dielectric materials used in this study has been successfully demonstrated by various researchers on ZnO [52], [53], [89], [90]. Next step is to find out the material indices like band-gap (E_g), dielectric constant (κ), conduction band offset to ZnO (CBO or ΔE_c) and difference in temperature coefficient of ZnO and high–κ dielectric. This will lead to construction of fundamental decision matrix. This is followed by particular material selection methodology, to find out the best suitable material candidate out of all the possible alternatives.

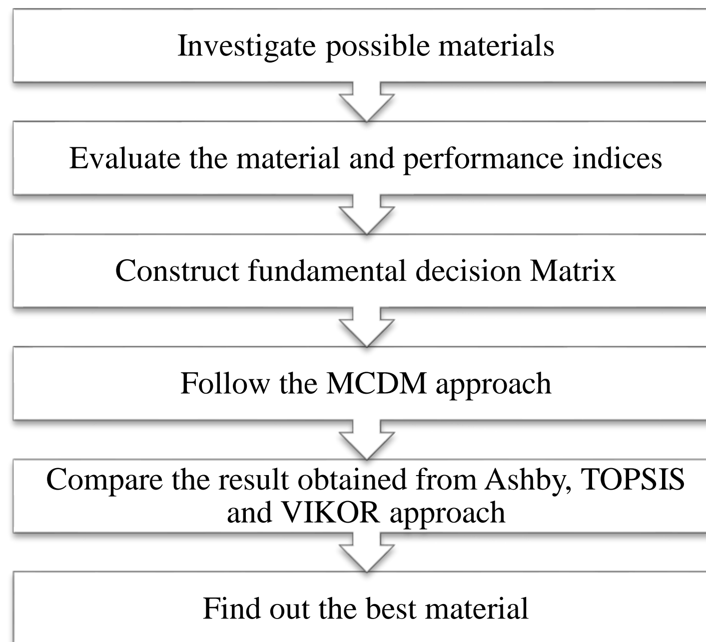


Fig. 4.1 Flow chart of material selection approach

4.2.1 Ashby's Approach

The Ashby's approach list all the design requirements based on objectives and sets screening constraints. Then it defines Ashby's function based upon performance parameters. In general, Ashby approach involves mainly four steps, i.e.

I. Translation of design requirements, based on objective, design constraints and free variables.

II. Screening using various constraints

III. Finding out suitable set of solution using the objectives

IV. Seeking additional information and validation with experimental results if available.

The objective is to minimize leakage and minimize EOT so that ZnO TFT can be operated at low voltage. The constraints for Ashby analysis for this device are:

I. Band-gap should be high (> 5 eV) [91]

II. Dielectric constant (κ_{ox}) > 15 [91]

III. Conduction band offset (ΔE_c) > 1 eV [92]

Here the variables are the choice of materials (from set of material reported for ZnO TFT in literature) and material indices (M) are band-gap (E_g), Dielectric constant (κ_{ox}) and CBO (ΔE_c). The functional parameter (F) is leakage current and the geometrical parameter is scaling limit (t_{ox} or EOT). Now, one can define Ashby function A, which will determine the performance of TFT as: A = *f* {F, G, M}

In any field effect transistor, the leakage current density for the case when tunneling is dominated by ECB (conduction band electron) tunneling mechanism, can be modeled by a semi empirical equation [93] and given by

$$J_{GL} \propto \exp\left\{-\frac{4\pi(2q)^{\frac{1}{2}}}{h} * \left(m_{eff}\,\phi_b\right)^{\frac{1}{2}} k * EOT\right\} \qquad \ldots(4.6)$$

where h is Planck's constant, q is electron charge, m_{eff} is electron tunneling mass, and ϕ_b is barrier height. In this case barrier height ϕ_b is ΔE_c. Eq. (4.6) can be rewritten as:

$$J_{GL} = b * \exp\{-a * f * EOT\} \qquad \ldots(4.7)$$

where $f = (m_{eff}\phi_b)^{1/2}\kappa_{ox}$ and a, b are the constant. From eq. (6) it can be seen that higher the value of f, lower will be the gate leakage current density (J_{GL}). For a given value of supply voltage and maximum leakage current density $J_{GL,max}$, the scaling limit is reciprocally related to the gate dielectric figure of merit (f) as:

$$t_{ox} = \frac{\ln\left(\frac{b}{J_{GL,\max}}\right)}{a} f^{-1} \qquad \ldots(4.8)$$

4.2.2 TOPSIS Approach

This approach was introduced by K. Yoon and H. C. Lai in 1981 [94]. This approach is used to find out the best alternative by finding out the shortest Euclidean distance (S*) from ideal solution (A*) and largest distance (S^-) from worst case solution (A^-) (or negative ideal solution). The steps followed in TOPSIS approach are:

Step 1- Preparation of normalized decision matrix N

Normalized decision matrix N, consists of n_{ij}, elements with i^{th} number of alternatives under j^{th} number of criterion. This matrix is normalized with RMS value given by:

$$n_{ij} = \frac{x_{ij}}{\sqrt{\sum_{i=1}^{u}\left(x_{ij}\right)^2}} \qquad \ldots(4.9)$$

Where i represents the set of alternative = $1, 2, 3 \ldots\ldots\ldots\ldots u$, and j represents set of criteria = $1, 2\ldots\ldots v$.

Step 2- Preparation of weighted normalized matrix

In this step we assign weight to all criteria where the value of weights is chosen such that $\sum_{J=1}^{v} w_j = 1$, now weighted normalized matrix $M_{ij} = n_{ij} \text{ x } w_j$.

Step 3- Computation of ideal and negative ideal solution

If J_1 is associated with the benefit criteria and J_2 is associated with cost criteria then, the ideal Solution A* is defined as: A*= $\{\max M_{ij} \mid j \in J_1\}$ or $(\min M_{ij} \mid j \in J_2)$ = $\{M_1^*, M_2^*, M_3^* \ldots\ldots M_v^*\}$, and the worst case solution A^- is defined as: $A^- = \{\min M_{ij} \mid j \in J_1\}$ or

$(\max M_{ij} \mid j \in J_2) = \{M_1^-, M_2^-, M_3^- \ldots\ldots M_v^-\}$.

Step 4- Calculation of separation measure from ideal and non ideal solution

Euclidean distance from ideal solution S_i^* can be measured as:

$$S_i^* = \sqrt{\sum_{j=1}^{v} \left(M_{ij} - M_j^*\right)^2} \quad \ldots(4.10)$$

Euclidean distance from non ideal solution S_i^- can be measured as:

$$S_i^- = \sqrt{\sum_{j=1}^{v} \left(M_{ij} - M_j^-\right)^2} \quad \ldots(4.11)$$

Step 5- Measurement of relative closeness (C_i) from ideal solution

The relative closeness from ideal solution C_i can be obtained using eq. (4.12) as:

$$C_i = \frac{S_i^-}{S_i^- + S_i^*} \qquad \text{for } 0 < C_i < 1 \quad \ldots(4.12)$$

The ranking of alternatives now depends upon the value of C_i, larger the value of C_i, better will be the performance of the alternative.

4.2.3 VIKOR Approach

This approach was first proposed by Opricovic in 1998 [95] and widely accepted for selecting the material for engineering design. However, Chang [96] developed a modification in VIKOR method to simplify numerical calculation in solving problems. This method focuses on ranking and selecting from various alternatives. It is a fuzzy logic based methodology which provides a compromising solution based on the following steps.

Step 1- Determination of x_j^* and x_j^- values

If x_{ij} element belongs i^{th} row (alternatives) and j^{th} column (criterion) of fundamental decision matrix, then we first determine x_j^* either as *max* $\{x_{ij}\}$ if it represents benefit criteria or as *min* $\{x_{ij}\}$ if it represents cost criteria, where $i = 1,2\ldots..u$, and $j = 1,2\ldots\ldots v$. Similarly x_j^- is defined as *min* $\{x_{ij}\}$ or *max* $\{x_{ij}\}$ if it represents benefit criteria or cost

criteria respectively.

Step 2- To construct the maximum group utility G_i and minimum regret of the opponent R_i

If w_j is the weight of jth criteria and $\sum_{j=1}^{v} w_j = 1$ then, the values for G_i and R_i is given by the following equations:

$$G_i = \sum_{j=1}^{v} w_j \frac{\left(x_j^* - x_{ij}\right)}{\left(x_j^* - x_j^-\right)} \qquad \text{...(4.13)}$$

$$R_i = \max_j \left[w_j \frac{\left(x_j^* - x_{ij}\right)}{\left(x_j^* - x_j^-\right)} \right] \qquad \text{...(4.14)}$$

Step 3- Calculation of Q_i for i^{th} alternative

If $G^- = \max\{G_i\}$ $G^* = \min\{G_i\}$, $R^- = \max\{R_i\}$, $R^* = \min\{R_i\}$ and σ is defined as weight of strategy G_i and (1- σ) as weight of strategy R_i, then the value of ith alternative of VIKOR (Q_i) is given as:

$$Q_i = \sigma \frac{\left(G_i - G^*\right)}{\left(G^- - G^*\right)} + \left(1 - \sigma\right) \frac{\left(R_i - R^*\right)}{\left(R^- - R^*\right)} \qquad \text{...(4.15)}$$

Usually the value of, weight of maximum group utility (σ) is chosen to be 0.5.

Step 4- *Sorting the value of R, G and Q*

This step includes, finding out the value of R, G and Q in increasing order to compute the ranking order of alternatives (A^1, A^2, A^3... A^u).

Step 5- Now one can find out the best alternative based upon the flow chart illustrated in Fig. 4.2, where $DQ = 1/(U-1)$; and U is number of alternatives.

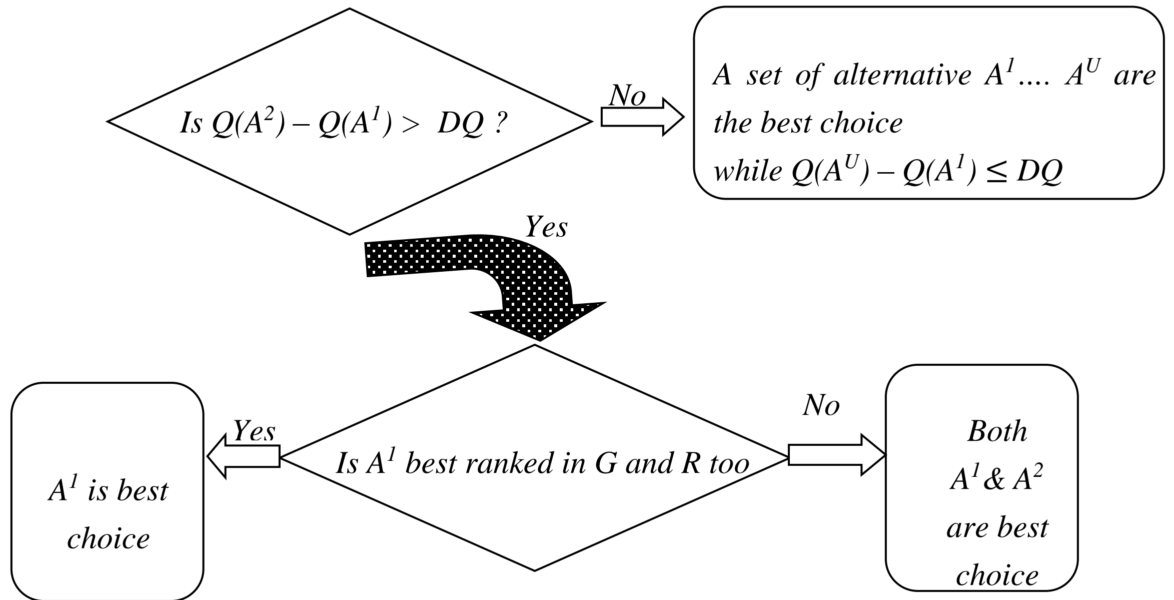


Fig. 4.2 Flow chart illustrating the decision making in VIKOR approach

4.3 Material Indices of the Gate- Dielectrics

To construct fundamental matrix for the material selection methodologies mentioned above, the value of band-gap (E_g) and dielectric constant for the high−κ material (κ_{ox}) can be found easily in literature [97]. However, in literature the band offset value for various dielectrics are mentioned with respect to silicon. Hence, in present work it is required to calculate the band alignment of dielectrics on ZnO.

Fig. 4.3 shows the dielectric-ZnO interface which is used to calculate the band offset of high−κ material on ZnO. From this figure it seems that conduction band offset (ΔE_c) is simply the difference between electron affinity of high−κ and ZnO. However, band offset also depends upon charge transfer across interface which creates interface dipole. J. Robertson and B. Falabertti [97], [98] have used charge neutrality level (CNL) method to find out the conduction band offset (ΔE_c) of high−κ gate oxide on III–V semiconductor. One can use the same model to find out the band offset of high−κ dielectrics on ZnO semiconductor.

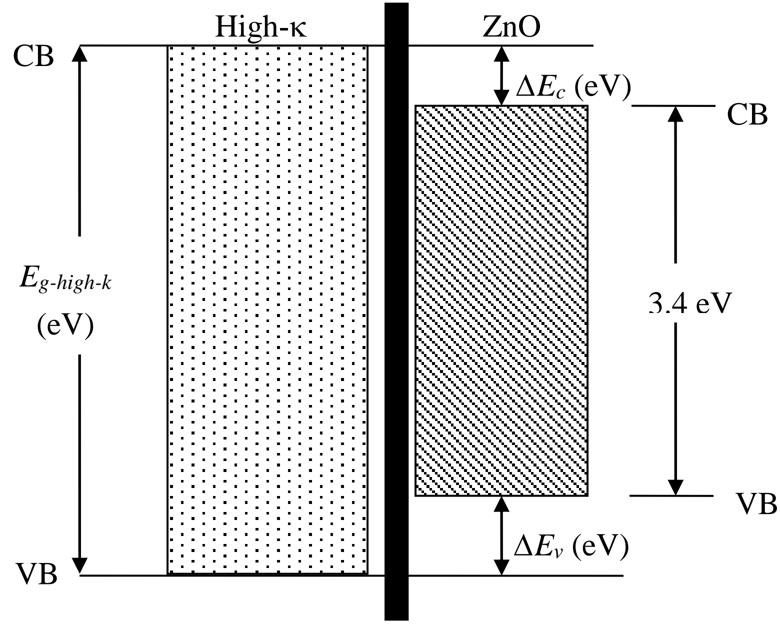


Fig. 4.3 Conduction band offset (ΔE_c) and valance band offset (ΔE_v) of high−κ material on ZnO

According to J. Robertson and B. Falabertti [97], the interface between oxide and semiconductor can be considered as an interface between two semiconductor, i.e. semiconductor *a* and semiconductor *b*. The conduction band offset (ΔE_c) is given by:

$$\Delta E_c = (\chi_a - CNL_{s,a}) - (\chi_b - CNL_{s,b}) + S(CNL_{s,a} - CNL_{s,b}) \qquad \ldots(4.16)$$

Where χ is electron affinity of semiconductor and *CNL* is the charge neutrality level of respective semiconductor measured from vacuum level. S is a Schottky barrier pinning factor, 0 < S < 1. The value of S is 1 in the absence of dipoles i.e. wide band-gap material and the value of S is 0 for the strongly pinned interface. So we can simplify the eq. (4.15) for ZnO/ high−κ interface as:

$$\Delta E_c = (\chi_{ZnO} - \chi_{High-k}) + (S-1)[(CNL_{ZnO} - CNL_{High-k})] \qquad \ldots(4.17)$$

The electron affinity (χ) and CNL value measured from top of valance band of ZnO are 4.6 eV and 3.27 eV [27] respectively. The values of electron affinity of various dielectrics can be found on J. Robertson [98] work. If ε_∞ is electronic part of dielectric

constant then, the value of S can be found by the empirical relation given by Monch [99].

$$S = \frac{1}{1 + 0.1(\varepsilon_{\infty} - 1)^2} \quad \ldots(4.18)$$

Table 4.1 gives the value of χ, S and CNL of dielectric materials. The CNL value given in Table 4.1 is measured from the top of valence band.

Table 4.1 Materials and their conduction band offset (ΔE_c)

Dielectric Materials	**χ (eV)**	***CNL* (eV)**	**S**	**CBO (eV)**
HfO_2	2.4	3.7	0.52	2.2
ZrO_2	2.5	3.6	0.52	2.1
$HfSiO_4$	2	3.6	0.56	2.7
La_2O_3	2	2.4	0.53	3.1
$LaAlO_3$	2.5	3.8	0.53	1.9
$SrTiO_3$	3.9	2.3	0.28	0.8
Ta_2O_5	3.3	3.3	0.4	1.1
Ga_2O_3	3.5	2.8	0.49	1.5
Gd_2O_3	2.4	2.3	0.41	2.9
Al_2O_3	1	6	0.69	3.3
SiO_2	0.9	4.5	0.95	3.7
Si_3N_4	2.1	2.6	0.59	2.5
$BaTiO_3$	----	----	-----	-0.75*

* C. H. Jia *et al.* [51], have measured the value of band offset using X-ray photoelectron spectroscopy

Dielectric like La_2O_3, Sc_2O_3 and Y_2O_3 show similar conduction band offset performance of 3.1 eV. Table 4.2 provides the values for band-gap (E_g), dielectric constant (κ_{ox}) and conduction band offset (ΔE_c). From the Table 4.2, most of the oxide e.g. La_2O_3, Al_2O_3, Gd_2O_3, ZrO_2 and more show excellent CBO because ZnO possesses large value of electron affinity. Once the ΔE_c values are known, the valence band offset (VBO) values can be easily computed. Fig. 4.4 shows the ΔE_c and ΔE_v of various high−κ oxides on ZnO. A positive value of ΔE_v indicates that the holes need particular amount of energy to cross energy barrier i.e. ZnO valence band to high−κ valence band. Table 4.2 gives material indices of various dielectrics.

Table 4.2 Material indices matrix

Dielectric Materials	E_g (eV)	κ_{ox}	ΔE_c(eV)
HfO_2	6	25	2.2
ZrO_2	5.8	25	2.1
$HfSiO_4$	6.5	11	2.7
La_2O_3	6	30	3.1
$LaAlO_3$	5.6	30	1.9
Ta_2O_5	4.4	22	1.1
Ga_2O_3	4.8	23	1.5
Gd_2O_3	5.8	16	2.9
Al_2O_3	8.8	9	3.3
SiO_2	9	3.9	3.7
Si_3N_4	5.3	7	2.5
Y_2O_3	6	15	3.1
Sc_2O_3	6.3	14	3.1
$BaTiO_3$	3.1	2000	-0.45
$SrTiO_3$	3.3	2000	0.8

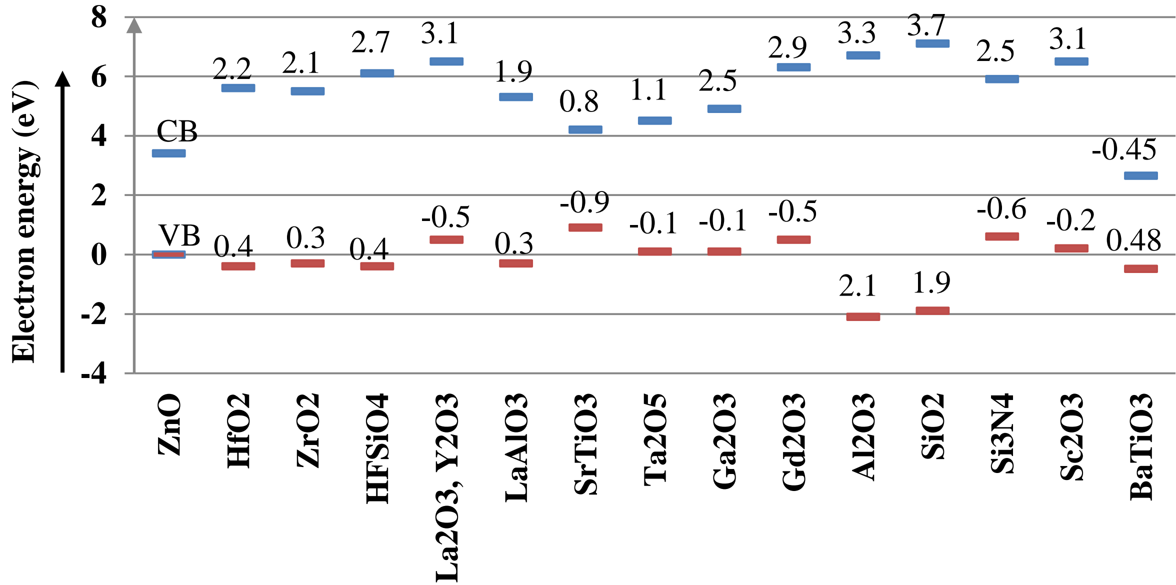


Fig. 4.4 The conduction band and valance band offset of various high–κ dielectrics on ZnO

Along with the material indices listed in Table 4.2; thermal expansion coefficient mismatch (|ΔTEC|) also plays an important role in deciding the performance of TFT because deposition of thin film on a substrate or channel may include high temperature process like post annealing treatment. Also a significant amount of temperature coefficient mismatch may lead to considerable amount of stress which will eventually leads to defects in interface, or excessive stress which can cause the device failure. Table 4.3 list the values of thermal coefficient mismatch in PPM/K of various gate dielectrics with ZnO [100]–[103].

Table 4.3 Material indices |ΔTEC| PPM/^{o}K for various dielectrics

Dielectric	|ΔTEC| PPM/K	Dielectric	|ΔTEC| PPM/K
HfO_2	0.1	Sc_2O_3	2.2
ZrO_2, Ga_2O_3	2.8	Gd_2O_3	1.26
$HfSiO_4$	6.3	Al_2O_3	3.9
La_2O_3	4.1	SiO_2	4
$LaAlO_3$	7.1	Si_3N_4	1.7
Ta_2O_5	0.5	Y_2O_3	2.9

ZnO has a thermal expansion coefficient close to 4.6 x 10^{-6}/ ^{o}C [104]. |Δ TEC| in PPM/ ^{o}C is computed by taking the difference between TEC of ZnO and dielectric irrespective of the nature of stress i.e. compressive or tensile. So |Δ TEC| is a cost criterion for TOPSIS and VIKOR approach.

4.4 Results and Discussion

4.4.1 Ashby's Analysis

In Ashby's approach, first step is to plot the graphs in between various material indices. Then it is required to apply the constraints to find out possible sets of dielectrics. Fig. 4.5 shows the plot between conduction band offset and band-gap for all the possible high−κ dielectric. As one requires E_g more than 5 eV and ΔE_c more than 1 eV it is clear that

Ga_2O_3, $SrTiO_3$, Ta_2O_5, $BaTiO_3$ do not fulfill the required conditions. The materials that satisfy the requirements are shown under the shaded rectangle.

Fig. 4.6 shows the plot between band-gap and dielectric constant of all possible materials. As one needs E_g more than 5 eV and κ_{ox} more than 15; SiO_2, Al_2O_3, $HfSiO_4$, Si_3N_4, Ta_2O_5, Ga_2O_3, Sc_2O_3, Gd_2O_3 violate the constraints and are removed from the selection of gate dielectric. Shaded rectangle shown in Fig. 4.6 covers all those materials that satisfy the conditions.

Fig. 4.7 shows plot between conduction band offset and dielectric constant. As stated, one needs ΔE_c greater than 1 eV and κ_{ox} greater than 15, SiO_2, Al_2O_3, Sc_2O_3, $HfSiO_4$, Si_3N_4 don't fit in constraint. Hence the material left that satisfies all the constraints are HfO_2, ZrO_2, La_2O_3, $LaAlO_3$, while Ga_2O_3 and Ta_2O_5 narrowly violate these constraints. Finally, for the dielectrics satisfying Ashby constraints, gate dielectric figure of merit (f) as given in eq. (4.7) is plotted. The typical values of tunneling effective mass for the dielectrics ranges from $0.1m_o$ to $0.5m_o$ [105]–[108]. From the Fig. 4.8, it is clear that best alternative as a gate dielectric of ZnO TFT for low leakage operation is La_2O_3. This is followed by $LaAlO_3$, ZrO_2 and HfO_2.

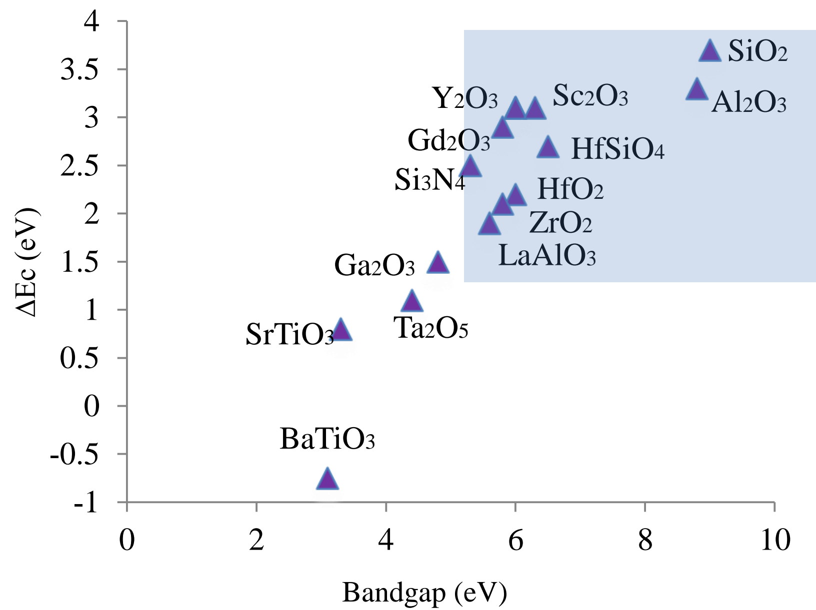


Fig. 4.5 Plot of conduction band offset versus band-gap of various dielectrics

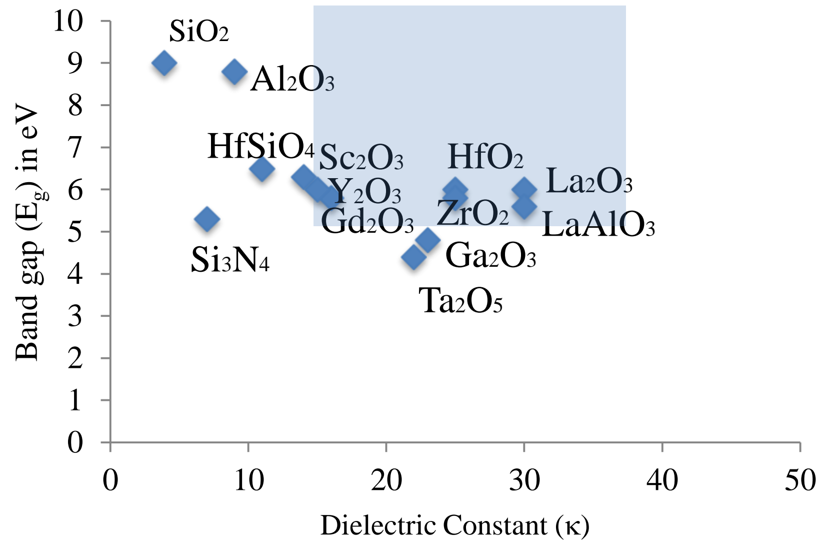


Fig. 4.6 Plot of band-gap versus dielectric constant for various dielectrics

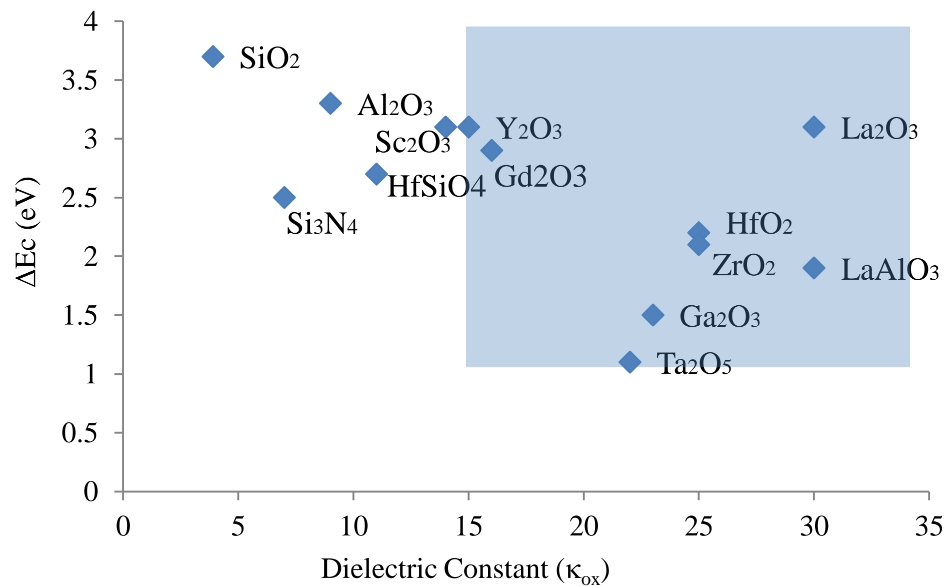


Fig. 4.7 Plot of conduction band offset versus dielectric Constant

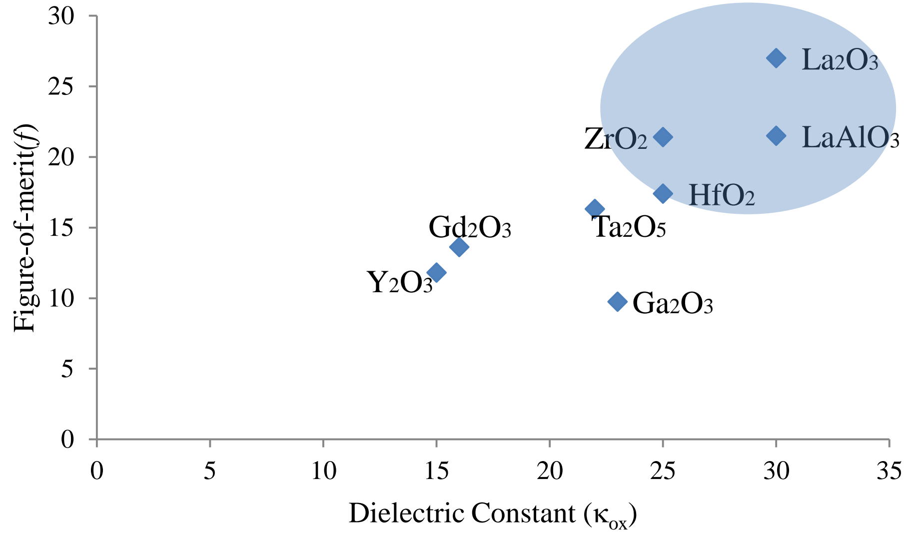


Fig. 4.8 Plot of figure of merit (f) versus dielectric constant

4.4.2 TOPSIS Analysis

For the TOPSIS and VIKOR one needs a weight matrix with proper justification. The dielectric constant can be given highest weight for low threshold voltage TFT. It is followed by conduction band offset (ΔE_c) and then by band-gap (E_g) and the least weight is given to temperature coefficient mismatch (|ΔTEC| PPM/^{0}K) because various process techniques are available which either can deposit oxides in low thermal budget or can use additional deposition of stress relieving material which can overcome the induced intrinsic stress. In addition, TFT fabrication is preferred with low thermal budget to allow wide range of compatible substrate material. So keeping $\sum_{j=1}^{v} w_j = 1$ in view, the weight matrix is $W = [0.4, 0.3, 0.2, 0.1]$. Using this weight matrix, a weighted normalized matrix (Table 4.4) is constructed.

The parameters in brackets in Table 4.4 are the normalized value of parameter with respect to root mean square value. From the Table 4.4 one can find out the ideal (A^*) and negative ideal (A^-) solution as:

A^* = {0.1696, 0.115927, 0.079125, 0.000763}

A^- = {0.022048, 0.034465, 0.038683, 0.054171}

Table 4.4 Weighted normalized matrix

Dielectric	0.4*[κ_{ox}]	0.3*[ΔE_c]	0.2*[E_g]	0.1*[|ΔTEC|]
HfO_2	0.141334	0.06893	0.05275	0.000763
ZrO_2	0.141334	0.065796	0.050992	0.021363
$HfSiO_4$	0.062187	0.084595	0.057146	0.048067
La_2O_3	0.1696	0.097128	0.05275	0.031282
$LaAlO_3$	0.1696	0.05953	0.049233	0.054171
Ta_2O_5	0.124374	0.034465	0.038683	0.003815
Ga_2O_3	0.130027	0.046997	0.0422	0.021363
Gd_2O_3	0.090453	0.090862	0.050992	0.009613
Al_2O_3	0.05088	0.103394	0.077367	0.029756
SiO_2	0.022048	0.115927	0.079125	0.030519
Si_3N_4	0.039573	0.078329	0.046596	0.01297
Y_2O_3	0.0848	0.097128	0.05275	0.022126
Sc_2O_3	0.079147	0.097128	0.055388	0.016785

Table 4.5 TOPSIS results with ranks

Dielectric	S^-	S^+	C	Rank
HfO_2	0.135894	0.060856	0.690695	2
ZrO_2	0.128213	0.06729	0.655811	3
$HfSiO_4$	0.067099	0.123451	0.352135	12
La_2O_3	0.162543	0.044502	0.785061	1
$LaAlO_3$	0.150037	0.083226	0.643211	4
Ta_2O_5	0.114045	0.101619	0.528809	7
Ga_2O_3	0.113601	0.090029	0.557881	5
Gd_2O_3	0.099984	0.088104	0.531581	6
Al_2O_3	0.087607	0.122863	0.416246	10
SiO_2	0.093974	0.150523	0.384356	11
Si_3N_4	0.063177	0.139742	0.31134	13
Y_2O_3	0.095337	0.093255	0.505521	8
Sc_2O_3	0.094147	0.096723	0.493251	9

Table 4.5 gives the values of Euclidean distance from ideal and non-ideal solution, relative closeness from ideal solution (C) and the TOPSIS rank. From the Table 4.5, top three ranked materials are La_2O_3, HfO_2, and ZrO_2.

4.4.3 VIKOR Analysis

VIKOR also uses the same weight matrix, as used for TOPSIS analysis. From the calculation of maximum group utility G_i and minimum regret of the opponent R_i one can find out the following.

Minimum $R_i = R^* = 0.130435$, Maximum $R_i = R^- = 0.4$

$G^* =$ Minimum $G_i = 0.256808$, $G^- =$ Maximum $G_i = 0.674679$

Table 4.6 gives the value R, G and Q for all the dielectrics and their ranking based on the values of corresponding R, G and Q.

Now using the flow chart given in Fig. 4.2, VIKOR rank can be decided. Since $Q(A^2) - Q(A^1) > 0.08334$ and A^1 is the same for R and G, hence La_2O_3 is best choice material followed by HfO_2. While comparing the result of all the three approaches all gives La_2O_3 a lead over other dielectrics. Other suitable dielectric materials that can be used are HfO_2, ZrO_2 and $LaAlO_3$.

To validate findings of this work, the results of proposed analysis are compared with the experimental data. Table 4.7 shows the comparative analysis of ZnO based TFT employing different dielectrics namely La_2O_3, HfO_2 and ZrO_2, which are deposited using RF sputtering. It clearly indicates that all the ZnO based TFT with high−κ gate dielectric (La_2O_3, HfO_2 and ZrO_2) shows a very low value of threshold voltage than SiO_2 and Si_3N_4 gate dielectrics [10-20 V]. It also shows, using La_2O_3 as a gate dielectric shows superior performance than HfO_2 and ZrO_2 in terms of threshold voltage (V_T) and leakage current (I_{off}). The close match between outcome of this work and experimental results shows the validity of the proposed analysis for the low voltage and low leakage TFT. However, other performance parameter like I_{on}/I_{off}, SS and mobility depends on quality of ZnO deposition and quality of gate dielectric and ZnO interface. These needs experimental parameters (like grain size and grain boundaries in ZnO channel, D_{it} at ZnO interface and many more) and cannot be simply decided from material intrinsic properties. But,

material selection methodologies clearly have helped to rank the dielectric material based upon intrinsic properties of materials. Top ranked dielectric material can be chosen for experimental analysis purpose and interface can be further studied and optimized.

Table 4.6 VIKOR R_i, G_i and Q_i values with respective ranks

Dielectric	$\boldsymbol{R_i}$	**Ranking based on($\boldsymbol{R}$)**	$\boldsymbol{G_i}$	**Ranking based on ($\boldsymbol{G}$)**	$\boldsymbol{Q}$	**Ranking based on $\boldsymbol{Q}$**
HfO_2	0.173076923	2	0.380140058	2	0.2267	2
ZrO_2	0.184615385	3	0.4389456	4	0.3184	3
$HfSiO_4$	0.291187739	9	0.603839436	11	0.7134	10
La_2O_3	0.130434783	1	0.256808409	1	0	1
$LaAlO_3$	0.207692308	4	0.455518395	5	0.3811	4
Ta_2O_5	0.3	10	0.62831965	12	0.759	12
Ga_2O_3	0.253846154	8	0.582305972	10	0.6184	9
Gd_2O_3	0.214559387	5	0.462568943	8	0.4022	5
Al_2O_3	0.32183908	11	0.430974293	3	0.5634	8
SiO_2	0.4	13	0.455714286	6	0.738	11
Si_3N_4	0.352490421	12	0.674678668	13	0.9119	13
Y_2O_3	0.229885057	6	0.469550609	9	0.439	6
Sc_2O_3	0.245210728	7	0.461832802	7	0.4582	7

Table 4.7 Experimental data for the validation of proposed analysis

Performance Parameter	$\boldsymbol{La_2O_3}$ [109]	$\boldsymbol{HfO_2}$ [110]	$\boldsymbol{ZrO_2}$ [90]
μ_{eff} ($cm^2V^{-1}s^{-1}$)	12.1	7.95	28
V_T (V)	1.85	2	3.2
I_{on}/ I_{off}	1.5×10^7	4.1×10^8	4.8×10^7
I_{off} (A)	3.29×10^{-11}	2.2×10^{-9}	$\sim 10^{-10}$
SS (V/Dec)	0.234	0.215	0.560
Deposition Technique	RF Sputtering	RF Sputtering	RF Sputtering

4.5 Conclusion

This chapter highlighted the importance of high−κ dielectrics for low voltage and low leakage ZnO TFT. Band offset values of various dielectrics on ZnO TFT were calculated analytically. Three different material selection methodologies like Ashby, TOPSIS and VIKOR were used to find out the best gate dielectric material. Intrinsic properties of materials; dielectric constant, band-gap, conduction band offset and thermal coefficient mismatch were used as material indices for these methodologies. These analyses converge that top three ranked materials are La_2O_3, HfO_2, and ZrO_2. The result shows good agreement among Ashby, TOPSIS and VIKOR approaches.

CHAPTER - 5

DEVICE MODEL FOR ZnO TFT

5.1 Introduction

A complete understanding on device physics is a first and foremost step needed to design and develop TFT systems. As discussed in section 1.2, other than fabrication cost and thermal budget, the oxide TFT differs to conventional metal oxide semiconductor (MOS) system in terms of its conduction mechanism. In MOSFET, current conduction is achieved when an inversion layer is formed close to the interface between silicon and gate dielectric, while in TFT; it is achieved by formation of an accumulation layer. In MOSFET, semiconducting channel is single crystal while, in oxide TFT it is either polycrystalline or amorphous. In MOSFET, the threshold voltage (V_T) is defined as, the gate to source voltage (V_{GS}) at which inverted minority carrier density at the semiconducting channel becomes same as majority carrier density at the bulk (i.e. surface potential becomes approximately twice of the bulk). However, oxide TFTs works in accumulation mode as opposed to inversion mode regardless the type of material. This implies, no polarity inversion of induced carriers, therefore, making the definition of threshold voltage different.

Threshold voltage in oxide TFT has remained ambiguous due to the complex density of localized states in energy band-gap [111]. Many researchers [62], [112], [113], have defined it as a gate to source voltage at which metal-insulator-semiconductor (MIS) system is in flat band, that is comprised of metal to semiconductor work function

difference (ϕ_{ms}), and potential due to fixed oxide charges present at dielectric. However, this definition fails to describe a very high V_T in low−κ dielectric system with high number of grain boundary trap density (N_t) in semiconductor. In oxide TFTs, due to polycrystalline nature of semiconducting channel, the carriers get trapped in grain boundaries, resulting in a limited number of carriers available in extended states at room temperature. Hence, even applying a voltage equal to flat band voltage in oxide TFT is not enough to release enough number of carriers that can participate in conduction[112].

The impact of grain boundaries and trap states not only affects the threshold voltage, but also affects the effective mobility of polycrystalline channel. This chapter provides an analytical model for TFT threshold voltage and investigates grain boundary scattering dominated mobility. Moreover, as the design engineers need SPICE models for the simulation of large area flat panel displays (FPDs), they need to develop either a new TFT SPICE model or adapt an existing SPICE model effectively. For TFT simulation HSPICE LEVEL-40 is available but, its use is coverd by a license which limits its use in early development phase of transparent TFT technology [114]. This chapter also presents the adaption of SPICE LEVEL-3 model for TFT simulation and its validation with the experimental work. Finally, as ZnO TFTs primarily suffers from threshold voltage instability thereby, a detailed investigation on C–V instability is carried out for high−κ dielectrics and ZnO interface using experimental results and by fabricating metal insulator semiconductor capacitor (MIS-C) structure.

5.2 Analytical Model for Threshold Voltage

Polycrystalline semiconducting materials are composed of small crystallite separated by grain boundary. Since the atoms at the grain boundary are disordered, there are large number of defects that act as trapping states capable of trapping the mobile carriers. This reduces the number of free carriers available for conduction. These trapping states or localized states are distributed throughout the energy band gap of semiconductor. According to F. Torricelli *et al.* [54], localized states are concentrated at the band edges i.e. conduction band and valance band at lower disorder levels. However, at higher disorder level, the entire band is filled with localized states which can be illustrated by

means of density of states (DOS) that acts as a trap center for charge carriers. This distribution is due to interface defects and grain boundary traps. In ZnO TFT, shallow states arise due to metal interstitial, while deep states are due to oxygen vacancies. At room temperature, very few carriers are available at extended states for the conduction.

The threshold voltage of ZnO TFT is affected mostly by the defect states that exist in grain boundary. In order to turn on the TFT or to start a significant flow of current, an extra voltage other than flat band voltage (V_{FB}) needs to be supplied to overcome the trapped charge effects. To estimate this extra voltage ($|\psi|$), one can find out the potential resulting from grain boundary line charge at the gate [115]. The charged states in the grain boundary are assumed to form continuous 1-D line charge (λ) extended across width of TFT and located adjacent to the interface of gate dielectric and semiconducting channel as shown in Fig. 5.1.

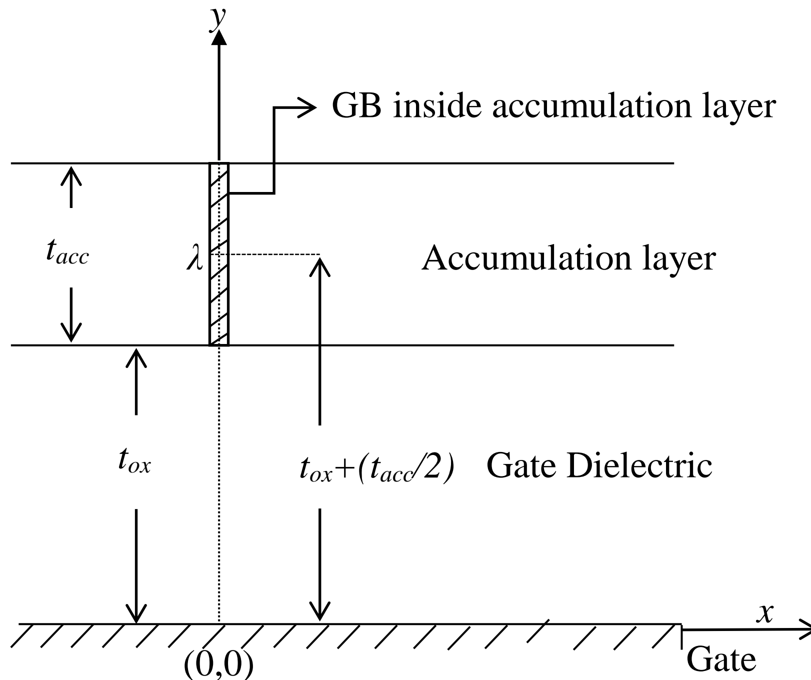


Fig. 5.1 Schematic of a bottom gate TFT system involving one dimensional line charge associated with a grain boundary present in ZnO semiconductor channel

The linear charge density λ is given as [115]:

$$\lambda = -qt_{acc}\int_{E_{igb}}^{E_f} D_{GB}(E)dE \quad \text{…(5.1)}$$

where, t_{acc} is the effective physical extent of the accumulation layer in the grain, adjacent to grain boundary. $D_{GB}(E)$ is the energy dependent DOS of the grain boundary. E_f is the Fermi level of ZnO and E_{igb} is intrinsic energy level or charge neutrality level of the grain boundary under flat band condition. Negative sign in eq. (5.1) reflects that the grain boundary traps are acceptor types which act as traps for electrons. The energy dependent acceptor type DOS for the ZnO TFT can be defined by single exponential function as [54]:

$$D_{GB}(E) = \hat{N}_t \exp\left(\frac{E - E_c}{k_B T_0}\right) \quad \text{…(5.2)}$$

In the DOS function $\hat{N}_t = (N_t / k_B T_0)$ $cm^{-2}\, eV^{-1}$, where k_B is the Boltzmann constant, T_0 is characteristic temperature and the value of $D_{GB}(E)$ is zero for $E > E_c$. The characteristic temperature T_0, is more for deep states than tail states and $k_B T_0$ represents amount of energy needed to ionize the trap. In similar manner, DOS function can be written for donor type traps but with respect to valance band edge (E_v). Using method of images and treating gate at ground potential as shown in Fig. 5.1, one can deduce the potential difference ψ between line charge and gate electrode as [115]:

$$\psi = \frac{\lambda}{2\pi\varepsilon_{ox}} \ln\left(\frac{2t_{ox} + (t_{acc}/2)}{(t_{acc}/2)}\right) \quad \text{…(5.3)}$$

From eq. (5.1) and (5.2), the 1-D line charge λ will become:

$$\lambda = -qt_{acc}N_t\left[\exp\left(\frac{E_f - E_c}{k_B T_0}\right) - \exp\left(\frac{E_{igb} - E_c}{k_B T_0}\right)\right] \quad \text{…(5.4)}$$

Fig. 5.2 shows the energy band diagram of poly-ZnO TFT channel consisting of a linear chain of discrete grain boundaries occupied with n−type carriers, at equilibrium ($V_{DS} = 0$ V).

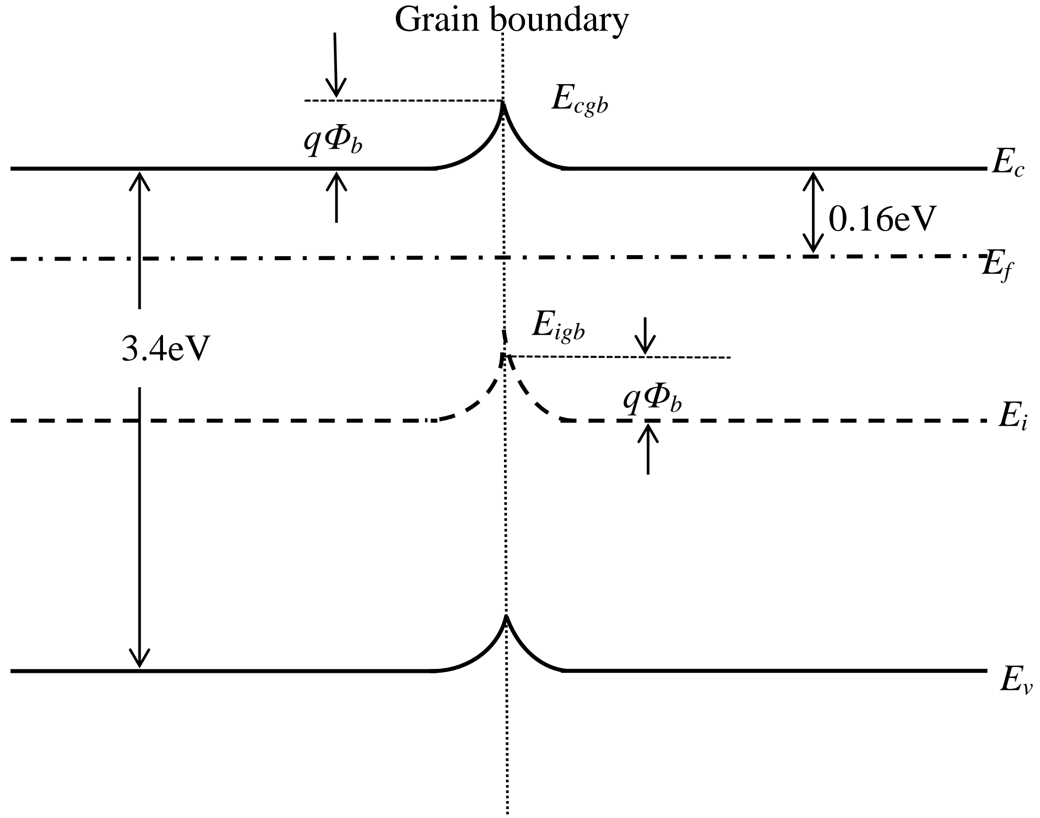


Fig. 5.2 Energy band diagram of ZnO TFT channel with potential barrier ($q\phi_b$) located at the grain boundary at equilibrium

From the band diagram, the difference between E_c and E_{igb} can be written as:

$$E_c - E_{igb} = \left[\frac{E_g}{2} - q\phi_b\right] \qquad \ldots(5.5)$$

Therefore,

$$\lambda = -qt_{acc}N_t\left[\exp-\left(\frac{E_c - E_f}{k_B T_0}\right) - \exp-\left(\frac{(E_g/2) - q\phi_b}{k_B T_0}\right)\right] \qquad \ldots(5.6)$$

This value of λ can be substituted in eq. (5.3) to get the potential difference $|\psi|$ between line charge and gate electrode as:

$$|\psi| = \frac{q t_{acc} N_t}{2\pi\varepsilon_{ox}}\left[\exp-\left(\frac{E_c - E_f}{k_B T_0}\right) - \exp-\left(\frac{(E_g/2) - q\phi_b}{k_B T_0}\right)\right]\ln\left(\frac{2t_{ox} + (t_{acc}/2)}{(t_{acc}/2)}\right) \quad \ldots(5.7)$$

$$[V_T = V_{FB} + |\psi|] \quad \ldots(5.8)$$

From the eq. (5.7) and (5.8) it is clear that, the threshold voltage of ZnO based TFT is directly related to grain boundary trap density N_t which means, higher the trap state density, more will be the threshold voltage. Moreover, V_T also depends on the dielectric constant of gate dielectric; higher the dielectric constant lower is the threshold voltage of ZnO TFT. Fig. 5.3 shows the grain boundary trap density N_t vs. $|\psi|$ for low−κ dielectrics (SiO_2, Si_3N_4) and high−κ dielectrics (ZrO_2 and La_2O_3).

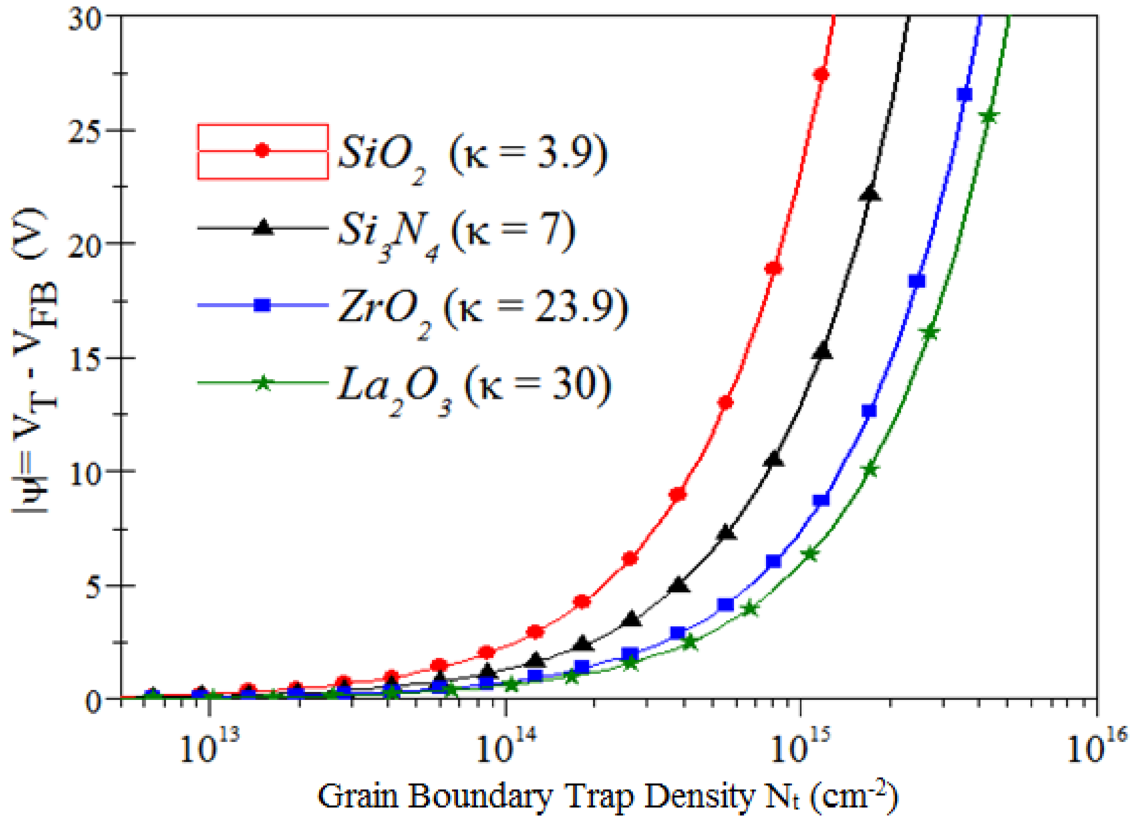


Fig. 5.3 Effect of grain boundary trap density (N_t) on threshold voltage (V_T) for different gate dielectrics.

For $N_t < 10^{13}$ cm^{-2} additional voltage ($|\psi|$) is not significant, but for higher disorder level e.g. $N_t = 10^{14}$ cm^{-2} this additional voltage ($|\psi|$) is a major contributor in threshold voltage for low−κ dielectrics such as SiO_2 and Si_3N_4 than high−κ dielectrics. For example, considering t_{ox} =200 nm, t_{acc} = 20 nm, T_0 = 625 K (for tail states), $q\phi_b$ = 0.226 eV and $N_t = 5 \times 10^{14}$ cm^{-2}. In case of SiO_2 gate dielectric, this additional voltage is about 11.64 V while for high−κ dielectric such as La_2O_3 and ZrO_2 this voltage is 1.50 V and 1.89 V respectively. Hence, the impact of grain boundary traps is more significant in low-κ dielectrics than high−κ dielectrics.

5.3 Mobility Model

As discussed in chapter-3, FE-SEM, AFM and XRD results confirmed polycrystalline deposition of undoped ZnO films. In polycrystalline material, several mechanism limits carrier transport, but primarily grain boundary scattering dominates. The grain boundary consists of few atomic layers of disordered atoms where large numbers of defects or trap states are present due to incomplete atomic bonding [116]. These trapping states trap the carriers and thus reduces the number of free carriers. As the carriers get trapped in grain boundaries, the surrounding region gets depleted and a potential barrier is formed. In case of polycrystalline ZnO, the barrier height is highest when depletion region is widest. Hence, thermionic emission is the only mechanism by which transport across grain boundary occurs [116]. If v_c is the mean velocity or collection velocity for the electron emitted over the barrier height (ϕ_b), the conduction current due to thermionic emission model is given by:

$$J = qnv_c \exp[-q/k_B T(\phi_b - V)] \quad \ldots(5.9)$$

where n is the free carrier density, T is absolute temperature, and V is the applied bias voltage across the depletion region. The collection velocity v_c is given by $v_c = \sqrt{k_B T / 2\pi m^*}$ where, m^* is the effective mass of an electron in ZnO. In equilibrium, carrier transport in the forward and reverse directions will result in equal forward current density J_F and reverse current density J_R, hence no net current flow. When an external

bias is applied, the barrier to carrier transport increases in one direction, while decreases in other. Generally, the applied voltage divides non-uniformly between the two sides of grain boundary; however, for small applied voltage, approximately half of the applied bias appears across each side of depletion region. Let us assume, voltage across single grain boundary V_{GB} is defined as the net applied bias across the polycrystalline channel divided by the number of grains, assuming all grain boundaries to be equivalent. Due to application of V_{GB}, the barrier height (ϕ_b) decrease in the forward direction and the barrier increase in the reverse direction by the same amount equal $|V| = V_{GB} / 2$.

Considering thermionic emission current in the two directions, the current density in forward and reverse direction (J_F and J_R respectively) is given by:

$$J_F = qnv_c \exp\left[-\frac{q}{k_B T}(\phi_b - \frac{1}{2}V_{GB})\right] \quad \text{...(5.10)}$$

$$J_R = qnv_c \exp\left[-\frac{q}{k_B T}(\phi_b + \frac{1}{2}V_{GB})\right] \quad \text{...(5.11)}$$

Hence, considering thermionic emission in both the direction, the net current density $J_{th} = (J_F - J_R)$ will become:

$$J_{th} = qnv_c \exp\left(-\frac{q\phi_b}{k_B T}\right)\left[\exp\left(\frac{qV_{GB}}{2k_B T}\right) - \exp\left(-\frac{qV_{GB}}{2k_B T}\right)\right] \quad \text{...(5.12)}$$

or

$$J_{th} = qnv_c \exp\left(-\frac{q\phi_b}{k_B T}\right)\sinh\left(\frac{qV_{GB}}{2k_B T}\right) \quad \text{...(5.13)}$$

For low applied voltage, i.e. $V_{GB} / 2 << k_B T / q$

$$\sinh\left(\frac{qV_{GB}}{2k_B T}\right) \approx \frac{qV_{GB}}{2k_B T} \quad \text{...(5.14)}$$

Simplifying eq. (5.13) using eq. (5.14); one can get a linear relation between current and applied voltage as follows:

$$J_{th} = \frac{q^2 n v_c}{k_B T}\left[\exp\left(-\frac{q\phi_b}{k_B T}\right)\right]V_{GB} \qquad \ldots(5.15)$$

If D_G is defined as average grain size, an expression for the average conductivity $\sigma = J_{th} / \mathrm{E} = J_{th} D_G / V_{GB}$ can be obtained from eq. (5.15) as:

$$\sigma = \frac{q^2 n v_c D_G}{k_B T}\exp\left(-\frac{q\phi_b}{k_B T}\right) \qquad \ldots(5.16)$$

Therefore, grain boundary scattering dominated mobility ($\mu_{GB} = q/ n\sigma$) can be defined as:

$$\mu_{GB} = \frac{q v_c D_G}{k_B T}\exp\left(-\frac{q\phi_b}{k_B T}\right) \qquad \ldots(5.17)$$

If the coefficient of exponential term is defined as μ'_{GB} then

$$\mu_{GB} = \mu'_{GB}\exp\left(-\frac{q\phi_b}{k_B T}\right) \qquad \ldots(5.18)$$

If D_G is given in *nm* and m^* (effective mass of electron in ZnO) is taken as 0.318 m_o [36], equation (5.18) can also be written as:

$$\mu_{GB}\left(cm^2V^{-1}s^{-1}\right) = 18.41 \times D_G \exp\left(-\frac{q\phi_b}{k_B T}\right) \qquad \ldots(5.19)$$

As discussed in chapter-3, the SEM and AFM results concluded that, an increase in ZnO film thickness results in increase in grain size (D_G). For different thickness of ZnO film, Fig. 5.4 shows the mobility in logarithmic scale vs. inverse of absolute temperature, keeping potential barrier $q\Phi_b = 6\ k_B\mathrm{T}$ (eV) in eq. (5.19). The thermionic emission based mobility model clearly shows that for low applied field, the thicker ZnO film shows higher mobility because of improved grain size.

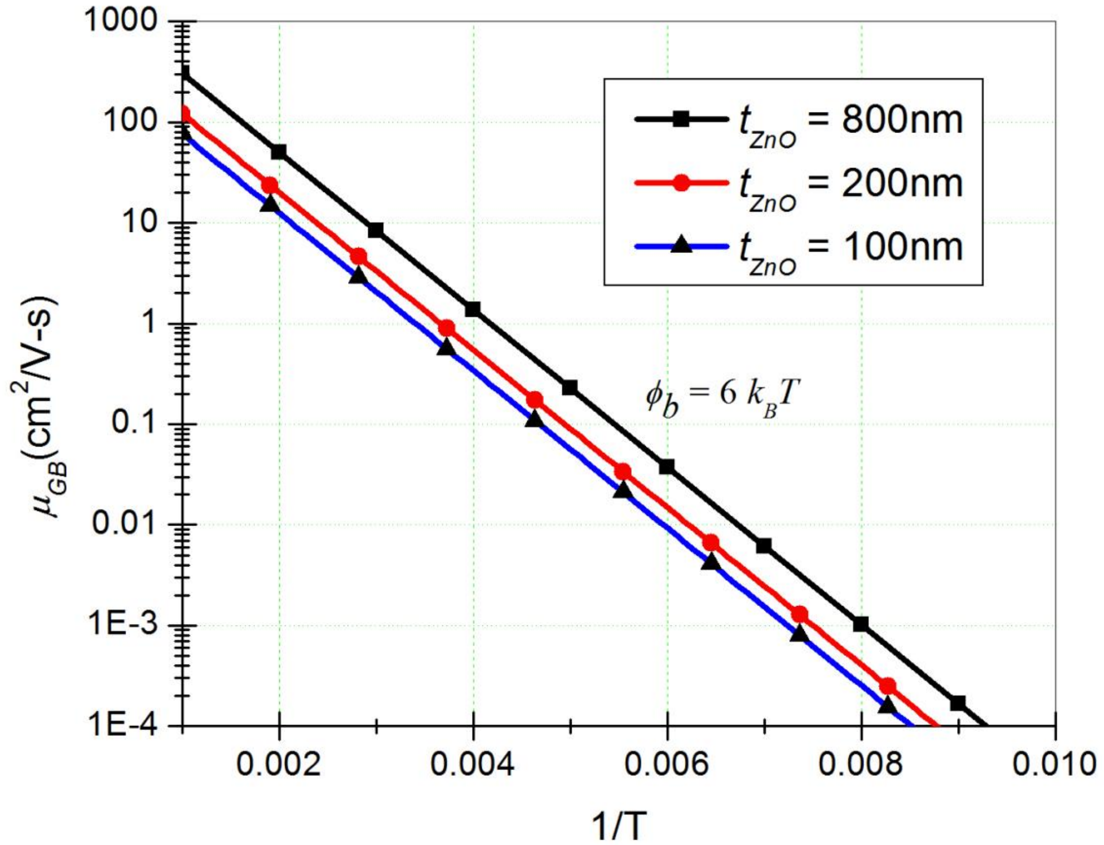


Fig. 5.4 Variation of mobility at grain boundary (μ_{GB}) vs. inverse of absolute temperature (1/T) for different ZnO film thicknesses

The case of single grain boundary can be further extended to multiple grain boundaries present in the polycrystalline channel. This model assumes that the polycrystalline ZnO channel is composed of equally sized grains separated by grain boundaries. Grain boundaries are aligned along the thickness (transverse direction) and along the channel (longitudinal direction) as shown in Fig. 5.5. The grains are partially depleted and depletion width associated to that is D_{dep}. Further one can compute the mobility due to transverse grain boundaries ($\mu_{GB\perp}$) and longitudinal grain boundaries ($\mu_{GB\|}$) and can take harmonic mean of those, to obtain effective grain boundary dominated mobility. However, earlier studies [117], [118] concludes that transverse grain boundaries degrades

the channel mobility more than the longitudinal grain boundaries. For longitudinal grain boundaries, direct crystalline path is available for the conduction from source to drain. Hence, effectively grain boundary scattering dominated mobility in polycrystalline channel (μ_{poly}) is equal to $\mu_{GB\perp}$.

To address the mobility due to transverse grain boundaries, this model considers an array of equally sized grains in the channel in which the current flows through the grains and transverse grain boundaries. Let us assume that, along the channel there are N_G number of grains separated by (N_G-1) grain boundaries. Fig. 5.6 shows a polycrystalline ZnO channel consisting of equal size grains (D_G) and transverse grain boundaries of width D_{GB}. Across each grain boundary, because of trapping of the carriers a potential barrier (ϕ_b) is formed which depletes the region around grain boundaries. The total channel resistance R_{net} can be calculated assuming series combination of resistances offered by grains and grain boundaries.

$$R_{net} = R_G N_G + (N_G - 1)R_{GB} \qquad \ldots(5.20)$$

If L is the channel length of polycrystalline ZnO channel, N_G can be defined as: $N_G = L/D_G$. If A is the cross sectional area and n is the carrier concentration, then R_{net}, R_G and R_{GB} further can be defined as:

$$R_{net} = \frac{L}{\sigma_{net} A}, \quad R_G = \frac{D_G}{\sigma_G A}, \quad R_{GB} = \frac{D_{GB}}{\sigma_{GB} A}$$

where, $\sigma_{net} = nq\mu_{GB\perp}$, $\sigma_G = nq\mu_G$, $\sigma_{GB} = nq\mu_{GB}$, μ_G is the mobility at grain and μ_{GB} is the mobility at grain boundary. Substituting these values in eq. (5.20) and further simplification gives:

$$\frac{1}{\mu_{GB\perp}} = \frac{1}{\mu_G} + \frac{1}{\mu_{GB}\left[\frac{N_G D_G}{(N_G - 1)D_{GB}}\right]} \qquad \ldots(5.21)$$

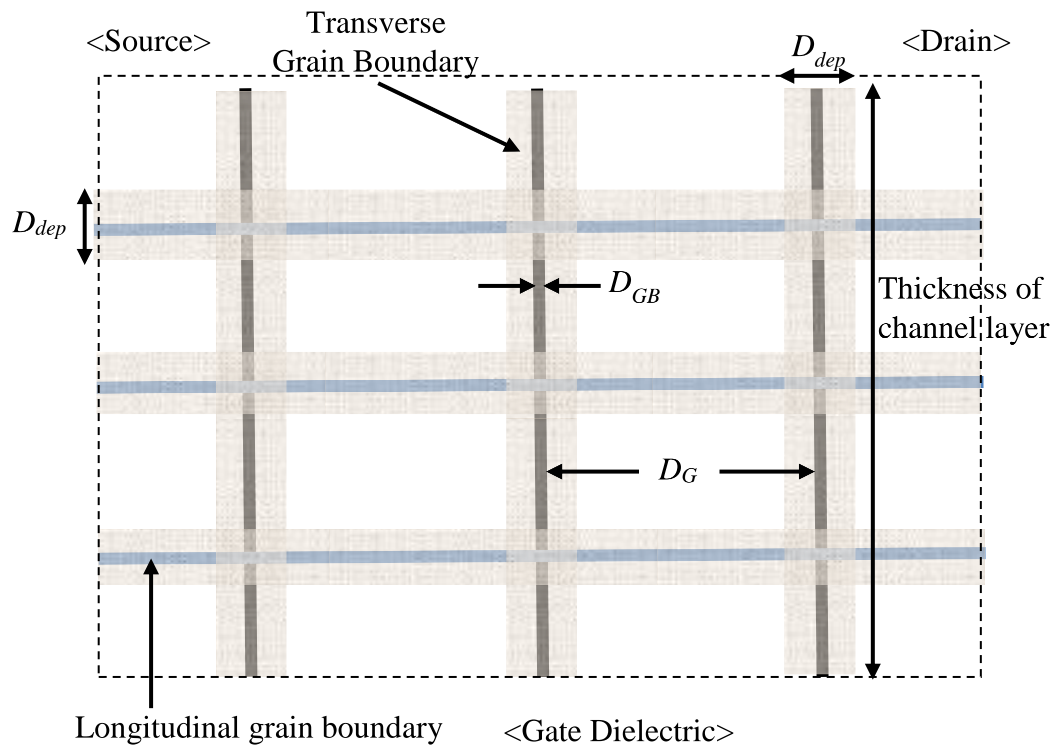


Fig. 5.5 Polycrystalline TFT Channel for bottom gate ZnO TFT

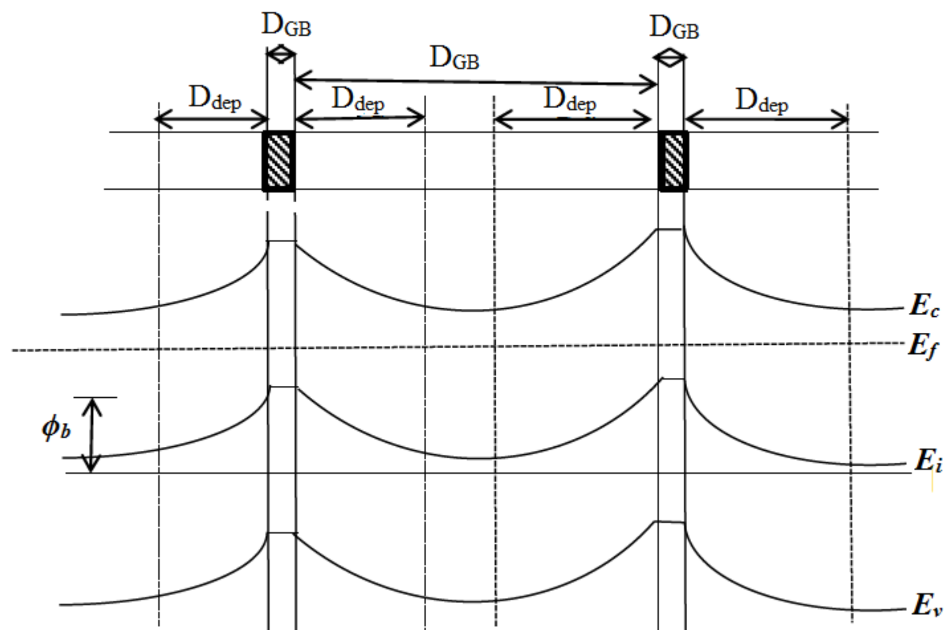


Fig. 5.6 Transverse grain boundaries in polycrystalline ZnO channel

After substituting the value of μ_{GB} from eq. (5.17), eq. (5.21) becomes:

$$\frac{1}{\mu_{GB\perp}} = \frac{1}{\mu_G} + \frac{1}{\frac{qv_c D_G}{k_B T}\exp\left(-\frac{q\phi_b}{k_B T}\right)\left[\frac{N_G D_G}{(N_G-1)D_{GB}}\right]} \quad \ldots(5.22)$$

In polycrystalline material, the mobility is defined as harmonic mean of mobility at grain (μ_G) and mobility at the grain boundary (μ_{GB}) multiplied by a constant term. In general, crystallite ZnO has a very high mobility (200 $cm^2V^{-1}s^{-1}$) compared to mobility at grain boundary [36], therefore second term consisting of μ_{GB} dominates in mobility equation. Hence, for long channel device ($L >> D_G$), $\mu_{GB\perp}$ can be written as:

$$\mu_{GB\perp} = \frac{\mu'_{GB} D_G}{D_{GB}}\exp\left(-\frac{q\phi_b}{k_B T}\right) \quad \ldots(5.23)$$

Eq. (5.23) and (5.17) indicates that the mobility of carriers in polycrystalline film increases with increase in grain size. Increase in grain size is also visualized as increase in crystallinity in the film, which means less number of grain boundary scattering encounters in carrier transport, hence better mobility will result in channel. Moreover, $\mu_{GB\perp}$ is also a function of barrier height, which itself depends upon dopant concentration. With increase in dopant concentration, ϕ_b first increases and reaches a maximum value when dopant concentration become equal to critical concentration ($N^* = N_t/L$), and is given by [116]:

$$\phi_b = \frac{qN}{2\varepsilon_{ZnO}} D_{dep}^2 \quad \ldots(5.24)$$

Where, D_{dep} is the depletion region width at one side of grain boundary and N_t is the grain boundary trap density. When the grains are completely depleted and traps are partially filled, D_{dep} becomes $D_G/2$, hence the barrier height can be expressed as:

$$\phi_b = \frac{qN}{2\varepsilon_{ZnO}}\left(\frac{D_G}{2}\right)^2 = \frac{qND_G^2}{8\varepsilon_{ZnO}} \quad \ldots(5.25)$$

According to J. Y. W. Seto [116], any further increase in dopant concentration ($N > N^*$), for partially depleted grains the barrier height reduces as:

$$\phi_b = \frac{qN}{2\varepsilon_{ZnO}}\left(\frac{N_t}{2N}\right)^2 = \frac{qN_t^2}{8\varepsilon_{ZnO}N} \quad \ldots(5.26)$$

Eq. (5.25) and eq. (5.26) shows non-monotonic behavior of barrier height with dopant concentration, which also affects electrical conductivity, and hence the mobility of polycrystalline material. From eq. (5.26) it is clear that, the barrier height decreases with increase in dopant concentration hence mobility improves. But, when dopant concentration in ZnO becomes more than 10^{20} cm^{-3} the columbic ionized impurity scattering starts dominating thus further reducing the mobility.

In TFT, the mobile carrier concentration varies with applied gate to source voltage V_{GS} as: $N = C_{ox}(V_{GS} - V_T)/qt_{acc}$. This implies that for sufficiently high value of V_{GS}, mobile carrier concentration in accumulation region increases thereby, the barrier potential (ϕ_b) drops significantly and carrier transport mechanism is governed by drift and diffusion mechanism than thermionic emission [115]. If low field mobility in a crystallite is defined as μ_0 and mobility degradation factor is defined as θ then, at sufficiently high V_{GS} the surface mobility is given by [17]:

$$\mu_s = \frac{\mu_0}{1+\theta(V_{GS} - V_T)} \quad \ldots(5.27)$$

Hence, effective mobility in all the regions can be defined as harmonic mean of thermionic emission dominated mobility ($\mu_{poly} = \mu_{GB\perp}$) and drift conduction dominated mobility μ_s.

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{GB\perp}} + \frac{1}{\mu_s} \quad \ldots(5.28)$$

Fig. 5.7 gives pictorial depiction of mobility vs. overdrive voltage (V_{GS}-V_T) and illustrates thermionic emission dominated and drift dominated regime. Modelling parameters μ_0, θ, D_G, D_{GB}, are taken as 22 $cm^2V^{-1}s^{-1}$, 0.04 V^{-1}, 40 nm and 2.5 nm

respectively [119]. Fig. 5.8 depicts mobility vs. (V_{GS}-V_T) for different grain sizes. The different grain sizes 25 nm, 40 nm and 96 nm were obtained from AFM characterization of ZnO film deposited using Zn metallic target as mentioned in Table 3.1. For low value of (V_{GS}-V_T) the conduction is dominated by thermionic emission while for its high value conduction is dominated by drift. However, in between these two regions dependency is complex which is shown as transition regime in Fig. 5.7 and Fig. 5.8.

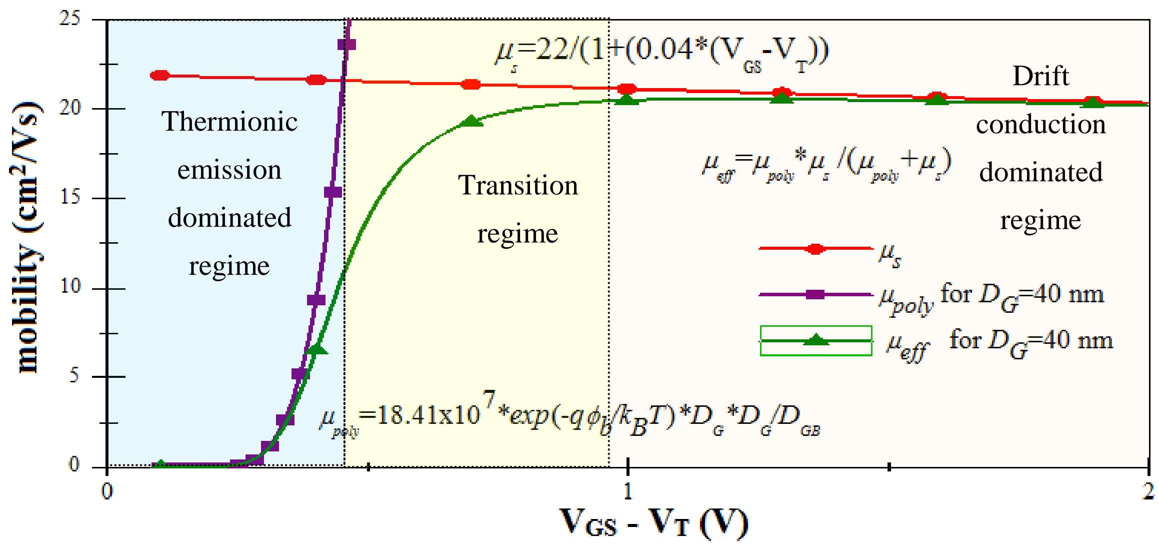


Fig. 5.7 Plot of effective mobility (μ_{eff}) versus overdrive voltage (V_{GS} - V_T), illustrating different conduction regime in ZnO based TFT

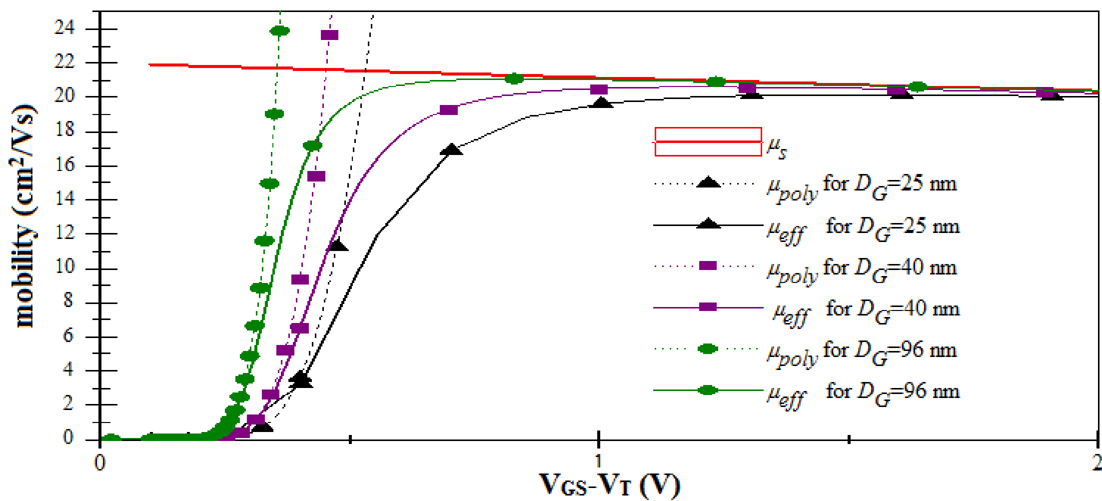


Fig. 5.8 Plot of effective mobility (μ_{eff}) versus overdrive voltage (V_{GS} - V_T) for different grain sizes

5.4 SPICE LEVEL-3 Model for ZnO TFT

This section describes the methodology to adapt SPICE LEVEL-3 models for ZnO based TFTs which are originally defined for MOSFETs.

5.4.1 Background

The computer aided design (CAD) tool compatible models have become a necessity for the implementation of ZnO based TFT circuits and systems. CAD always needs high speed, reliable and accurate device models. To achieve high level of accuracy, physical models based on device physics are required. But, physical models need not to be good for CAD as the equations originated from device physics could be very complex, thereby slow to execute and faces convergence problem. For poly-Si and a- Si:H based TFT technology several SPICE (Simulation Program with Integrated Circuit Emphasis) models were developed in past 30 years [120], [121]. SPICE is an open source, powerful general-purpose circuit simulator, used to verify circuit designs and to analyze circuit characteristics which are of utmost importance for integrated circuits. Till now, model developed by Rensselar Polytechnique Institute [120] has been used in many CAD simulators like Spectre, HSPICE and SmartSpice. However, so far in the area of oxide and organic TFT technology, no such model has become a standard because of rapid evolution of material and device structures. Although, there is growing interests in the area for implementation of circuits and systems using ZnO based TFT (e.g. IGZO, GZO and more), modeling efforts are still in their infancy. Compact SPICE LEVEL-3, known as semi-empirical Model, has exhibited best results for silicon MOSFETs. However, in this work, it is shown that LEVEL-3 model can be successfully employed as a behavioral model for ZnO based TFT.

Physical and empirical modelling approaches are usually defined to describe current conduction mechanism of any transistor in all the possible region of operation. In device modelling and simulation, major consideration is accuracy and speed of computation. Hence, developed model need not to be physical always. However, while using empirical

modelling, the device physics of the TFT device helps to minimize number of variables or parameters, hence enhances the computational speed and reduces complexity. SPICE LEVEL-3 model defined for silicon based MOSFET is both physical and empirical. As we have discussed, TFT and MOSFET have lots of similarity but they differ in their conduction mechanism. Hence, while extending SPICE LEVEL-3 model for oxide-TFT, we need to capture these differences.

5.4.2 Methodology

Fig. 5.9 gives the flow chart which describes the methodology used for adapting SPICE LEVEL-3 model for ZnO based TFT simulation. From the experimental characteristics of ZnO based TFT, extraction of various TFT performance parameter that includes subthreshold slope (SS), I_{on} to I_{off} ratio (I_{on}/I_{off}), effective mobility (μ_{eff}) and threshold voltage (V_T) is done. The SPICE parameter responsible for these performance parameters are identified and set to respective values. Table 5.1 gives information about key SPICE LEVEL-3 parameters and capture their effect on transfer and output characteristic of TFT. Apart from the parameters listed in Table 5.1 other process related parameters like sheet resistance of channel, parasitic capacitances, junction depth, corners etc. are needed to be provided to the LEVEL-3 model for high accuracy of simulation results.

SPICE LEVEL-3 gives unified model for current conduction in all the region [17]. Once the regional approximation is done, the following equations are used as the drain current equation for long channel ZnO based TFT ($V_{GS} > V_T$).

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 \text{ , } (V_{DS} \geq V_{GS} - V_T) \qquad \ldots(5.29)$$

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS} \text{ , } (V_{DS} \leq V_{GS} - V_T) \qquad \ldots(5.30)$$

Drain current equations, eq. (5.29) and eq. (5.30) defines current in saturation region and linear region respectively.

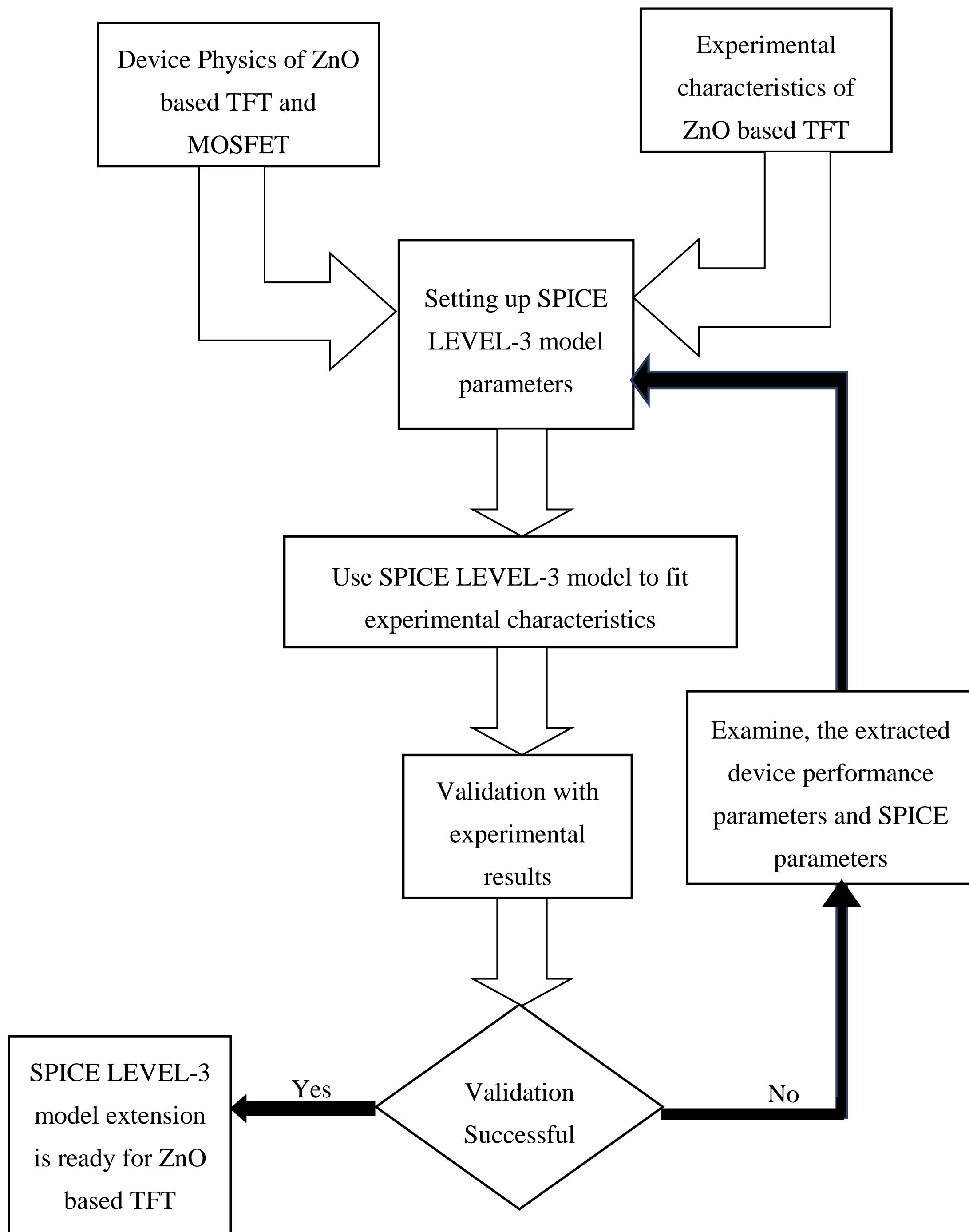


Fig. 5.9 Flowchart illustrating SPICE LEVEL-3 model adaption flow for ZnO based TFT.

Table 5.1 Key SPICE LEVEL-3 model parameters

SPICE Parameters	Description	Remarks
TOX (m)	Oxide thickness	By default defined for SiO_2. Therefore, if TFT employs high−κ gate dielectrics, TOX needs to be replaced by equivalent oxide thickness (EOT)
VTO (V)	Threshold voltage	To capture the effect of grain boundaries and interface trap density, analytical model of V_T eq. (5.7) can be directly used if N_t is known. Otherwise, from experimental characteristic V_T can be extracted.
NFS ($cm^{-2}V^{-1}$)	Fast surface state density	Captures the subthreshold behavior of oxide TFT. From the extracted value of subthreshold slope, the value of D_{it} can be obtained and NFS is replaced by qD_{it}.
RDS (Ω)	Drain-Source resistance	Decided by sheet resistance of ZnO channel and determine I_{off} current of TFT. RDS can be adjusted according to I_{off} value extracted from transfer characteristic of device.
UO ($cm^2V^{-1}s^{-1}$)	Low field bulk mobility	Effective low field mobility assuming grain boundary trap limited conduction doesn't dominate (Fig. 5.7). However, this approximation can introduce an error but still give acceptable accuracy.
THETA (V^{-1})	Mobility degradation factor	Define mobility degradation at high field, effective mobility (Fig. 5.7), need to be adjusted from μ_{eff} or μ_{FE} value.
RD, RS (Ω)	Drain/ Source resistance	Captures the effect of contact resistance.

The value of threshold voltage V_T can either be extracted from experimental characteristics or can be computed analytically using eq. (5.8), if N_t is known. In eq. (5.29) and (5.30), (W/L) is aspect ratio of the TFT and also known as design parameter. For sub-threshold ($V_{GS} < V_T$) conduction, dominating transport mechanism is diffusion, which is due to concentraion gradient between source and drain, for a certain value of V_{DS}. The diffusion current is given as [112]:

$$I_{Diff} = \mu_{eff} \frac{k_B T}{q} Q_{fi} \frac{W}{L} \exp\left(\frac{q}{k_B T} \left(\frac{V_{GS} - V_T}{1 + q^2 D_{it} / C_{ox}} \right) \right) \left(1 - \exp\left(\frac{-qV_{DS}}{k_B T} \right) \right) \quad \ldots(5.31)$$

where D_{it} is interface state density and Q_{fi} is weak inversion charge. However, off current (I_{off}) has two parts; one is diffusion current and other is current due to finite resistance of channel (RDS). As discussed in section 4.3, every dielectric has different conduction band offset to ZnO, thereby different leakage current. Hence, RDS can be adjusted according to extracted value of minimum I_{off}.

Using eq. (5.31) and eq. (1.1), the expression for subthreshold slope (SS) of the ZnO based TFT can be obtained as:

$$SS = \ln 10 \frac{k_B T}{q} \left(1 + \frac{q^2 D_{it}}{C_{ox}} \right) \quad \ldots(5.32)$$

In order to capture the subthreshold performance of the device using SPICE LEVEL-3, first SS value should be extracted from the experimental characteristic. Now, this can be used to determine the interface state density D_{it} value using eq. (5.32). In SPICE, NFS is replaced by qD_{it} to capture subthreshold performance of device.

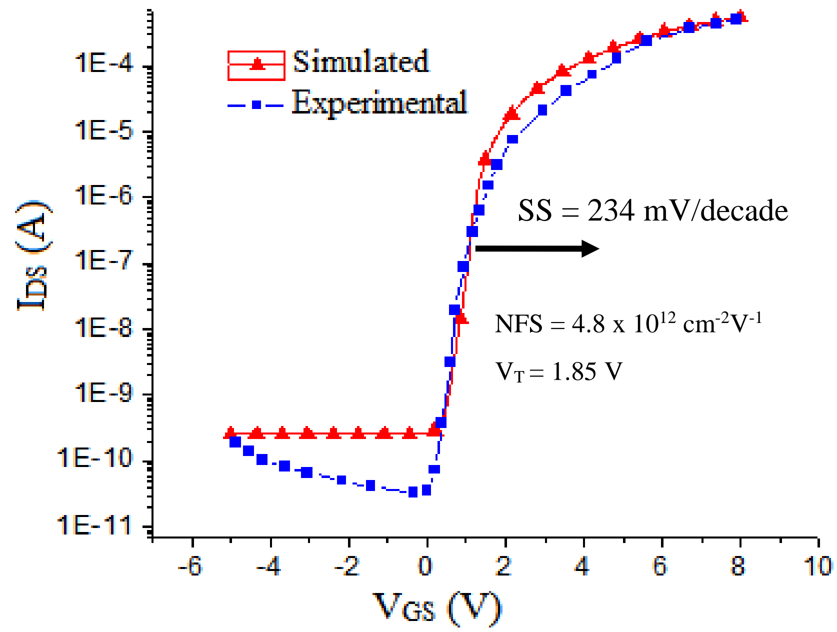
5.5 SPICE LEVEL-3 Model Validation

To validate the SPICE LEVEL−3 model for ZnO based TFT, the results are compared with experimental work on ZnO based TFT with high−κ dielectrics reported by L. X. Qian *et al.* (La_2O_3 gate dielectric)[109] and Xiao Zou *et al.* (HfO_2 gate dielectric) [122] . The device parameters reported in the experimental work are listed in Table 5.2. These parameters are used in SPICE LEVEL−3 model according to methodology discussed in previous section, and the simulated results are compared with experimental characteristics.

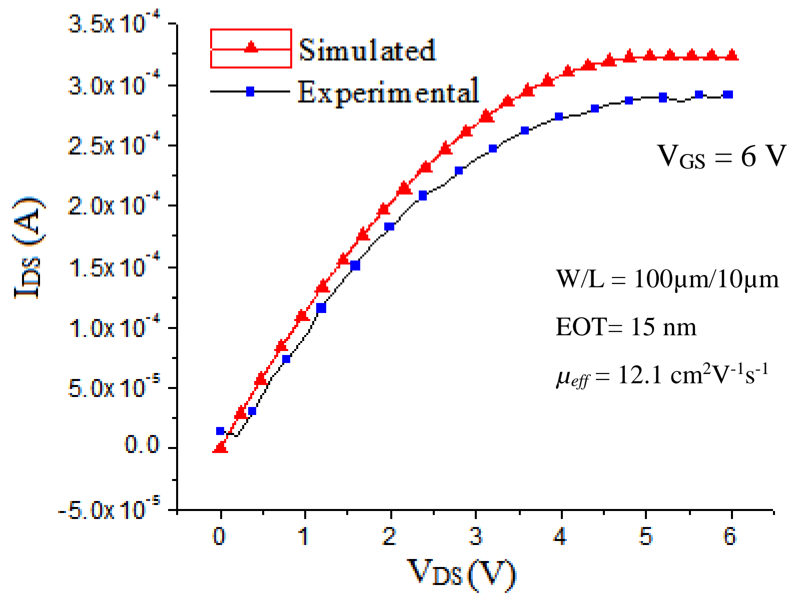
Table 5.2 List of device parameters used in analysis

Parameters	**La_2O_3** [109]	**HfO_2** [122]
Effective mobility ($cm^2V^{-1}s^{-1}$)	12.1	6.9
Gate oxide thickness (nm)	40	10
Dielectric constant	10.4	15.4
Subthreshold Swing (V/dec)	0.234	0.068
Aspect ratio, W/L (μm/ μm)	100/10	500/20
Threshold voltage (V)	1.85	0.33

Fig. 5.10 (a) and 5.11 (a) shows the simulated and experimental transfer characteristic of ZnO based TFT using La_2O_3 and HfO_2 gate dielectrics. Since, the drain current I_{DS} is shown in logarithmic axis, subthreshold slope can be determine by taking inverse of the slope of I_{DS} with respect to V_{GS}, in I_{DS}-V_{GS} curve. Simulated results shows excellent match with experimental results in subthreshold region. Fig. 5.10 (b) and 5.11 (b) shows the simulated and experimental output characteristic of ZnO based TFT using La_2O_3 and HfO_2 gate dielectrics. The maximum error in simulated and experimental curve is less than 10% hence, SPICE LEVEL-3 models for MOSFET can be extended as the behavioural model for ZnO based TFT with acceptable accuracy.

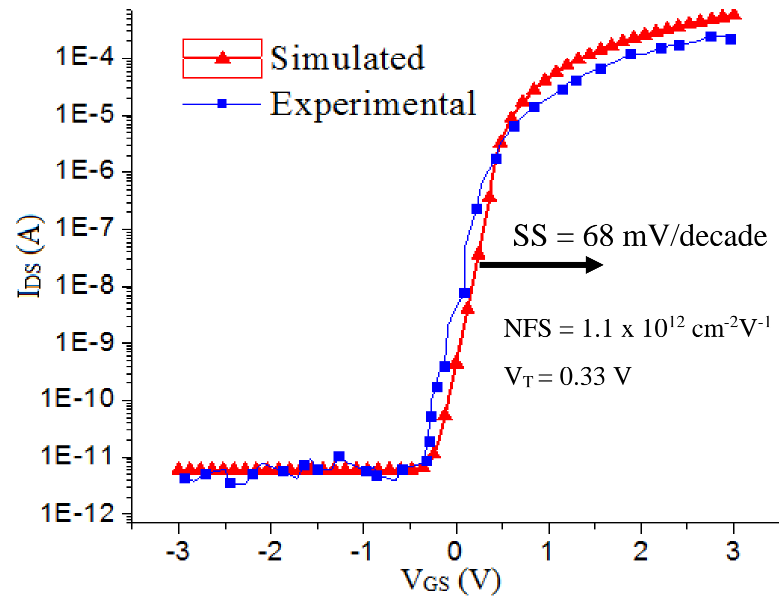


(a)

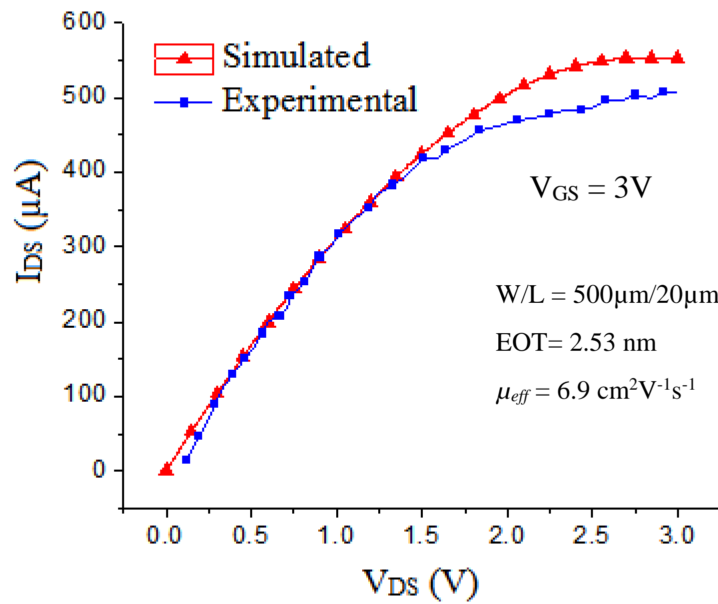


(b)

Fig. 5.10 Experimental [109] versus simulated characteristics of ZnO based TFT with La_2O_3 gate dielectric (a) Transfer characteristics, (b) Output characteristics



(a)



(b)

Fig. 5.11 Experimental [122] versus simulated characteristics of ZnO based TFT with HfO_2 gate dielectric (a) Transfer characteristics, (b) Output characteristics

5.6 Threshold Voltage Instability

As discussed in chapter-4 that ZnO TFT primarily suffers from the high threshold voltage. Though high−κ gate dielectric solves the problem of high threshold voltage to some extent but, threshold voltage instability (ΔV_T) still remains a concern. Threshold voltage instability is present in all kind of TFT and visible as a hysteresis voltage and translational shift in C−V characteristic. For reliable operation, this instability should be kept as minimum as possible. In this section we investigated the threshold voltage instability, by calculating the hysteresis voltage from C−V and/ or I−V characteristic of ZnO based TFT with high−κ gate dielectric. In these devices, La_2O_3 and ZrO_2 are considered as gate dielectrics. These two gate dielectrics were found as the promising gate dielectrics for low threshold voltage and low leakage operation as reported in chapter-4.

To investigate ZnO/ZrO_2 interface in detail, fabrication of MIS-C structure is done. Fabrication of MIS-C structure was done in CSIR- Central Electronics Engineering Research Institute, Pilani, India. ZrO_2 of thickness 120 nm is deposited on glass substrate using DC magnetron sputtering which is followed by the ZnO deposition using reactive RF-sputtering. This interface is studied using C−V and I−V characterization. Appendix section A.1− A.4 provides the detail of MIS-C fabrication and results of C−V and I−V characterization. From the results discussed in A.1- A.4, the I_{DS}−V_{GS} characteristic of the ZrO_2/ ZnO TFT is plotted using SPICE LEVEL-3 model and shown in Fig. 5.12. From C−V characterization, the hysteresis voltage for ZrO_2/ ZnO interface is found to be −1.4 V. From Fig. 5.12, it is clear that due to counter-clockwise hysteresis in C-V curve, V_T shifts to negative value in backward sweep, that disturb enhancement type operation of TFT. However, the hysteresis voltage itself depends upon oxide thickness as $\Delta V_H = (qN_{it}/C_{ox})$, and scales down with decreasing oxide thickness. Hence, for scaled devices, this hysteresis voltage is less, which in turn, gives lesser V_T shift, but still enough for varying pixel illumination intensity and causing instability.

The work of L. X. Qian *et al.* [109] is also used in this study to investigate ZnO/ La_2O_3 interface for TFT application. They fabricated ZnO based TFT with La_2O_3 gate dielectric

using RF sputtering. The physical thickness of deposited La_2O_3 was 40 nm. Hysteresis property of ZnO/ La_2O_3 was investigated using transfer characteristics measured under forward and reverse V_{GS} sweep and shown in Fig. 5.13. This work also shows a counter clockwise hysteresis of -0.76 V.

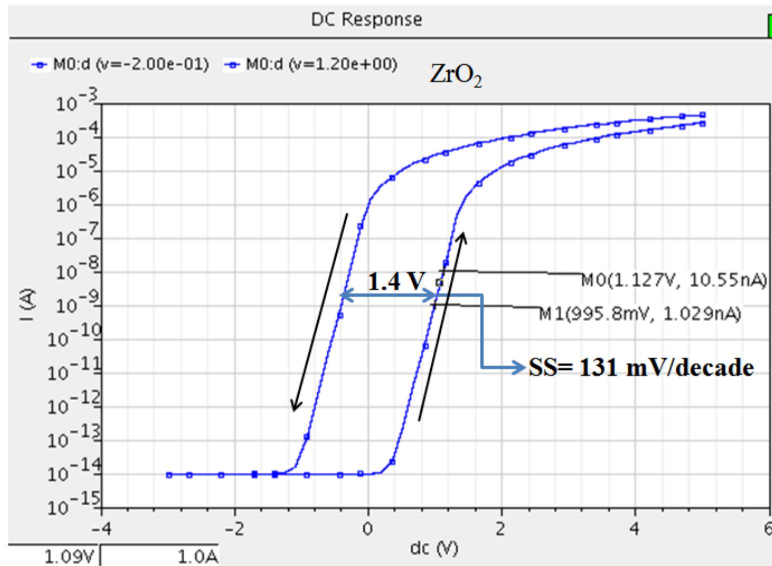


Fig. 5.12 Transfer characteristic of ZnO/ ZrO_2 based TFT under forward and reverse V_{GS} sweep.

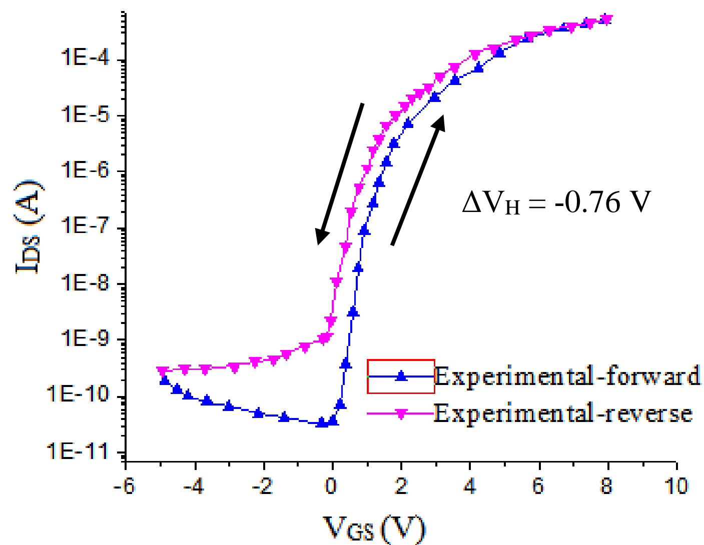


Fig. 5.13 Transfer characteristic of ZnO/ La_2O_3 based TFT under forward and reverse V_{GS} sweep [109]

From the Fig. 5.12 and 5.13, it is clear that ZnO based TFT exhibits counter-clockwise hysteresis. The main reason of counterclockwise hysteresis is the existence of oxygen vacancies in the gate dielectric and in the ZnO. High number of oxygen vacancies are originated during ZnO sputtering which act as donor-like traps at the interface. These states are neutral when occupied and become positively charged when ionized. These traps become positively charged during forward sweep by releasing electron and trapping hole.

Fig. 5.14 gives a pictorial depiction of the presence of donor and acceptor like traps in ZnO band gap at the interface with dielectric. For ZnO, charge neutrality level (CNL) is very near to conduction band edge (3.27 eV upwards from the valence band edge) [97]. CNL level separates donor like traps and acceptor like traps and this is defined as the energy level below which the surface states must be filled for the charge neutrality at the interface. However, in case of ZnO, some of the donor like trap remain uncovered from the Fermi level and become positively charged by releasing an electron. The positive charge at the interface screens the gate voltage during backward sweep thereby, decreasing the threshold voltage.

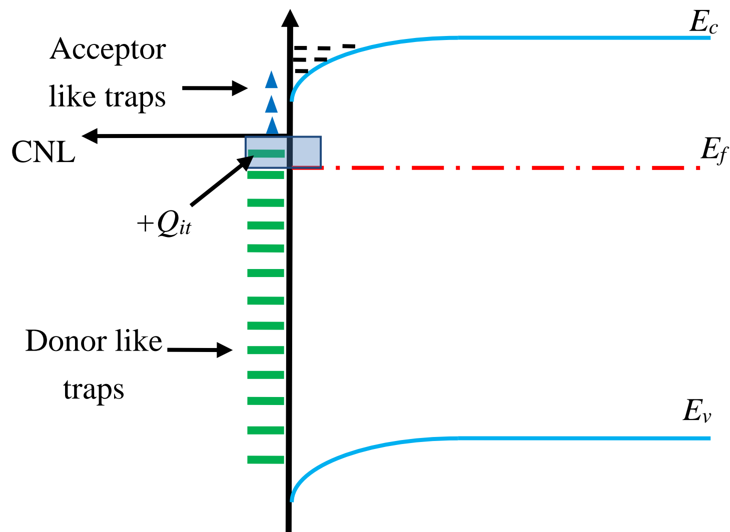


Fig. 5.14 Band diagram at ZnO/ dielectric interface showing charge neutrality level (Shaded region denotes unoccupied donor like traps at the interface)

5.7 Conclusion

This chapter provided an analytical model for threshold voltage (V_T) of polycrystalline-ZnO TFT as a function of grain boundary trap density and dielectric constant of gate dielectric. This model assumes grain boundary as continuous one dimensional line charge and concludes that for higher density of grain boundary traps, threshold voltage of ZnO TFT increases. The effect of grain boundary dominated scattering in mobility is also discussed in detail and it is obtained that, the thermionic emission dominated regime in ZnO based TFT is limited to low value of overdrive voltage. This discussion was followed by successful adaption of SPICE LEVEL–3 model for ZnO based TFT. This provided behavioral model for ZnO based TFT with good accuracy.

Finally, this chapter provided an investigation on threshold voltage instability of ZnO based TFT by examining hysteresis voltage, from transfer characteristic. To measure the C–V hysteresis, fabrication of ZnO/ ZrO_2 MIS–C structure is done and C–V plots in forward and reverse sweep were plotted. The work of L. X. Qian *et al.* was also used to investigate ZnO/ La_2O_3 interface. The hysteresis voltage was found to be -1.4 V and -0.76 V for ZrO_2 and La_2O_3 gate dielectric respectively. Due to counterclockwise hysteresis not only the threshold voltage instability is caused, but also the I_{off} current (defined at V_{GS} = 0 V) increases by several order, thereby increases the standby power consumption of a TFT panel.

It was observed that even top ranked dielectrics like, La_2O_3 and ZrO_2 (as reported in chapter-4) also suffer from threshold voltage instability as determined by experimental results. Hence for reliable operation of TFT, apart from low leakage and low threshold voltage it is also important to have a clean and charge free dielectric/ ZnO interface. This can eliminates threshold voltage instability issues. Theoretical analysis reveals that, the main reason of counterclockwise hysteresis is the existence of oxygen vacancies in the gate dielectric which may be originated during ZnO sputtering. Though, the hysteresis voltage scales down with decrease in dielectric thickness, yet, the interface needs to be further optimized for almost zero hysteresis voltage.

CHAPTER - 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

The objective of the thesis was to investigate electronic behavior and stability issues of ZnO based TFT. In order to achieve the research goals, following objectives were made:

1. Room temperature deposition of ZnO thin film, for analyzing structural and electrical properties.
2. Identification of optimal gate dielectric material from a pool of dielectrics for low leakage and low threshold voltage operation.
3. Development of analytical model for threshold voltage and effective mobility for polycrystalline ZnO TFT.
4. Adaption of existing SPICE model for behavioral modelling of ZnO based TFTs to facilitate design engineers.
5. As all kind of TFT suffers from threshold voltage instability, therefore study of ZnO- dielectric interface using C–V and I–V characterization and theoretical investigation on the cause of instability.

To get better insight of ZnO based TFT technology, a detailed literature review was done on ZnO based TFT and its performance parameters. Fabrication process flow of bottom gate ZnO based TFT using back side ultraviolet (BUV) exposure with two mask steps was also reported. Moreover, electrical instability due to prolonged stress, and time dependency of the threshold voltage instability using an empirical stretched exponential relation was also discussed in detail.

The room temperature deposition using RF magnetron sputtering was carried out and discussed in chapter-3. Zn metallic target and ZnO ceramic target was used for sputtering. In both the cases, polycrystalline nature of deposited ZnO film was confirmed. It was also observed that crystallinity of film improves with increase in film thickness. ZnO film deposited using ZnO target offered ideal stoichiometry and low sheet resistance, while ZnO film deposited using Zn metallic target were more oxygen rich and exhibited high sheet resistance which gave an advantage over ZnO deposition using ZnO target in terms of higher deposition rate.

Choice of gate dielectric played an important role in determining leakage and threshold voltage of TFT. ZnO TFT suffers from high threshold voltage requirements, which makes display panels power hungry. In order to address this issue, a detailed investigation on potential high−κ dielectrics was done to propose optimal gate dielectric using three material selection methodologies namely Ashby, TOPSIS and VIKOR. Band-gap, dielectric constant and thermal coefficient mismatch between dielectric and ZnO layer were taken from literature, while conduction band offset of high−κ dielectric on ZnO was computed analytically. From all the three analysis, top three ranked materials are La_2O_3, HfO_2, and ZrO_2 respectively.

Polycrystalline nature of ZnO film was confirmed from structural characterization. Thus, effect of grain boundaries or structural disorder was examined in analytical model of threshold voltage and mobility. In ZnO based TFT, current conduction is achieved by formation of an accumulation layer, i.e. no polarity inversion of induced carriers like in MOSFET. Most of the researchers have defined flat band voltage as the threshold voltage of accumulation mode TFTs, but this definition has failed to define a very high threshold voltage reported in low−κ gate dielectric based ZnO TFTs. Due to polycrystalline nature of ZnO channel, carriers gets trapped in grain boundaries and hence very few carriers are available for conduction at the room temperature. This leads to requirement of additional voltage other than V_{FB} to be applied for significant flow of current. This work provided an analytical model for threshold voltage of polycrystalline ZnO based TFT as a function of grain boundary trap density and dielectric constant of gate dielectric. It assumes grain boundary as continuous 1–D line charge averaged over single exponential density of state

function in ZnO band-gap. It concludes that for higher density of grain boundary traps, the threshold voltage increases. However, incorporation of high−κ gate dielectric can minimize the effect of grain boundary trap density on threshold voltage by providing strong coupling of gate field to the channel.

For effective mobility of ZnO based TFT, a detailed mobility model was proposed. That model investigated thermionic emission dominated and drift conduction dominated regime. The model assumes rectangular grain boundaries across the thickness and length of ZnO channel. It is found that perpendicular grain boundaries scattering dominates the conduction for low overdrive voltage, while for high value of overdrive voltage, the conduction is primarily dominated by drift conduction mechanism.

A compact SPICE-LEVEL-3 model was then adapted as behavioral model for ZnO based TFT. It captures the effects related to high−κ dielectric like higher oxide capacitance and different leakage current than SiO_2 using equivalent oxide thickness and channel resistance. Subthreshold behavior was captured using interface state density (D_{it}). Threshold voltage and low field mobility was directly extracted from experimental characteristics. Further, the experimental work of L. X. Qian *et al.* [109] and Xiao Zou *et al.* [122] was used to validate the SPICE LEVEL–3 model. In order to investigate, stability related issues in ZnO based TFT, fabrication of MIS-C structure using ZrO_2 gate dielectric was reported. It also used experimental work reported by L. X. Qian *et al.* [109] with La_2O_3 gate dielectric. In both the cases, counter clockwise hysteresis was obtained. Theoretical investigation revealed that main reason of counter clockwise hysteresis was oxygen vacancies present in gate dielectric and in ZnO - dielectric interface. Though the hysteresis voltage scales down with scaling the TFT dimensions, a small value of hysteresis voltage can adversely affect the pixel luminescence. Hence for reliable operation, it is required to have hysteresis free operation.

6.2 Future Scope of the Work

In depth literature review and experimentation have opened up future possibilities of ZnO based TFT research. Following are the few areas which can be further explored.

- This work provided a detailed investigation on potential gate dielectric materials using material selection methodology for low operating voltage and low leakage ZnO based TFT. However, experimental study needs to be carried out to study ZnO dielectric interface. It can give better insight on reliability and robustness of device.
- Like silicon on insulator (SOI) devices, ideally TFT can also provide a subthreshold slope equal to 60 mV/ decade, as substrate is insulator. However, the biggest hurdle is high value of interface state density (D_{it} = 10^{11} – 10^{13} $cm^{-2}eV^{-1}$). Efforts need to be put forward to optimize ZnO-dielectric interface to minimize the D_{it} value.
- For successful use of ZnO based TFT in display devices, robustness is expected. To investigate electrical instability device can be tested in four practical stress conditions that includes positive / negative bias, illumination, temperature and environment. To achieve more robustness, optimizing the structure, use of suitable gate dielectric material, passivation layers and robust semiconductor channel can help.
- Mobility model defined in this work assumes perpendicular and longitudinal grain boundaries. However, in practical case grain boundaries mostly are tilted. Hence, the effect of tilt angle of grain boundary with respect to channel can be introduced in mobility model or a correction factor can be proposed.
- In order to achieve high switching speed, effective mobility is a key factor. Currently, contemporary technologies like LTPS TFT [123] are offering a mobility upto 100 $cm^2V^{-1}s^{-1}$. The mobility requirement of HD AMOLED television is typically 30 $cm^2V^{-1}s^{-1}$[123]. As discussed, the polycrystalline material encounters grain boundary scattering thereby resulting in low effective mobility. Hence, effort needs to be undertaken to increase the mobility of ZnO based TFT. One way is to deposit single crystalline ZnO, but it may require high thermal budget and can restrict the choice of substrate material. However, another choice is the use of amorphous structure of oxide semiconductor. The key property which enables amorphous structure is “crystal frustration” i.e. use of different materials (In, Sn and Zn) where all try to form their

own crystal structure, resulting in amorphous structure.

- So far we have restricted our work either in silicon substrate or glass substrate. However, ZnO based TFT are also getting popular with flexible substrate. One need to fabricate ZnO based TFT in plastic substrate and check its performance (like V_T, μ_{eff} etc.) with upward and downward bending of the substrate.

APPENDIX

A.1 Fabrication of MIS-C Structure

A ZnO / ZrO_2 Metal-Insulator-Semiconductor (MIS) structure was fabricated on Corning glass (1737) substrate. Corning glass (1737) substrate is selected because these substrates are widely used for active matrix flat panel displays. MIS−C structure is typically a four layer structure consists of bottom gate electrode (Pt), the gate dielectric (ZrO_2), semiconductor (ZnO) and top ohmic metal contact (Ti/Au), as shown in Fig. A.1.

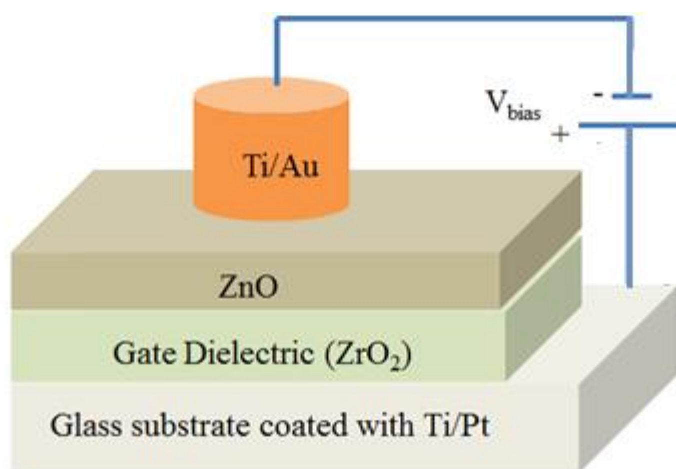


Fig. A.1 Schematic representation of bottom-gate MIS structure.

Initially substrates were chemically cleaned using acetone, methanol and ultrasonic method. To form a bottom gate contact, Ti (20 nm)/Pt (200 nm) was deposited using DC magnetron sputtering. Seed layer titanium (Ti) was deposited to promote adhesion of platinum (Pt) on glass substrate. Now, the deposition of Zirconium oxide (ZrO_2) was carried out using reactive sputtering process. ZrO_2 was deposited using a metallic Zr target with DC power of 120 W and sputter pressure of 10 mTorr. A deposition rate of

0.33 Å/s was achieved for ZrO_2 gate dielectric. For an hour long deposition, ZrO_2 film thickness was 120 nm as measured using step profiler (DEKTEK). Further, 800nm thick ZnO film was deposited at room temperature using reactive sputtering. The top electrode was deposited using a customized shadow metal mask which has circular through holes. Ohmic contacts of Ti (20 nm)/Au (200 nm) of different diameters (2.1 mm, 1.6 mm, 1 mm and 0.5 mm) were deposited using DC sputtering. Corner edge of substrate was etched in wet chemical solution to access the bottom electrode. Fig. A.2 shows optical micrograph image of top view of MIS structure and XRD spectra of ZnO thin film deposited on ZrO_2 gate dielectric. Diffraction peak at an angle $2\theta = 34°$ corresponds to strong c-axis oriented phase (002) of hexagonal wurtzite structure of ZnO. The peak at $2\theta = 39.9°$ corresponds to gate electrode Pt (111).

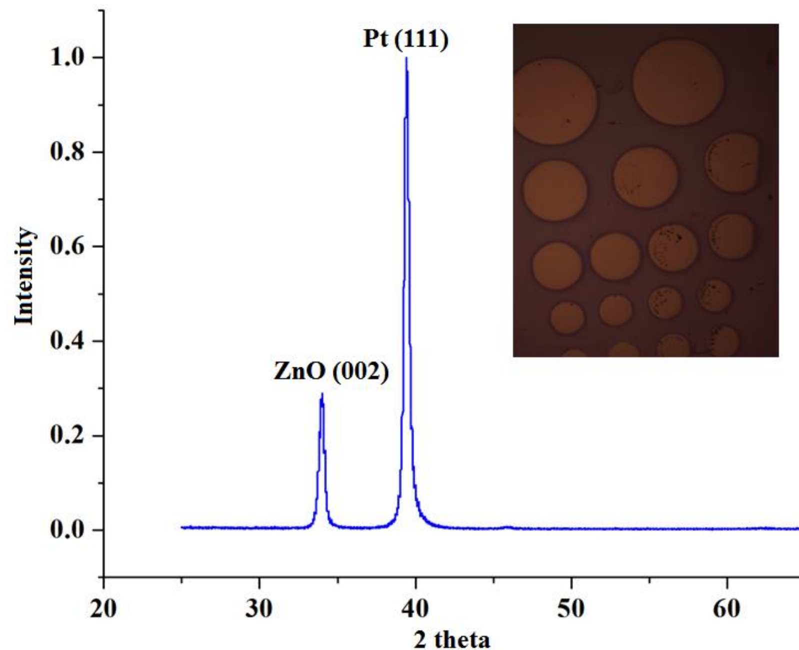


Fig. A.2 Optical micrograph image of MIS-C structure and XRD spectra of ZnO Film deposited over ZrO_2 gate dielectric

A.2 MIS-C (ZrO_2/ ZnO) C-V Characterization Results

Semiconductor device analyzer (Agilent B1500A) was used to measure C−V and I−V characteristics of MIS-C device. C−V curve was dual swept, biased at maximum positive voltage of 3 V for 10 seconds, then swept backward and forward at a constant rate of 0.6 V/sec. Net capacitance of MIS−C structure can be seen as the capacitance of depletion region that forms in ZnO in series with the capacitance of dielectric. For gate to bulk voltage (V_{bias}) greater than the flat band voltage (V_{FB}), MIS-C structure is said to be in accumulation region; while for V_{bias} less than V_{FB}, MIS-C structure is in depletion region. For the MIS structure shown in Fig. A.1, the ϕ_{ms} is work function difference of bottom platinum gate contact ($q\phi_m$= 5.65 eV) with ZnO semiconductor ($q\phi_s$= 4.45 eV). Fig. A.3 shows C−V measurement curve of ZrO_2 gate dielectric. From the C−V analysis of ZrO_2 MIS-C, the dielectric constant of deposited ZrO_2 dielectric is found to be 23.9 and flat band voltage shift (ΔV_H) is -1.4 V. The C−V characteristic of ZrO_2 MIS−C devices gives a counter-clockwise hysteresis.

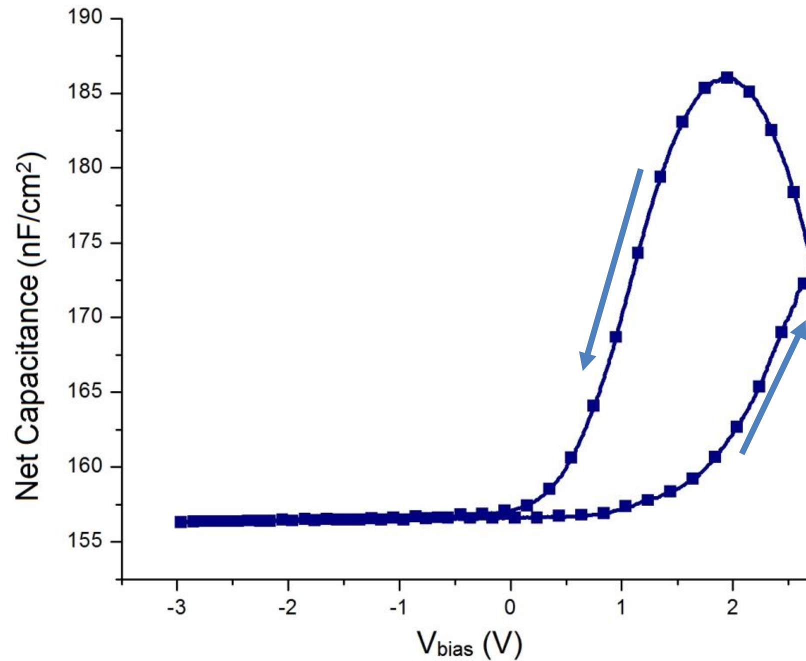


Fig. A.3 High frequency (at 1 MHz) capacitance-voltage (C-V) analysis of ZrO_2/ ZnO MIS Structure

A.3 MIS-C (ZrO_2/ ZnO) D_{it} Measurement Results

Measurement of D_{it} is done using conductance technique proposed by Nicollian and Goetzberger [124]. It measures, MIS−C equivalent circuit's admittance real part, known as parallel conductance (G_P) with frequency as a sweep parameter. G_P is a function of interface density and capture time constant. Fig. A.4 shows the Gp/ω curve with frequency as a sweep parameter. The peak at higher frequency corresponds to slower interface trap than a peak at lower frequency (i.e. 3 MHz.). The value of D_{it} can be computed using[124]:

$$D_{it} = \left[\left(\frac{G_P}{\omega}\right)_{peak}\right]\left[\frac{2.5}{q}\right] \tag{A.1}$$

From Fig. A.4 and eq. (A.1), the value of D_{it} for ZrO_2 and ZnO interface is found to be 1.28×10^{12} $cm^{-2}eV^{-1}$. This value of D_{it} can be substituted in eq. (5.32) to obtain subthreshold slope (SS), which is found to be 131 mV/ decade.

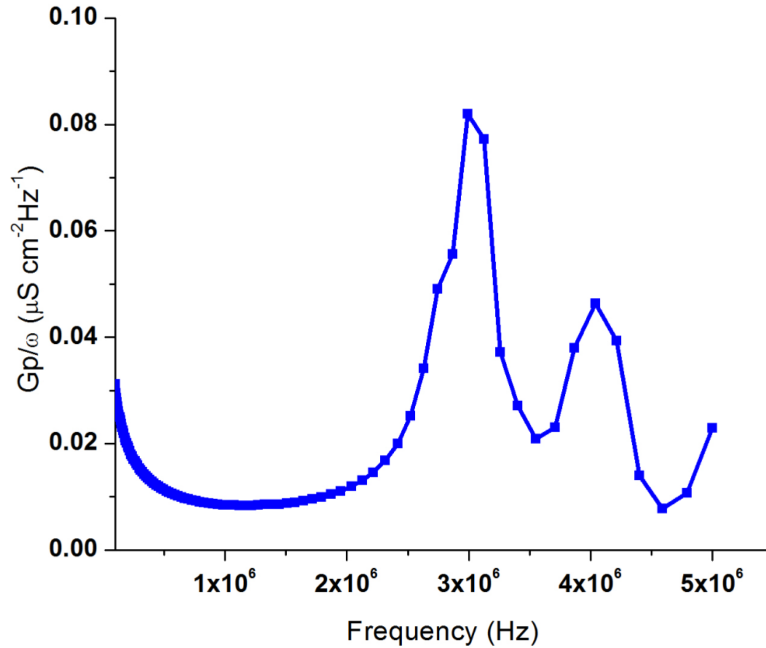


Fig. A.4 Gp/ω graph with respect to frequency to find out interface state density (D_{it})

A.4 MIS-C (ZrO_2/ ZnO) I-V Measurement Results

Fig. A.5 shows the leakage current density (J) with respect to gate bulk voltage (V_{bias}). For ZrO_2 gate dielectric the leakage current density (J_{GL}) is 2.94×10^{-7} Acm^{-2}. For any gate dielectric, gate leakage current density goes up exponentially with decrease in gate insulator thickness due to tunneling. The main reason of good leakage performance of ZrO_2 is its very good conduction band offset to ZnO ($\Delta E_c = 2.1$ eV).

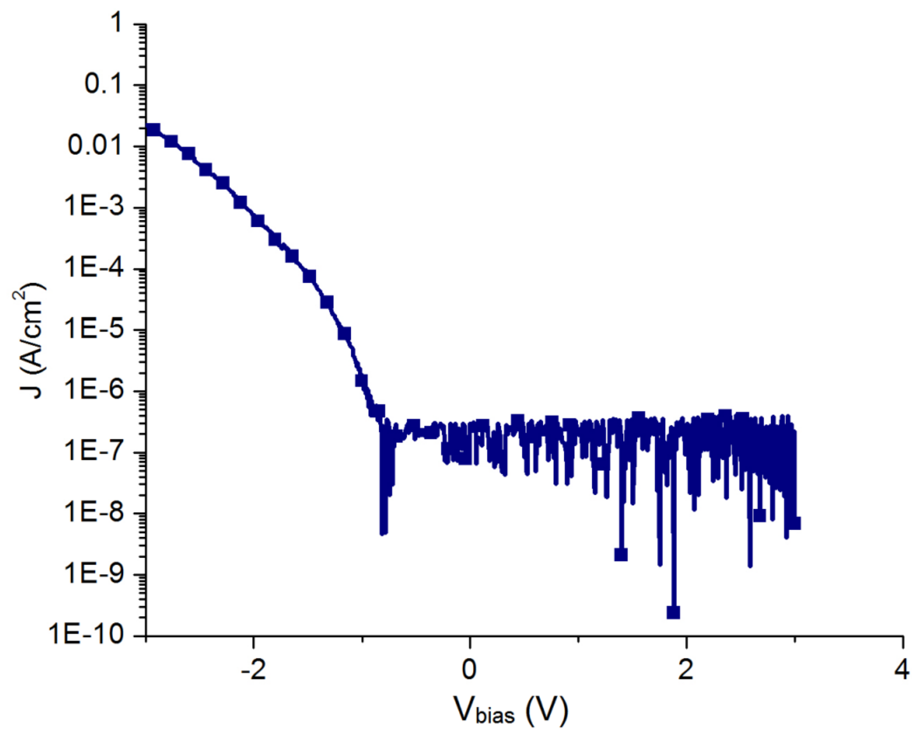


Fig. A.5 Gate leakage current density versus applied gate to bulk bias (V_{bias}) for ZrO_2/ ZnO MIS- structure.

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LIST OF PUBLICATIONS

Publications in Peer Reviewed Journals:

1. **Kavindra Kandpal** and Navneet Gupta, “Perspective of Zinc Oxide based Thin Film Transistors: A Comprehensive Review” *Microelectronics International (Emerald Publishing),* vol. 35, issue 1, pp. 52-63, 2018. **[SCOPUS, SCIE]**
2. **Kavindra Kandpal** and Navneet Gupta, "Study of structural and electrical properties of ZnO thin film for thin-film transistor (TFT) applications" *Journal of Materials Science: Materials in Electronics (Springer)*, vol. 28, issue 21, pp. 16013-16020, 2017. **[SCI indexed]**
3. **Kavindra Kandpal** and Navneet Gupta, “Investigations on high−κ dielectrics for low threshold voltage and low leakage Zinc Oxide Thin-Film Transistor, using material selection methodologies” *Journal of Materials Science: Materials in Electronics (Springer)*, vol. 27, issue 6, pp. 5972-5981, 2016. **[SCI Indexed]**
4. **Kavindra Kandpal**, Jitendra Singh, Navneet Gupta and Chandra Shekhar, “Effect of Thickness on the Properties of ZnO Thin Films Prepared by Reactive RF Sputtering”, *Journal of Materials Science: Materials in Electronics (Springer)*, April 2018. [SCI Indexed] [communicated]
5. **Kavindra Kandpal,** Navneet Gupta, Jitendra Singh and Chandra Shekhar, “On the Threshold Voltage and Performance of ZnO based Thin Film Transistors with ZrO_2 Gate Dielectric”, *IEEE* Transactions on Electron Devices, February 2018. [SCI Indexed] [communicated]
6. **Kavindra Kandpal** and Navneet Gupta, “Adaption of compact SPICE LEVEL-3 model for Oxide Thin Film Transistors”, *IET Electronic Letters*, April 2018. [SCI Indexed] [communicated].

Peer Reviewed Conferences and Workshop Attended

1. **Kavindra Kandpal**, Jitendra Singh, Navneet Gupta and Chandra Shekhar, "Effect of Thickness on the Properties of ZnO Thin Films Prepared by RF Sputtering", *17th International Conference on Thin Films (ICTF-2017)*, NPL, New Delhi, 13-17 November, 2017.
2. **Kavindra Kandpal** and Navneet Gupta "Zinc Oxide Thin Film Transistors: Advances, Challenges and Future Trends", *National conference on Advances in Microelectronics, Instrumentation and Communication (MICOM-2015)*, BITS Pilani, 20-21 November, 2015. Proceeding of the conference is available in Bulletin of Electrical Engineering and Informatics, vol. 5, 205-212.
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