Mitigation of Power Quality Problems Using Interline Dynamic Voltage Restorer

THESIS

Submitted in partial fulfilment

of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

RAMCHANDRA NITTALA
ID NO. 2012PHXF0508H

Under the Supervision of
Dr. Alivelu M. Parimi

&

Under the Co-Supervision of
Dr. K. Uma Rao

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

2018

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI

CERTIFICATE

This is to certify that the thesis entitled **Mitigation of Power Quality Problems Using Interline Dynamic Voltage Restorer** submitted by **RAMCHANDRA NITTALA** ID.No **2012PHXF0508H** for award of Ph.D. of the Institute embodies original work done by him/her under my supervision.

Signature of the Supervisor

Dr. ALIVELU M. PARIMI
Asst. Professor, Dept. of EEE,
BITS-Pilani, Hyderabad Campus.

Date:

Signature of the Co-supervisor

Dr. K. UMA RAO
Professor, Dept. of EEE,
R. V. College Of Engineering,
Bengaluru.

Date:

Acknowledgements

As I am reaching the end of a long journey with ups and downs, I wish to acknowledge the remarkable individuals who stood with me in my ups and downs. I want to give thanks to God for sustaining me and guiding me throughout this arduous journey.

At an outset, I would like to express my deep sense of gratitude and thanks to **Dr. Alivelu Manga Parimi**, my thesis supervisor and **Dr. K Uma Rao,** my thesis co-supervisor. I will always be grateful, for their valuable guidance and constant encouragement.

I would like to thank my Doctoral Advisory Committee members**, Prof. BVVSN Prabhakar Rao** and **Dr. Shaikshavali Chitraganti** for their inspiring support and invaluable scientific suggestions from time to time. They always extended helpful hands towards me whenever I needed them.

I would like to thank **Prof. Y. Yoganandam**, for his moral support throughout my thesis.

I express my sincere thanks to all the faculty members, Research Scholars and Technicians of Department of Electrical Engineering, BITS Pilani, Hyderabad campus for their kind help and encouragement in carrying out my research work.

Constant moral support extended by my friends and well-wishers are gratefully acknowledged. The Financial assistance from BITS Pilani, Hyderabad is gratefully acknowledge.

Words are inadequate to express thanks and appreciation to my wife, **V. Sumadeepthi** for all her love and support when I was irritable and depressed. Her patience and sacrifice will remain my inspiration throughout my life.

I appreciate the unending love and affection from my parents, **Dr. N.Parthasarathy** and **Smt. N.Jwalamamba**. They have sacrificed many things for me. I have no phrases to praise them. Their blessings have helped me in reaching this goal. Love you both for your everlasting supports extended towards me.

My heart felt regard goes to my father in law and my mother in law, **Sh.V.SubbaRao** and **Smt.**

V.Jayasree for their love and moral support. Last but not the least, the undying love and affection who directly or in-directly had influence on me in the path of achieving the goal can never be completely expressed with words alone.

Ramchandra Nittala

Abstract

Mitigation of Power Quality problems using Interline Dynamic Voltage Restorer

by Ramchandra Nittala

The effective function of sensitive loads is dependent on the quality of power delivered to it and quantified in terms of its efficiency, security and reliability of loads connected to the same distribution line. However the loads connected on the same end are diversified from electronically controlled loads to heavy machinery. These cause minor to major power quality issues on the distribution system. However the sensitive electronic equipment loads are more effected with the power quality problems especially the voltage sag which eventually cause disruption in the performance of the load, raise in temperature, and damage to equipment etc. Mitigating voltage sag at the distribution level of power system network is of vital importance for enhanced performance of these loads. Custom power devices have been the part of the latest technology which provides the compensating measure as the mitigation equipment and thus improving the equipment immunity.

Among the customer power devices also referred to as the distribution Flexible AC Transmission System (D-FACTS) devices, the Interline dynamic voltage restorer (DVR) device, is utilized for mitigation of voltage sag/swell. The IDVR system comprises of several DVRs connected to different feeders with a common DC link. This IDVR scheme facilitates transfer of power between loads on different individual line through the common DC link of the DVRs. When one of the DVRs in IDVR system compensates for voltage sag in one feeder by importing real power from the DC link, the other DVRs replenish the DC-link energy to maintain the DC-link voltage at a specific level. In order to have control required output from IDVR detailed modelling of the components of IDVR is very important.

The DC link of IDVR provides the required energy to the IDVR for mitigating the voltage sag. The restoration of the DC link energy of the IDVR is a weighted factor in the robust operation of IDVR. The proposed novel methods to replenish the DC link of IDVR, employ Phase Shifting Transformer and PV system.

The advantage of IDVR over the other D-FACTS devices is the ability to mitigate voltage sag in multiple feeders at same instance of time. This is called multidirectional compensation. To test the functionality of IDVR with two DVRs in the bidirectional compensation, IDVR is tested in a two line power system and a voltage sag is applied in two feeders at same instance of time. This part of bidirectional compensation of IDVR is also verified with the experimental results obtained from a hardware IDVR prototype set up.

Additionally current source inverters (CSI) have certain advantages like current control capability, more regulation of ac voltage. Implementing CSI in IDVR to inject voltage for improvement of power quality is investigated. With usage of the current source inverters the injected voltage from IDVR may get improved. Hence in the proposed research the current source inverters are replaced with voltage source inverters and the comparison of the two inverters as the building blocks of IDVR are analysed in a test power system.

The functionality of IDVR is also tested by simulating the IDVR with a real time data. The real time data of some institute or industry is considered in the proposed research and the probable chances of voltage sag occurrences in that load are analysed. The efficiency of IDVR in compensating the voltage sags is also analysed. This real time simulation of IDVR brings more practicality towards the research on IDVR. Hence the overall research brings about the design of IDVR in mitigating voltage sag/swell, its DC link restoration and more importantly the bidirectional compensation ability of IDVR sustained by the experimental results obtained from a laboratory prototype model.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background

Power Systems is sub-divided into Generation, Transmission and Distribution where the power is generated from the generation side and is fed to the various loads on the distribution side by other transmission line. In addition to the variability of the power deliver to the loads, power quality is also a vital importance. Subsequently lack of quality effects the customers with sensitive loads. Although the distribution side contains different loads, the sensitive loads are the one which are effected by these power quality problems. The escalation of sensitive loads such as life support operation theatres in hospitals, data base systems, processing plants contain the semiconductor devices and air control traffic equipmements and numerous other data processing and service providers requires clean and uninterrupted power. Such customers are very vary of dips since each interruption cause some substantial amount of money. Consequently the power quality is an important role on the distribution side. Power quality sets the limits of electrical properties that allows electrical systems to function in their intended manner without significant loss of performance or life. Among the several power quality problems, the problems considered in the thesis are voltage sag and harmonics.

1.1.1 Sag

Sag is a reduction of AC voltage at a given frequency for the duration of 0.5 cycles to 1 minute's time as shown in fig 1.1. Sags are usually caused by system faults, and are also often the result of switching on loads with heavy start up currents.

Common causes of sags include starting large loads (such as one might see when they first start up a large air conditioning unit) and remote fault clearing performed by utility equipment. Similarly, the starting of large motors inside an industrial facility can result in significant voltage drop (sag). A

motor can draw six times its normal running current, or more, while starting. A large amount of reactive power is absorbed by the motor during its starting. This leads to formation of voltage sag.

Fig. 1.1 Wave form with Sag.

1.1.2 Harmonics

Harmonic distortion is the corruption of the fundamental sine wave at frequencies that are multiples of the fundamental. (e.g., 150Hz is the third harmonic of a 50Hz fundamental frequency; 3 X 50 = 150) as shown in fig 1.2. The power electronics loads produce harmonics because of their switching action of power electronic switches.

Symptoms of harmonic problems include overheated transformers, neutral conductors, and other electrical distribution equipment, as well as the tripping of circuit breakers and loss of synchronization on timing circuits that are dependent upon a clean sine wave trigger at the zero crossover point.

Fig. 1.2 Waveform with harmonics.

Custom power is a technology-driven product and service solution which embraces a family of devices to provide power-quality enhancement functions. Among the several novel custom-power devices, the Interline dynamic voltage restorer (DVR) [1], [2] is the most technically advanced and economical device for voltage-sag mitigation in distribution systems. The Interline Dynamic Voltage Restorer (IDVR) system consists of several DVRs protecting sensitive loads in different

distribution feeders emanating from different grid substations, and these DVRs share a common DC link. The interline power-flow controller (IPFC) addresses the problem of compensating a number of transmission lines at a given substation. The IPFC scheme provides a capability to transfer real power directly between the compensated lines, while the reactive power is controllable within each individual line. The IDVR scheme provides a way to transfer real power between sensitive loads in individual line through the common DC link of the DVRs, as it does in the IPFC. However, the lines in the IPFC originate from a single grid substation while the lines in the IDVR system originate from different grid substations.

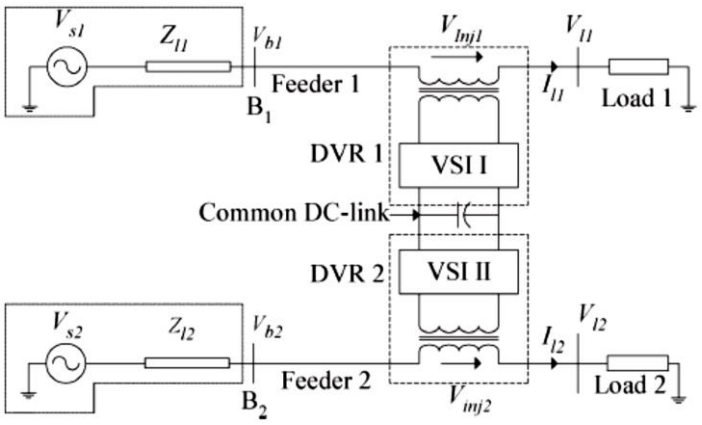


Fig. 1.3 Schematic diagram of an IDVR in a two-feeder system.

When one of the DVRs in IDVR system compensates for voltage sag in a feeder it draws energy from the DC link, the other DVRs replenish the DC-link energy to maintain the DC-link voltage at a specific level. Thus the IDVR provides a way to replenish the energy in the common DC-link energy storage dynamically. An example of a potential location for such a scheme is an industrial park where power is fed from different feeders connected to different grid substations, those that are electrically far apart. The sensitive loads in this park may be protected by DVRs connected to respective loads. The DC links of these DVRs can be connected to a common terminal, thereby forming an IDVR system. This would cut down the cost of the custom-power device, as sharing common DC link reduces the size of the DC-link storage capacity substantially, compared to that of a system in which loads are protected by clusters of DVRs with separate energy storage systems.

1.2 Motivation of the Research

Literature on IDVR presents various methodologies for restoring the DC energy and controlling the voltage compensation ability of IDVR. There were many schemes proposed in the research for replenishing the DC link energy of IDVR. When one of the DVR's is working in voltage compensation mode, the second DVR of IDVR works in power compensation and restore the DC link energy. The limitation for this type of restoration is, one of the DVR should always be working in power compensation mode, which implies that the feeder connected to that particular DVR will be treated as healthy feeder in all conditions. This is a big deviation from practical scenario.

The second gap in the research of IDVR are bidirectional compensation and utilisation of current source inverters in the building blocks of IDVR. The IDVR constitutes of two or more DVRs sharing a common DC link. Since these DVRs are connected to multiple feeders, the voltage compensation in multiple feeders can be performed with each one of them at one instance. This type of compensation is called as bidirectional compensation. This is the unique capability of IDVR to mitigate voltage sag in multiple feeders at same instant and yet to be investigated. To examine the functionality of IDVR in the bidirectional compensation, a two line IDVR system will be considered and voltage sag will be applied in two feeders at same instant. The efficiency of IDVR in compensating the voltage sag can be tested. This part of bidirectional compensation of IDVR will be verified with the experimental results obtained from a hardware IDVR prototype set up.

The third major gap in the IDVR research is use of current source inverters as the building blocks of IDVR. The voltage source inverters are utilized as the traditional building blocks of IDVR. The current source inverters have certain advantages like current control capability, more regulation of AC voltage etc. The possibility of the improvement of voltage sag mitigation with CSI is too investigated. Hence this current source inverters will replace with voltage source inverters and the

comparison of the two inverters as the building blocks of IDVR will be performed in a test power system.

The functionality of IDVR in mitigating the voltage will be examined with a real time electrical load network data. In previous research on IDVR [3]–[11], the simulations on IDVR were performed with a test power system. A basic power system network was considered and various possible ways of occurrence of sag were analysed. Using these results, the IDVR cannot be concluded as ideal device for mitigating voltage sag/swell. This is the fourth deviation observed. Hence in order to prove the reliability of IDVR, a real time electrical network load is to be considered. The real time data of would be the distribution network of BITS Pilani Hyderabad Campus. The efficiency of IDVR in compensating the voltage sags will be analysed in the network. This real time simulation of IDVR brings more practical weight towards the research on IDVR. Hence these are four major research gaps on IDVR to be addressed.

Considering the literature review on IDVR, the research gaps are identified. To address these research gaps, the objectives of the research are contributed as.

1.3 Aims and Objectives of the Research

1. Mathematical Modelling of IDVR: The main aim of IDVR is mitigation of power quality problems. In order to inject the required voltage for voltage sag mitigation, a controller has to be designed for IDVR which requires modelling of IDVR. The mathematical model includes the components of IDVR i.e. the inverter and DC link. The study and performing the calculations relating to methods of voltage compensation and control are done. The modelling of IDVR is discussed in chapter 3.
2. Incorporation of IDVR into a Power Distribution Network: Once the modelling of IDVR is established, it is incorporated in the power system network and its performance is to be investigated and analysed for voltage sag mitigation.

3. Restoring the DC link with PST and PV: The DC link of IDVR provides the required energy to the IDVR for mitigating the voltage sag, due to this the DC link energy diminishes. The restoration of the DC link energy of the IDVR is a weighted factor in the robust operation of IDVR. One of the methods employed is by utilizing the capacity of phase shifting transformer to shift the phase and controlling the power necessary to change the DC link. Additionally a PV system is utilized which is connected across the DC link to aid in the restoration process. A controlled algorithm is designed between PST and PV source depending upon the loading conditions of the feeder and surplus power available with the PV source respectively to replenish DC link energy.
4. IDVR Performance by replacement of VSI with CSI: The performance of IDVR with VSI and CSI as its building will be compared for a test power system. In addition the bidirectional compensation will be verified with the adopted controlling technique and replenishing using current source inverters.
5. Simulation of IDVR with Real Time Data: The adaptability of IDVR in real time scenario to be verified. The real time data of various loads in BITS Pilani Hyderabad Campus will be considered. The protection offered by the IDVR to the sentive loads is practically examined.
6. Experimental set up of IDVR: The simulation results of voltage sag and harmonics mitigation by IDVR is to be substantiated with experimental prototype model of IDVR. A small scale power distribution network is considered and effectiveness of IDVR in bidirectional compensation is to be proven.

   Thus the IDVR mitigation of few power quality problems will be demonstrated.

1.4 Organization of the Research

The thesis is organised in the following chapters to report the results of the above studies.

Chapter 1: The summary of the problem addressed is described in this chapter. The aims and objectives of proposed research is covered in this thesis.

Chapter 2: In this chapter, a survey of the literature on various Power Quality issues are discussed. A review of various compensation techniques utilized to compensate the voltage sag and harmonics is described followed by the FACTS devices utilized for the voltage compensation is presented. Based on the literature survey, the chapter concludes highlighting the research gaps that are being taken forward in the successive chapters.

Chapter 3: This chapter discusses about the mathematical modelling of IDVR and its design. The design part of IDVR includes rating of individual inverter, DC link and the series injection transformer.

Chapter 4: This chapter establishes the control system developed for IDVR to compensate the voltage sag and the restoration of the DC link energy through the novel techniques by utilizing the phase shifting transformers (PST) and PV Source.

Chapter 5: In this chapter, voltage source inverters are replaced with current source inverters and the comparison of the two inverters as the building blocks of IDVR is performed in a test power system to mitigate voltage sag/swell.

Chapter 6: In this chapter, IDVR is simulated using a real time data. An IDVR is designed for a specific application at the network of BITS Pilani Hyderabad Campus to mitigate power quality problems.

Chapter 7: In this chapter, a laboratory prototype of IDVR is developed with the two feeder power system using VSI (semikron make) and DSPACE 1103 integrated with MATLAB to test

effectiveness of IDVR in mitigating voltage sag/swell in practical scenario.

Chapter 8: Finally, this chapter summarizes the specific contributions of the current study and conclusions gained from this research. Further, future scope and directions for research in this area is also been presented.

Chapter 2

Literature Survey

2.1 Introduction

This chapter gives the review of various conventional methods for mitigation of voltage sag and harmonics in the distribution side of power system. The limitations of the traditional devices are discussed. These limitations are overcome by FACTS devices. Various FACTS devices utilised on the distribution side are described. Finally the importance of Interline Dynamic Voltage Restorer in mitigating voltage sag and harmonics along with its literature review is covered.

Day by day the load demand is increasing at the distribution side. The loads of sensitive nature are increasing. Power Quality is a bigger concern to these sensitive loads. According to the Institute of Electrical and Electronics Engineers (IEEE) standards IEEE1100 defines power quality as the "concept of powering and grounding sensitive electronic equipment in a manner suitable for the equipment" [12]. The issues related to power quality faced by the sensitive loads on the distribution side are called power quality problems. There are many power quality problems on the distribution side. The major of the power problems occurring on the distribution side are

1. Transients
2. Interruptions
3. Sag / Under voltage
4. Swell / Overvoltage
5. Harmonics
6. Frequency variations
7. Voltage fluctuations

Transients: Sudden disturbance in AC waveform evidenced by a sharp, brief discontinuity of the waveform. Transients occur when there is a sudden change in voltage or current in power system.

Interruptions: A small disturbance in the voltage magnitude for a period of time. Interruptions can be short term and long term.

Sag/Under voltage: A reduction in the voltage magnitude for a small period of time is called voltage sag and if this reduction in the voltage magnitude last for more than 30 cycles it is referred to as under voltage.

Swell/Over voltage: An increment in the voltage magnitude for a small period of time is called voltage swell and if this increase in the voltage magnitude last for more than 30 cycles it is referred to as over voltage.

Harmonics: Harmonic distortion is the corruption of the fundamental sine wave at frequencies that are multiples of the fundamental.

Frequency Variations: Changes in the fundamental frequency are referred as frequency variations.

Voltage fluctuations: A sudden increase or decrease in the voltage magnitude for a very short duration are called voltage fluctuations.

Among the above mentioned power quality problems, the most severely occurring the power quality problems is voltage sag and harmoincs. According to the IEEE standards voltage sag is defined as “the drop in voltage magnitude from 10 to 90 percent of the nominal value for a duration of half cycle to one minute”. Harmonics are referred as “superimposition of various frequencies over fundamental frequencies”[13]. Common causes of sags include starting large loads (such as one might see when they first start up a large air conditioning unit) and remote fault clearing performed by utility equipment. Similarly, the starting of large motors inside an industrial facility

can result in significant voltage drop (sag). A motor can draw six times its normal running current, or more, while starting. Creating a large and sudden electrical load such as this will likely cause a significant voltage drop to the rest of the circuit it resides on. The common cause of harmonics are power electronic loads, faults or any other malfunctions. The effects of voltage sag or harmonics are loss of data, frequent tripping of circuit breaker and most important damage of the sensitive loads. In the recent years sensitive loads are becoming more in number at the distribution side of the power system. These sensitive loads have low resistance towards the voltage sag/swell and get easily damaged when there is a voltage deviation.

To mitigate the voltage sag/swell and protect the sensitive loads, there are some traditional devices developed which are listed below,

1. Static Capacitors
2. Synchronous condensers
3. Shunt reactors
4. Voltage Regulators

2.1.1 Static Capacitors

Shunt or static capacitors shown in fig 2.1 are primarily used to improve the power factor in transmission and distribution network, resulting in improved voltage regulation, reduced network losses, and efficient capacity utilization. Improved transmission voltage regulation can be obtained during heavy power transfer conditions when the system consumes a large amount of reactive power that must be replaced by compensation [14]–[16].

At the line surge impedance loading level, the shunt capacitor would decrease the line losses by more than 30%. In distribution and industrial systems, it is common to use shunt capacitors to compensate for the highly inductive loads, thus achieving reduced delivery system losses and network voltage drop.

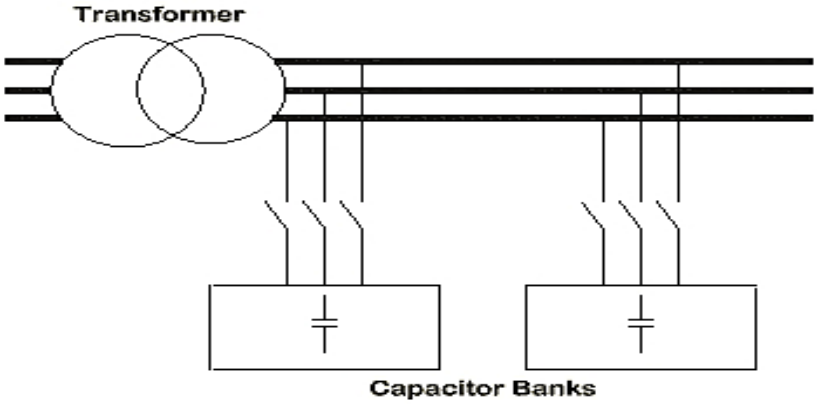


Fig. 2.1 Static Capacitor or shunt capacitor banks

2.1.2 Synchronous Condensers

An over excited synchronous machine running on no load is called is called synchronous condenser which is represented in fig 2.2. When the synchronous condenser is placed in parallel to the system it regulated the power factor by controlling the reactive power. By maintaining the reactive power the voltage regulation is possible. The reactive power taken by a synchronous motor depends on two factors, DC filed excitation and mechanical load delivered by the motor. Maximum leading power is taken by a synchronous motor with maximum excitation and zero load [17], [18].

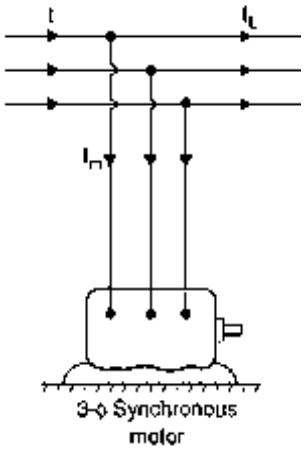


Fig. 2.2 Synchronous Condenser

2.1.3 Shunt Reactors

The primary purpose of the shunt reactor is to compensate for capacitive charging voltage, a phenomenon getting prominent for increasing line voltage. Long high voltage transmission lines and relatively short cable lines (since a power cable high capacitance to earth) generate a large amount of reactive power during light power transfer conditions which must be absorbed by compensation. Otherwise, the receiving terminals of the transmission lines will exhibit a voltage rise voltages. A better fine tuning of the reactive power can be made by the use of a tap changer in the shunt reactor .It can be possible to vary the reactive power between 50 to 100% of the needed power.

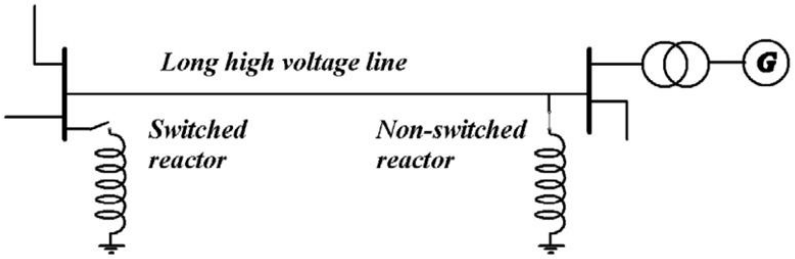


Fig. 2.3 Shunt Reactors

2.1.4 Voltage Regulators

A voltage regulator generates a fixed output voltage of a constant magnitude regardless of changes to its input voltage or load conditions. There are two types of voltage regulators: linear and switching. A linear regulator employs an active (BJT or MOSFET) pass device (series or shunt) controlled by a high gain differential amplifier. It compares the output voltage with a precise reference voltage and adjusts the pass device to maintain a constant output voltage. A switching regulator converts the dc input voltage to a switched voltage applied to a power MOSFET or BJT switch. The filtered power switch output voltage is fed back to a circuit that controls the power

switch on and off times so that the output voltage remains constant regardless of input voltage or load current changes.

The traditional methods have advantages like

1. The usage of capacitor banks improves power factor along with voltage regulation
2. The installation of shunt reactors and series capacitors is easy.
3. All the devices can work under normal atmospheric conditions. No special temperature conditions should maintained for their function.
4. With the use of synchronous condensers faults can be removed easily because of the high thermal stability of the motor.
5. Simple and robust customer solution with low installation costs and minimum maintenance

However, the disadvantages of these traditional methods are

1. Short Service
2. The devices get easily damaged if the voltage exceeds the rated value.
3. Once damaged their repair is uneconomical.
4. Using synchronous condensers creates additional losses and noise.
5. As the synchronous motor has no self-staring torque, additional equipment has to be installed.

Due to these disadvantages the traditional devices are slowly replaced with Flexible AC Transmission Systems (FACTS) devices. The IEEE definition of FACTS devices is “a power electronic based system and other static equipment that provide control of one or more AC transmission system parameters to enhance controllability and increase power transfer capability”[19]. The early FACTS devices were mostly thyristor controlled devices. Most of the installed FACTS devices are the thyristor controlled reactor or capacitor based Static VAR Compensator (SVC), which mainly controls voltage by injecting to or absorbing reactive power

from the grid. With the drastic developments in the area of power electronics, the research on FACTS devices is mainly focused on Voltage Source Inverter (VSI) based devices. VSI utilizes self-commutated power electronics devices, such as GTOs and IGBTs, to invert the DC supply to AC supply.

The FACTS devices are used in both transmission and distribution side. The major FACTS devices utilized on the transmission side are [19]

1. Static Synchronous Compensator (STATCOM).
2. Static Synchronous Series Compensator (SSSC).
3. Unified Power Flow Controller (UPFC).
4. Interline Power Flow Controller (IPFC).

2.1.5 Static Synchronous Compensator (STATCOM)

A STATCOM shown in fig 2.4 is comparable to a Synchronous Condenser (or Compensator) which can supply variable reactive power and regulate the voltage of the bus where it is connected. STATCOM is a VSI in shunt connected to the grid. The VSI is controlled to inject or absorb reactive current to or from the grid, thus supporting the voltage and improving the system stability [20]–[23].

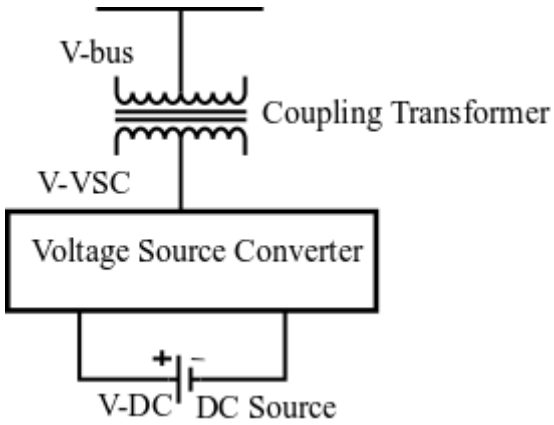


Fig. 2.4 Schematic diagram of STATCOM

Fig 2.4 represents the general configuration of STATCOM. The compensation provided by the STATCOM is with the exchange of reactive power, hence the active power capability of the STATCOM is very low.

2.1.6 Static Synchronous Series Compensator (SSSC)

SSSC is a VSI connected in series with the grid through a transformer. The device injects voltage in series to the receiving end voltage to control power flow and thereby to improve the power oscillation damping on power grids. Fig 2.5 shows the configuration of SSSC. The operation of SSSC has some similarity to a controllable series capacitor and series inductor. The major difference is that its injected voltage is not related to the line intensity and can be managed independently. This primary feature allows the SSSC to work satisfactorily with high loads as well as with lower loads.

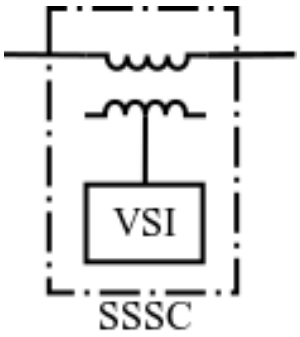


Fig. 2.5 Schematic diagram of SSSC

2.1.7 Unified Power Flow Controller (UPFC)

UPFC is the combination of a STATCOM and a SSSC by back-to-back connecting them together with a common DC link. With this combination, the UPFC inherits all the functions of the STATCOM and SSSC and maximize the operational region. UPFC mainly provides fast acting reactive power compensation on high voltage electricity transmission networks. The UPFC can control both active and reactive power flows in the transmission line. The controllable parameters by UPFC in the line are reactance in the line, phase angle and voltage. Fig 2.6 shows the

configuration of UPFC. As shown in fig 2.6 the series and shunt device share a common DC link. Therefore the active or reactive power needed by one device can be supplied by the other device [24]–[28] .

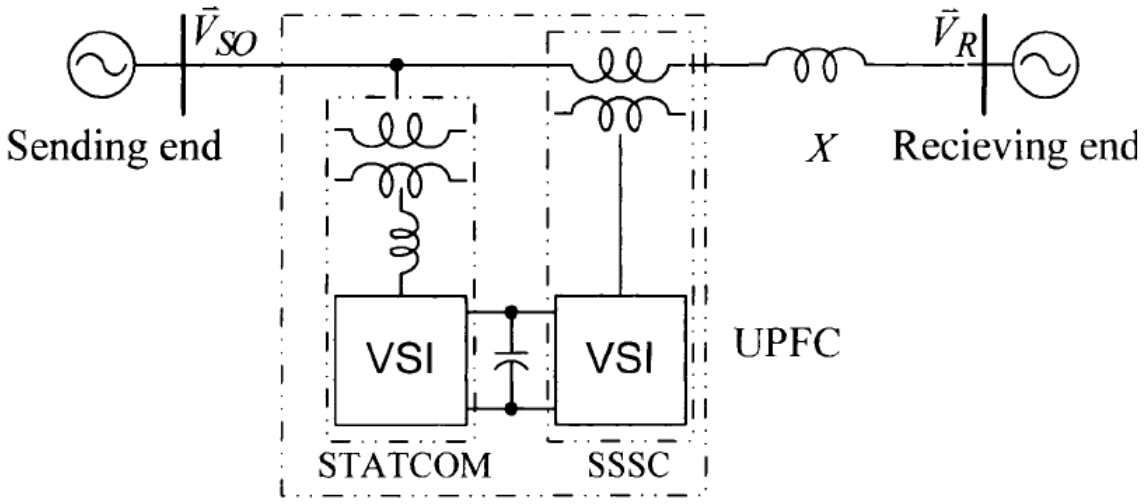


Fig. 2.6 Schematic diagram of UPFC

2.1.8 Interline Power Flow Controller (IPFC)

IPFC is designed for the compensation of active and reactive power in a multi-line transmission system. The VSIs share a common DC link, and are connected in series to different transmission lines. In other word, an IPFC is a combination of several SSSCs with one common DC link. Fig 2.7 gives the configuration of IPFC. In this structure, power flows from line to line through the DC link. With proper control, the power exchange between different lines can be conditioned and optimized. Similar to SSSC, an IPFC controls the grid's voltage, phase and impedance [29]–[32].

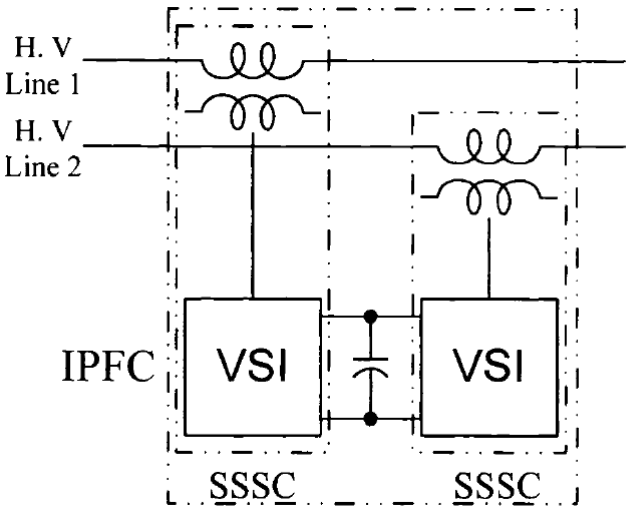


Fig. 2.7 Schematic diagram of IPFC

The table 2.1 summarizes the circuit structures of the FACTS devices on the transmission side.

Table2.1: Summary of FACTS configuration on transmission side

FACTS Device	Number of Converters	Configuration
STATCOM	1	Shunt
SSSC	1	Series
UPFC	2	Combined Shunt and Series connected back to back
IPFC	2	Combined Series and Series connected back to back.

The FACTS devices discussed are implemented in the transmission line. However, as the power quality issues are observed on the distribution side of the grid network, consequently FACTS devices installed on the distribution side to mitigate the power quality issues. These FACTS Devices on the distribution side are called custom power devices.

2.2 Custom Power

Custom power is the employment of power electronic or static controllers in medium and low voltage distribution systems for the purpose of supplying a level of reliability and/or power quality that is needed by electric power customers sensitive to power quality variations. In other words custom power is intended to protect the customers from interruptions and voltage reductions originating in the utility system as well as those transferred to customers from other customers via the utility system and even internal disturbances.

Custom power devices, or controllers, include static switches, active filters, DVRs, injection transformers, energy storage modules that have the ability to perform current interruption and voltage regulation functions in a distribution system to improve reliability and/or power quality.

In a Custom Power system customer should receive specified power quality from a utility or a service provider which includes an acceptable combination of the following features:

- No (or rare) power interruptions
- Magnitude and duration of voltage reductions within specified limits.
- Magnitude and duration of over voltages within specified limits.
- Low harmonic voltage.
- Low phase unbalance

The need for the Custom Power concept arises from the fact that:

1. Most of the interruptions and voltage reductions occur in the utility system on account of lightning faults on transmission and distribution lines, trees touching the wires, equipment failure, switching, etc. Voltage sag may also be a consequence of large load changes affecting customers own equipment or affecting other equipment via the utility system.

2. Impulses, switching surges and over voltages affecting the insulation, would most likely result from lightning strikes and switching events in the transmission and distribution system.

3. Temporary over voltages lasting from several cycles to several seconds would largely result from large load changes, capacitor switching, transformer switching, excessive leading-VARs during light loads, etc. in the utility system.

4. Voltage unbalances in a three-phase supply would occur mostly due to large unbalanced loads on a utility's distribution lines and long lines with unbalanced phase impedances.

5. Harmonics would most likely be the consequence of high harmonics in the customer load, or the saturation of a utility's transformers. These harmonics would then be amplified by the natural resonances in the utility system and/or the customer system.

2.2.1 Custom Power Devices

Just as FACTS controllers improve the reliability and quality of power transmission systems, the custom power enhances the quality and reliability of power delivered to customer. Custom Power Devices are intended for improving the power quality of distribution networks against disturbances such as

- Sags, swells,
- Transients, harmonics.

The incorporation of the classical devices, such as D-STATCOM (Distribution Static Synchronous Compensator), DVR (Dynamic Voltage Restorer), and UPQC (Unified Power Quality Conditioner), means a continuous control, with a very fast response time, and they allow and assure an improvement in the wave quality of the power supply.

A DSTATCOM can compensate for distortion and unbalance in a load such that a balanced sinusoidal current flows in the feeder. A DVR can compensate for voltage sag/swell and distortion

in the supply side voltage such that the voltage across a sensitive/critical load terminal is perfectly regulated. A UPQC can perform the functions of both DSTATCOM and DVR.

2.3 Distribution STATCOM (DSTATCOM)

The DSTATCOM is basically one of the custom power devices. It is similar to STATCOM but used at the Distribution level. The key component of the DSTATCOM is a power VSC that is based on high power electronics technologies.

The Distribution STATCOM is a versatile device for providing reactive compensation in AC networks. The control of reactive power is achieved via the regulation of a controlled voltage source behind the leakage impedance of a transformer, in much the same way as a conventional synchronous compensator. However, unlike the conventional synchronous compensator, which is essentially a synchronous generator where the field current is used to adjust the regulated voltage, the DSTATCOM uses an electronic voltage sourced converter (VSC), to achieve the same regulation task. The fast control of the VSC permits the STATCOM to have a rapid rate of response [33]–[37].

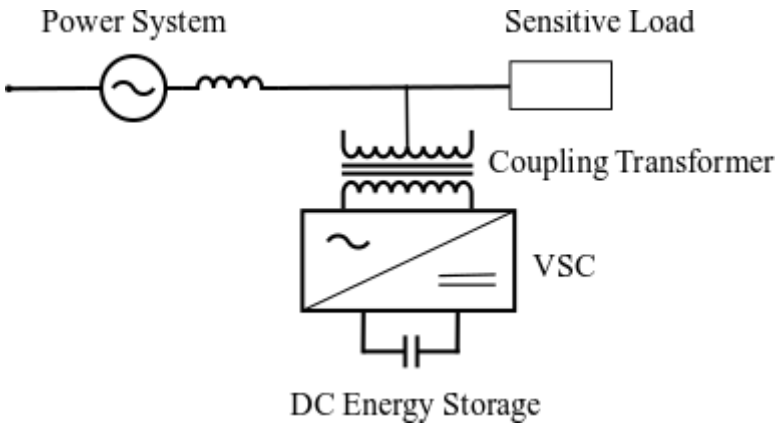


Fig. 2.8 Schematic representation of the DSTATCOM

The DSTATCOM is the solid – state based power converter version of the SVC. Operating as a shunt – connected SVC, its capacitive or inductive output currents can be controlled independently

from its connected AC bus voltage. Because of the fast switching characteristic of power converters, the DSTATCOM provides much faster response as compare to SVC. DSTATCOM is a shunt connected, reactive compensation equipment, which is capable of generating and or absorbing reactive power whose output can be varied so as to maintain control of specific parameters of the electric power system. DSTATCOM provides operating characteristics similar to a rotating synchronous compensator without mechanical inertia, due to the DSTATCOM employ solid state power switching devices it provides rapid controllability of the three phase voltages, both in magnitude and phase angle.

2.3.1 Principle of operation of Shunt-Connected VSC

The basic idea of the shunt-connected VSC is to dynamically inject a current $I_r(t)$ of desired amplitude, frequency and phase into the grid. The typical configuration of a shunt-connected VSC is shown in fig 2.9. The device consists of a VSC, an injection transformer, an AC filter and a DC link capacitor. Energy storage can also be mounted on the dc link to allow active power injection into the AC grid.

The line impedance has a resistance R_g and inductance L_g. The grid voltage and current are denoted by Es (t) and Ig (t), respectively. The voltage at the point of common coupling (PCC), which is also equal to the load voltage, is denoted by $E_g(t)$ and the load current by $i_l(t)$. The inductance and resistance of the ac-filter reactor are denoted by L_r and R_r respectively.

Fig 2.10 shows a simplified single-line diagram, where the VSC is represented as a current source. Amplitude, frequency and phase of the current $I_r(t)$ can be controlled. By injecting a controllable current, the shunt-connected VSC can limit voltage fluctuation leading to flicker and cancel harmonic currents absorbed by the load, thus operating as an active filter. In both cases, the principle is to inject a current with same amplitude and opposite phase as the undesired frequency components in the load current, so that they are cancelled in the grid current.

These mitigation actions can be accomplished by only injecting reactive power. A shunt-connected VSC can also be used for voltage dip mitigation. In this case, the device has to inject a fundamental current in the grid, resulting in increased voltage amplitude at the PCC, as shown in the phasor diagram in fig 2.11. The voltage phasor at PCC is denoted by E_g, Z_g is the line impedance, E_s, dip is the grid voltage phasor during the dip and Ψ is the phase-angle jump of the dip. From the diagram it is possible to understand that when the shunt-connected VSC is used to mitigate voltage dips, it is necessary to provide energy storage for injection of active power in order to avoid phase-angle jumps of the load voltage.

If only reactive power is injected, it is possible to maintain the load voltage amplitude E_g to the pre-fault conditions but not its phase. Therefore, the voltage dip mitigation capability of a shunt-connected VSC depends on the rating of the energy storage and on the rating in current.

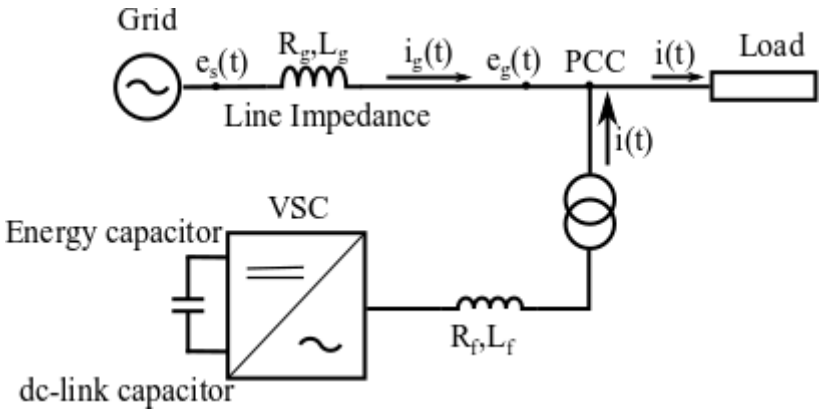


Fig. 2.9 Single line diagram of shunt connected VSC

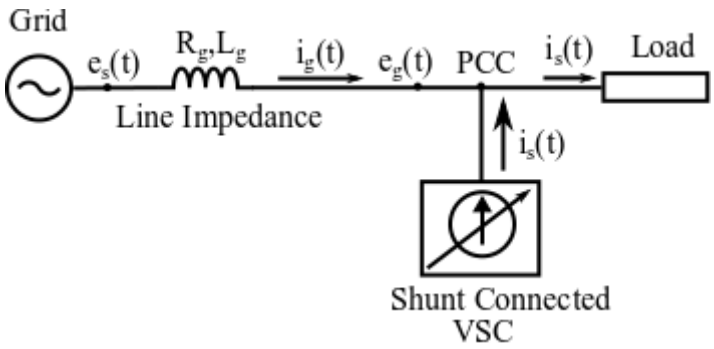


Fig. 2.10 Simplified line diagram of shunt connected VSC

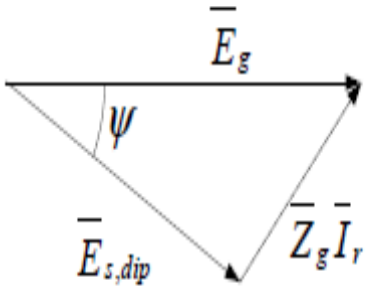


Fig. 2.11 Phasor diagram of voltage dip mitigation using shunt VSC

2.4 Dynamic Voltage Restorer (DVR)

The DVR is a powerful controller that is commonly used for voltage sags mitigation at the point of connection. The DVR employs VSC, coupling Transformer and DC energy storage capacitor and the coupling transformer connected in series with the ac system, as illustrated in fig 2.12. The VSC generates a three-phase AC output voltage, which is controllable in phase and magnitude. These voltages are injected into the AC distribution system in order to maintain the load voltage at the desired voltage reference [37]–[43].

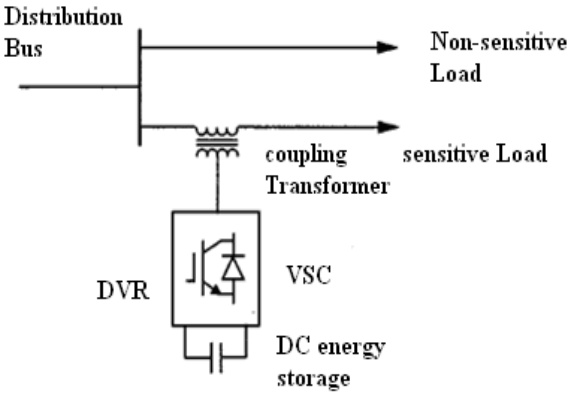


Fig. 2.12 Schematic representation of the DVR

The DVR is a solid state DC to AC switching power converter that injects a set of three single phase AC output voltages in series with the distribution feeder and in synchronism with the voltages of the distribution system. By injecting voltages of controllable amplitude, phase angle and

frequency (harmonic) into the distribution feeder in instantaneous real time via a series injection transformer, the DVR can restore the quality of voltage at its load side terminals when the quality of the source side terminal voltage is significantly out of specification for sensitive load equipment.

2.4.1 Principle of operation of Series-connected VSC (DVR)

The basic idea involved in principle of operation is to inject a voltage $e_c(t)$ of desired amplitude, frequency and phase between the Point of comon Coupling (PCC) and the load in series with the grid voltage. A typical configuration of the DVR is shown in fig.2.12. The simplified single-line diagram of the system with DVR is shown in fig 2.13. The DVR can be represented as a voltage source with controllable amplitude, phase and frequency.

The DVR is mainly used for voltage dip mitigation. The device maintains the load voltage E_l (t) to the pre-fault condition by injecting a fundamental voltage of appropriate amplitude and phase. Fig 2.11 shows the phasor diagram of the series injection principle during voltage dip mitigation, where Ec is the phasor of the voltage injected by the compensator, I_L is the phasor of the load current and where Ψ is the angle displacement between load voltage and current.

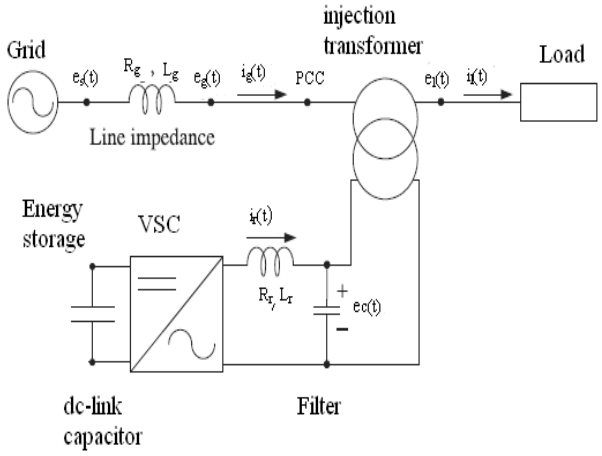


Fig. 2.13 Single line diagram of series connected VSC

In order to be able to restore both magnitude and phase of the load voltage to the pre-fault conditions, the DVR has to inject both active and reactive power. The voltage dip mitigation capability of this device depends on the rating of the energy storage and on the voltage ratings of the VSC and the injection transformer

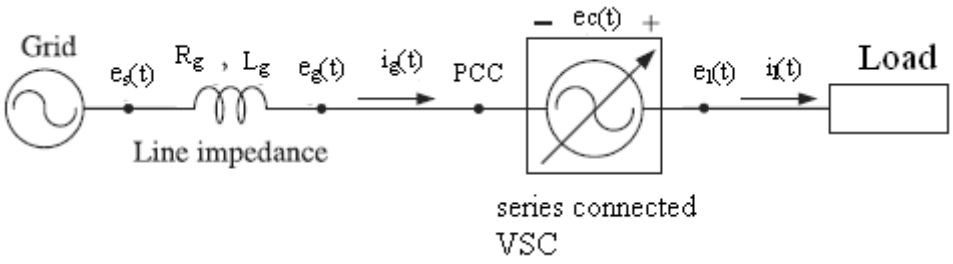


Fig.2.14 Simplified line diagram of series connected VSC

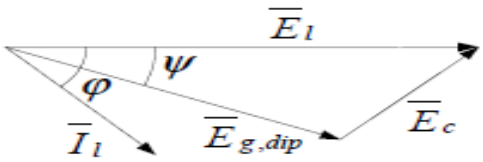


Fig. 2.15 Phasor diagram of voltage mitigation using series VSC

The reactive power exchanged between the DVR and distribution system is internally generated by the DVR without any AC passive reactive components, i.e. reactors and capacitors. For large variations in the source voltage, the DVR supplies partial power to the load from a rechargeable energy source attached to the DVR dc terminal. The DVR, with its three single phase independent control and inverter design is able to restore line voltage to critical loads during sags caused by unsymmetrical L-G, LL, L-L-G, as well as symmetrical three phase faults on adjacent feeders or disturbances that may originate many miles away on the higher voltage interconnected transmission system. Connection to the distribution network is via three single-phase series transformers there by allowing the DVR to be applied to all classes of distribution voltages. At the point of connection the DVR will, within the limits of its inverter, provide a highly regulated clean output voltage.

2.5 Literature Survey of DVR

The basic topology under which DVR was classified as DVR with medium voltage and DVR with low voltage. In both systems the purpose of the DVR was mitigate the voltage sag but the difference between low and medium voltage level connection was the flow of zero sequence currents and generation of zero sequence voltages. DVR compensates the voltage sag by injecting the proper amount of voltage in series with supply voltage so that the load voltage is maintained within the specified limits [38], [44], [45]. The DVR consists of an energy storage device, series inverter which was coupled to the grid via series injection transformer. The control strategy for DVR majorly has two parts detection and determining the reference signal. The first one was mainly about the voltage sag detection in grid. There are different detection methods such as peak measurement, dqo component measurement, phasor parameters estimation using kalman filtering or complex Fourier transformation [39], [46]–[48]. The second one was about the determination of the reference signal of the series injected voltage. The method to determine the reference signal generation depends upon the energy storage device that DVR contains.

The voltage sag compensation of DVR was classified into three methods; in phase compensation, pre-sag, energy minimized. The in phase compensation method is the straightest method of compensation where the injected voltage by the DVR was in phase with the source voltage irrespective of the pre fault condition [49]–[51]. The commonly used method of compensation was pre-sag compensation method. In this method, the load voltage was restored to level before the occurrence of the voltage sag. Since the load voltage was compensated to pre-sag condition, the compensation was done with respect to the magnitude as well with the phase. In the first two methods of compensation the active power was injected by the DVR. The injected power was supplied from the energy storage device at the DC link. Thus the active power should be supplied to DC link or the DC link voltage will be dropped. To avoid such pressure on the DC link, the next method of compensation is energy minimized compensation. The basic principle of this method was

injecting to or absorbing from power grid as much reactive power as possible to compensate the voltage sag. Therefore, the DVR voltage must be controlled in such a way that the DVR does not exchange active power with power grid and as result, the amount of active power needed from the dc-link can be minimized. Therefore with the three methods the DVR is able to compensate voltage sag able to maintain the load voltage to its specified value.

2.6 Unified Power Quality Conditioner (UPQC)

Poor power quality in a system could be due to different factors such as voltage sag, voltage swell, voltage outage and over correction of power factor and unacceptable levels of harmonics in the current and voltage. Modern solution for poor power quality is to take advantage of advanced power electronics technology [52]–[56].

Recent research efforts have been made towards utilizing a device called unified power quality conditioner (UPQC) to solve almost all power quality problems. The main purpose of a UPQC is to compensate for supply voltage flicker/imbalance, reactive power, and harmonics. In other words, the UPQC has the capability of improving power quality at the point of installation on power distribution systems or industrial power systems. The UPQC, therefore, is expected as one of the most powerful solutions to large capacity loads sensitive to voltage flicker/imbalance.

Unified Power Quality Conditioner (UPQC) for non-linear and voltage sensitive loads has following facilities.

• It eliminates the harmonics in the supply current, thus improves utility current quality for nonlinear loads.

• UPQC provides the VAR requirement of the load, so that the supply voltage and current are always in phase, therefore, no additional power factor correction equipment is necessary.

• UPQC maintains load end voltage at the rated value even in the presence of supply voltage sag.

• The voltage injected by UPQC to maintain the load end voltage at the desired value is taken from the same dc link, thus no additional dc link voltage support is required for the series compensator.

The UPQC in fig 2.16 consists of two three phase inverters (VSI) connected which are also known as active power filters in cascade in such a manner that one inverter is connected in parallel with the load. Second Inverter is connected in series with the supply voltage through a transformer.

The main purpose of the shunt compensator is to compensate for the reactive power demanded by the load, to eliminate the harmonic components of nonlinear loads in such a way that the source current is sinusoidal and balanced. This equipment is a good solution for the case when the voltage source presents distortion and a harmonic sensitive load is close to a nonlinear load.

The series compensator is operated in PWM voltage controlled mode. It injects voltage in quadrature advance to the supply voltage (current) such that the load end voltage is always maintained at the desired value. The two inverters operate in a coordinated manner.

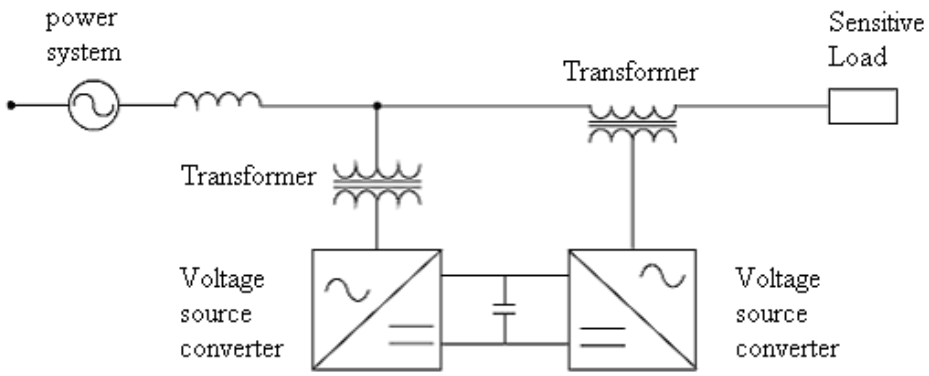


Fig. 2.16 Basic Block Diagram of UPQC

If UPQC is connected between two feeders it would be called as Interline Unity Power Quality conditioner (IUPQC). This IUPQC comes under series-shunt facts device.

2.7 Literature Survey of UPQC

Initially there were two types of active power filters (APF) namely shunt APF and series APF. The shunt APF was mainly to tackle current related problems and series APF was manly to tackle voltage related problems. Moran[57] described a system configuration in which both series and shunt APFs were connected back to back with a common DC reactor. Fujita and Akagi[58] implemented the practical application of the topology proposed by Moran with 20 kVA experimental results. They named this device as unified power quality conditioner (UPQC).

Basic classification of UPQC was on physical structure and voltage sag compensation. There were majorly four methods of compensation of voltage sag by UPQC. First method of compensation with active power control. Reference [59]–[63] had represented active power control of UPQC to mitigate the voltage sag. In this method the voltage sag was injected in phase to the system. This in-phase component was equal to make the load voltage magnitude to the desired level. The shunt inverter of UPQC draws the necessary active power required by the series inverter plus the losses associated with UPQC so that the effective sag compensation was achieved. The second method of compensation of voltage sag by UPQC was by injecting of the reactive power through series inverter of UPQC [64]–[66]. The injected voltage was by the series inverter of UPQC in quadrature to the source voltage such that the vector sum of source voltage and the injected voltage equals the required voltage of the load. With this method the need of the active power to compensate the voltage sag was eliminated. The injected voltage in this method was shifted to some angle so that the injected voltage is quadrature to the source voltage. The third type of compensation by UPQC was minimum Volt Ampere (VA) loading. In this method of compensation, the series voltage was injected at a certain optimal angle with respect to the source current instead of injecting in quadrature or in-phase [67]–[71]. The fourth method of compensation was simultaneous active and reactive power control. In this method the series inverter injects both real and reactive power. As the control both active and reactive power are involved the complexity in this method was more.

This complexity was decreased with use of DSP processor. Hence with the described four methods, the voltage sag is compensated with UPQC. The literature review on DVR is covered in the following section.

2.8 Limitations to the DVR and UPQC

From the literature survey it can be concluded that the voltage sag mitigation in the distribution side can be successfully performed with both UPQC and DVR. Both of the devices inject the required voltage and maintains the load voltage to the set value. Hence the power quality at the distribution side of the power system can be improved with utilization of UPQC and DVR. The major limitation for DVR is the energy storage device at the DC link. Whenever the DVR needs to compensate the deeper voltage sags, the requirement of active power to mitigate the deeper sags is very huge. Hence there has to be larger DC links to supply the required active power to the DVR. Even during the multiple voltage sag conditions, the energy storage device is to be quite high to supply the required energy to the DVR. Hence the requirement of large DC links may not be economically good.

The distribution side contains multiple feeder line to which different loads are connected. The sensitivity of the loads are increasing in the modern days. Hence the power quality is to be ensured in all the feeders of the distribution side. For instance the voltage sag has occurred in two feeders which contain the sensitive loads at same time, the compensation of the voltage sag cannot be done with neither UPQC nor DVR, which implies the both UPQC and DVR are restricted to only one feeder. To ensure the power quality in all the feeders several DVRs or UPQCs have to be connected which also an economical problem. The feasible solution to these problems is an extended version of DVR known as Interline Dynamic Voltage Restorer (IDVR).

2.9 Interline Dynamic Voltage Restorer

An Interline Dynamic Voltage Restorer (IDVR) comprises of two or more DVRs sharing a common DC link. The ability of IDVR is, it can simultaneously eliminate voltage sag/swells in different feeders at same instance of time with one common DC link and also when one of the DVR is mitigating deeper voltage sag, the required power can be supplied with another DVR. This will reduce the size of DC link which will also benefit economically.

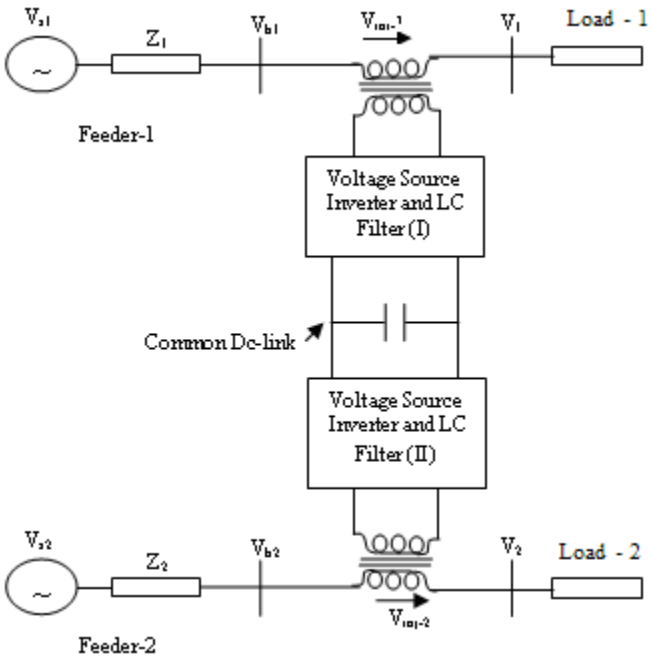


Fig. 2.17: Basic Layout of two line IDVR

A simple two feeder IDVR layout is shown in fig 2.17. It consists of two DVRs sharing a common DC link. The two DVRs of IDVR are connected to two different feeders with aid of series injection transformers. The building block of IDVR consists of a control system, voltage source inverter or current source inverter and the filter. The network shown in fig 2.17 contains two feeders. V_{b1} and V_{b2} are the bus voltages of feeder 1 and feeder 2 respectively. The two loads, Load 1 and Load 2 are considered as the sensitive loads connected to feeder 1 and feeder 2 respectively. For an instance a

voltage sag is assumed at the load 1, then the DVR 1 injects the voltages V_{inj1} to maintain the V_{l1} equal to V_{b1}.

The main advantage of IDVR over DVR is having low rating DC link. The concept of IDVR is if the primary DVR compensates the voltage sag/swell, the secondary DVR provides the required energy to mitigate the voltage sag. If the secondary DVR cannot supply the required energy to the DC link of IDVR, in such case the stored energy in DC link is utilised the by the primary DVR to mitigate the voltage sag. Hence the DC link energy has to be maintained constant. Therefore the main research on IDVR is focused on the restoration of its DC link energy. Apart from the restoration of DC link, the other contributions of research is on the control system of IDVR. The control system function is to mitigate the voltage sag as well monitor the DC link energy of IDVR. The various research work on IDVR is presented in the next section.

2.10 Literature Survey of IDVR

Different authors have proposed different methods for replenishing the energy at the DC link. Vilathgamuwa et.al [72] proposed an Interline Dynamic Voltage Restorer (IDVR) to mitigate voltage sag in a two line power system. The proposed IDVR consists of several DVRs connected to different feeders while sharing a common DC Link. When one of the DVR compensates for voltage sag appearing in that feeder, the other DVRs replenish the energy in the common DC link dynamically. Thus, one DVR in the IDVR system works in voltage-sag compensation mode while the other DVRs in the IDVR system operate in power-flow control mode. The authors designed a novel control strategy in which the phase angle of the reference voltages of the DVR shifts with certain angle. This phase shift increases the active power of the feeder which is used to replenish the DC link energy. They have also proposed a multi loop control systems to provide necessary reference signal voltages for shifting phase angle.

Ahmed Elserougi et.al [6] provided, the in-phase technique for two different types of loads i.e. constant impedance and three phase induction motor. Since the voltage restoration process may need real power injection into the distribution system. The power controller in one of the DVRs of IDVR, injects this power via voltage injection; this voltage injection was simulated by voltage drop across series virtual impedance. A new scheme was proposed to select the impedance value. The impedance value was selected such that the power consumed by this impedance represents the required power to be transferred without perturbing the load voltage. The performance of this system was also studied during voltage swell condition. The same author recently proposed an IDVR model to improve displacement factor by the exchange of real and reactive power between the feeders and IDVR [73].

Carl Ngai-Man Ho et.al [49] implemented a fast dynamic control scheme for capacitor-supported IDVR. The power stage of the IDVR consists of three inverters sharing the same dc link via a capacitor bank. Each inverter had an individual inner control loop for generating the gate signals for the switches. The inner loop was formed by a boundary controller with second-order switching surface, which made the load voltage ideally revert to the steady state in two switching actions after supply voltage sags. The load-voltage phase reference was common to all three inner loops and was generated by an outer control loop for regulating the dc-link capacitor voltage. This structure made the unsagged phase(s) and the DC link capacitor to restore the sagged phase(s).

P. Usha Rani [74] had proposed a Space vector modulation technique consisting of open loop and closed loop system for IDVR to mitigate voltage sag. The proposed single phase model of the IDVR system was illustrated which was operated by Multiple Pulse Width Modulation (PWM). A power system was created using Matlab Simulink tool for 20% of the voltage swell/sag which was compensated using open loop control and 20% of the voltage swell was compensated using closed loop control.

P Vasudevanaidu et.al [3] have designed a hysteresis voltage control based IDVR in three phase system under different considerations and had proposed the IDVR for improving power quality in parallel feeder distribution system with help of multi converts. The IDVR was developed to inject the required volt ampere power into faulty feeder system in order to regulate the load voltages. The proposed method was able to compensate voltage sag and unbalanced voltages with optimal phase jump angle by using IDVR and with minimum VA rating.

Masoud Shahabadini et.al [75] had proposed a new idea to reduce the load power factor under sag condition, and therefore, the compensation capacity of IDVR was increased. The proposed IDVR employed two cascaded H-bridge multilevel converters to inject AC voltage with lower THD and eliminated necessity to low-frequency isolation transformers in one side. The cascaded H-bridge inverter which reduces load power factor under sag condition so that compensation capacity was reduced.

Moradlou M et. al [4] have explored the limitations of IDVR in absorbing power from a healthy feeder which is further narrowing its voltage sag compensation range. After identifying and formulating various limitations in IDVR operation, a design procedure was presented to determine the optimum size (or rating) of the DVRs in an IDVR structure

2.11 Gaps in Research

Limited research is focussed on replenishing the DC link energy of IDVR. The major observation is that in the methods proposed [76], [77], [11] in a IDVR, only one DVR is injecting voltage while the other DVR works on replenishing the DC link energy. It is always assumed that the feeder connected to that particular DVR is assumed as healthy in all conditions. This is not always feasible. Hence bidirectional compensation of IDVR i.e. the two DVRs should function for voltage sag compensation and replenishing energy at dc link is not covered either in simulation or with a prototype model. This is the first deviation in the research of IDVR.

The second major observation is that the inverters used in the IDVR is always voltage source inverters. None of the papers were using current source inverters in the building blocks of IDVR. As the current source inverters have quite advantages than voltage source inverters, the current source inverters can be replaced with voltage source inverters. The current source inverter has inductor in DC link. A SMES coil could instead be incorporated onto the DC bus. Interfacing the coil to the ac system through a current source inverter results in a device that injects a controlled current with the ability to regulate ac voltage or power flow under normal conditions and supply when the power supply is off-line [6]. Also the Total Harmonic Distortion (THD) of the current source inverters is less than voltage source inverters [6].

P. Usha Rani, P Vasudevanaidu have not considered any real time existing load for performing the simulation on IDVR. This is the third major gap of IDVR. If the IDVR is simulated with real time electrical network data, the performance of IDVR in mitigating voltage sag/swell can be substantiated in a better way.

2.12 Discussion

The research gaps related to the Interline Dynamic Voltage Restorer (IDVR) are identified. These gaps are addressed in this research. In order to have control output from IDVR detailed modelling of the components of IDVR is important. The mathematical modelling is addressed. A novel methods are introduced to replenish the DC link energy of IDVR. The limitation observed in previous research for restoration of DC link energy will be covered by the proposed novel method. Further research focuses on replacement of voltage source inverters with current source inverters. A comparative analysis of the two inverters as the building blocks of IDVR is examined on a test power system.

The next phase of the research is the simulation of IDVR using a real time data. IDVR is designed for a specific application to mitigate power quality problems in an existing real time load. In order to substantiate the simulation results obtained, a laboratory prototype model of IDVR is also

covered in this research. The experimental set up of IDVR is developed in a laboratory environment and performance of IDVR is tested in practical scenario. The next chapter discusses the modelling of IDVR.

Chapter 3

Modelling of IDVR

3.1 Introduction

The significant components of IDVR are its inverters and the DC link. In order to have control output from IDVR detailed modelling of these components is important. Subsequently the ability of IDVR in mitigating the voltage sag is to be investigated in a test power system. A control system is designed to monitor the voltage profile and control the voltage injection of IDVR to maintain the load voltage. Thus this chapter establishes the modelling of IDVR's inverter and its DC link along with its application in maintaining voltage profile.

3.2 Interline Dynamic Voltage Restorer

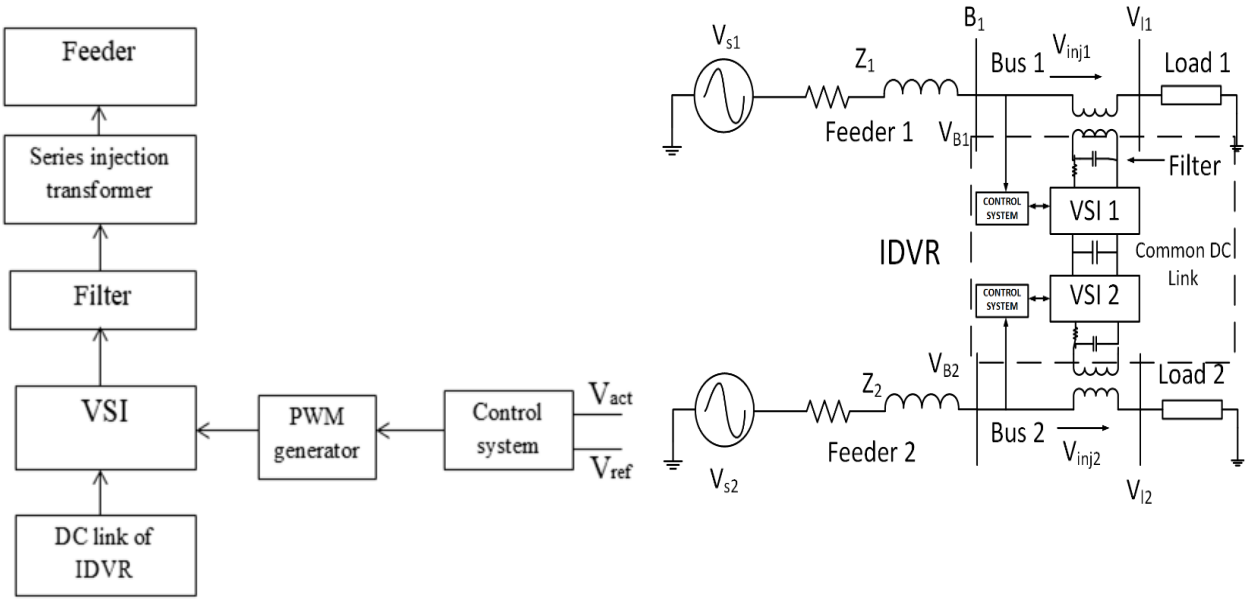


Fig. 3.1 Schematic layout of two line IDVR

The IDVR constitutes of minimum two **VSI**'s, where the inverters are connected together at the **DC link**. The required series injected voltage magnitude is computed by the **Control system** and whose output modulates the VSI's to inject the voltage through the series **injection transformer**.

The involvement of the power electronic devices would introduce harmonics in the injection voltage which are mostly eliminated by the **filters**. The details of these building blocks are discussed in the following sections.

3.2.1 Inverters

The function of inverters in IDVR is to inject the necessary series voltage into the distribution power system to which IDVR is connected. The inverter takes the DC link energy of IDVR as the input voltage and converters into the required AC voltage. The broad classification of inverters in the voltage source inverter (VSI) and the current source inverter (CSI). VSI can be classified on various types depending on the VSI configuration. VSI can be further classified as half-bridge inverters and full-bridge inverters, or depending on the phases as single phase and three phase inverters. VSI can also be further classified into square wave inverters and pulse width inverters. The advantages of VSI are low cost, small size, less complicated compared to CSI. Despite of these advantages it has also some disadvantages like slow control of the converter, no short circuit or overcurrent protection. On the other side, CSI are the type of inverters fed with a current source with high impedance. The source at the AC side of the inverter may be a current source or inductor in series with a DC source. As the input voltage is constant in VSI, in CSI the input current is constant but adjustable. The amplitude of the output current is independent of load. The waveform and magnitude of the output voltage depends on nature of load. The advantages of CSI are its excellent current control capability, easy protection from short circuit or overcurrent, and output current is ripple free, though it is costlier than VSI.

Initially the DC to AC conversion is carried out by using the transistors. The basic circuit of the DC to AC conversion consist of two transistors. One is PnP transistor and second is npn transistor. The transistors are connected in push-pull manner, and operates in common emitter configuration. The collector, base for two trnasistors are shorted. The collector of npn transistor is associated with positive DC supply(E+), and collector of the pnp transistor is associated with the negative DC

supply(E-). For the positive voltage the npn transistor behaviors and we get the positive pulse at the o/p and for the negative supply voltage pnp transistor behaviors and we get the negative pulse at the o/p voltage.

Voltage Source Inverter Types

Based on the construction, output voltage and implementation level, the VSI are divided into three main types as [41], [78]–[82]:

1) Single-phase half-bridge inverter

2) Single-phase full-bridge inverter

3) Three phase voltage source inverter

1) Single-phase half-bridge inverter

The push pull sort converter has a few impediments. It requires the double power supply for operation of transistors. Likewise transistorized VSI requires the two distinctive sort of transistors, for example, npn and pnp, and both the transistors have diverse switching speed. In view of these two drawbacks

IGBT are utilized as a part of the circuit. The single stage VSI comprise of two IGBT. The IGBT are work like the switches. In half bridge topology the i/p DC voltage is symmetrically partitioned because of similar capacitors associated over the DC supply.

2) Single-phase full-bridge inverter

The single stage voltage source rectifier incorporates two fundamental inverter legs i.e. two half bridge inverters. It is like the o/p waveform of the half extension VSI. As in the half bridge VSI, the o/p waveform of the full bridge VSI comprise of the disturbances. In full bridge inverter, when T1, T2 direct the o/p voltage is V_s and when T3, T4 conducts the o/p voltage is - Vs. The switches T1, T2 conducts for time of 0¡tT/2 and the switches T3, T4 conducts for time of T/2

3) Three phase VSI

The three stage VSI comprise of the three inverter legs i.e. three half extension inverters. The three

stage voltage is created by taking the o/p from every inverter leg. These are the essential three sorts of the VSI. It can be additionally divided on the no. of bases in o/p voltage waveform, for example, 5 stage, 7 stage, and so forth. Additionally VSI can be divided on the premise of controlling parameters of o/p waveform.

The VSI used in this thesis work is single phase and three phase voltage source inverters.

3.2.2 DC Link of IDVR

This a very important part of IDVR. The amount of energy required by IDVR to mitigate the voltage sag is supplied by the DC link of IDVR. If sufficient amount of energy is not present in the DC link, the IDVR will fail to perform the voltage compensation. Hence the calculation of DC link of Energy of IDVR is very important. In general, the DC link of IDVR consists of a capacitor is the inverter is VSI and a inductor if the inverter is CSI.

3.2.3 Control System

As the inverter injects the necessary voltage into the power system, there should be controlling mechanism to monitor and control the injected voltage. The control system of IDVR checks the error between the reference and actual voltages of the feeder to which IDVR is connected and it provides necessary gate signals to the inverter which of the IDVR through the PWM generator.

3.2.4 Series Injection Transformer

The injection transformer acts like a bridge between the inverter and the power system to which the IDVR is connected. The injected voltages are introduced into the power system through an injection transformer connected in series with the feeder. In general Factors that should be taken into consideration when deciding on the primary winding rated voltage of the injection transformer are the Sag magnitude specification and inverter rating of IDVR.

Among the various parts of IDVR the modelling of the inverter and the DC link voltage of IDVR is important. Proper design of IDVR depends on the modelling of inverter and the DC link voltage of

IDVR. The following section discussed the modeling equations of IDVR.

3.3 Modelling of IDVR

A simple IDVR constitutes of two VSI's connected together at the common DC link. Each of these VSI's are incorporated in the feeder through series injection transformer. A two line custom power device IDVR integrated into the power system distribution network is shown in fig 3.2(a). Each VSI injects series voltage $V_{inj,i}$ (where $i = 1,2$) whose magnitude is controlled through the designed the control system along with its harmonics being eliminated through a filter. The distribution network shown in fig 3.2(a) contains two feeders having two buses 1 and 2 in each feeder with bus voltages V_{b1} and V_{b2} respectively. Two loads, represented as load 1 and load 2 are connected at the end of the each feeder respectively. These loads are assumed to be sensitive loads. Sensitive loads are the modern appliances integrated with electronics and microprocessors such as Digital Computers, Variable Frequency Motor Drives, Programmable Logic Controllers, Computer Numerical Control (CNC) Equipment, servers, computing centers, communication equipment, Automated Systems and Processes, etc. They improve performance capability but are sensitive to common power quality and reliability problems. Thus, an excessive number of industrial process interruptions has been verified as a results of voltage variations., even without of electric power outage as these devices are more vulnerable to deviations from the minimum requirements. Protection of these critical loads is essential.

The voltages at the load are defined as V_{L1} and V_{L2} for load 1 and load 2 respectively as shown in Fig. 3.2(a). The load voltages are to be maintained at the rated value which is equal to V_{b1} and V_{b2}. Due to the variation in addition of loads the load voltages fluctuate from the nominal value. However the series injected voltages V_{inj1} and V_{inj2} from the VSI's of the IDVR maintains the load voltage profile constant in the event of voltage sag or swell condition. The relationship between the bus voltage, load voltage and injected voltage can be represented as:

$$V_{b1} = V_{inj1} + V_{L1} \tag{3.1}$$

$$V_{b2} = V_{inj2} + V_{L2} \tag{3.2}$$

The model of IDVR consists of two parts; Inverter Model and DC capacitance model

3.3.1 Inverter Modelling

The inverter considered is the VSI shown in fig 3.2(a).

The voltage of the sources of two feeders V_{s1} and V_{s2} respectively are discussed as:

$$V_{s1} = I_1 Z_1 + V_{inj1} + V_{l1} \tag{3.3}$$

$$V_{s2} = I_2 Z_2 + V_{inj2} + V_{l2} \tag{3.4}$$

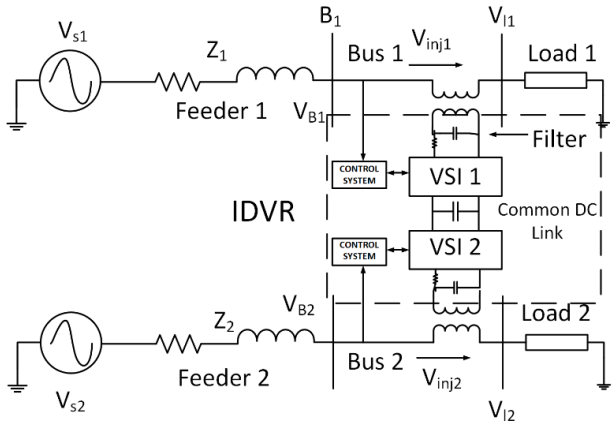
Neglecting losses (IZ) in the both feeders equations (3.3) and (3.4) can be written as

$$V_{inj1} = V_{s1} - V_{l1} \tag{3.5}$$

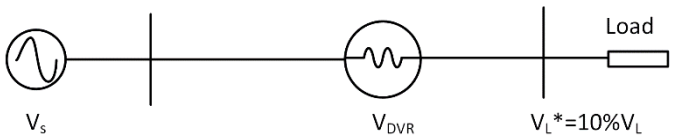
$$V_{inj2} = V_{s2} - V_{l2} \tag{3.6}$$

From equations (3.5) and (3.6), the voltage injected from the IDVR is approximately the difference of supply and load voltages of the feeder. Hence, the inverter voltage rating of IDVR can be determined if the amount of voltage sag that needs to be compensated by the IDVR.

Fig. 3.2 represents the one line diagram of one of the feeder shown in fig. 3.2(a). According to equations (3.7) and (3.8) if $V_s = V_L$ then $V_{DVR} = 0$ which implies there is no need for compensation. The need for voltage compensation is only if $V_s \neq V_L$.



(a)



(b)

Fig. 3.2 (a) Schematic layout of two line IDVR (b) One line diagram of one of the feeder shown in (a)

The voltage compensation by the IDVR will be initiated when

$$V_L^* < V_s \tag{3.7}$$

Where $V_L^* = V_L - (0.10 * V_L)$

Therefore the V_{DVR} is given as

$$V_{DVR} = V_S - V_L^* \tag{3.8}$$

Hence the voltage rating of the two voltage source inverters

Shown in fig 3.2(a) can be determined by using equation 3.7.

The voltage rating of inverter can be determined by using equation 3.7 only when the in phase

compensation method is considered [83]. The in phase method of compensation is used among various compensation control strategies because, in the in phase method of compensation the inverter rating is proven less compared to the other methods of compensation like pre sag compensation and quadrature compensation.

The phasor diagram of the in phase compensation method is shown in fig. 3.3.

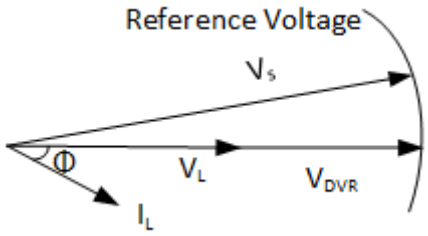


Fig. 3.3 Phasor diagram of in phase method of compensation

In the in phase method of compensation, the voltage injected by the DVR is in phase with load (sagged) voltage. Fig.3.3 represents the phasor diagram of in phase compensation. The injected voltage V_{DVR} is in phase with load voltage. As shown in fig. 3.3 the load current is having a phase difference with injected voltage, hence the DVR should inject active power along with reactive power to the load nearly at all times. The reason for choosing the in phase methods over various voltage compensation methods is because the inverter rating with in phase compensation is less compared to the other methods like energy saving method, quadrature compensation method etc. [83]. From fig. 3.3 the real power of the each DVR of IDVR is

$$P_{DVR} = V_{DVR} \times I_L^* \times \cos\phi \tag{3.9}$$

Where

V_{DVR}: Voltage injected by the DVR

I_L: Load current

$\cos\phi$: Load Power factor

Therefore using equations (3.8) and (3.9) the power and voltage rating of the inverter of IDVR can be determined. The next section describes about modelling of DC link of IDVR.

3.3.2 DC link Capacitor Modelling

Designing the DC link of IDVR is very essential because the energy for IDVR to mitigate the voltage sag is supplied from the DC link. As the voltage source inverters are used as the building blocks of IDVR to mitigate the voltage sag, a capacitor is connected at the DC link of two DVRs of IDVR which is shown in fig 3.2(a).

The expression for the DC link power is given as

$$P_{DC} = P_{DVR1} + P_{DVR2} + P_{losses} \tag{3.10}$$

Where P_{DVR1} and P_{DVR2} are power required by the two DVRs of IDVR for mitigating the voltage sag and P_{losses} is the losses in the DVR system.

Assume $P_{losses} = 0$ then

$$P_{DC} = P_{DVR1} + P_{DVR2} \tag{3.11}$$

Since a capacitance is used as the DC link, the DC link power P_{DC} can also be expressed as

$$P_{DC} = \Delta W_{DC} \times t \tag{3.12}$$

Where ΔW_{DC} is the energy provided by the DC link capacitor. Whenever the IDVR compensates the voltage sag, the energy provided by the DC link link capacitor is expressed as

$$\Delta W_{DC} = \frac{1}{2} \times C \times (V_{DC\max}^2 - V_{DC\min}^2) \tag{3.13}$$

V_{DCmax}: DC link voltage

V_{DCmin}: Permissible DC link voltage (The maximum limit below which the DC link voltage should not decrease)

From equations 3.12 and 3.13 the DC link capacitance is given as

$$C = \frac{2\times(P_{DVR1}+P_{DVR2})}{(V_{DC\max}^2 - V_{DC\min}^2)\times t} \tag{3.14}$$

The DC link voltage is

$$V_{DC\max} = \frac{3\sqrt{3}}{\Pi}\times V_S \tag{3.15}$$

where V_s is source voltage of the feeder to which the IDVR is connected.

In equation 3.14 if the amount of voltage compensated by the two DVRs of IDVR is equal then $P_{DVR1} = P_{DVR2} = P$. The capacitance is given as

$$C = \frac{4\times P}{(V_{DC\max}^2 - V_{DC\min}^2)\times t} \tag{3.16}$$

Following the modeling of IDVR, the testing capability of IDVR in mitigating the voltage sag is to be investigated. The IDVR is simulated with a test power system. The power system network with IDVR shown in fig 3.2(a) is developed in MATLAB Simulink. The parameters of the elements of the system are given in table 3.1

Table 3.1: Parameters of the Two Line IDVR Shown in fig 3.2(a)

Parameter	**Feeder 1**	**Feeder 2**
Supply voltage (V_s)	230V	230V
Load Voltage (V_l)	230V	230V
Load Resistance (R_l)	40Ω	40Ω
Load inductance (L_l)	95.5mH	95.5mH
Transformer resistance (R_t)	3 Ω	1 Ω
Transformer inductance (L_t)	10mH	6mH
DC capacitance (C_{dc})	3200μF	
DC capacitance Voltage (V_{dc})	210V	

Subsequently important aspect of the IDVR is its control system. The control system checks the error between the reference and actual voltages of the feeder to which IDVR is connected and it provides necessary gate signals to the Voltage source inverter through the PWM generator. Proportional Integral (PI) Controller is used in both VSI‘s of the IDVR to control the voltage injection into the feeder to eliminate voltage sag. Additionally it eliminate harmonics produced by the load. The following section discusses the PI controller of IDVR.

3.4 Control Systems of IDVR

The functionality of IDVR is to eliminate voltage sag in a system. During the occurrence of a voltage sag, the IDVR detects the deviation in the voltage and injects the necessary voltage into the network thereby maintaining the system voltage constant at all conditions. The control system of IDVR plays an important role in controlling the necessary injected voltage from IDVR. The controller checks the error between source and load voltage (where the voltage sag occurred) and the error is given to the PWM generator to generate the required gate pulses for Voltage source inverters to inject the required voltage to the system. In second DVR VSI of IDVR compensates the energy at the DC link with assistance from Phase Shifting Transformers. The controller simultaneously maintains the required load voltage in addition while replenishing the energy at the DC link.

The schematic layout of the control system of IDVR is given fig 3.4.

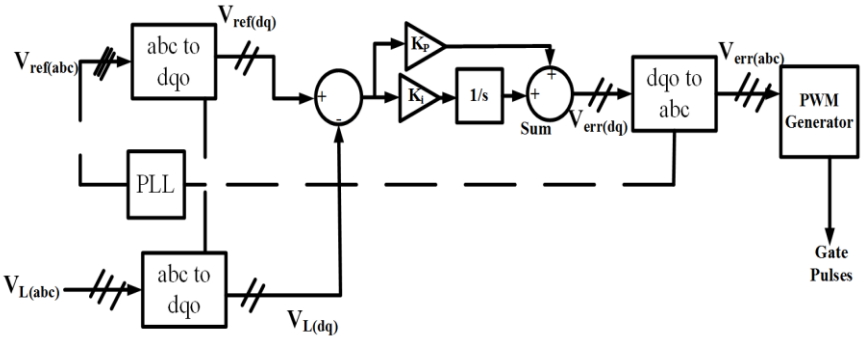


Fig. 3.4 Schematic Layout of Control System

According to the schematic layout represented in fig 3.4, the reference voltage $V_{ref(abc)}$ is converted to dq axis reference frame $V_{ref(dq)}$ axis using parks transformation for reducing the complexity of calculation given by

$$\begin{bmatrix} V_{refd} \\ V_{refq} \\ V_{refO} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta-\frac{2\Pi}{3}) & \cos(\theta+\frac{2\Pi}{3}) \\ -\sin\theta & -\sin(\theta-\frac{2\Pi}{3}) & -\sin(\theta+\frac{2\Pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} V_{refa} \\ V_{refb} \\ V_{refc} \end{bmatrix} \quad (3.17)$$

Similarly $V_{L(abc)}$ is also converted to $V_{L(dq)}$. The error between the reference voltage and load or actual voltage is given is given as input to the Proportional Integral controller. The Proportional Integral controller regulates error and the output of the Proportional Integral controller is given by equations (3.18) and (3.19)

$$V_{errd} = (K_p + \frac{K_i}{S})(V_{refd} - V_{Ld}) \quad (3.18)$$

$$V_{errq} = (V_{refq} - V_{Lq})(K_p + \frac{K_i}{S}) \quad (3.19)$$

Where

K_p and Ki are proportional integral gains of PI controller.

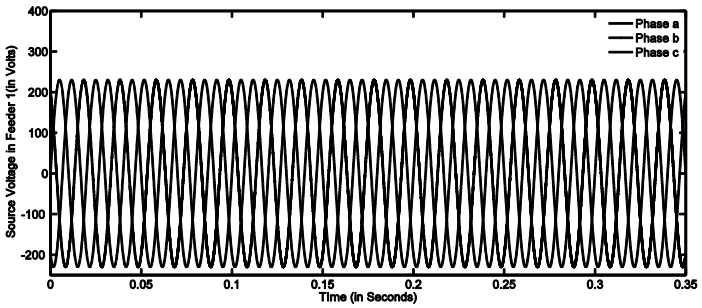
The $V_{err(dq)}$ is converted to $V_{err(abc)}$ by the dqo to abc transformation and $V_{err(abc)}$ is given to the PWM generator. The PWM generator generates the required gate pulses to the inverter. The values of K_p and K_i are determined by zigler- Nicholas method.

3.5 Results

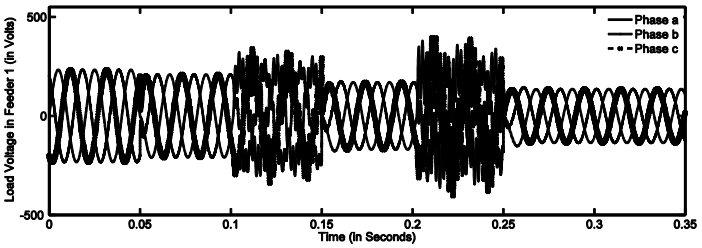
The total IDVR system is constructed in MATLAB Simulink software. The ratings of the various parameters of fig 3.1 are given according to table 3.1. The total simulation is performed for 0.35 seconds. This short duration indicates the speed of the IDVR is responding to the system. IDVR having two DVRs connected in series to the feeders with transformers. When there is a voltage sag in feeder 1, DVR 1 acts to mitigate it. In order to supply the required energy to DVR 1 for

mitigating the voltage sag, the capacitor connected at the DC link contains some initial energy stored. When there is voltage sag, DVR 1 responds and the energy stored in the capacitor is being utilized to compensate for the sag.

The Simulink results of the two line IDVR system are given in fig 3.5 and fig 3.6. The results show the Power Quality problem like voltage sag and harmonics with absence of IDVR and the rectification of these problems with IDVR.



(a)

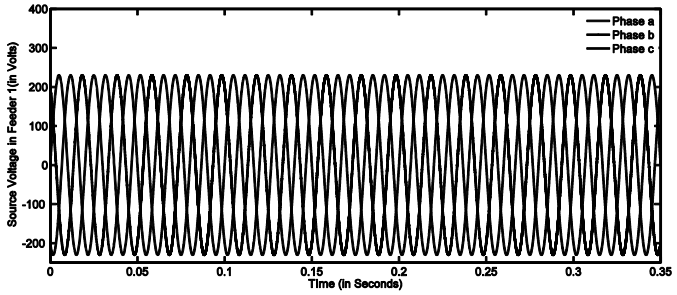


(b)

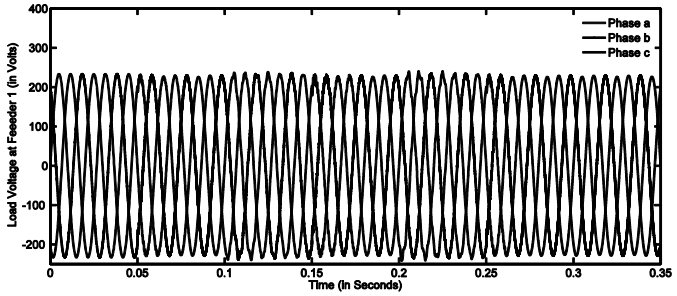
Fig. 3.5 (a) Source Voltage waveform (b)Load Voltage waveform in feeder 1 without IDVR

Figs. 3.5a and 3.5b show the response of the voltage at feeder 1 on the supply side and load side respectively, when the IDVR is not connected. Load at feeder 1 is continuously switched ON and OFF in three intervals. In the first interval it is ON from 0.05 to 0.1s, 0.15 to 0.2s in second interval and similarly third interval load is ON from 0.25 to 0.35 seconds. This is to show the concept of dynamic nature of load. According to the fig 3.5a, the supply voltage is balanced. In fig 3.5b it can be seen that the load voltage magnitude of feeder 1 is completely distorted. The voltage sags can be

seen from 0.05 to 0.1, 0.15 to 0.2 and from 0.25 to 0.35 seconds when load is ON and OFF respectively. In the time intervals from 0.1 to 0.15, 0.2 to 0.25 voltage swells are observed because there is no load ON at the time, so voltage has risen. This nature of voltage is observed and monitored put to the PI controller in the control strategy of DVR 1. PI controller modulates the error and output of the PI controller is given to PWM generator to generate required gate pulses to switches in Voltage Source Inverter to modulate the magnitude of the injected voltage.



(a)



(b)

Fig. 3.6 (a) Source Voltage waveform (b)Load Voltage waveform in feeder 1 with IDVR

Figs.3.6a and 3.6b show the voltage waveform of he feeders are connected with IDVR. Fig. 3.6a is the supply voltage of feeder 1 which is similar to fig 3.5a. With the presence of IDVR the voltage sag that is observed in fig 3.5b is completely eliminated as seen in fig 8b. The load voltage magnitude is maintained to 230V by IDVR. The harmonics are eliminated by the PI controller and inductor, which are used as a filter. Hence complete pure sinusoidal waveform is observed in fig 3.5b.

As shown in fig. 3.7, the required energy for the IDVR to mitigate the sag feeder 1 is supplied by the DC link as seen in the decrease of DC link voltage. The charge of the capacitance will be utilized to mitigate the sag feeder 1. As observed in fig 3.7 the capacitance voltage is discharged from 210V to 208V.

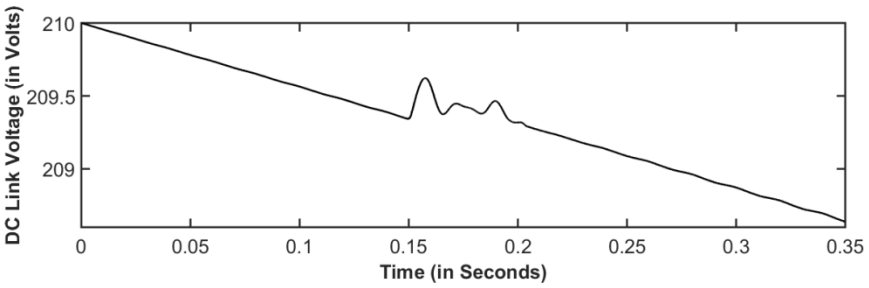


Fig. 3.7 DC Link Capacitance Voltage

Hence, we can conclude that the IDVR is successfully in mitigating the voltage sag and the PI controller in IDVR checks the error between reference and actual voltages and provides necessary gate signals to voltage source inverter through PWM generator, there by the PI controller controls the injected voltage by the IDVR to mitigate voltage sag. But the only problem is replenishing the DC link energy. In fig 3.7, the DC link energy has given some energy for IDVR to mitigate the voltage. If this process repeats, at one stage the DC link voltage will become zero which would be determined in the operation of IDVR. Hence there has to be a process to restore the DC link energy. In the next chapter, a novel method of restoring the energy at the DC link of IDVR either from PV source or with PST is discussed.

3.6 Conclusion

This chapter discussed about the modelling of IDVR. Mathematical Modelling of inverter and DC link of IDVR are the key factors in the design of IDVR. Therefore a detailed mathematical modelling of Inverter and the DC link of IDVR is covered in this chapter. Followed to the modelling equations, the IDVR is tested to its capability of mitigating voltage sag with a test power system. The results have proven that the IDVR is capable of compensating voltage sag. In addition

it is observed that there should be a mechanism to replenish the DC link energy of IDVR, as the DC link supplies the required energy to the IDVR for mitigating the voltage sag. In the next chapter the restoration of DC link energy with PST and PV source is discussed. A details description of PST and PV are given.

Chapter 4

Replenishing DC Link of IDVR

4.1 Introduction

In the previous chapter IDVR has been simulated to mitigate the voltage sag in test power system. The DC link of IDVR provides the required energy to the IDVR for mitigating the voltage sag, due to this the DC link energy diminishes. The restoration of the DC link energy of the IDVR is a weighted factor in the robust operation of IDVR. This chapter describes the novel methods employed in restoration of DC Link energy. One of the methods employed were by utilizing the capacity of phase shifting transformer to shift the phase and controlling the power necessary to change the DC link. Additionally a PV system is utilized which is connected across the DC link to aid in the restoration process. A controlled algorithm is designed between PST and PV source depending upon the loading conditions of the feeder and surplus power available with the PV source respectively to replenish DC link energy.

4.2 DC Link of IDVR

The major component of the DC link of the IDVR is its energy restoration. The amount of energy required by IDVR to mitigate the voltage sag is supplied by its DC link. If sufficient amount of energy is not present in the DC link, the IDVR will fail to perform the voltage compensation. Restoration of the DC link energy plays a vital role in the capability of the VSI of the IDVR to mitigate multiple deep sags with long durations. Hence the restoration of DC link Energy of IDVR is very important. In general, the DC link of IDVR consists of a capacitor is the inverter is VSI and an inductor if the inverter is CSI. There are several methods and techniques proposed for replenishing the DC link energy of IDVR and are discussed in following section.

4.2.1 Literature Review on Replenishing DC Link Energy of IDVR

Traditional method of restoring the DC link for other FACTS devices like SSSC were with the help of battery but requirement of huge rating battery is foreseen as IDVR may be utilized for voltage sag mitigation in both feeders simultaneously. Alternate methods were proposed avoiding a battery.

Literature review presents different methods for restoring the DC Link energy. Mahinda et.al [72] have introduced a control strategy which shifts the angle of the considered DVR voltages so that the DC link energy is restored with increase of real power in the feeder. They have also proposed a multi loop control systems for shifting phase angle of necessary reference signal voltages [84]. Ahmed etal [73] proposed a virtual impedance to compensate the energy of DC link. The authors also proposed an IDVR model to improve displacement factor by the exchange of real and reactive power between the feeders and IDVR [85]. Carl et.al [49] designed a control strategy to increase the phase shift of DVR voltages. Thereby the real power in the feeder where the controller is connected increases. This increment in real power is fed to the DC link. P. Usha Rani has proposed a Space vector modulation technique for IDVR to mitigate voltage sag [77]. P Vasudevanaidu et.al [3] have proposed a method of optimal phase angle jump computed by particle swarm optimization method to reduce the VA rating of the IDVR. Masoud Shahabadini et.al have designed cascaded H-bridge inverter which reduces load power factor under sag condition so that compensation capacity is reduced [75]. Moradlou M et.al have given the compensation of capability of IDVR under various balanced and unbalanced voltage sag scenarios [11] . In the above literature the authors have restored the DC link by considering one of the feeder to be healthy which will provide surplus amount of real power, however it is not possible in practical scenario. So there should be a provision to restore the DC link energy of IDVR from any of the feeder to which IDVR is connected. In this chapter it is proposed to utilize a Phase Shifting Transformers (PST) and PV source to replenish the energy at the DC link in between the two DVR's of IDVR.

The industries are now focusing on renewable source energies for providing electrical power that is used for different purposes like feeding the local load, supplying the auxiliaries etc. PV or solar is one of the finest source that can be installed in the industries very easily. Hence, the energy from either PV source or with PST will be selected for replenishing the DC link energy. Based on the sag condition and various power system conditions, the appropriate source (among PV source and PST) is selected for replenishing the DC link energy using an algorithm

Different cases proposing the management of energy is presented in this chapter. The following sections in this chapter are related to the control system of IDVR, Phase Shifting Transformers, and finally the simulation results.

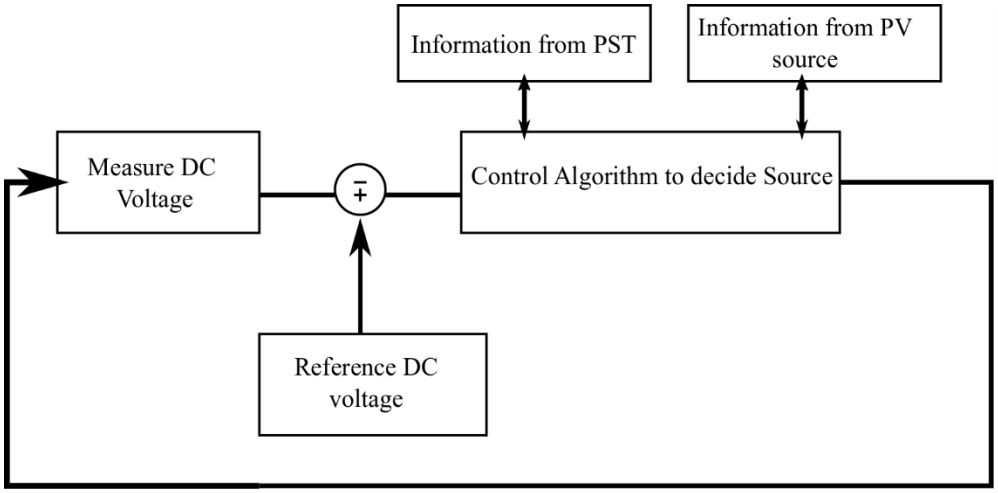
4.3 DC Link Controller

The block diagram of the DC Link controller of IDVR is represented in fig 4.1(a) and the function algorithm is given in fig 4.1 (b). The function of the DC Link controller is to compare the reference DC link and actual DC link voltage during the voltage sag condition and based on prevailing conditions the controller chooses the suitable source appropriately among the PV system or PST. Therefore, the DC link energy is replenished as observed in maintain the DC link voltage constant.

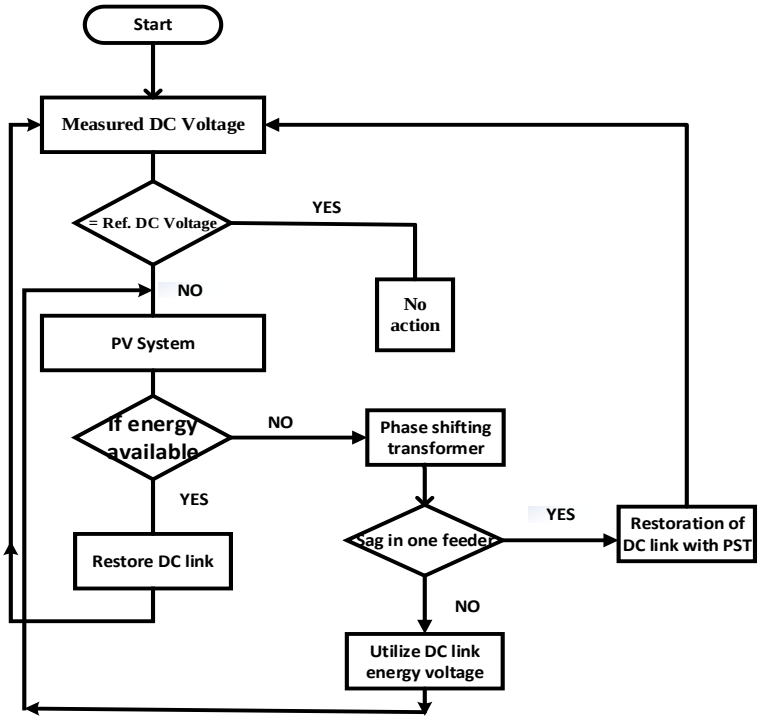
The control algorithm of the DC link controller is explained in fig 4.1(b). Initially the DC link controller checks the difference between reference DC link voltage and actual DC link voltage. If the voltages are deviating then the DC link controller checks the availability of PV source. If PV generation is surplus and sufficient enough to give the required energy then it is utilized to restore the DC link energy. If PV has insufficient energy for the restoration process then the controller checks with the PST.

However the secondary and necessary condition for is that if the voltage sag occurs in one feeder, the second feeder should be healthy, if so then the DC link controller restores the DC link energy with PST using real power from the healthy feeder. If neither of the two sources are able to restore

the energy then it utilises the stored DC link energy from the capacitance. This advantage is the battery requirement is eliminated and the rating of DC link capacitor is reduced since its energy is almost replenished either by the two procedures. The next section explains about Phase Shifting Transformer.



(a)



(b)

Fig. 4.1 (a) Schematic Block Diagram of DC Link Controller of IDVR (b). Control algorithm of DC link controller

4.4 Phase Shifting Transformers

A Phase shifting Transformer (PST) controls the active power flow in a network by inserting the voltage with a controlled phase angle [86]. Fig.4.2 [86] represents the PST comprising of magnetizing transformer connected in parallel to the feeder and transformer which is connected in series to the feeder is boosting transformer. The phase shift is created by connecting these two transformers together and there by controlling real power flow in the line. The secondary side of magnetizing transformer consists of a tap changer. By regulating the tap changer the real power will be regulated. The power angle equation is

$$P = \frac{V_1 \times V_2}{x} \sin \delta \qquad (4.1)$$

The operation of PST is illustrated by the phase diagram in the figs 4.3(a) and 4.3(b). To shift the phase angle in one phase (say R phase), the input of the magnetizing transformer is connected to the other two phases (Y and B phases).

V_{YB} is the resultant voltage in the phasor diagram which is fed to the primary winding of the boosting transformer. Observing the phasor diagram in fig 4.3(a), the voltages V_{YB} and V_{RN} have phase difference of 90^0. The resultant voltage between V_{YB} and V_{RN} will be the output of the boosting transformer. Depending on the magnitude of voltage vector $V_{YB,}$ the resultant voltage phase and magnitude can be determined. According to the power equation in 4.4, the active power will be increased with the increment in the phase difference between the resultant voltage and load voltage as shown in fig 4.3(b). Thus by vary of δ with the assistance of PST, the active power in the line is controlled. This controlled power is supplied to DC link via VSI which connected to the DC link. Additionally the load voltage of feeder 2 remains unaffected in this process. It is discussed that along with PST, PV source is also used for restoration of DC link energy of IDVR. The next section describes about PV Source.

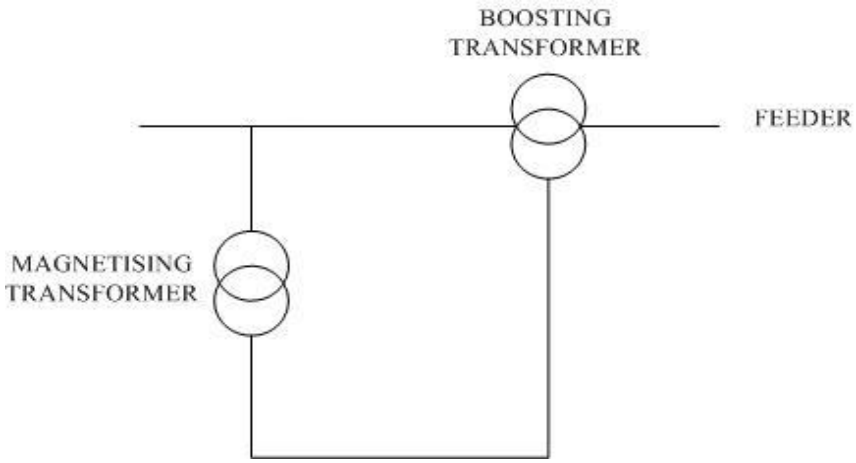
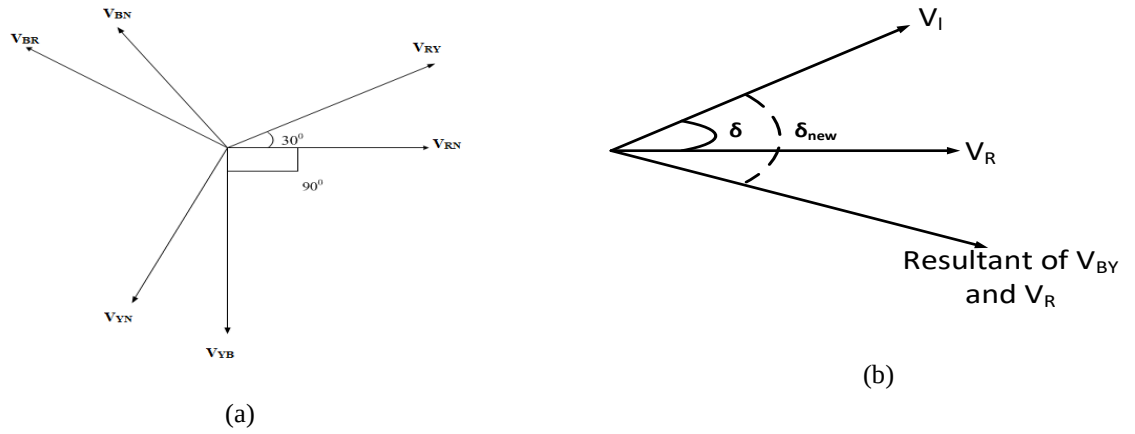


Fig.4.2 Schematic Layout of Phase Shifting Transformers



(a) (b)

Fig.4.3 (a) Phasor Diagram of Voltages in healthy feeder with PST (b) resultant phasor diagram of healthy feeder

4.5 PV Source

Lately industries are focusing on utilizing renewable sources to feed their local load. The widely captured renewable energy source is Solar. Capitalizing this factor in industry where the voltage sag compensation is a requirement, PV source is considered as alternate means of restoring the DC link energy.

As the insolation and cell temperature varies from time to time due to environmental factors, several algorithms were proposed to design the mechanism such that the PV cells will generate maximum power at each interval. This is called maximum power tracking (MPPT). Numerous algorithms based on Perturb and Observe (P&O), fuzzy controller, neural network, ripple correlation control, load current voltage maximization etc. were considered for MPPT [87][88]. P&O is considered in the paper because of its simplicity and low cost. In this algorithm maximum power point is tracked once, if the second value is more than the recorded one, then this second value overwrites the first one. This process is repeated continuously with the PV system supplying the local load.

Assuming the load is dynamic in nature, when load demand is less than the supply, the differential amount of energy between source and load can be utilized to replenish the energy at the DC link This PV system is connected across DC link power generated is in DC. The

next section explains about the simulation results of IDVR with test system.

4.6 Results

The test power system is constructed using MATLAB SIMULINK software is represented in fig 4.4. The two feeders each are having three phases connected to three different single phase loads i.e. the total load on one feeder is unbalanced load. Consider the case where one of the loads (Load 1 in this case) connected to the three phases of a feeder is sensitive, then this load clearly requires a protection from power quality issues mainly voltage sag. Hence IDVR is connected to that particular phase to ensure that the sensitive load is protected from the voltage sag. Loads 1 and 4 which are connected to feeder 1 and 2 are assumed as sensitive loads. The considered test power system parameters is represented in fig 4.4 are given in Table 4.1.

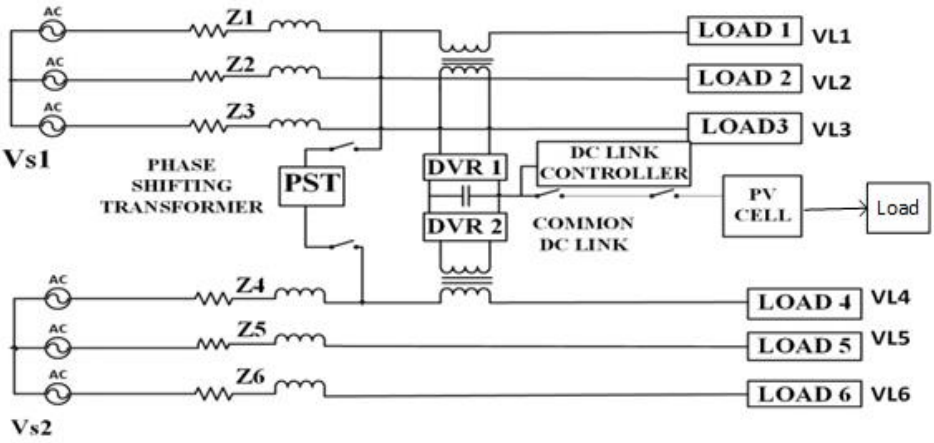


Fig.4.4 Simulink model of IDVR

TABLE 4.1 Parameters of two line IDVR

Parameter	**Feeder 1**	**Feeder 2**
Supply Voltage	230V	230V
Load Voltage (Load 1,2,3,4)	230V	230V
Load Resistance	40Ω	40Ω
Load Inductance	95.5mH	95.5mH
Transformer Resistance	3Ω	3Ω
Transformer Inductance	10mH	10mH
DC Capacitance	3200μF	
DC Capacitance Voltage	210V	

The DC link capacitor should be charged to a DC voltage given by (4.2) [89]

$$V_{ac} = \frac{3}{2} V_{dc} \tag{4.2}$$

Hence from 4.2, the DC capacitor voltage is calculated to 57V. As the DC link should supply energy to two DVRs of IDVR, the amount of DC link capacitor voltage should be doubled which is equal to 114V. Considering case of multiple sags and safety factor the final value of

DC link capacitor is 210V. The test system is run for 0.2 s.

Due to application of various loads during the interval a voltage sag is observed at corresponding period of times. The IDVR mitigates these sags as described in chapter 3. The DC link voltage restoration is examined in various cases of load application. The corresponding restoration of the energy to the DC link of IDVR is represented in different cases summarised in Table 4.2

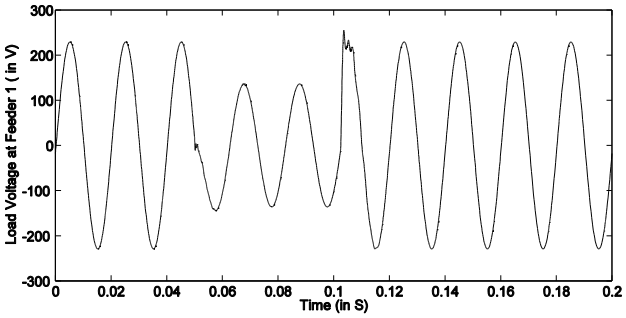
TABLE 4.2 Summary of the three cases considered

Case	**Number of Feeders affected with Voltage Sag**	**PV Source**	**Phase Shifting Transformer**
Case 1	One	On	Off
Case 2	One	Off	On
Case 3	Two	Off	Off

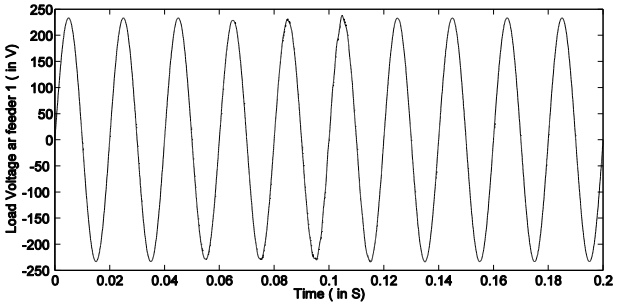
4.6.1 Voltage sag Observed in first feeder and restoring of the DC link energy with PV source

In this case, phase A of feeder 1 is assumed to be effected with a voltage sag for an interval of time and the second feeder is assumed to be unaffected. If the PV source is generating surplus power i.e., when the local load is consuming less power than the rating of its generation, then the controller selects the PV source to restore the DC link energy. The difference between the source and load powers of PV generation is fed to the DC link of IDVR to restore the DC link energy. The simulation of the power system with IDVR is performed in MATLAB for 0.2s. The voltage sag is applied in first feeder for a time interval

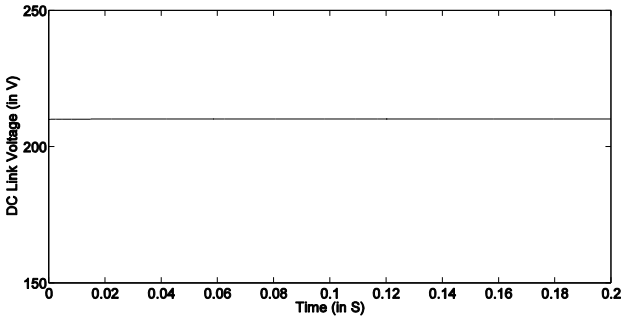
of 0.05s to 0.1s. The effectiveness of the IDVR in eliminating the voltage sag in the short duration is observed.



(a)



(b)



(c)

Fig.4.5 (a) Load Voltage at feeder 1 (in Volts) without IDVR (b) Load voltage in feeder 1 (in Volts) (c) DC link voltage (in volts) with IDVR and PV system

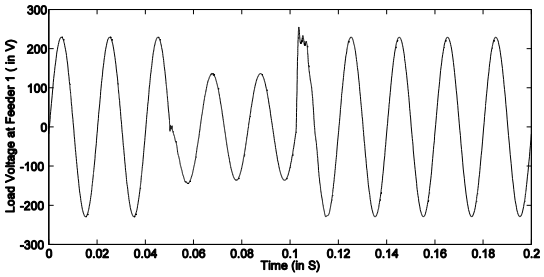
Fig. 4.5(a) represents the load voltage of feeder one without IDVR. It is shown from fig 4.5(a) that voltage at load 1 is declined from 230V to 150V in the duration of 0.05 to 0.1s due to the voltage sag. A small voltage swell along with harmonics are also observed after 0.1s.

Fig. 4.5(b) shows the compensated voltage of the load with the presence of IDVR. When the IDVR is compensating the voltage sag, the required power to restore the DC link energy is given by PV system. This can be observed by measuring the DC link voltage which is constant throughout i.e. 210V as shown in fig 4.5(c). In the event of delay the initially charged DC link will ensure no interruption in compensating the sag. This compensation is useful when there is voltage sag simultaneously.

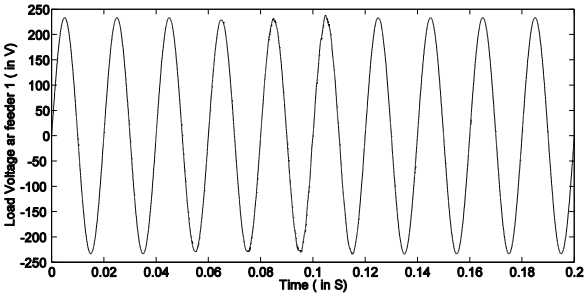
4.6.2 Voltage sag Observed in first feeder and restoring the DC link energy with PST

Likewise in first case, first feeder is effected with voltage sag for a period of time. Feeder 2 is considered to be unaffected. If control unit senses that the PV system is ineffective to supply the power to the DC link, at that point the control unit associates the PST to the second feeder. The angular Phase of the feeder 2 is shifted by Phase Shifting Transformer. The real power flow in the feeder 2 increases due to the phase shift. The incremental active power will be utilized for DC link restoration by second DVR present on the second feeder. The Proportional Integral controller present in the second DVR keeps the voltage of the load on second feeder to the rated value. Load voltage of feeder 1 during the voltage sag condition with the absence and presence of IDVR and voltage at the DC link with PST are represented in fig 4.6(a) and figs 4.6 (b), (c) respectively.

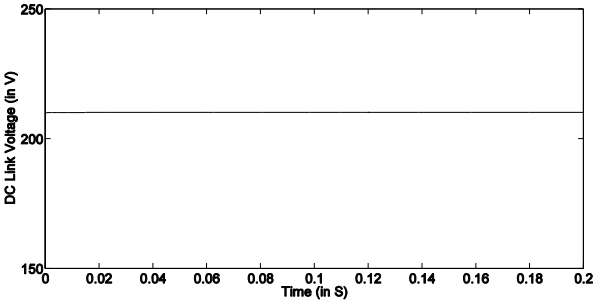
A reduction in load voltage due to the voltage sag is observed in fig 4.6(a). In the presence of IDVR the voltage sag is eliminated which is observed in fig 4.6(b). The load voltage of feeder 2 to which PST are connected is represented in fig 4.6(d). It is observed that while restoring the DC link energy, the feeder 2 load voltage is also maintained constant by the PI controller of the control system in second DVR.

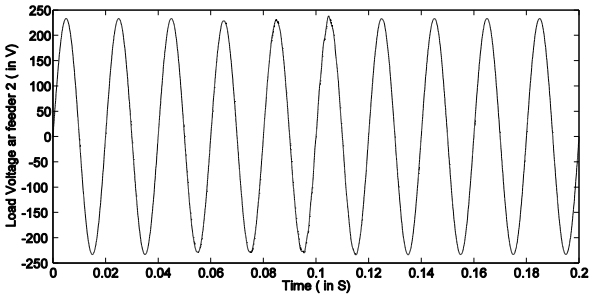


(a)



(b)





(c)

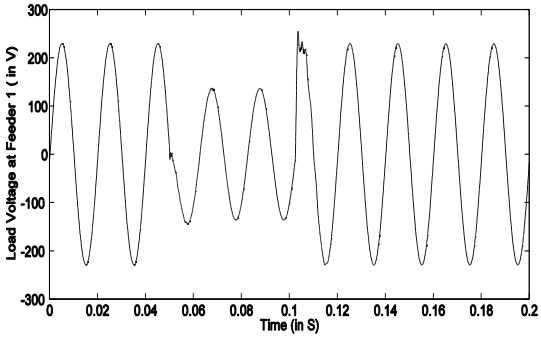
(d)

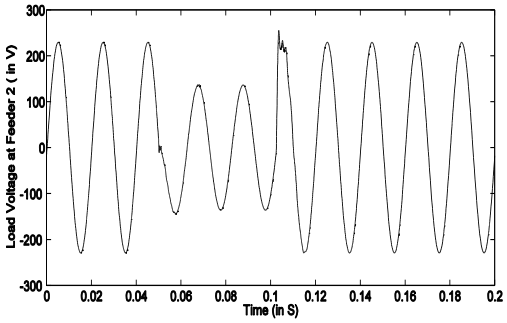
Fig. 4.6 (a) Load voltage at feeder 1 (in Volts) without IDVR (b) Load voltage in feeder 1 (in Volts) (c) DC link voltage (in volts) with IDVR and Phase Shifting Transformer (d) Load voltage at feeder 2 (in Volts)

In the literature [5], [90] , PST is uncontrolled which means that the phase shift produced by PST is default one value (depends on the turns ratio of the magnetizing and boosting transformers) irrespective of the power that should be compensated. To improve this a control action is developed which calculates the required power needed for the compensation. From that phase shift is calculated using the equations shown in modelling of PST [86]. When the angle is known according, the turns ratio of boosting transformer is adjusted there by the output of PST will give calculated phase shift. The drawback of using PST for replenishing the DC link energy is; the maximum phase angle shift between source and load voltage can be 90^0. At this instant power is maximum and beyond which the power cannot be increased. Hence PST is limited to certain limits of the compensation.

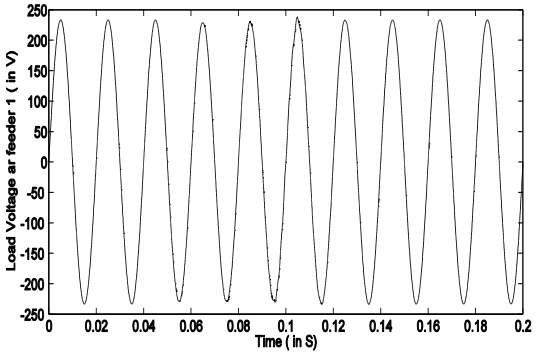
4.6.3 Voltage sag Applied in two feeders in the absence of PV and PST for restoration

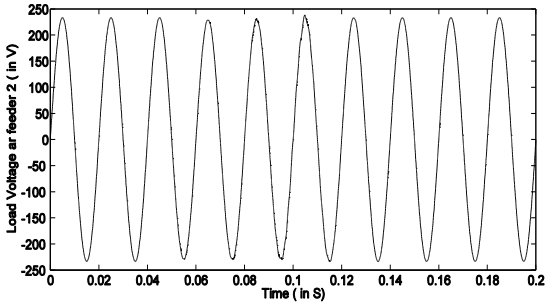
If both feeders are simultaneously effected with voltage sag, then the possible way to restore the DC link energy is with PV source. The restoration of DC link energy with PST can only be possible if there is a healthy feeder. Hence PST cannot be utlised for restoring the DC link energy in this case. If PV source is also not avaible then the energy stored in DC link capacitance will be utilized for the providng the energy to the IDVR for voltage compensation.


Load Voltage at Feeder 1 (in V)
Time (in S)

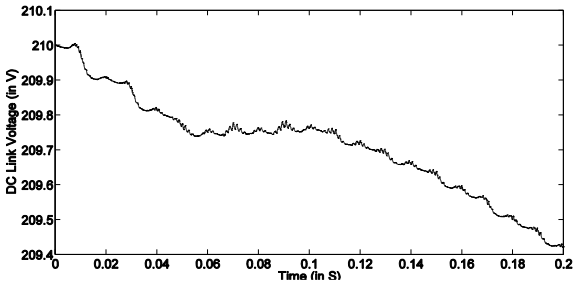

Load Voltage at Feeder 2 (in V)
Time (in S)

(a)


Load Voltage ar feeder 1 (in V)
Time (in S)


Load Voltage ar feeder 2 (in V)
Time (in S)

(b)



(c)

Fig.4.7 (a) Load voltage in feeder 1 and in feeder 2(in Volts) without IDVR (b) Load voltage in feeder 1 and feeder 2(in Volts) with IDVR (c) DC link voltage (in volts) without PV system and PST

4.7 Conclusion

A novel way of replenishing the DC link energy of IDVR is proposed. PST or PV systems is utilized for the DC link restoration. A Phase shifting Transformer (PST) controls the active power flow in a network by inserting the voltage with a controlled phase angle. The phase shift is created by connecting the two transformers (magnetizing and boosting transformers) of PST together, there by controlling real power flow in the line. The secondary side of magnetizing transformer consists of a tap changer. By regulating the tap changer the real power is regulated. A PV source is aided along with PST to restore the DC Link of IDVR. A DC Link controller is designed to select the suitable source among PST and PV for the DC link restoration. Different cases are presented showing how the PV and PST are used to restore the energy at DC link when the IDVR is compensating the voltage sag. The next chapter discuss about replacement of voltage source inverters with current source inverters as the building blocks of IDVR.

Chapter 5

CSI Based IDVR

5.1 Introduction

The voltage source sag mitigation by the DFACTS device IDVR was investigated while maintaining the DC link voltage. The DC link was replenished by either PST or PV source. However the major component of IDVR which is the inverter was based on voltage source inverter. This chapter focuses on replacement of voltage source inverters with current source inverters. A comparative analysis of the two inverters as the building blocks of IDVR is examined on a test power system. The next section explains about the current source inverters.

5.2 Current Source Inverters

The Current Source Inverters (CSI) are the type of inverters fed with a current source with high impedance. The source at the AC side of the inverter may be a current source or inductor in series with a DC source. As the input voltage is constant in VSI, in CSI the input current is constant but adjustable. The amplitude of the output current is independent of load. The waveform and magnitude of the output voltage depends on nature of load. fig 5.1 represents the three phase CSI. In fig 5.1 S1 to S6 represents the switches (MOSFET or IGBT) and D1 to D6 are the diodes connected in series to the switches to block the reversal of current. [78], [79], [91]–[96]

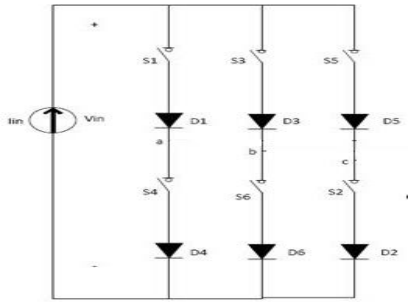


Fig. 5.1 Schematic diagram of CSI

The following gives the comparative study between VSI and CSI [10]

VSI	CSI
VSI is fed from a DC voltage source having small or negligible impedance.	CSI is fed with adjustable current from a DC voltage source of high impedance.
Input voltage is maintained constant	The input current is constant but adjustable.
Output voltage does not dependent on the load	The amplitude of output current is independent of the load.
The waveform of the load current as well as its magnitude depends upon the nature of load impedance.	The magnitude of output voltage and its waveform depends upon the nature of the load impedance.
VSI requires feedback diodes	The CSI does not require any feedback diodes.
The commutation circuit is complicated	Commutation circuit is simple as it contains only capacitors.
Power BJT, Power MOSFET, IGBT, GTO with self commutation can be used in the circuit.	They cannot be used as these devices have to withstand reverse voltage.

There is lack of research on current source inverters with IDVR. Though current source inverters are more economical than voltage source inverters, they have certain advantages like current control capability because the DC current in current source inverters is unidirectional unlike voltage source inverters, high reliability, common dc link is ripple free. The current source inverter has inductor in DC link, A SMES coil could instead be incorporated onto the DC bus. Interfacing the coil to the ac system through a current source inverter results in a device that injects a controlled current with the

ability to regulate ac voltage or power flow under normal conditions and supply when the power supply is off-line. The SMES coil should be large enough if the sags are occurring simultaneously in both the feeders at the same time and also when the depth of voltage sag is more. In addition to this, the economic cost will be more by the usage of the large SMES coil. An alternative solution to this proposed in this chapter, is using the PV source with small size charged SMES coil. Whenever IDVR mitigates the voltage sag/swell in the system, the energy to mitigate the voltage sag/swell is taken from the PV source. Hence the SMES coil which is connected to the PV source has it energy maintained at the constant level even at the time of mitigation of voltage sag/swell. In any voltage sag conditions the PV source is not able to give its maximum energy then the deficient energy which PV is unable to give can be utilized from the charged SMES coil.

In order to compare CSI and VSI as the building blocks of IDVR, an IEEE 8 bus power system is taken for study. The IEEE 8 bus system is divided into three stages; generation, transmission and distribution. Loads are connected to buses at the transmission and distribution side. Loads connected at the distribution side are assumed to be sensitive loads. IDVR will be connected at the distribution side and the power quality problems are simulated in different conditions. The effect of IDVR in mitigating the voltage sag and harmonics separately with VSI and CSI as its building blocks is examined and compared. The total system simulation is carried in MATLAB SIMULINK software. In addition to this, the IDVR-CSI is simulated with a test power system with a superconducting magnetic storage system (SMES) as the DC link to provide the required energy when the IDVR is mitigating the voltage sag or swell [10]. The next section explains about SMES

5.3 Super Conducting Magnetic Energy Storage System (SMES)

Superconducting Magnetic Energy Storage (SMES) is a method of energy storage based on the fact that a current will continue to flow in a superconductor even after the voltage across it has been removed. When the superconductor coil is cooled below its superconducting critical temperature it has negligible resistance, hence current will continue to flow (even after a voltage source is

disconnected). The energy is stored in the form of a magnetic field generated by the current in the superconducting coil. It can be released by discharging the coil. As SMES stores electrical current the only conversion involved with the process is the conversion from AC to DC. Hence the efficiencies of SMES systems are very high. SMES can switch from full discharge to full charge very quickly and vice- versa. It has negligible deterioration due to cycling. However, SMES has a high self-discharge rate due to the energy expenditure of cooling via cryogenic liquid and mechanical stability problems. The magnetic energy stored in a conducting coil is given by:

$$E = \frac{1}{2} LI^2 \tag{5.1}$$

Where I is the current in amperes and L is the inductance in Henries.

Due to its very high cycling capacity and high efficiency over short time periods SMES is very well suited to high power short duration applications. They are used in many voltage stability and power quality applications, for example to provide very clean power in microchip manufacture. On-site SMES is suitable to mitigate the negative impacts of renewable energy in power quality related issues, especially with power converters – needed for solar photovoltaic and some wind farms – and wind power oscillations and flicker. The SMES coil is used as the DC link of IDVR. The SMES coil provides the necessary energy to the IDVR for mitigating voltage sag/swell. As mentioned above in order to reduce the size the SMES coil for longer duration voltage sag/swell, a PV source is used in addition to the coil. The description of PV source is given chapter 4. The comparative study of CSI and VSI as building blocks of IDVR is given in the next section. The simulations are executed in MATLAB Simulink software tool.

5.4 Results

5.4.1 Comparison of VSI and CSI on an IEEE 8 Bus System

The schematic diagram of the power system is simulated in MATLAB Simulink is shown in fig 5.2. The total system consists of 8 buses with two power sources. The voltages from power sources are

33KV which is step down to 11KV using transformer T1 and T4 transformers. T1 and T4 are connected to bus 1 and bus 2. The details of the resistance and reactances of the network lines are given in Table 1 [97]. Bus 1 to bus 6 represent the transmission network at 11KV voltage which is step down to 415V with transformers T2 and T3. The total system contains 4 loads; load 1 and load 2 are connected to bus 7 and bus 8 respectively at the distribution end. Load 3 and load 4 are connected at the transmission side bus 3 and bus 4 respectively. Loads 1 and 2 are three phase sensitive loads which require protection from the power quality problems like voltage sag and harmonics.

Table 5.1: Line data of the system

Line no	**Between buses**	**R in P.u.**	**X in P.u.**	**Susceptance**
1	1-6	0.123	0.518	0.03
2	1-4	0.080	0.370	0.010
3	2-3	0.0723	1.05	0.022
4	2-5	0.282	0.064	0.12
5	3-4	0	0.133	0.33
6	4-6	0.097	0.407	0.01
7	6-5	0	0.3	0.025

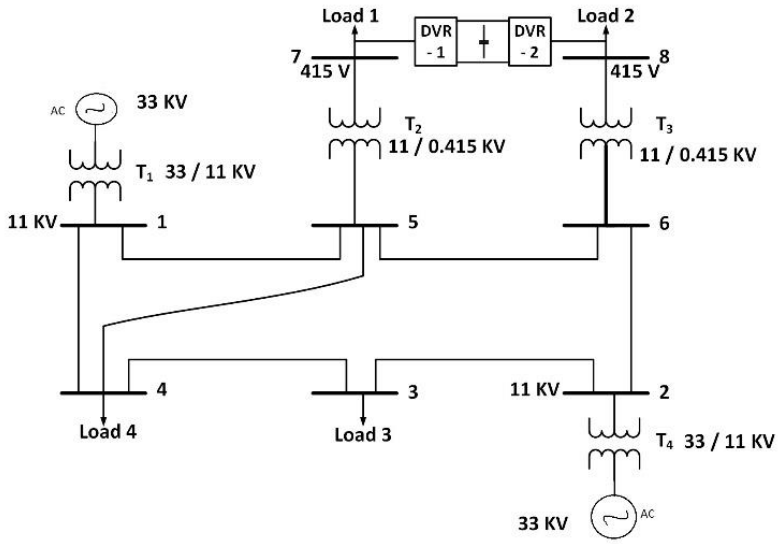


Fig. 5.2 Schematic diagram of the total system

To protect these loads from power quality issues IDVR is connected at the end of bus 7 and bus 8 as shown in fig 5.2. The IDVR is connected near the loads. The IDVR consists of either VSI or CSI as building block, a PI controller which controls the error between reference and actual voltage and PWM generator to generate pulses. If the building block of IDVR is VSI then capacitor is connected at the DC link. If the building block of IDVR is CSI then an inductor or Super Conducting Magnetic Storage System (SMES) is connected at the DC link. A voltage sag condition is created near load 1 with different cases and load 2 is assumed to be healthy. The three different scenarios are considered where voltage sag is observed.

1. Sudden ON and OFF of load 1.
2. Single line to ground fault at load 1 for a duration of 1 cycle.
3. Double line to ground fault at load 1 for a duration of 1 cycle.

Due to nonlinear nature of load connected at the distribution side, harmonics also occur in addition to the voltage sag. IDVR is used to eliminate the voltage sag and harmonics. IDVR is connected with VSI or CSI as its building blocks separately and the performance of each VSI and CSI based IDVR in eliminating voltage sag and harmonics in the various cases are observed.

Case 1: Voltage sag and harmonics created by sudden ON and OFF of load 1

The total simulation of the system is run for 0.16 seconds. In this case the voltage sag and harmonics are created by sudden ON and OFF of load 1 between 0.04 and 0.08 seconds.

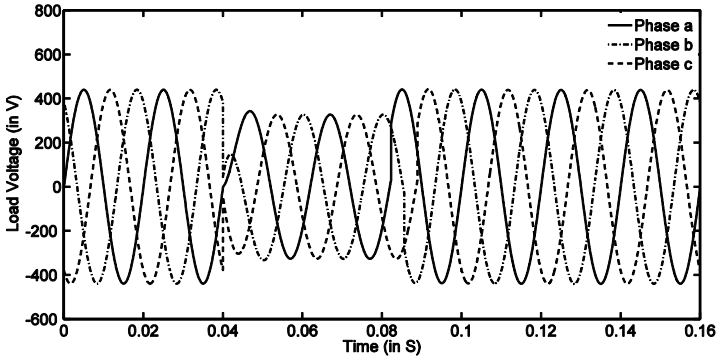


Fig. 5.3 Load Voltage without IDVR

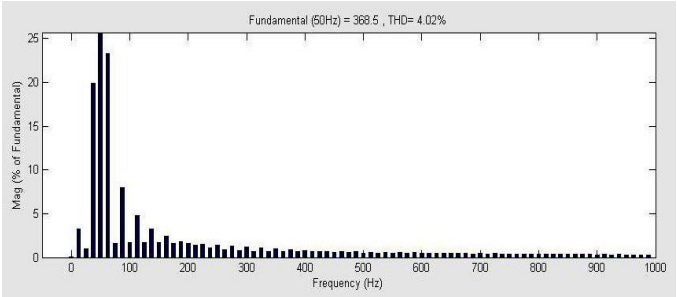


Fig. 5.4 THD without IDVR

In the absence of the IDVR the voltage sag is observed as shown in fig 5.3 which gives the voltage profile. The voltage reduces to 300V from 415V in that particular interval of 0.04 to 0.08s. Along with voltage sag, harmonics can also be observed as indicated in fig 5.2 where voltage fluctuates at the edge of the intervals. Thus the total harmonic distortion (THD) without IDVR is computed and shown in fig 5.4. THD is defined as square root of sum of squares of all harmonics presented in the voltage The THD without IDVR is 4.02%.

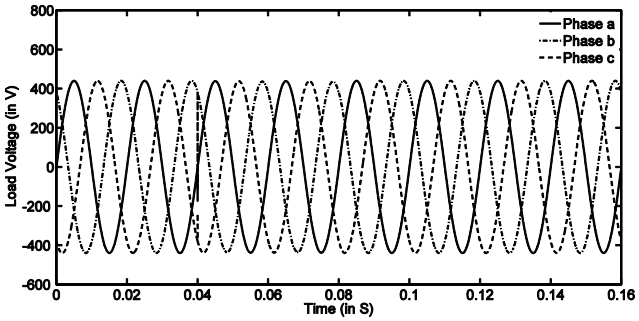


Fig. 5.5 Load voltage with VSI based IDVR

Fig 5.5 and fig 5.6 represent the load voltage in the presence of IDVR with VSI and CSI as its building blocks respectively. For both VSI and CSI as its building blocks, IDVR is mitigating the voltage sag in same proportions. While fig 5.7(a) and (b) represent THD with VSI and CSI based IDVR respectively. THD with VSI is 0.06% (shown in fig 5.7(a)) and with CSI with 0.05% (shown in fig 5.7(b)). The individual magnitudes of harmonics are decreased with CSI when compared to VSI.

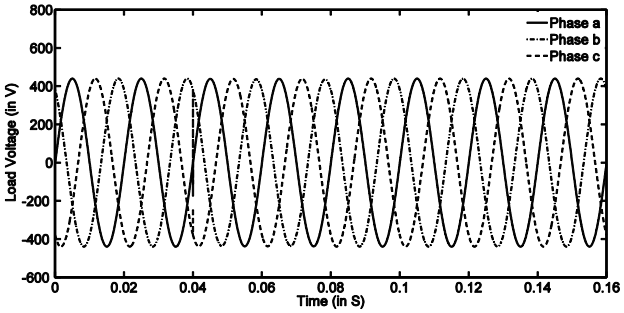
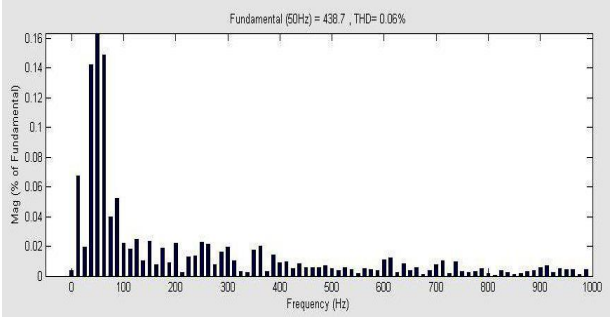
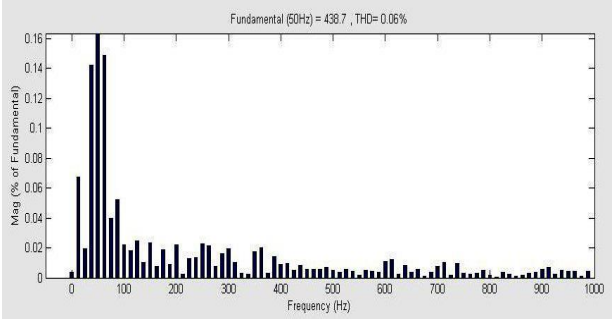


Fig. 5.6 Load voltage with CSI based IDVR



(a)



(b)

Fig. 5.7 THD (a) with VSI (b) with CSI as building blocks of IDVR

Hence, CSI based IDVR is performing better than VSI based IDVR as the THD is slightly reduced.

Case 2: Voltage sag and harmonics created by single phase to ground fault at load.

To simulate this condition, a single phase to ground fault is applied to R phase. Fig 5.8 represents load voltage during the fault condition. As single phase to ground fault is occurred in R phase, the voltage is zero in R phase in the interval of 0.04 to 0.06 s.

The impact of fault creates a voltage sag in other two phases. Hence, the magnitude of voltages in B and Y phase are decreased from 415V to 300V as shown in fig 5.9. The THD is 14.27% (as shown in Fig 5.9) in this condition. Similar to above case voltage sag is mitigated with IDVR. As observed in fig 5.5 and fig 5.6, similarly the voltage sag is eliminated by either IDVR based with VSI or CSI.

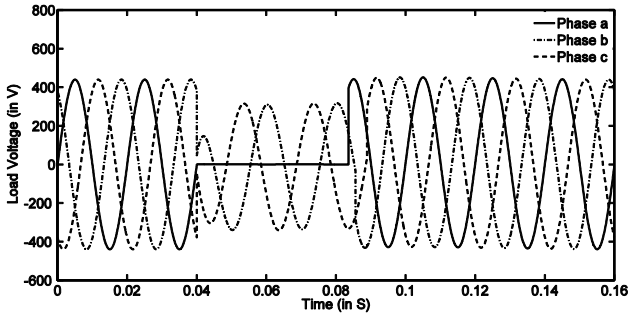


Fig. 5.8 Load voltage for single phase to ground fault without IDVR

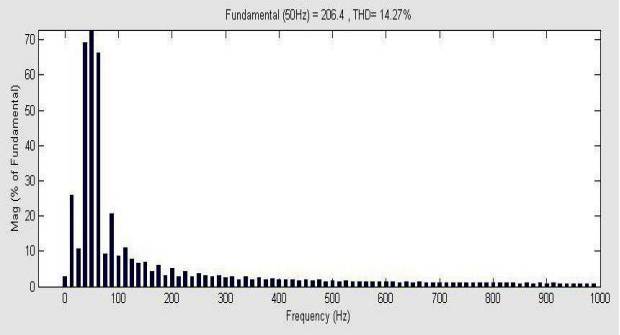
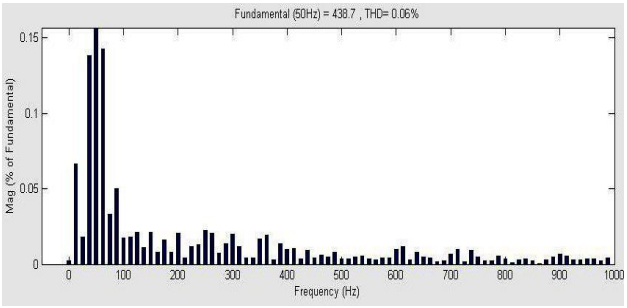
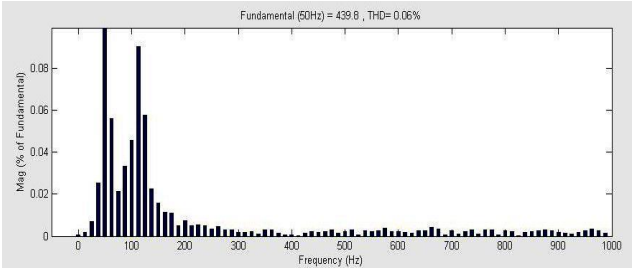


Fig. 5.9 THD for single phase to ground fault

The THD is also decreased with IDVR. Fig 5.10(a) and (b) represents the THD value with VSI and CSI as building blocks of IDVR respectively. In this case THD is same for CSI and VSI which is 0.06%.



(a)



(b)

Fig. 5.10 THD (a) with VSI (b) with CSI as building blocks of IDVR

Case 3: Voltage sag and harmonics created by double phase to ground fault at load.

Here voltage sag is caused with double phase to ground fault. The two phases (R and Y in this case) are affected with fault and due to this fault the third phase (B phase) experiences a voltage sag as

shown in fig 5.11. The voltage in R and Y phases is zero and voltage in B phase is decreased from 415V to 300V. The THD during the fault condition is 11.74% shown in fig 5.12.

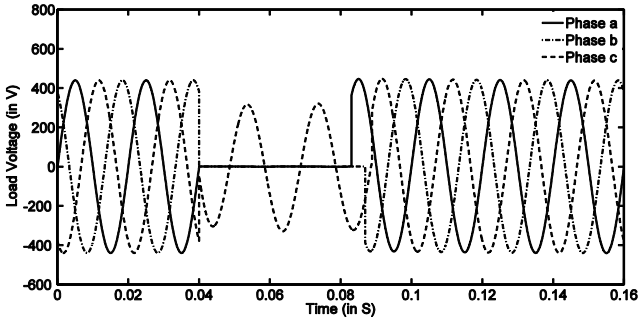


Fig. 5.11 Load voltage during double phase to ground without IDVR

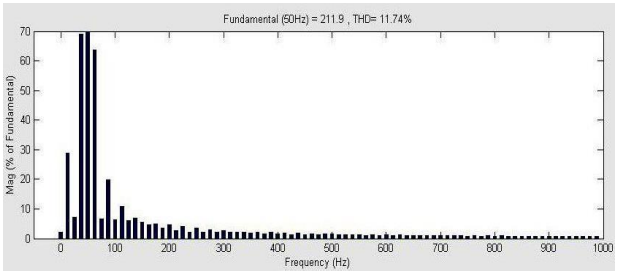
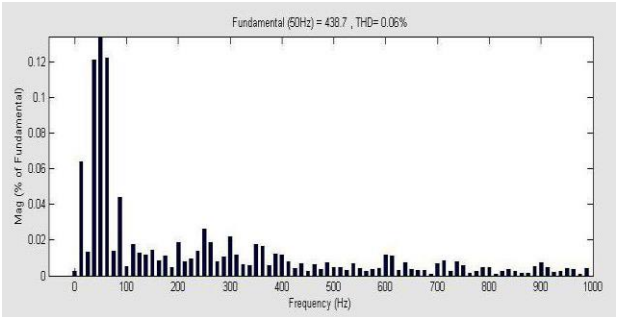
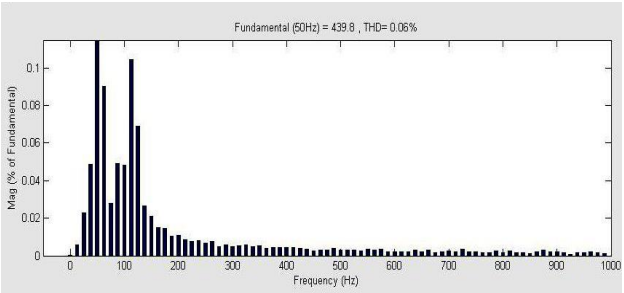


Fig. 5.12 THD during double phase to ground fault.



(a)



(b)

Fig. 5.13 THD (a) with VSI (b) with CSI as building blocks of IDVR

Similar to the previous cases the voltage sag is mitigated by IDVR with VSI and CSI as its building blocks in equal proportions which can be seen in fig 5.5 and fig 5.6. Fig 5.13(a) and (b) represents the THD with VSI and CSI. According to Fig 5.13(a) the THD is 0.05% for CSI based IDVR and according to fig 5.13(b), the THD is 0.06% for VSI based IDVR. From the observations the THD is slight decreased when using CSI as the building blocks of IDVR.

5.4.2 Summary of the Cases

In all the cases it is found that the voltage across the phases (where there is no impact of the fault) has dropped from 415V to 300V irrespective of the faults applied on the load. The reason for this is, the rating of the load considered for the these cases is unchanged and only the type of the fault on the load is changing in all the three cases and due to this the drop of the voltage is constant in the three cases. In addition, the phase which is effected with the fault is completely short and there by the voltage across those phase is observed to be zero.

It is also observed that the voltage sag is mitigated in similar manner using VSI and CSI as the building blocks of IDVR in all the considered cases. However, for THD, except the second case in other two cases THD is slightly decreased with CSI compared with VSI. Also, the magnitudes of the harmonic order from 0 to 100 Hz is decreased quite a lot with CSI as the building block of IDVR compared to VSI in all the three cases which can be observed in fig 5.7, fig 5.10 and fig 5.13. Table 5.2 gives the summary of all the three cases.

Table 5.2 Summary of the three cases

Fault Type	**Performance of IDVR-VSI in mitigating voltage sag**	**Performance of IDVR-VSI in mitigating voltage sag**	**THD without IDVR**	**THD with CSI based IDVR**	**THD with VSI based IDVR**	**Mitigation of Individual harmonics by VSI and CSI**
Sudden ON & OFF of Load	Effective	Effective	4.02%	0.05%	0.06%	The magnitudes 0 to 100 Hz is decreased with CSI than VSI
Single Line to Ground Fault	Effective	Effective	14.27%	0.06%	0.06%	Mitigation of harmonics is same with VSI and CSI
Double Line to Ground Fault	Effective	Effective	11.74%	0.05%	0.06%	The magnitudes 0 to 100 Hz is decreased with CSI than VSI

The next section explains simulation of IDVR with CSI as building blocks with a test power system. The SMES coil is used as the DC link along with PV source.

5.5 Simulation Results of IDVR with CSI as Building Block

The total system of IDVR with SMES and PV source connected to two feeders simulated in MATLAB is shown below in fig 5.14.

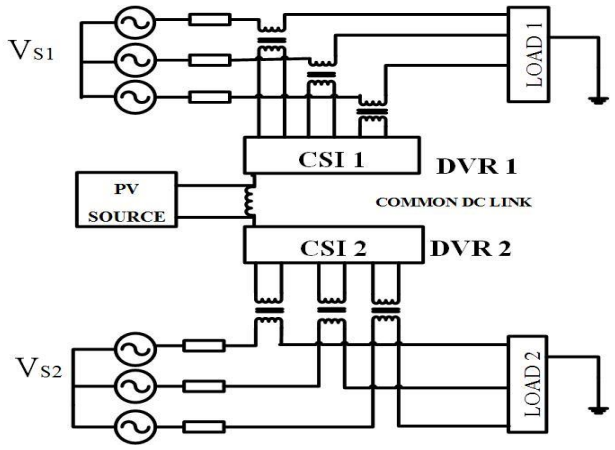


Fig. 5.14 Schematic diagram of total system simulated in MATLAB

In fig 5.14, feeder 1 and feeder 2 are at different voltage levels. The PV source is connected to SMES and the total set up gives the required energy at the DC link energy. Whenever IDVR mitigates the voltage sag/swell in the system, the energy to mitigate the voltage sag/swell is supplied from the PV source. If any case, the PV source is not able to provide the necessary energy to IDVR, then the required energy should be supplied by the SMES coil connected at the DC link of IDVR. For this, SMES coil has to initially charge before it is connected to the DC link.

The parameters of the system shown in fig 5.14 is given in the below Table 5.3. In general there are several conditions where voltage sag is produced. However, in this chapter voltage sag/swell is considered in four different conditions which is listed below

A. Using sudden start of induction motor at feeder 1.

B. With a LG fault at feeder 1.

C. A multiple sag and swell at feeder 1.

D. A simultaneous voltage sags in both feeders.

TABLE 5.3 PARAMETERS OF THE TWO LINE IDVR SYSTEM

Parameter	**Feeder 1**	**Feeder 2**
Supply voltage (V_s)	415V	230V
Load Voltage (V_l)	415V	230V
Load Resistance (R_l)	40Ω	40Ω
Load inductance (L_l)	95.5mH	95.5mH
Transformer resistance (R_t)	3 Ω	1 Ω
Transformer inductance (L_t)	10mH	6mH
Inductance at the DC link	1H	
PV source at the DC link	1.8KW	

In all proposed cases, the performance of IDVR in mitigating voltage sag is observed. The simulation results are presented in each case

5.5.1 Using sudden start of induction motor at feeder 1

A 5hp, 415V, 1500 RPM induction motor is connected at the position of load 1 shown in fig 5.14 to the feeder 1. The total simulation is for 0.4 seconds. In this interval the induction motor is switched ON at 0.3 seconds. The load voltage at feeder 1 when the induction motor is ON is shown below.

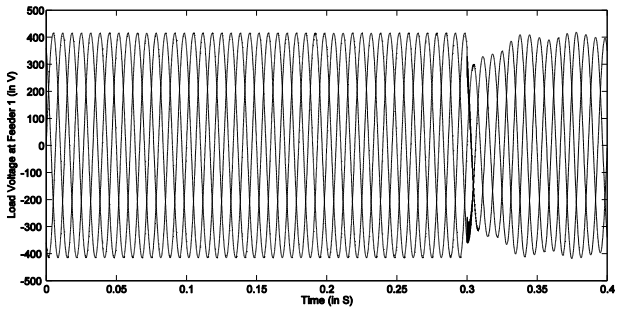


Fig. 5.15 Load voltage with induction motor as load without IDVR

Fig 5.15 is the load voltage at feeder 1 without IDVR. When induction motor is ON at 0.3S, it

consumes large reactive power at initial startup which leads to voltage sag for a few cycles which can be observed in fig 5.15. After few cycles of voltage sag, the voltage is being regained to the normal value. If in case any sensitive load is connected to feeder 1 in this condition, this load will get effected by the voltage sag. To mitigate this sag and protect the sensitive loads connected to the feeder 1, an IDVR is placed at the feeder 1 shown in fig 5.14.

Fig 5.16 represents the load voltage profile of feeder 1 with IDVR when the induction motor is ON. When the induction motor is ON at 0.3S, the PI controller in IDVR building block compares dropped voltage with reference voltage and allows PWM generator to generate the pulses to the CSI to inject the required voltage.

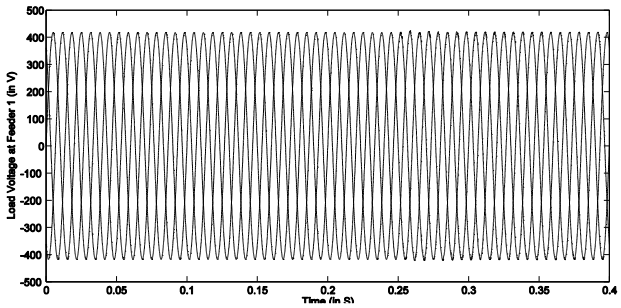


Fig. 5.16 Load voltage with induction motor as load with IDVR

Hence the load voltage is maintained at the rated value even when the induction motor is consuming reactive power. The required energy to mitigate the sag is given by PV source connected at the DC link.

Hence, it is proved that the IDVR clearly mitigates the voltage sag even at the sudden start of induction motor. The next case explains about the occurrence of voltage sag with LG fault.

5.5.2 Voltage sag/swell with A LG fault at feeder 1

There are faults like LG (line to ground), LLG (double line to ground) and LLL (triple line) which occur at the distribution end. Among these faults the frequently occurring fault is LG fault. The presence of LG fault makes the voltage zero in the particular phase where the fault is created, but

this fault also creates voltage sag or voltage swell in other two phases. If a LG fault is assumed to be applied near the load on R phase in fig 5.14, the load voltage in this condition is shown fig 5.17. Fig 5.17 is load voltage without IDVR. As shown in fig 5.17, due to the LG fault in the R phase, the voltage in that phase completely collapses and a voltage swell is observed in the Y and B phases respectively. This sudden increase in the voltage may cause tripping of the circuit breakers in Y and B phases and if circuit breakers are not responding, then this may lead to the damage of load. The load voltage in the above condition in the presence of IDVR is shown in fig 5.18.

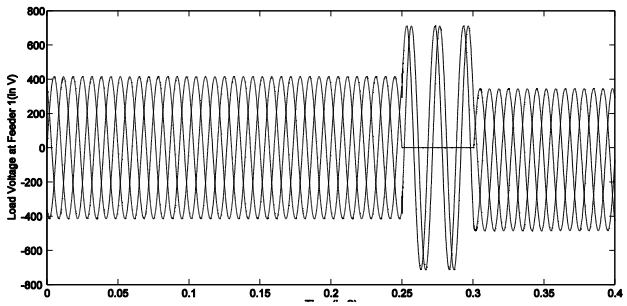


Fig. 5.17 Load voltage at feeder 1 with LG fault without IDVR

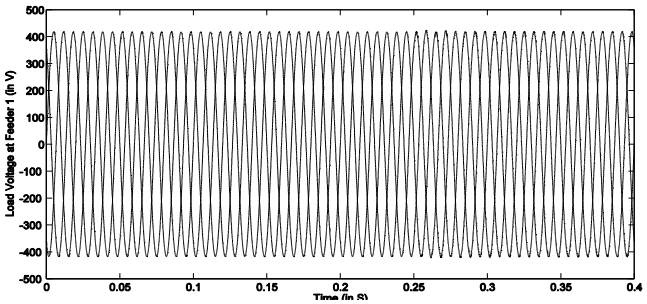


Fig. 5.18 Load Voltage at feeder 1 with LG fault with IDVR

In fig 5.18 it is shown that the load voltage is maintained in the rated value even during the fault condition with the presence of IDVR. The voltage is totally compensated in R phase with IDVR at which the LG fault has occurred. In addition the voltage swells in Y and B phases are eliminated with presence of IDVR. Hence this case also proves that the IDVR eliminates voltage swell in the

distribution side. The previous two cases have proven the performance of IDVR in a single sag condition while the next case represents the performance of IDVR with multiple sags.

5.5.3 Multiple sags at feeder 1

The load voltage with multiple sags in the absence of IDVR is shown in fig 5.19

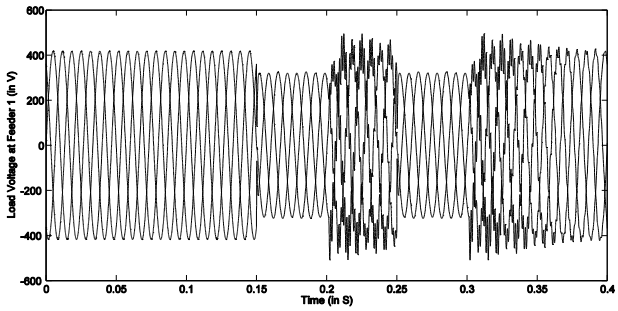


Fig. 5.19 Load voltage with multiple sags without IDVR

As shown in fig 5.19, a multiple voltage sags are created between the intervals 0.15S to 0.2S and 0.25 to 0.3S respectively. The load voltage is distorted between the intervals of 0.2S to 0.25S and 0.3S to 0.35S are post sag conditions. The reason for the distortion is due to harmonics present at the load side. This will be a major problem mainly to the sensitive loads connected on the same feeder. Due to the harmonics, there may be loss of data and cause sensitive load to get damaged. To eliminate this problems the IDVR is connected to feeder and the performance of IDVR with these multiple sags is observed in fig 5.20.

In fig 5.20 the voltage sags are completely mitigated by the IDVR connected to the feeder 1. The IDVR senses the decrease in voltage and injects the required voltage and maintains the required voltage. The PV source supplies the required energy to mitigate the sags.

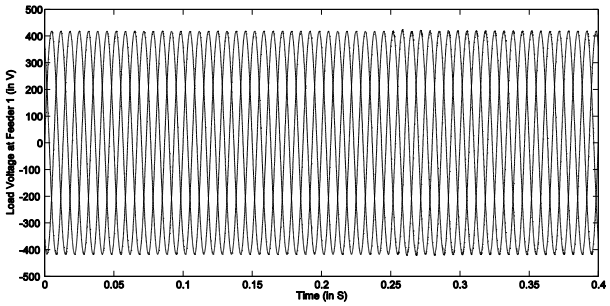


Fig. 5.20 Load voltage with multiple sags with IDVR

Hence, the IDVR is performing well in the multiple voltage sag conditions. In all the three considered cases, the sag conditions are applied to one feeder considering the second feeder to be healthy and the sag/swell mitigation process is observed in that particular feeder. In the next case the performance of IDVR is studied when both feeders get effected by voltage sag at same time.

5.5.4 Simultaneous Voltage Sag in Both Feeders

The two feeders of the system shown in Fig 5.15 are being affected with voltage sag at the same time.

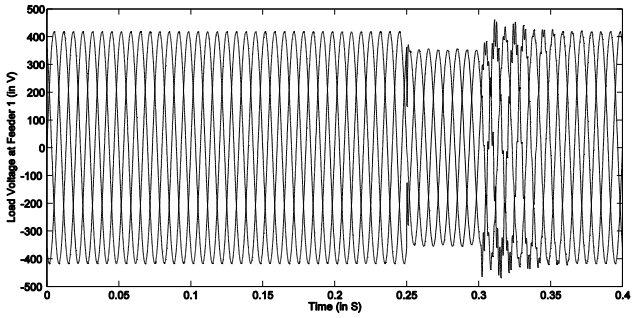


Fig. 5.21 Load Voltage at feeder 1 without IDVR

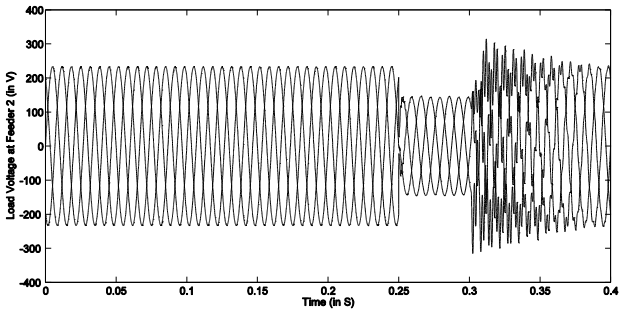


Fig. 5.22 Load Voltage at feeder 2 without IDVR

fig 5.21 and fig 5.22 represent the load voltages of feeder 1 and feeder 2 in the sag condition. The voltage is decreased from 415V to 380V in the first feeder and from 230V to 180V in second feeder respectively during the voltage sag. Due to the presence of harmonics the voltage is observed to be distorted in second feeder after the voltage sag.

With the presence of IDVR connected to both the feeders, the voltage sag in both feeders is eliminated and the voltage is maintained at the normal value which can be observed in fig 5.23 and fig 5.24.

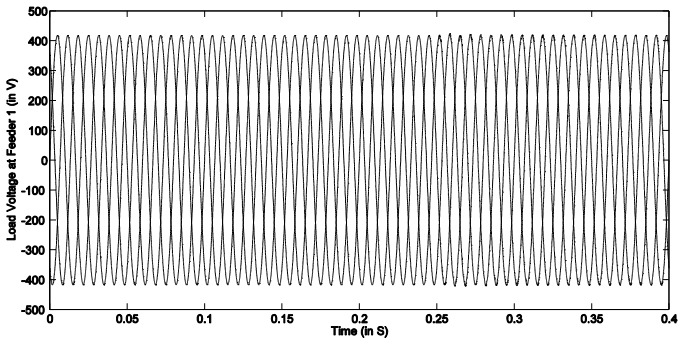


Fig 5.23 Load voltage at feeder 1 with IDVR

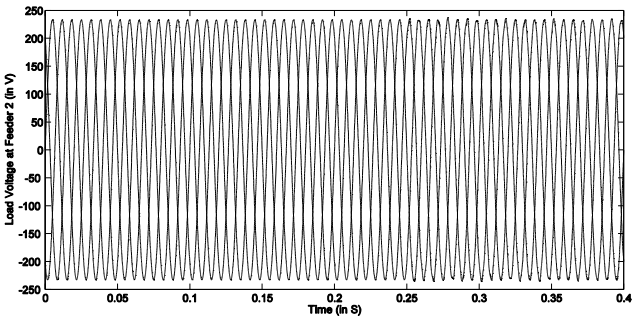


Fig 5.24 Load voltage at feeder 2 with IDVR

The PV source is able to give the required energy for IDVR to mitigate both sags simultaneously at the two feeders. The limitation to this case is the availability of PV source and charge in SMES coil. If the PV source and charged SMES coil are unable to give the required energy during the mitigation of voltage sag in both feeders, then the compensation process is not possible.

Therefore it is observed, IDVR with PV source at its DC link has mitigated the voltage sag/swell in different scenarios. This IDVR topology also solves the problem of simultaneous sag because of the PV source presented at the DC link. Due to the presence of CSI as the building blocks of IDVR and additionally with the presence of filter, the harmonics which are observed in some cases along with voltage sag are also eliminated. The PV source is able to give the required energy to IDVR for mitigating the sags. Hence, the sensitive loads at the distribution end can be protected with IDVR irrespective of severity of the voltage sag/swell.

5.6 Conclusion

In this chapter the performance of IDVR with CSI and VSI as its building blocks for mitigating voltage sag and harmonics is compared. Voltage sag and harmonicas are created in three different ways and in all the three cases the efficiency of IDVR in mitigate voltage sag and harmonics with either CSI or VSI as its building blocks is compared. Based on the results obtained in all the three cases, the performance of IDVR in mitigating voltage sag with VSI or CSI is observed to be same. But, for THD the performance of IDVR with CSI as building block is better than IDVR with VSI as

its building block. The individual magnitudes of harmonics are decreased with CSI than VSI. Hence this comparison has proven that the ability of IDVR in compensating voltage sag/swell is unchanged by the use of CSI as its building block. In practical scenario the SMES coil connected to the DC link of IDVR is little complex to handle. Due to this the CSI is more expensive than VSI. Considering these constraints for CSI, the further research in this thesis is carried out with VSI as the building block of IDVR.

All the simulations conducted on IDVR until this chapter is with a test power system. But in order to understand the efficiency of IDVR in mitigating voltage sag, a real time test has to be performed. This part is covered in the next chapter where the IDVR is simulated with a real time load. The performance of IDVR is tested in the real time scenario.

Chapter 6

Real Time Simulation of IDVR

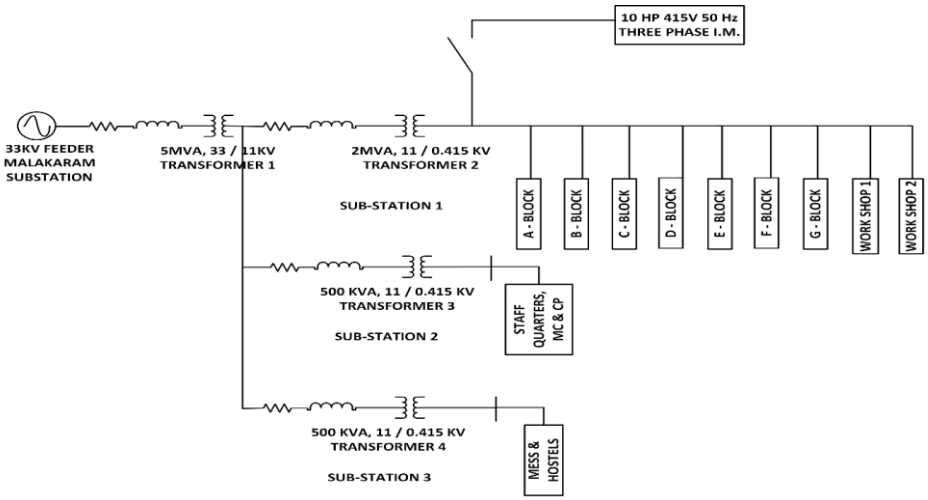
6.1 Introduction

The efficiency of IDVR in mitigating voltage sag/swell in various sagged conditions is proven so far. The simulations of IDVR discussed in chapter 4 and chapter 5, are performed on a test power system. The IDVR is connected to the test power system and its efficiency for mitigating the voltage is tested. The parameter values considered in a test power system does not signify any existing real time load. Thereby the results obtained by testing the IDVR with a test power system does not exhibit the accuracy of IDVR. Hence in order to prove the reliability of IDVR, a real time electrical network load is to be considered. In this chapter, the IDVR is designed to mitigate power quality problems in an existing real time load. The load network data of BITS Pilani Hyderabad Campus in Telangana, India which is spread over 200 acres is considered as the real time load. Various multiple voltage sag/swell scenarios are analyzed in the real time load

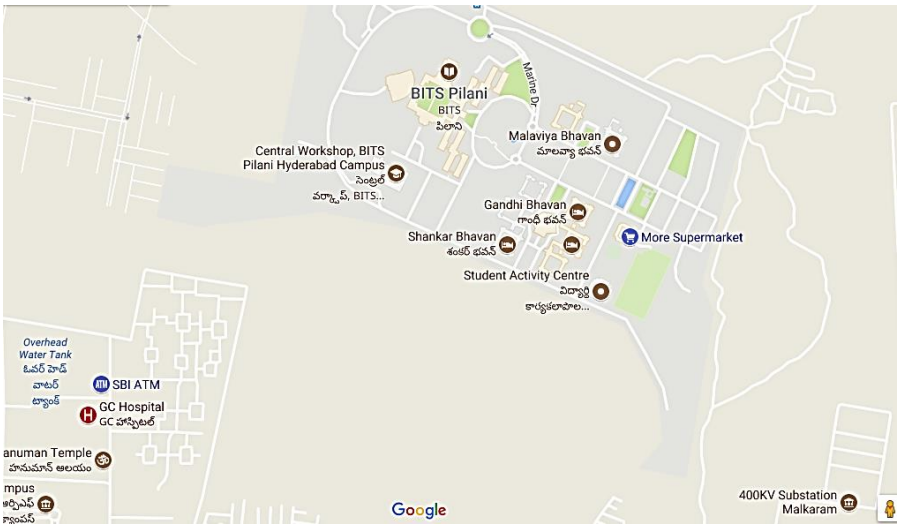
6.2 Description of the Real Time Load

The electrical load network of BITS Pilani Hyderabad Campus, located in Hyderabad, Ranga reddy district spread over 200 acres, is considered as real time load. Fig 6.1 (a) represents the schematic layout of the real time load. The google map picture of the load is shown in fig 6.1(b).

Fig 6.1 (a) gives a schematic layout of BITS Pilani Hyderabad Campus containing various loads connected to three different internal substations. The power is drawn from a substation at Malkaram through 33KV feeder line. This is step down to 11KV at the main substation through a 5KVA, 33KV/11KV transformer. This voltage is further step down to domestic level of 415V by three distribution transformers located in mini substation at three different locations.



(a)



(b)

Fig. 6.1 (a) Schematic layout of the real time load. (b) Google Map of BITS Campus

Substation 1: The major load of the campus in on substation 1. The input voltage to substation 1 is 11KV which is stepped down to 415V by 2MVA, 11KV/415V three phase step down transformer within the substation. The load consists of totally 9 different blocks from ‘A’ block to ‘G’ block and two workshop units. These blocks consist of administration wing, class rooms and the various departments of the institute. All the loads ae inductive in nature. A 10hp induction motor is connected along with the blocks to substation 1. This induction motor is used to pump water to

various places of BITS campus. This induction is not a continuous load and is ON only when the pumping of water is required. The maximum demand on substation 1 is 1000KVA. The other loads of BITS campus are connected to substation 2 and substation 3.

Substation 2: The 11kV voltage is given as input to the substation 2 which steps down to 415V using a 500 kVA, 11kV/415V three phase step down transformer. Staff Quarters, Medical centre and CP, security office and remaining street lights are the various loads connected to substation 2. The maximum demand at substation 2 is 200KVA.

Substation 3: The 11KV voltage is given as input to the substation 3 which is stepped down to 415V by a 500KVA, 11KV/415V three phase step down transformer. The load at substation 3 consists of 6 boy's hostels, 2 girl's hostels and two dinning messes and some street lights. The load data substation 3 is given in table 6.1. The maximum demand at substation 3 is 300KVA.

The major challenges on a real time load are

1. *Examine the Voltage Sag/Swell Conditions*: The various possible cases of occurrence of voltage sag is to be investigated.

2. *Identification of sensitive load*: In order to connect the IDVR to the real time load, the loads which are more effected with voltage sag/swell need to be identified.

3. *Bidirectional Nature of IDVR to be tested*: In general, the IDVR contains more that two DVRs sharing a common DC link. Since several DVRs are connected to multiple feeders, the voltage compensation in multiple feeders can be performed with one device at one instance. This type of compensation is called as bidirectional compensation. Hence this bidirectional nature of IDVR is to be tested in the real time scenario.

Hence taking these challenges into the consideration, the functionality of IDVR is tested with real time load. The results of IDVR with the considered real time load is explained in the next section.

6.3 Results

The real time load of BITS Pilani Hyderabad Campus, is simulated using MATLAB Simulink software. The ratings of all the loads shown in fig 6.1(a) is given in table 6.1.

The various changes in the load at different timings during day and its effect on voltage change has been recorded. Thus the occurrence of voltage sag/swell on the various possible load conditions in the real time is studied. The sensitive loads of the BITS campus are present in B- block connected to substation 1 and in medical centres connected to substation 2. These are loads which should be protected from voltage sag/swell.

The B- block the contais computer servers which require continuous requirement of rated voltage, failing to which leads to the loss of data. Hence this load is considered as sensitive load because it has greater impact of voltage sag. The second sensitive load is the medical centre. The medical centre of BITS Pilani Hyderabad campus contains X ray type of equipment which require continuous supply of rated voltage. Therefore these sentive loads needs to be protected from voltage sag/swell.

The severity of voltage sag/swell occurs at Point of Common Coupling (PCC) of any substation is due to a fault occurring at one of its connected load. To observe a voltage sag/swell, a line to ground (LG) fault is simulated at one of the loads connected to substation 2.

Table 6.1 Load ratings of each block the BITS campus (all the blocks are three phase loads rated to 415V, 50Hz)

Block	Active Power rating in KW	Reactive Power rating in KVAR
Substation 1		
A block	170	127.5
B block	106	79.5
C block	38.159	28.619
D block	90.638	67.978
E block	92.224	69.168
F block	37.376	28.032
G block	17.944	13.458
Work Shop 1	189	141.75
Work shop 2	47	32.25
Substation 2		
Hostels and Messes	240	180
Substation 3		
Staff Quarters, Medical Center and CP	160	120

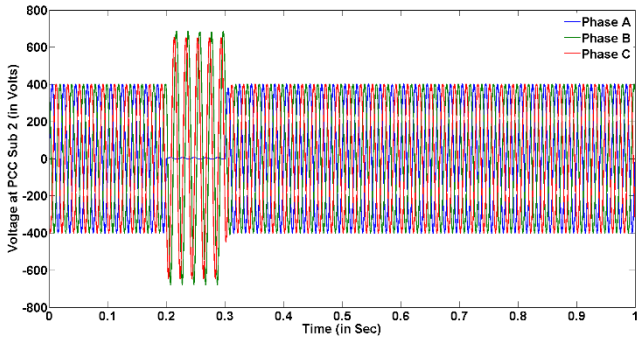


Fig. 6.2 Voltage at PCC of Substation 2 when A LG fault is applied.

Fig 6.2 indicates the voltage at PCC of substation 2 during the fault condition. A LG fault is created in R phase at 0.2sec on Canaught Place (CP) load connected to substation 2 and is cleared at 0.3sec. Due to the occurrence of LG fault, the CP load is suddenly disconnected from the substation 2 in

the interval 0.2sec to 0.3sec. For this reason a voltage swell is observed at PCC of substation 2 in Y and B phases and the R phase voltage is nearly zero because the LG fault occurred in R phase.

Apart from fault condition, the voltage at PCC of substation 2 is dropped down from 415V to 400V at the initial point of simulation itself which can be observed in fig 6.2. This is because all loads connected to substation 2 are inductive in nature. By observing fig 6.2, we can observe that the voltage is not maintained at 415V and additionally the voltage is distorted between 0.2Sec and 0.3Sec. This will affect the sensitive loads present in the medical centre load connected to substation 2. To protect these loads from the voltage sag/swell IDVR should be installed at the PCC of substation 2.

Second possible condition for voltage sag/swell occurrence in the real time load during on the induction motor connected to substation 1. In the schematic layout of the real time load shown in fig 6.1, an induction motor is connected to substation 1. If this induction motor is switched ON, a voltage sag will be created at PCC of substation 1. The voltage at PCC of substation 1 when the induction motor is switched ON is represented in fig 6.3.

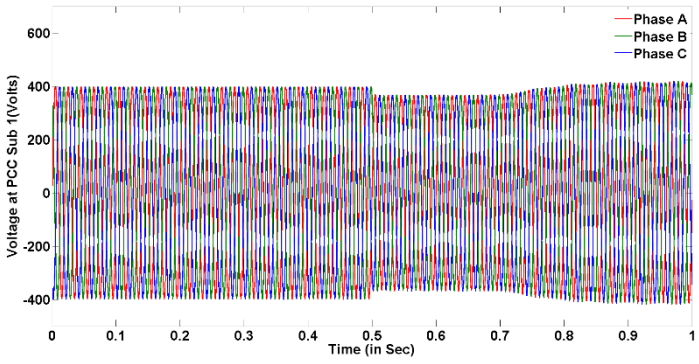


Fig. 6.3 Voltage at PCC of Substation 1

When the induction motor connected to substation 1 is switched ON at 0.5sec, voltage sag is created at PCC of substation 1 for few cycles which is shown in fig 6.3. Similar to the voltage of substation 2, the voltage at PCC of substation 1 is dropped down to 400V from the initial point of

simulation because of the 9 inductive loads connected to substation 1. When the motor is started, the voltage is further dropped to 365V at 0.5sec. The voltage sag will have a significant impact on the sensitive load i.e. the servers present in B block load connected to substation 1. The voltage sag/swell occurring in the two cases described above, should be mitigated to protect the sensitive loads present in substation 1 and substation 2. To mitigate the voltage sag/swell, IDVR is developed and placed at PCC of substations 1 and 2.

Fig 6.4 represents the schematic diagram of the real time load with the presence of IDVR. The IDVR in fig 6.4 consists of two DVRs, one DVR connected to PCC of substation 1 and the other DVR is connected to substation 2. The reason for connecting the IDVR to substation 1 and substation 2 is to protect the sensitive loads at both substations from voltage sag/swell. To mitigate these voltage sag/swell occurring in the two conditions, the DVR, injection transformer and the DC link are designed with respective ratings.

In both conditions the voltage at the PCC of substation 1 and substation 2 are dropped to 400V from 415V from the initial point of simulation because of the inductive loads connected to substations. As shown in fig 6.3, the voltage at PCC of substation 1 is further dropped to 365V when the induction motor is switched ON. Considering these values and substituting them in equations 3.3 to 3.15, the rating of DVR 1 is 75KVA and DVR 2 is 30KVA. Both the DVRs are use three phase VSI described in chapter 3, as the building blocks. The bidirectional compensation is not covered in previous literature of IDVR. Most of research covered voltage compensation on where IDVR is connected to two feeders, one feeder is always assumed as healthy and other feeder is assumed to be effected with the voltage sag [72], [73], [98]. Real time instances included sags in various lines so bidirectional compensation is necessary. To mitigate the voltage sag/swell simultaneously in both feeders, IDVR should require enough energy at the DC link. The design parameters of IDVR is given in table 6.2

Table 6.2 The parameters of IDVR

Parameter	**Rating**
AC Line Voltage	3Φ, 415V, 50Hz
DVR rating connected to substation 1 (DVR1)	3Φ, 75KVAR, 415V
DVR rating connected to substation 2 (DVR2)	3Φ, 30KAVR, 415V
DC link Voltage	600V
DC link capacitor	5000μF
Ripple filter for DVR 1	R=10Ω, C=35μF
Ripple Filter for DVR 2	R=4.8Ω, C=15μF
Values of PI controller for two DVR1 and DVR 2	K_p= 0.2, K_i= 10
Rating of individual injection transformer of DVR 1	1Φ, 100KVAR, 415V/415V, 50Hz
Rating of individual injection transformer of DVR 2	1Φ, 50KVAR, 415V/415V, 50Hz
PWM switching frequency	10KHz

The output voltage from the DVR is injected into the system via the injection transformer. In this work, three single transformers are connected to three phase DVR.

Substituting all the ratings of IDVR, the total system represented in fig 6.4 is simulated for three cases.

1. Switching ON induction motor at substation 1.

2. Occurrence of an LG fault at one of the load connected to substation 2

3. Occurrence of a fault at substation 2 and switching ON induction motor at substation 1 at same instant of time.

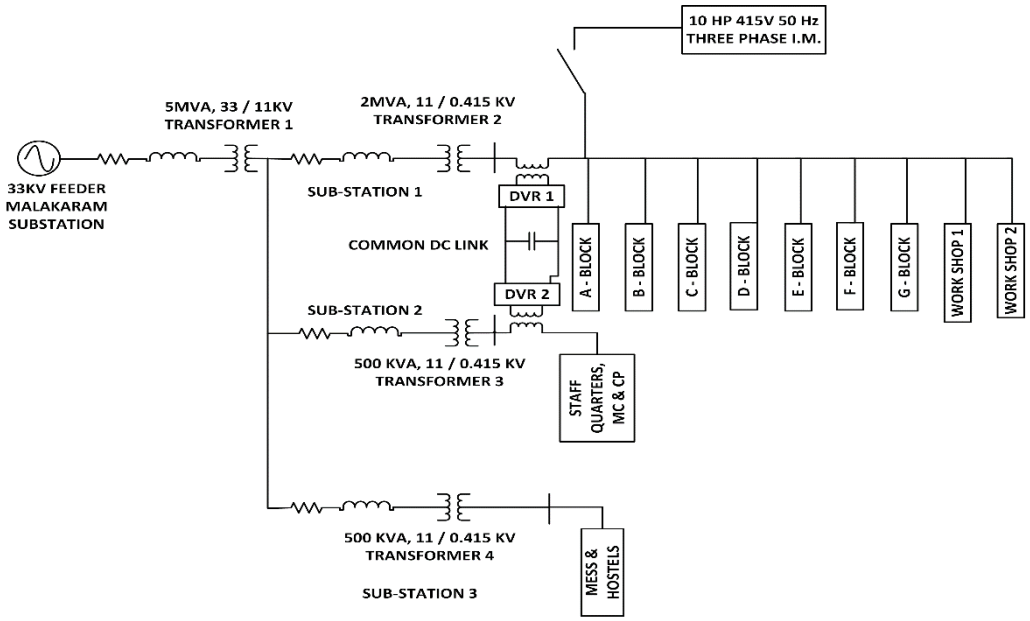


Fig. 6.4 Schematic layout of real time load with IDVR (VSI)

6.3.1 Switching On induction motor load

As mentioned earlier the induction motor which is connected to substation 1 shown is switched ON at 0.5sec, due to which voltage sag is created PCC of substation 1, as represented in fig 6.3. In the presence of IDVR, the voltage sag that occurred during the switching condition of the induction motor is completely mitigated, as shown in fig 6.5. When the voltage sag occurs, the control system of IDVR discussed in chapter 3 and chapter 4 senses the voltage error and signals the PWM inverter to inject the required voltage into the system. Hence, the voltage at 0.5sec is maintained at 415V in the presence of IDVR. Therefore, the voltage sag caused when induction motor is switched ON is completely compensated by the IDVR, thereby protecting the sensitive loads which are connected to substation 1 from the effect of voltage deviations. In addition, the voltage drop caused due to the inductive loads connected at substation 1, is mitigated and the voltage maintained at 415V, in the presence of IDVR. The next case explains about the operation of IDVR during an LG fault.

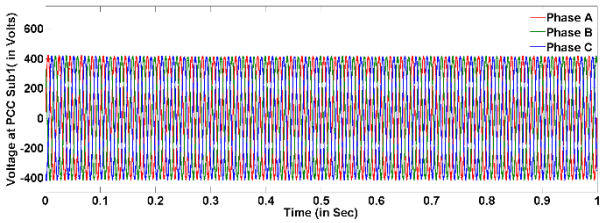


Fig. 6.5 Voltage at PCC of substation1 when the induction motor is switched ON in the presence of IDVR

6.3.2 LG Fault at Substation 2

In this case an LG fault is created at one of the loads connected to substation 2. The reason for choosing an LG fault is because it is the most frequently occurring fault among all unbalanced faults. The voltage profile at PCC of substation 2 during the condition of fault and in the absence of IDVR is shown in fig 6.2.

The fault created at CP load connected to substation 2 on R phase, results in a voltage swell in Y and B phases at PCC of substation 2. With the IDVR connected, the voltage at PCC of substation 2, for the fault condition is as shown in fig 6.6.

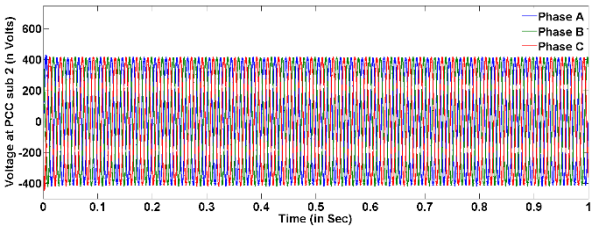


Fig. 6.6 Voltage at PCC of substation 2 when LG fault is applied with IDVR

Comparing fig 6.2 and fig 6.6, it can be observed that the voltage swell observed in Y and B phases at PCC of substation 2, is completely mitigated by the IDVR. The control system of IDVR detects swell in the voltage and the inverter injects a voltage so as to maintain 415V in Y and B phases. In addition, IDVR also injects voltage in R phase to make the voltage 415V. So the voltage in all the

three phases is maintained at rated value thereby the sensitive loads at the medical centre load which are connected to substation 2 are protected from the voltage fluctuations by the IDVR. In both case 1 and case 2, the voltage sag/swell is not created at a same instant in both the feeders. If one feeder is affected with voltage sag/swell, the other feeder is considered to be healthy.

6.4 Conclusion

This chapter deals with mitigation of voltage sag/swell with an IDVR. The electrical load of BITS Pilani Hyderabad Campus is considered as real time load, where the sensitive loads which get affected with the voltage sag/swell are identified. IDVR is connected to the PCC of those substations to which the sensitive loads are connected. Based on the intensity of voltage sag/swell that occurred at the substations, the appropriate ratings for the IDVR, DC link of IDVR and injection transformer are designed. Various possible chances of voltage sag/swell occurrences in the real time load have been considered. The bidirectional compensation of voltage sag/swell in both substations with IDVR is observed. The IDVR effectively maintains the voltage at the substations at the rated value. Therefore the IDVR is helpful in solving the problems of voltage sag/swell in the considered real time load and with IDVR, multiple voltage sags/swells can be mitigated at same time, thereby protecting the sensitive loads from the voltage disturbances. Thus with the insight of the simulation results a prototype model of IDVR is developed and analysed on a power system simulator. The experiment on laboratory prototype model of IDVR is discussed in the next chapter.

Chapter 7

Laboratory Prototype of IDVR

7.1 Introduction

The performance of IDVR for mitigating voltage sag/swell in various possible scenarios is analyzed with simulation results. In order to substantiate the simulation results, the IDVR should be tested in laboratory environment. This chapter presents the hardware implementation of novel bidirectional voltage sag compensation by the IDVR in multiple feeders at same instance. A two line feeder power system is considered with IDVR installed. The IDVR is implemented using two VSI with filter. As discussed in chapter 3, the voltage compensation ability of VSI and CSI are same and also the CSI is quite expensive. Hence the CSI is not chosen as the inverters of IDVR. The control system of IDVR for the voltage compensation is developed using DSPACE 1103.

The test power system for bidirectional compensation with IDVR considered is represented in fig 7.1.

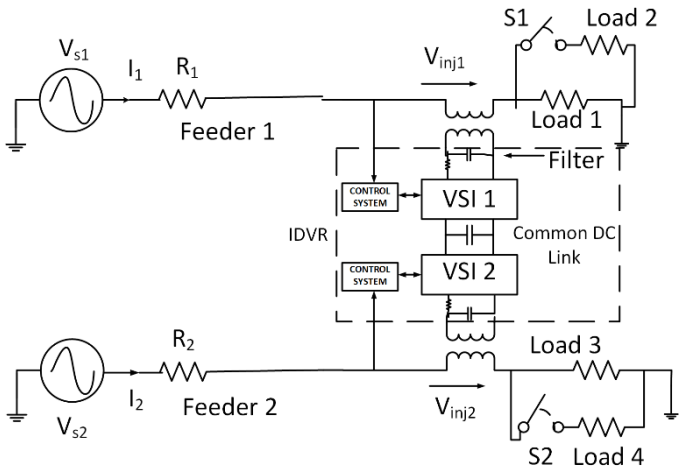


Fig. 7.1 Schematic Diagram of IDVR

The test power system with IDVR is developed in a single phase system. The test power system consists of two feeders with individual sources feeding Load 1 and Load 3 respectively. In order to apply a voltage sag in both feeder Load 2 and Load are suddenly ON at a particular period of time.

The major components used for developing laboratory prototype model of IDVR is given below

Voltage Source :

A regulated Power supply is used a voltage source for giving the power to the load. The power supply consists three phase and single phase panel. The input for the regulated power supply is a three phase AC supply which gets converted to a single phase AC supply.

Feeder/Loads:

The voltage source shown in fig 7.1 is connected to the respective loads through a feeder resistance. A resistive panel is used as feeder resistance in prototype of IDVR. The resistive panel consists of 10 resistances each of 100Ω respectively. These resistances can be connected in series or parallel depending upon the type of configuration. A tapping for 50Ω is also provided for each resistance of the panel. Load resistances shown in fig 7.1 are also taken from this resistive panel.

Voltage Source Inverter:

The Voltage Source Inverter used in the prototype is 4 leg 3 wire IGBT inverter. The make of the inverter is Semikron. The rating of inverter is 415V AC and 600V DC. The DC link of the inverter consists of two capacitors each of 250μF connected in parallel. A safety panel is provided at the gate terminal of each inverter. The minimum gate pulse voltage to turn ON the gate devices of the inverter is should be 14V. This is inverter is connected to the feeder through a series injection transformer.

Series Injection Transformer:

A 2KVA 110V/110V transformer is used for injecting the output voltage from the inverter into the feeder. A fuse protection is provided at the input and output terminals of the transformer.

DSPACE 1103 Controller:

The control system of IDVR for the voltage compensation is developed using DSPACE 1103. The DPSACE 1103 is real time interface control system. The DSPACE provides interface between the computer and the hardware. The controller has been designed and simulated using both the

Simulink and the DSPACE block sets, the MATLAB to-DSP interface libraries, Real-Time Interface to Simulink, and Real-Time Workshop, all located on the workstation PC. The control algorithm is developed in MATLAB and the dumped in the controller at one end. The other end of the controller is interfaced with gate signals of the IGBT inverter. The advantage of using the DSPACE is it can be closed loop controller and the accuracy of the controller is good. The control system developed in DPSACE 1103 is explained in the next section.

7.2 Control System of IDVR

The major function of control system of IDVR is to detect the voltage sag in the line to which IDVR is connected and then to regulate the IDVR for proper voltage injection to mitigate the voltage sag. The control system designed in this chapter is for a single phase IDVR system.

Fig 7.2 represents the block diagram of the control system of IDVR. The source voltage and load voltage are fed to the input of the control system. The following are working steps for algorithm in control system:

Step 1: The load voltage is given to a control block. The control block checks whether $V_L = V_L^*$, where $V_L^* = V_L - (0.10 * V_L)$

Step 2: The reference and load voltages are computed with the following equations.

$$V_{ref}^* = \sqrt{\frac{1}{T}\int_{t-T}^{T} V_S^2(t)} \tag{7.1}$$

$$V_{L1}^* = \sqrt{\frac{1}{T}\int_{t-T}^{T} V_L^{*2}(t)} \tag{7.2}$$

Where $T = \frac{1}{f}$, f is the fundamental frequency.

Step 3: The voltage error is calculated

$$V_{err} = V_{ref}^* - V_{L1}^* \tag{7.3}$$

Step 4: The error is fed to a proportional integral controller.

Step 5: The proportional Integral controller regulates the voltage error

$$V_{err}^{*} = V_{err} K_P + V_{err} \frac{K_i}{S} \tag{7.4}$$

Step 6: The regulated voltage error is given to the input of the PWM logic for generating the required gate pulses to the single phase inverter.

Therefore, whenever a voltage sag is detected, the control system detects the sag and generates the required gate pulses to the inverter for the voltage injection. This control system is present in the building blocks of the DVRs of a considered IDVR. With the modelling equations and the control logic, a test system with IDVR is experimented practically to test the bidirectional compensation ability of IDVR. The next section describes about simulation results and followed by experimental results.

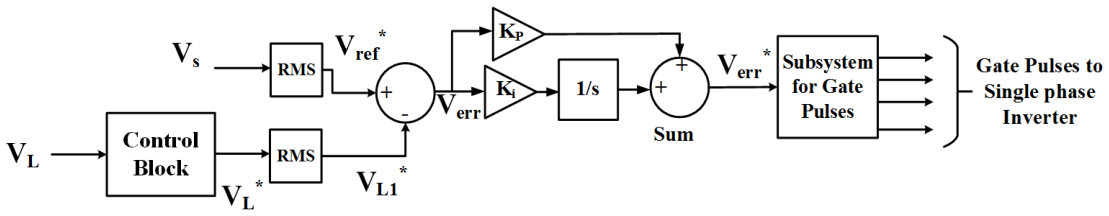


Fig. 7.2 Control System of IDVR

7.3 Simulation Results

The test power system shown in fig 7.1 consists of two single phase feeders, each fed with a voltage source. Each voltage source is rated to 230V. The values of R_1 of feeder 1 and R_2 of feeder 2 are given as 25Ω each. There are two loads load 1 and load 3 connected to feeder 1 and feeder 2. Each load is rated to 100Ω. The parameters of simulation block diagram shown in fig 7.1 are given in table 7.1. The source and load voltages of two feeders in the absence of IDVR are given in fig 7.3 and fig 7.4.

Since the two voltages are rated to same voltage level and consists of same rated loads, the magnitude of voltage sag is same in two cases.

Table 7.1 Parameters of Simulink Block Diagram

Parameters	**Rating**
Voltage Source of two Feeders	1Φ, 230V, 50Hz
Feeder Resistance of two Feeders	25Ω
Load Resistance of two Feeders	100Ω
DC link Voltage	250V
DC link capacitor	2500μF
Ripple filter for DVR 1	R=10Ω, C=35μF
Ripple Filter for DVR 2	R=10Ω, C=35μF
Values of PI controller for two DVR1 and DVR 2	K_p= 0.2, K_i= 10
PWM switching frequency	10KHz

Consider feeder 1 in fig 7.1, the total resistance in feeder when switch S_1 is open is 125Ω. With the total resistance and source voltage, the current I_1 in feeder 1 is calculated as 1.84A. Hence the voltage across Load 1 is 184V (1.84A*100Ω). In fig 7.3(b), the load voltage is observed to be 184V. The RMS voltage is 130V which is shown in fig 7.3(c).

The voltage sag is simulated at Load 1 of feeder 1 and Load 3 of feeder 2 between the interval of 0.2 to 0.6 seconds by switching ON and OFF the switches S_1 and S_2 of the two feeders respectively. Consider, S_1 of feeder 1 is ON, an additional load (load 2) of 100Ω is added in parallel to the existing load 1. With the impact of load 2, the total resistance in feeder 1 is now changed to 75Ω. The current I_1 is 3.06A. The load voltage is 3.06*50= 153V. Therefore, a voltage sag is observed in both feeders shown in the fig 7.3(b) and fig 7.4(b) in the interval of 0.2 and 0.6 seconds. At 0.6 seconds when S1 is open, the voltage is resorted to 184V. The IDVR should compensate the voltages in both feeders to 230V.

According to step 1 of control algorithm given in section 3, the control logic of IDVR enables the mitigation of voltage sag if $V_L = V_L^*$ where, $V_L^* = 90\% V_L$ which is 207V. From Fig 7.3(b) and 7.4(b), the load voltage of feeder is 184V initially and 153 V during sag condition. Fig 7.5 and fig 7.6 represents the source and load voltages in the presence of IDVR. By observing fig 7.5(b) and

7.6(b), it can be concluded that the IDVR could clearly compensate the voltage sags in fig 7.3(b) and 7.4(b) in both feeders at same time. With aid of PWM logic and RC filters, the distortion in the output of inverter of IDVR is completely eliminated. Hence the voltage injected by the two DVRs of IDVR is sinusoidal. With the presence of IDVR, the two feeders are protected against the voltage sag at same instance of time. Therefore, the bidirectional compensation of IDVR is justified with the evaluation of simulation results.

In order to justify the in phase compensation technique of IDVR, the resistive loads, Load 1 and Load 3 shown in Fig 5 are replaced as RL and RC loads in two different cases.

7.3.1 Case 1- Load 1 and Load 3 Replaced as RL Loads

The loads 1 and 3 shown in fig 7.1 are assumed as RL loads with the value of R=99.59Ω and L=0.183H for calculation convenience. As the supply frequency is 50Hz, the impedance of the each load is Z= (99.59+57.5i) Ω. Consider load 1, as the supply voltage is the current passing through load 1 is calculated as $I = 2\angle -30A$.

The value of the current indicates that the current passing through load 1 lags the voltage by 30^0. The simulation results shown fig 7.7 substantiate the calculated values. Fig 7.7(a) represents the load voltage and current at load 1 in the presence of IDVR during the compensation and the zoomed portion is shown in fig 7.7(b). From the results obtained, it is clearly understood that the phase angle of the load voltage remains same and the phase angle of the current is only changed by the replacing the load 1 with RL load. Hence it is clearly acceptable that the in phase compensation technique of IDVR can mitigate the voltage sag for RL load also. The results are similar to load 3 connected to feeder 2

7.3.2 Case 2-Load 1 and Load 3 Replaced as RC loads

In the above case the in phase compensation technique is explained for RL load. In order justify the technique in more in all the possible cases of load, the load 1 and load 3 in fig 7.1 are replaced with

RC load. The values of R and C are assumed as 99.59Ω and 55μF respectively. With the same supply voltage the load 1 current is calculated as $I = 2\angle -30A$. Here in this case the current is leading the voltage by 30^0. Fig 7.8 shows the simulation results of voltage and current of load 1 in the presence of IDVR during the compensation. Likewise in case 1 with RL load, the in phase compensation technique is working efficiently for RC load.

Hence it can be concluded that the in phase technique proposed for voltage compensation of IDVR is proven efficient in mitigating voltage sag irrespective to the type of load.

Therefore, the bidirectional compensation of IDVR is justified with the evaluation of simulation results. For further evaluation a laboratory prototype of IDVR is developed. The experimental results are explained in the next section.

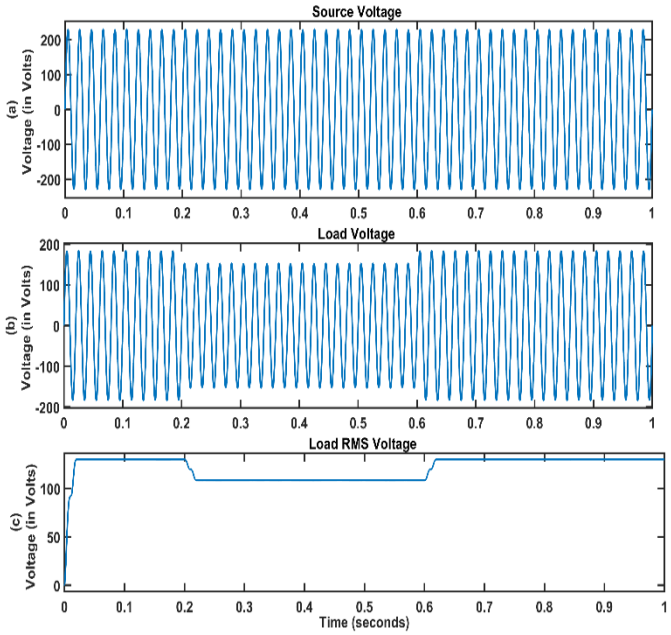


Fig. 7.3 (a) Source Voltage of Feeder 1 (b) Load Voltage of Feeder 1 (c) RMS Voltage of Load 1 in the absence of IDVR.

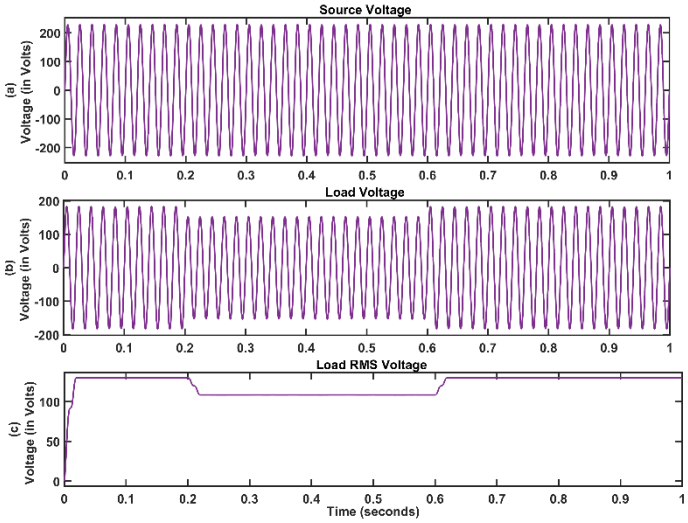


Fig. 7.4 (a) Source Voltage of Feeder 2 (b) Load Voltage of Feeder 2 (c) RMS Voltage of Load 2 in the absence of IDVR.

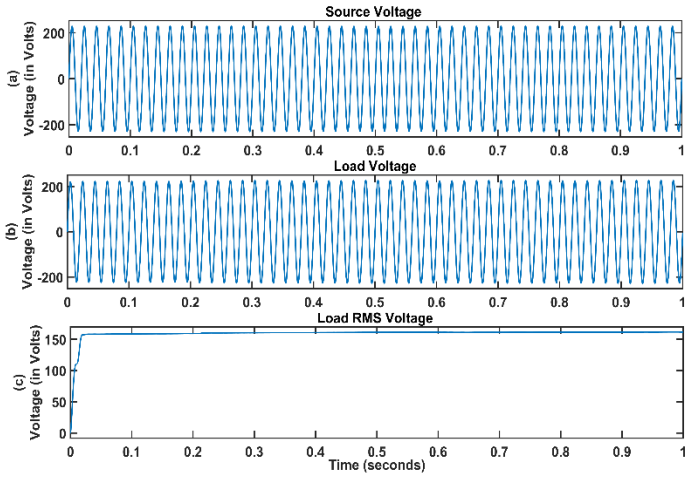


Fig. 7.5 (a) Source Voltage of Feeder 1 (b) Load Voltage of Feeder 1 (c) RMS Voltage of Load 1 in the presence of IDVR.

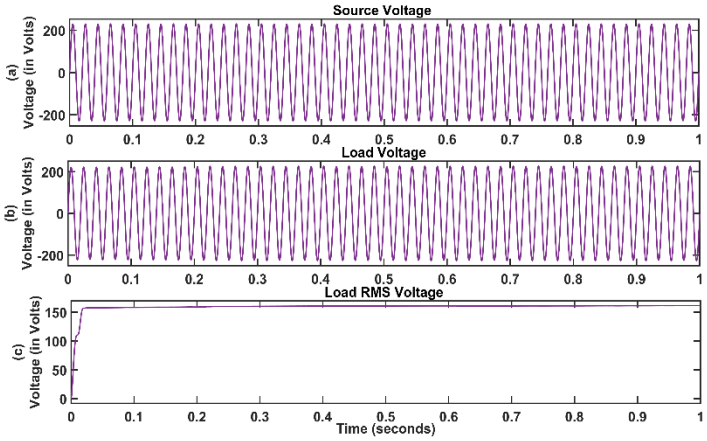
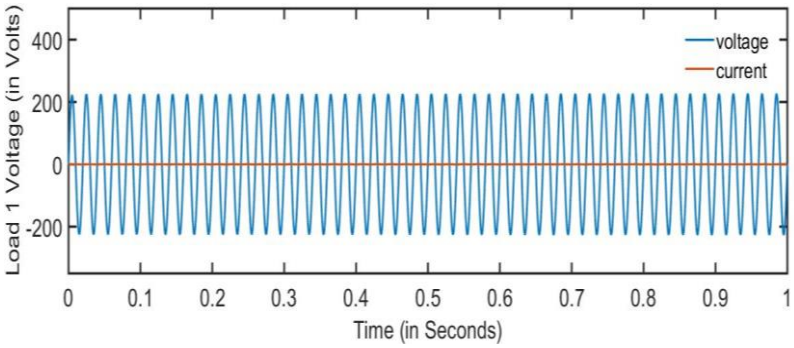
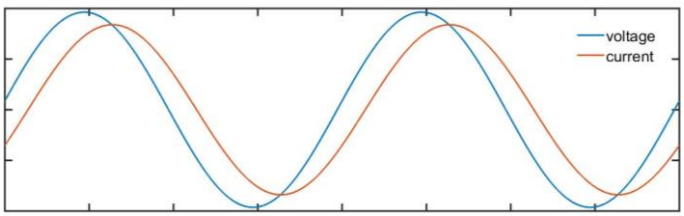


Fig. 7.6 (a) Source Voltage of Feeder 2 (b) Load Voltage of Feeder 2 (c) RMS Voltage of Load 2 in the presence of IDVR.

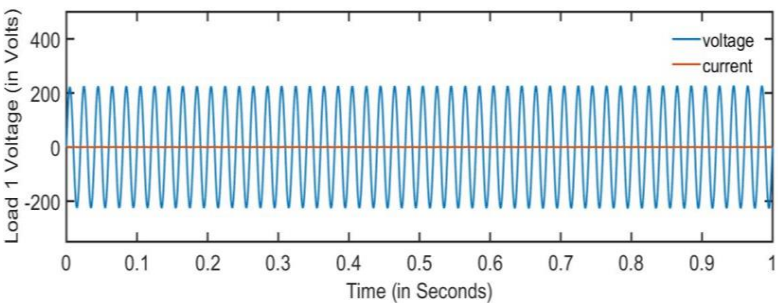


(a)

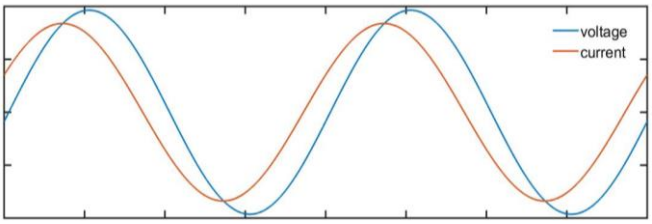


(b)

Fig. 7.7 (a) Simulation of load 1 as RL load in the presence of IDVR. (b) Zoomed Portion of voltage and current in 7.7 (a)



(a)



(b)

Fig. 7.8 (a) Simulation of load 1 as RC load in the presence of IDVR. (b) Zoomed Portion of voltage and current in 7.8 (a)

7.4 Experimental Results

A two line IDVR laboratory prototype model is shown in fig 7.9. The prototype model is developed for experimental verification of bidirectional compensation of IDVR. The schematic layout of hardware set up is shown in fig 7.10. The parameters of prototype model are given in table 7.1. Due to laboratory technical constraints the total experiment is performed in low voltage levels. A voltage source of 25V is fed to each feeder. The voltage source of each feeder is fed to a resistance of 90Ω. The loads of each feeder are rated to 100Ω. A double pole single throw switch is provided to add an additional load of 100Ω for both feeders so that the voltage sag is created in both feeders at same instance of time. The voltage source inverters shown in fig 7.9 are PWM based voltage source inverters having insulated gate bipolar transistor (IGBT) switches. The LC filters are present to filter the harmonics in injected voltage and current present at the output of the voltage source inverter. The implementation of algorithms of control system of IDVR system are accomplished with DSPACE DS1103 control board.

Table 7.2 Parameters of Prototype Model

Parameters	**Rating**
Voltage Source of two Feeders	1Φ, 25V, 50Hz
Feeder Resistance of two Feeders	90Ω
Load Resistance of two Feeders	100Ω
DC link Voltage	50V

DC link capacitor	500μF
Ripple filter for DVR 1	R=5Ω, C=10μF
Ripple Filter for DVR 2	R=5Ω, C=10μF
Values of PI controller for two DVR1 and DVR 2	K_p= 0.2, K_i= 10
PWM switching frequency	10KHz

Fig 7.11 and fig 7.12 represents the load voltages of feeder 1 and feeder 2 in the absence of IDVR. Consider one feeder in the experimental set up in the absence of IDVR. The total resistance in feeder before switch is open is 190Ω. The current in the feeder 1 is 0.13A. Therefore, the load voltage of feeder is 13V (0.13A*100Ω) which can be observed in fig 7.11. The second feeder voltage is also similar because the two feeders have same parameters ratings. The second feeder voltage is 13V which can be observed in fig 7.12.

The load voltages of two feeders are dropped to 8V at 0.15S when switch is closed. After closing switch the total resistance in each feeder is 140Ω. Hence the current is 0.17A and the load voltage is 0.17*50= 8.9V. Hence a voltage sag is applied in both feeders at same time between 0.15s to 0.5 s. The load voltage in both feeders (fig 7.11 and fig 7.12) is observed to be restored to 13V, when switch is open. The set value of IDVR to initiate compensation is 20.7V (90% of V_S=25V). The compensation algorithm starts to compensate as the load voltage observed is 13V and 8V during sag condition. .

In the presence of IDVR, the load voltages of both feeders are given in Fig 7.13 and Fig 7.14. Whenever the load voltage is less than the compensation limit, the control system of IDVR senses the voltage error and regulates the PWM logic to generate the gate signals to the voltage source inverter. The inverter injects the necessary voltage into the system so that the voltage sag is mitigated. As observed in fig 7.13 and fig 7.14, the load voltage in two feeders is maintained to 25V by the IDVR and the voltage sag between the intervals of 0.15 to 0. 5 seconds is compensated

by the IDVR at same instance of time. Therefore the bidirectional voltage compensation with IDVR is verified with the experimental results.

Hence considering experimental results, the IDVR can be utilized for mitigation of voltage sag simultaneously in multiple feeders at same instance of time.

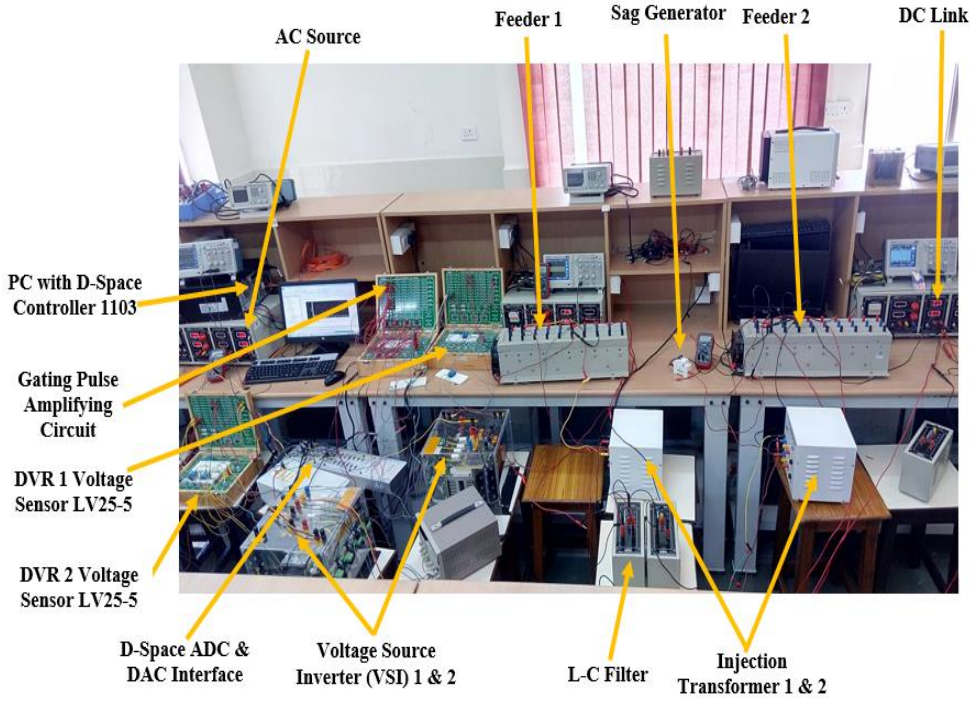


Fig. 7.9 Laboratory Prototype of IDVR system

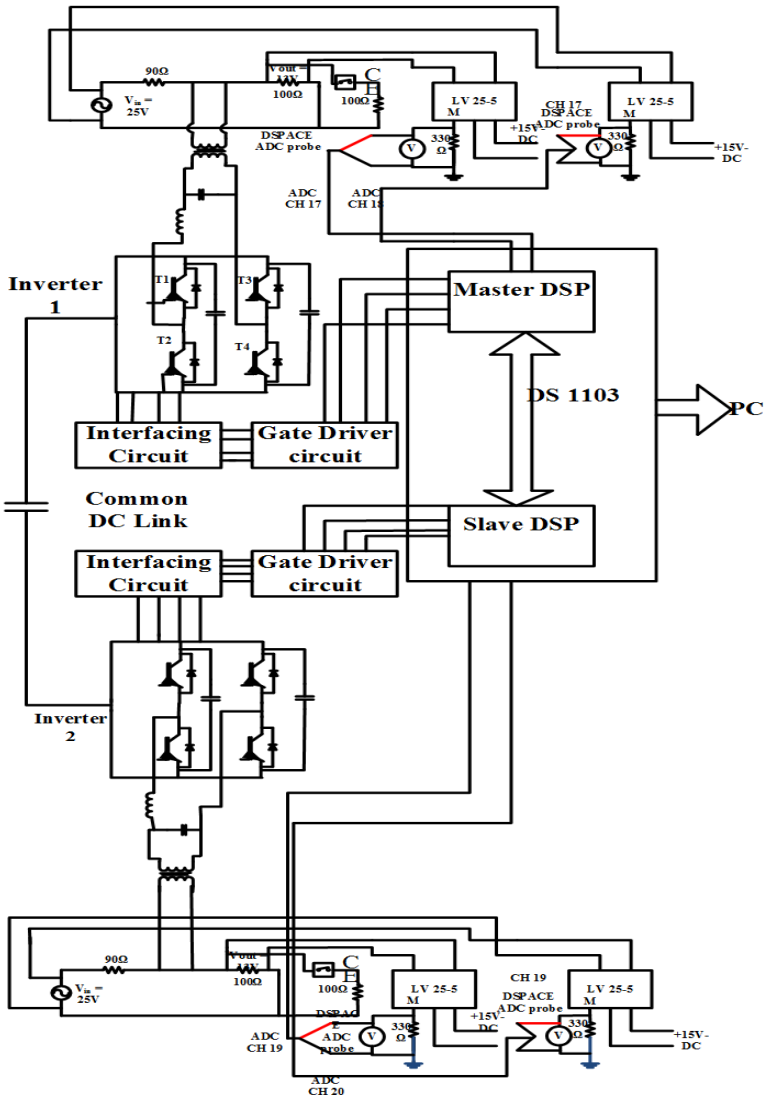


Fig. 7.10 Schematic diagram of hardware prototype

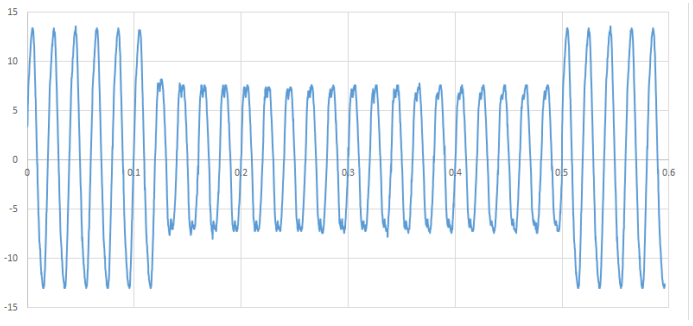


Fig. 7.11 Load Voltage of Feeder 1 in the absence of IDVR

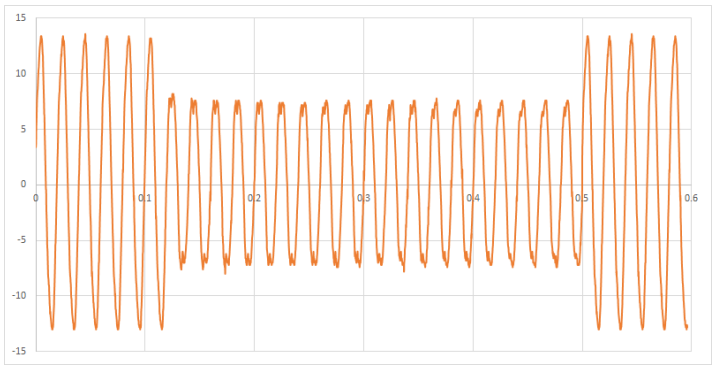


Fig. 7.12 Load Voltage of Feeder 2 in the absence of IDVR

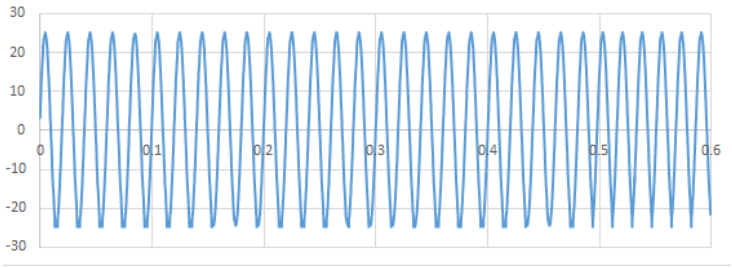


Fig. 7.13 Load Voltage of Feeder 1 in the presence of IDVR

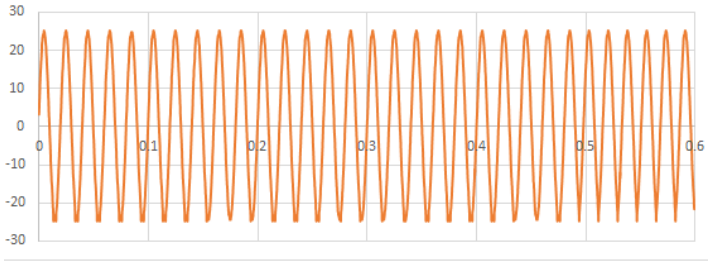


Fig. 7.14 Load Voltage of Feeder 2 in the presence of IDVR

7.5 Conclusion

This chapter proposes the concept of bidirectional compensation of IDVR. A test system comprising of a two feeder IDVR system is considered. The voltage sag is applied in two feeders at same instance and the effectiveness of IDVR in mitigating the voltage sag in both feeders at same instance is verified with experimental setup. The experimental results are obtained by developing a laboratory prototype model of IDVR. A control system for IDVR is developed for sensing the voltage error and regulating the IDVR to inject the required voltage for the mitigation of voltage sag. The experimental results have proven the efficient operation of IDVR in mitigating the voltage sag in two feeder topology at same instance. Hence IDVR can be utilized for multi-level feeder voltage compensation.

Chapter 8

Conclusion

8.1 Conclusion

The electronic equipment loads are sensitive towards the power quality problems. Consequently the power quality is playing a vital role in effective operation of sensitive loads. One of the major and frequently occurring power quality problems is voltage sag/swell and harmonics. The optimal solution for this is the Flexible AC Transmission Systems (FACTS) device known as Interline Dynamic Voltage Restorer (IDVR). In this thesis, the IDVR is utilised to mitigate the voltage sag/swell and harmonics in the distribution level of power systems. The inverter and DC link of IDVR are modelled to get a controlled output from IDVR. Further, the IDVR is tested in various configurations and applications of power system. The IDVR has proven its efficiency in mitigating the voltage sag/swell in all the considered cases.

The major contribution of the research work is the implementation of bidirectional compensation of IDVR. IDVR is the only D-FACTS device which has a capability of compensating simultaneous voltage sag/swell in multiple feeders at same instance of time. Hence, bidirectional compensation of IDVR is one of biggest advantage of IDVR.

The second major contribution of thesis work is represented in chapter 5. In this chapter the performance of IDVR with CSI and VSI as its building blocks for mitigating voltage sag and harmonics was compared. Voltage sag was created in three different ways; sudden switching of load, with single phase to ground fault and double phase to ground fault. In all the three cases the IDVR with either CSI or VSI as its building blocks was used to mitigate voltage sag and harmonics. The results with VSI and CSI are compared in all the three cases. Based on the results obtained in all the three cases, the performance of IDVR in mitigating voltage sag in all the three conditions

with VSI or CSI was observed to be same. But, for THD the performance of IDVR with CSI as building block was giving better result than IDVR with VSI. The individual magnitudes of harmonics are decreased with CSI than VSI due to the DC link inductance of CSI.

The real time application of IDVR, is IDVR designed for a specific application to mitigate power quality problems in an existing real time load. The electrical load of BITS Pilani Hyderabad Campus is considered as real time load, where the sensitive loads that are effected with the voltage sag/swell are identified. It is observed that the IDVR is able to maintain the voltage to the rated value effectively. Therefore the IDVR is helpful in solving the problems of voltage sag/swell in the considered real time load and with the IDVR, multiple voltage sags/swells are mitigated at same time, thereby protecting the sensitive loads from the voltage disturbances.

With the insight of the simulation results a prototype model of IDVR is developed. The experiment on laboratory prototype model of IDVR with the two feeder power system has been developed using DSPACE 1103. A test system comprising of a two feeder IDVR system is considered. The voltage sag is applied in two feeders at same instance and the effectiveness of IDVR in mitigating the voltage sag in both feeders at same instance was verified with experimental setup on a small scale rating. The experimental results have established the efficient operation of IDVR in mitigating the voltage sag in two feeder topology at same instance.

Over all the IDVR is the economical and optimal device for mitigating the voltage sag/swell in the distribution system. IDVR suits well to mitigate multiple voltage sags in various distribution feeders.

8.2 Future Work

The research on IDVR can be extended further in the level of voltage sag compensation. The first recommendation for future work in the thesis is extension of voltage sag compensation to multi-level i.e. more than two feeders. In total thesis work the voltage sag compensation was only

experimented to only two feeders. The performance of IDVR in mitigating voltage sag can be experimented with more than two feeders. With multi-level compensation, utilization of IDVR for voltage sag compensation can be justified in a better way.

The experimental prototype of IDVR is developed to substantiate the effectiveness of the IDVR in improving the voltage profile during the case of simultaneous voltage sag in different feeders. Due to technical constraints the voltage source level is scaled down to 25V for each feeder. The future scope of research is to scale up the voltage level to 230V for single phase and 415V for three phase IDVR system. The prototype results can be analyzed in a better way by connecting the IDVR to a power system simulator. The power system simulator resembles the generation, transmission and distribution of a power system. If the IDVR is connected to the distribution side of power system simulator, the results obtained will justify the voltage compensation ability of IDVR in a more practical manner.

Bibliography

[1] A. Ghosh and G. Ledwich, "Compensation of distribution system voltage using DVR," *IEEE Trans. Power Deliv.*, vol. 17, no. 4, pp. 1030–1036, 2002.

[2] S. S. Choi, B. H. Li, and D. M. Vilathgamuwa, "Dynamic voltage restoration with minimum energy injection," *IEEE Trans. Power Syst.*, vol. 15, no. 1, pp. 51–57, 2000.

[3] P. V. Naidu, "Design of a Hysteresis Voltage Control Based Interline DVR (IDVR) with VA Optimization," 2014.

[4] M. Moradlou and H. R. Karshenas, "Design strategy for optimum rating selection of interline DVR," *IEEE Trans. Power Deliv.*, vol. 26, no. 1, pp. 242–249, 2011.

[5] R. Nittala, A. M. Parimi, and K. Uma Rao, "A new approach for replenishing DC link energy for Interline Dynamic Voltage Restorer to mitigate voltage sag," in *2014 5th International Conference on Intelligent and Advanced Systems: Technological Convergence for Sustainable Future, ICIAS 2014 - Proceedings*, 2014.

[6] A. Elserougi *et al.*, "An Interline Dynamic Voltage Restoring and Displacement Factor Controlling Device (IVDFC)," vol. 29, no. 6, pp. 2737–2749, 2014.

[7] K. Abojlala, D. Holliday, and L. Xu, "Transient analysis of an interline dynamic voltage restorer using dynamic phasor representation," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2016, pp. 1–7.

[8] S. SivaRanjani and K. Suresh, "Hybrid interline dynamic voltage restoring and displacement factor controling device for improving power quality of the distribution," in *2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, 2016, pp. 4581–4585.

[9] M. R. Banaei, S. H. Hosseini, and G. B. Gharehpetian, "Inter-line dynamic voltage restorer control using a novel optimum energy consumption strategy," *Simul. Model. Pract. Theory*, vol. 14, no. 7, pp. 989–999, 2006.

[10] I. Journal and E. Science, "SIMULATION OF INTERLINE DYNAMIC VOLTAGE RESTORER," vol. 3, no. 8, pp. 6454–6463, 2011.

[11] M. Moradlou and H. R. Karshenas, "Compensation range calculation in an interline dynamic voltage restorer (IDVR) encountering different voltage sag types," *Int. Trans. Electr. Energy Syst.*, vol. 24, no. 7, pp. 992–1005, Jul. 2014.

[12] C. Sankaran, *Power Quality*. CRC Press, 2001.

[13] M. H. Bollen, *Understanding Power Quality Problems: Voltage Sags and Interruptions*. Wiley, 2000.

[14] K. Kitagawa and T. Omori, "Static Capacitors for High-Voltage Use in Japan," *Trans. Am. Inst. Electr. Eng.*, vol. 70, no. 2, pp. 1233–1239, Jul. 1951.

[15] K. Raman Nayar and A. Kuppurajulu, "Optimisation of static-capacitor installations and switching schedules in distribution systems," *Proc. Inst. Electr. Eng.*, vol. 122, no. 4, p. 415, 1975.

[16] F. B. K. Mahmood *et al.*, "Weakest location exploration in IEEE-14 bus system for voltage stability improvement using STATCOM, synchronous condenser and static capacitor," in *2017 International Conference on Electrical, Computer and Communication Engineering (ECCE)*, 2017, pp. 623–629.

[17] Hongyang Zhang, J.-P. Hasler, N. Johansson, L. Angquist, and H.-P. Nee, "Frequency response improvement with synchronous condenser and power electronics converters," in *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, 2017, pp. 1002–1007.

[18] Z. Ling, Y. Cui, L. Ruan, W. Cai, Y. Zhang, and R. Yang, "The effect of load condition on dynamic response capability of synchronous condenser," in *2017 20th International Conference on Electrical Machines and Systems (ICEMS)*, 2017, pp. 1–4.

[19] N. G. Hingorani and L. Gyugyi, *Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems*. Wiley, 2000.

[20] R. K. Varma and R. Salehi, "SSR Mitigation With a New Control of PV Solar Farm as STATCOM (PV-STATCOM)," *IEEE Trans. Sustain. Energy*, vol. 8, no. 4, pp. 1473–1483, Oct. 2017.

[21] Q. Su, W. Quan, W. Quan, G. Cai, and J. Li, "Improved robust adaptive backstepping control approach on STATCOM for non-linear power systems," *IET Gener. Transm. Distrib.*, vol. 11, no. 13, pp. 3428–3437, Sep. 2017.

[22] M. R. Shaik and A. S. Reddy, "Optimal placement of STATCOM with ABC algorithm to improve voltage stability in power systems," in *2016 International Conference on Signal Processing, Communication, Power and Embedded System (SCOPES)*, 2016, pp. 648–652.

[23] D.-N. Truong, V.-T. Ngo, and Mi-Sa Nguyen Thi, "Voltage stability enhancement of the Bac Lieu wind power system connected to power grid using a STATCOM," in *2017 International Conference on System Science and Engineering (ICSSE)*, 2017, pp. 160–164.

[24] S. K. Mishra, S. C. Swain, L. N. Tripathy, P. D. K. Yadav, and A. K. Nahak, "A differential relay based UPFC compensated line," in *2016 International Conference on Signal Processing, Communication, Power and Embedded System (SCOPES)*, 2016, pp. 1976–1981.

[25] A. Hamache, M. O. Bensidhoum, H. Chekireb, and A. Ouslimani, "Sliding Mode Observer

based Fault Tolerant Controller of UPFC for power flow tracking," in *2017 6th International Conference on Systems and Control (ICSC)*, 2017, pp. 291–296.

[26] Sang-Hoon Lee, Myeong-Chan Kang, and Young-Doo Yoon, "Single-phase UPFC topology using autotransformer structure based on two half-bridge converters," in *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, 2017, pp. 789–794.

[27] P. Song, Z. Xu, and H. Dong, "UPFC-based line overload control for power system security enhancement," *IET Gener. Transm. Distrib.*, vol. 11, no. 13, pp. 3310–3317, Sep. 2017.

[28] J. Khodaparast, M. Khederzadeh, F. F. da Silva, and C. Leth Bak, "Power Swing Detection in UPFC-Compensated Line by Phase Angle of Current," *IEEE J. Emerg. Sel. Top. Circuits Syst.*, vol. 7, no. 3, pp. 459–468, Sep. 2017.

[29] S. B. Karanki *et al.*, "An optimal power flow control method of power system using interline power flow controller (IPFC)," *IEEE Trans. Ind. Appl.*, vol. 3, no. 3, pp. 2414–2425, 2011.

[30] L. Gyugyi, C.-C. Liu, and A.-A. Edris, "Interline Power Flow Controller (IPFC)," in *Advanced Solutions in Power Systems: HVDC, FACTS, and Artificial Intelligence*, Hoboken, NJ, USA: John Wiley & Sons, Inc., 2016, pp. 629–649.

[31] S. B. Daram, P. S. Venkataramu, and M. S. Nagaraj, "Performance index based contingency ranking under line outage condition incorporating IPFC," in *2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, 2016, pp. 2589–2593.

[32] E. de Vargas Fortes, P. B. de Araujo, L. H. Macedo, B. R. Gamino, and L. F. B. Martins, "Analysis of the influence of PSS and IPFC-POD controllers in small-signal stability using a Simulated Annealing algorithm," in *2016 12th IEEE International Conference on Industry Applications (INDUSCON)*, 2016, pp. 1–8.

[33] H. Li, "Design and implementation of TMS320F2812 digital control system based on DSTATCOM," in *2017 36th Chinese Control Conference (CCC)*, 2017, pp. 3793–3797.

[34] A. A. Loubassou, Y. Zhang, Qijun, and Yesen, "Enhancement of isolated distributed generation system power quality using DSTATCOM," in *2017 36th Chinese Control Conference (CCC)*, 2017, pp. 9278–9284.

[35] M. T. Ahmad, N. Kumar, and B. Singh, "AVSF-based control algorithm of DSTATCOM for distribution system," *IET Gener. Transm. Distrib.*, vol. 11, no. 13, pp. 3389–3396, Sep. 2017.

[36] M. T. Ahmad, N. Kumar, and B. Singh, "Generalised neural network-based control algorithm for DSTATCOM in distribution systems," *IET Power Electron.*, vol. 10, no. 12, pp. 1529–1538, Oct. 2017.

[37] Nguyen Van Minh, Bach Quoc Khanh, and Pham Viet Phuong, "Comparative simulation results of DVR and D-STATCOM to improve voltage quality in distributed power system," in *2017 International Conference on System Science and Engineering (ICSSE)*, 2017, pp. 196–199.

[38] Y. W. Li, P. C. Loh, F. Blaabjerg, and D. M. Vilathgamuwa, "Investigation and Improvement of Transient Response of DVR at Medium Voltage Level," *IEEE Trans. Ind. Appl.*, vol. 43, no. 5, pp. 1309–1319, 2007.

[39] A. K. Sadigh, S. H. Hosseini, S. M. Barakati, and G. Gharehpetian, "Stacked multicell converter based DVR with energy minimized compensation strategy," in *41st North American Power Symposium*, 2009, pp. 1–6.

[40] A. Ghosh and G. Ledwich, "Compensation of distribution system voltage using DVR," *IEEE Trans. Power Deliv.*, vol. 17, no. 4, pp. 1030–1036, Oct. 2002.

[41] S. Sasitharan, M. K. Mishra, B. K. Kumar, and V. Jayashankar, "Rating and design issues of DVR injection transformer," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 449–455, 2008.

[42] A. Hossam-Eldin and A. Elserougi, "Renewable energy fed interline DVR for voltage sag mitigation in distribution grids," *Electr. Distrib. (CIRED 2013), 22nd Int. Conf. Exhib.*, no. 36, pp. 1–4, 2013.

[43] Z. Jie, H. Yuxiang, S. Hui, D. Li, and H. Yonghong, "Interactive detection method applied in DVR," in *2017 29th Chinese Control And Decision Conference (CCDC)*, 2017, pp. 1045–1052.

[44] Y. W. Li, F. Blaabjerg, and D. M. Vilathgamuwa, "Design and Comparison of High Performance Stationary-Frame Controllers for DVR Implementation," in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, 2006, pp. 912–918.

[45] J. G. Nielsen, F. Blaabjerg, and N. Mohan, "Control strategies for dynamic voltage restorer compensating voltage sags with phase jump," *Appl. Power Electron. Conf. Expo.*, vol. 2, pp. 1267–1273, 2001.

[46] H. Awad, J. Svensson, and M. Bollen, "Mitigation of Unbalanced Voltage Dips Using Static Series Compensator," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 837–846, May 2004.

[47] A. Khoshkbar Sadigh, E. Babaei, S. H. Hosseini, and M. Farasat, "Dynamic Voltage Restorer based on stacked multicell converter," in *2009 IEEE Symposium on Industrial Electronics & Applications*, 2009, vol. 1, pp. 419–424.

[48] A. K. Sadigh, S. H. Hosseini, S. M. Barakati, and G. Gharehpetian, "Flying capacitor

multicell converter based dynamic voltage restorer," in *41st North American Power Symposium*, 2009, pp. 1–6.

[49] C. N. Ho, H. S. H. Chung, and K. T. K. Au, "Design and Implementation of a Fast Dynamic Control Scheme for Capacitor-Supported Dynamic Voltage Restorers," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 237–251, Jan. 2008.

[50] B. Wang and G. Venkataramanan, "Dynamic Voltage Restorer Utilizing a Matrix Converter and Flywheel Energy Storage," in *2007 IEEE Industry Applications Annual Meeting*, 2007, pp. 208–215.

[51] J. G. Nielsen, F. Blaabjerg, and N. Mohan, "Control strategies for dynamic voltage restorer compensating voltage sags with phase jump," in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, 2001, vol. 2, pp. 1267–1273.

[52] V. F. Pires, D. Foito, A. Cordeiro, and J. F. Martins, "PV generators combined with UPQC based on a dual converter structure," in *2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, 2017, pp. 1781–1786.

[53] H. Hafezi and R. Faranda, "Open UPQC series and shunt units cooperation within Smart LV Grid," in *2017 6th International Conference on Clean Electrical Power (ICCEP)*, 2017, pp. 304–310.

[54] S. Devassy and B. Singh, "Design and Performance Analysis of Three Phase Solar PV integrated UPQC," *IEEE Trans. Ind. Appl.*, pp. 1–1, 2017.

[55] S. Devassy and B. Singh, "Control of solar photovoltaic integrated UPQC operating in polluted utility conditions," *IET Power Electron.*, vol. 10, no. 12, pp. 1413–1421, Oct. 2017.

[56] U. S. Vadivu and B. K. Keshavan, "Power quality enhancement of UPQC connected WECS using FFA with RNN," in *2017 IEEE International Conference on Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe)*, 2017, pp. 1–6.

[57] S. Moran, "A line voltage regulator/conditioner for harmonic-sensitive load isolation," in *Conference Record of the IEEE Industry Applications Society Annual Meeting*, 1989, pp. 947–951.

[58] H. Fujita and H. Akagi, "The unified power quality conditioner: the integration of series- and shunt-active filters," *IEEE Trans. Power Electron.*, vol. 13, no. 2, pp. 315–322, Mar. 1998.

[59] M. F. Farias, P. E. Battaiotto, and M. G. Cendoya, "Wind Farm to Weak-Grid Connection using UPQC custom power device," *2010 IEEE Int. Conf. Ind. Technol.*, pp. 1745–1750, 2010.

[60] J. Eakburanawat, P. Darapong, U. Yangyuen, and S. Po-ngam, "A simple control scheme of single phase universal active filter for power quality improvement," in *2004 IEEE Region 10 Conference TENCON 2004.*, 2004, vol. C, pp. 248–251.

[61] B. Han, B. Bae, S. Baek, and G. Jang, "New Configuration of UPQC for Medium-Voltage Application," *IEEE Trans. Power Deliv.*, vol. 21, no. 3, pp. 1438–1444, Jul. 2006.

[62] V. Khadkikar, A. Chandra, A. Barry, and T. Nguyen, "Analysis of Power Flow in UPQC during Voltage Sag and Swell Conditions for Selection of Device Ratings," in *2006 Canadian Conference on Electrical and Computer Engineering*, 2006, pp. 867–872.

[63] K. Hatua and V. T. Ranganathan, "A Novel VSI- and CSI-Fed Active–Reactive Induction Motor Drive with Sinusoidal Voltages and Currents," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3936–3947, 2011.

[64] W. C. Lee, D. M. Lee, and T. K. Lee, "New Control Scheme for a Unified Power-Quality Compensator-Q With Minimum Active Power Injection," *IEEE Trans. Power Deliv.*, vol. 25, no. 2, pp. 1068–1076, Apr. 2010.

[65] M. Basu, S. P. Das, and G. K. Dubey, "Investigation on the performance of UPQC-Q for voltage sag mitigation and power quality improvement at a critical load point," *IET Gener. Transm. Distrib.*, vol. 2, no. 3, p. 414, 2008.

[66] V. Khadkikar and A. Chandra, "A Novel Control Approach for Unified Power Quality Conditioner Q without Active Power Injection for Voltage Sag Compensation," in *2006 IEEE International Conference on Industrial Technology*, 2006, pp. 779–784.

[67] D.-S. Hyul, "A new control scheme of unified power quality compensator - Q with minimum power injection," in *30th Annual Conference of IEEE Industrial Electronics Society, 2004. IECON 2004*, 2004, vol. 1, pp. 51–56.

[68] Y. Y. Kolhatkar, R. R. Errabelli, and S. P. Das, "A sliding mode controller based optimum UPQC with minimum VA loading," in *IEEE Power Engineering Society General Meeting, 2005*, 2005, pp. 2240–2244.

[69] Y. Y. Kolhatkar and S. P. Das, "Experimental Investigation of a Single-Phase UPQC With Minimum VA Loading," *IEEE Trans. Power Deliv.*, vol. 22, no. 1, pp. 373–380, Jan. 2007.

[70] D. O. Kisck, V. Navrapescu, and M. Kisck, "Single-Phase Unified Power Quality Conditioner with Optimum Voltage Angle Injection for Minimum VA requirement," in *2007 IEEE International Symposium on Industrial Electronics*, 2007, pp. 2443–2448.

[71] G. S. Kumar, P. H. Vardhana, B. K. Kumar, and M. K. Mishra, "Minimization of VA loading of Unified Power Quality Conditioner (UPQC)," in *2009 International Conference on Power Engineering, Energy and Electrical Drives*, 2009, pp. 552–557.

[72] D. M. Vilathgamuwa, H. M. Wijekoon, and S. S. Choi, "A novel technique to compensate voltage sags in multiline distribution system - The interline dynamic voltage restorer," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1603–1611, 2006.

[73] A. Elserougi, A. Hossam-Eldin, A. Massoud, and S. Ahmed, "Investigation of inter-line dynamic voltage restorer with virtual impedance injection," *IECON Proc. (Industrial Electron. Conf.*, pp. 1975–1980, 2010.

[74] R. P. Usha, R. Sudha, and S. R. Reddy, "Voltage sag/swell compensation in an interline dynamic voltage restorer," *2011 Int. Conf. Emerg. Trends Electr. Comput. Technol. ICETECT 2011*, pp. 309–314, 2011.

[75] M. Shahabadini and H. Iman-Eini, "Improving the Performance of Cascaded H-Bridge Based Interline Dynamic Voltage Restorer," *IEEE Trans. Power Deliv.*, vol. 8977, no. c, pp. 1–1, 2015.

[76] D. M. Vilathgamuwa, H. M. Wijekoon, and S. S. Choi, "Interline dynamic voltage restorer: A novel and economical approach for multiline power quality compensation," *IEEE Trans. Ind. Appl.*, vol. 40, no. 6, pp. 1678–1685, 2004.

[77] P. U. Rani, "MODELING AND SIMULATION OF INTERLINE DYNAMIC VOLTAGE RESTORER USING SVPWM TECHNIQUE," *J. Theor. Appl. Inf. Technol.*, vol. 60, no. 1, 2014.

[78] V. D. Colli, P. Cancelliere, F. Marignetti, and R. Di Stefano, "Voltage Control of Current Source Inverters," vol. 21, no. 2, pp. 451–458, 2006.

[79] B. Wu and M. Narimani, "PWM Current Source Inverters," in *High-Power Converters and AC Drives*, Hoboken, NJ, USA: John Wiley & Sons, Inc., 2016, pp. 225–256.

[80] B. Wu and M. Narimani, "Other Multilevel Voltage Source Inverters," in *High-Power Converters and AC Drives*, Hoboken, NJ, USA: John Wiley & Sons, Inc., 2016, pp. 185–223.

[81] B. Wu, "Two-Level Voltage Source Inverter," in *High-Power Converters and ac Drives*, Hoboken, NJ, USA: John Wiley & Sons, Inc., 2007, pp. 93–118.

[82] D. G. Holmes and T. A. Lipo, "Modulation of SinglePhase Voltage Source Inverters," in *Pulse Width Modulation for Power Converters*, IEEE, 2009, pp. 155–213.

[83] P. Jayaprakash, B. Singh, D. P. Kothari, A. Chandra, S. Member, and K. Al-Haddad, "Control of Reduced-Rating Dynamic Voltage Restorer With a Battery Energy Storage System," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1295–1303, 2014.

[84] H. M. Wijekoon, D. M. Vilathgamuwa, and S. S. Choi, "Interline dynamic voltage restorer: an economical way to improve interline power quality," *IEE Proc. - Gener. Transm. Distrib.*,

vol. 150, no. 5, p. 513, 2003.

[85] A. Elserougi, A. M. Massoud, A. S. Abdel-Khalik, S. Ahmed, and A. A. Hossam-Eldin, "An Interline Dynamic Voltage Restoring and Displacement Factor Controlling Device (IVDFC)," *Power Electron. IEEE Trans.*, vol. 29, no. 6, pp. 2737–2749, 2014.

[86] J. Winders, *Power Transformers: Principles and Applications*. CRC Press, 2002.

[87] L. Piegari and R. Rizzo, "Adaptive perturb and observe algorithm for photovoltaic maximum power point tracking," *IET Renew. Power Gener.*, vol. 4, no. 4, p. 317, 2010.

[88] T. Esram and P. L. Chapman, "Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 439–449, 2007.

[89] A. Emadi, A. Nasiri, and S. B. Bekiarov, *Uninterruptible Power Supplies and Active Filters*. CRC Press, 2004.

[90] R. Nittala, A. M. Parimi, and K. U. Rao, "Phase shifting transformer based Interline dynamic voltage Restorer to mitigate voltage sag," in *2013 Annual IEEE India Conference, INDICON 2013*, 2013.

[91] F. Liu, B. Wu, and M. Pande, "Zero-Speed Operation of High-Power PWM Current-Source-Inverter Fed Induction Motor Drive," *Power Electron. IEEE*, vol. 27, no. 6, pp. 3020–3027, 2011.

[92] M. H. Bierhoff and F. W. Fuchs, "Pulse Width Modulation for Current Source Converters – A Detailed Concept."

[93] S. A. S. Grogan, D. G. Holmes, and B. P. McGrath, "High performance voltage regulation of current source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2439–2448, 2010.

[94] W. Wang, F. Gao, Y. Yang, and F. Blaabjerg, "Operation and Modulation of H7 Current Source Inverter with Hybrid SiC and Si Semiconductor Switches," *IEEE J. Emerg. Sel. Top. Power Electron.*, pp. 1–1, 2017.

[95] B. Wu and M. Narimani, "Multipulse SCR Rectifiers," in *High-Power Converters and AC Drives*, Hoboken, NJ, USA: John Wiley & Sons, Inc., 2016, pp. 65–81.

[96] J. D. Ma, B. Wu, N. R. Zargari, and S. C. Rizzo, "A space vector modulated CSI-based ac drive for multimotor applications," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 535–544, 2001.

[97] S. Meshram and O. Sahu, "Application of Ann in Economic Genera-Tion Scheduling in Ieee 6-Bus System," vol. 3, no. 3, pp. 2461–2466, 2011.

[98] C. I. Dvr, C. N. Ho, H. S. Chung, and S. Member, "Implementation and Performance Evaluation of a Fast Dynamic Control Scheme for," *IEEE Trans Power Electron.*, vol. 25, no. 8, pp. 1975–1988, 2010.

[99] SivaRanjani and K. Suresh, "Hybrid interline dynamic voltage restoring and displacement factor controlling device for improving power quality of the distribution," 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, 2016, pp. 4581-4585.

[100] K. Abojlala, D. Holliday and L. Xu, "Transient analysis of an interline dynamic voltage restorer using dynamic phasor representation," 2016 IEEE 17th Workshop on Control and Modelling for Power Electronics (COMPEL), Trondheim, 2016, pp. 1-7.

List of Publications

Journals

1. **Nittala Ramchandra**, Alivelu M. Parimi, and K. Uma Rao "Experimental Prototype Model of IDVR for Bidirectional Voltage Compensation", International Journal of Power Electronics and Drive Systems (IJPEDS), Vol. 9, No. 1, March 2018, pp. 297-304 (**Scopus Journal**)

2. **Nittala Ramchandra**, Alivelu M. Parimi, and K. Uma Rao "A Real Time Implementation of IDVR for Improvement of Power quality", International Journal of Power Electronics, Inderscience (**Scopus Journal**) (In Press)

3. **Nittala Ramchandra,** Alivelu M. Parimi, and K. Uma Rao. "Application of PST Source Based DC Link Restoration for IDVR", International Journal of Electrical and Computer Engineering (IJECE), Vol. 10 No.3, pp 1103-1111, June 2017. (**Scopus Journal**)

4. **Nittala, Ramchandra**, Alivelu M. Parimi, and K. Uma Rao. "A Real Time Application of IDVR for Improvement of Power quality", International Journal of Control Theory and Applications, Vol. 10, Issue 16 ,2017, pp-95-102. (**Scopus Journal-2016**)

International Journals under Review

1. **Nittala Ramchandra**, Alivelu M. Parimi, and K. Uma Rao " An Experimental Prototype Model of IDVR for Bidirectional Voltage Compensation", Electrical Power Components ad Systems, Taylor and Francis (**SCI Index Journal**)

International Conferences

1. **Nittala Ramchandra**, Alivelu M. Parimi, and K. Uma Rao. "Mitigation of voltage sag/swell with CSI-IDVR." Recent Developments in Control, Automation and Power Engineering (RDCAPE), 2015 International Conference on. IEEE, 2015.

2**. Nittala Ramchandra**, Alivelu M.Parimi, and K. Uma Rao. "Comparing the performance of IDVR for mitigating voltage sag and harmonics with VSI and CSI as its building blocks." Signal Processing, Informatics, Communication and Energy Systems (SPICES), 2015 IEEE International Conference on. IEEE, 2015.

3. **Nittala Ramchandra**, Alivelu M. Parimi, and K. Uma Rao. "A new approach for replenishing DC link energy for Interline Dynamic Voltage Restorer to mitigate voltage sag." Intelligent and Advanced Systems (ICIAS), 2014 5th International Conference on. IEEE, 2014.

4. **Nittala Ramchandra**, Alivelu M. Parimi, and K. Uma Rao. "Phase shifting transformer based Interline Dynamic Voltage Restorer to mitigate voltage sag." India Conference (INDICON), 2013 Annual IEEE. IEEE, 2013.

Biography

Candidate Biography

Ramchandra Nittala is a full time research scholar at Department of EEE, BITS Pilani Hyderabad Campus. He received B.Tech. in Electrical and Electronics Engineering from Acharya nagarjuna university, Guntur, Andhra Pradesh, India in 2010. He received M.tech in Power System Specialization in Electrical and Electronics Engineering from KL university Guntur, Andhra Pradesh in 2012. He completed Ph.D. in Department of Electrical and Electronics Engineering in BITS Pilani Hyderabad Campus, Hyderabad in 2018. His Research interests are Power Quality improvement in distribution systems and FACTS Devices.

Supervisor Biography

Alivelu M. Parimi received M.E. with specialization in Control Systems in Electrical Engineering from Andhra University, Visakhapatnam, Andhra Pradesh, India in 2004. She received Ph.D. in Electrical and Electronics Engineering from, Universiti Teknologi Petronas, Tronoh, Perak, Malaysia in 2011. Currently, she is working as an Assistant Professor in Department of Electrical and Electronics Engineering in BITS Pilani Hyderabad Campus, Hyderabad. Her Research Interest is Application of FACTS devices to improve Power System Stability and Power Quality.

Co-Supervisor Biography

K Uma Rao received B.E. degree in Electrical Engineering from University Visvesvaraya College of Engineering, Bangalore in 1984 and M.E. degree in 1987 from the same University in Power Systems specialization. She received Ph.D. degree from Indian Institute of Science, Bangalore in 1996 in Power Engineering specialization. She also pursued MBA, Project Management from Indira Gandhi Open University, New Delhi in the year 2004. Currently, she is working as Professor in Electrical Engineering Department, RV college of Engineering, Bangalore. She has published many books, National, and International conferences and journals. Her research interests are Power Quality, FACTS.