CHAPTER 5

STATE RETENTIVE HYBRID D FLIP-FLOP

5.1 Introduction

With the exponential increase in leakage current with each process node [1]–[4], applications operating in low duty modes (inactive period is greater than active period) such as wearable devices, wireless sensor network, healthcare monitoring systems, and Internet of Things, suffers from large static power dissipation [5], [6]. They are mainly powered by a battery or an energy harvester with a power budget of few microwatts such that power consumption during standby mode often becomes a bottleneck in achieving long operational lifetimes [7]. Some of the techniques to reduce leakage currents are dynamic voltage scaling, reverse biasing, and the use of multi-threshold transistors, etc. These techniques help in reducing the leakage current, but they are not able to achieve zero leakage current. Thus, switching off the circuit (gating power supply vdd to zero) during standby mode seems to be the most efficient way to achieve zero standby power in these devices. However, direct gating of power results in the loss of the current system state, and waking up requires an energy-intensive boot process for systems re-initialization. Since the boot process requires thousands of processor cycles, hundreds of microseconds and hundreds of nanojoule of energy, it becomes limiting in an event-based application where quick wake up is required [8]. Therefore, a large proportion of power can be saved provided state is retained.

The two approaches for state retention are in-place and out-of-place, as shown in Figure 5.1 [9]. Out-of-place retention involves the movement of entire data to dedicated non-volatile memory. Dedicated off-chip memory results in large power dissipation in I/O pads where dedicated on-chip memory realized using FRAM or Flash suffers from high access energy and reliability issues [9]. Although the out-of-place retention scheme allows system to be completely switched off during idle/sleep mode, but it result in large energy and delay overhead during store and restore operation, especially from the register distributed across the processor which do not allow random access [6]. In-place state retention eliminates the overhead associated with data movement by substituting conventional flip-flops with State Retentive Flip-Flops (SRFF), which ensures quick wake up by reducing restoration time. In

conventional State Retentive Flip-Flop, data is preserved by additional data retention circuitry while the rest of the circuit is powered down to achieve lower power consumption [2], [10]–[14].

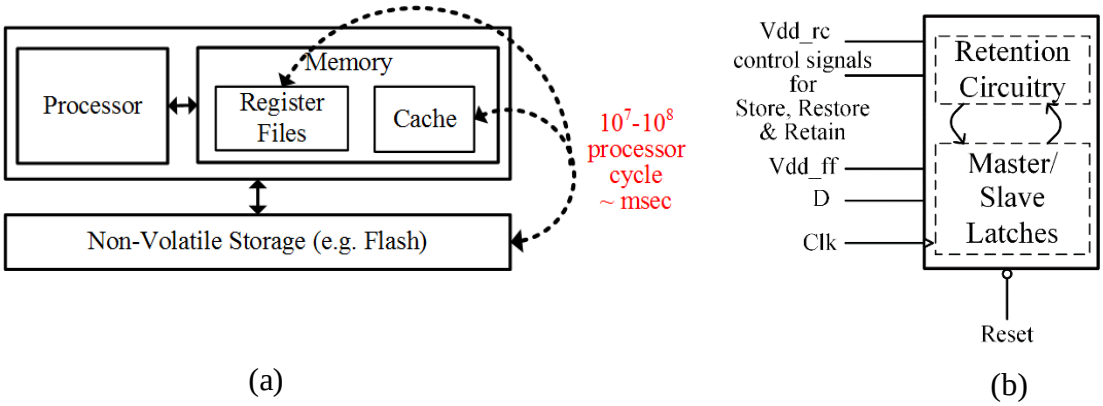


Figure 5.1: Different approaches to state retention (a) Out-of-place Retention b) In-place Retention

'Always ON' data retention circuitry still contributes to power dissipation which can be eliminated by integrating non-volatile memory elements with CMOS. Therefore, in this work, we modify the conventional volatile D flip-flop to incorporate non-volatility by using the STT-MTJ device, which eliminates the leakage power consumption. Data in flip-flop is stored into MTJ device before power down and restored to flip-flops to resume the operation from pre-standby state [15]. However, high power saving is achieved at the cost of little performance degradation as delays in the proposed hybrid D-FF are relatively greater than conventional D-FF. STT-MTJ have low write energies and latencies, CMOS compatibility, large endurance and long retention times compared to others non-volatile memory which makes it an ideal candidate for ultra-low-power applications with low-performance requirement [16][17].

5.2 Existing Stata Retention Flip-Flop (SRFF)

D Flip-Flop forms the major part of the control logic of a processor, where control logic is reported to consume 20% of the total processor's power [18]. In more advanced and complex architecture like superscalar architecture, a large number of DFFs are used, therefore, it is important to have energy efficient FF design to reduce the overall power dissipation. Power gating along with clock gating is one of the most common low-power technique employed which result in loss of system state [19]. Therefore, we need additional circuitry to preserve the content of flip-flop so that the output node will have the correct state after the sleep period.

Various low-power data retention circuits have been proposed, which reduce the leakage power consumption in standby mode and preserve the data state during the sleep period. Kitagata et al. [12] proposed a retentive flip-flop with dual-mode inverters that act as a schmitt trigger inverter during standby mode and a conventional inverter during normal/active mode. Whereas Kobayashi et al. [11] use low-voltage retentive operation mode during standby mode. It proposes a self-controllable voltage (SVL) block to adaptively change the voltage supply to the flip-flop, i.e., vdd during active mode and lower than vdd during standby mode. S. Mutoh [10], S. Shigemastu [2], H. Jiao [14], and Moreau et al. [12] uses an additional cross-coupled inverter pair to retain the state during idle mode. Furthermore, S. Mutoh [10], S. Shigemastu [2], H. Jiao [14] uses multi-threshold technique which uses both low V_{th} and high V_{th} transistors to obtain low leakages without compromising circuit speed [20]. We discuss the conventional state retentive flip-flop circuits proposed by S. Mutoh [10], S. Shigemastu [2] and H. Jiao [14] in the following sections:

5.2.1 Mutoh MT-CMOS Flip-Flop

5.2.1.1 Structure of mutoh MT-CMOS flip-flop

The state retentive MT-CMOS Flip-Flop, as shown in Figure 5.2, was first proposed by Mutoh [10], which could preserve the state of the master latch. All the transistors shown with a thick line in Figure 5.2 are high V_{th} transistors. The transistors in the critical path are replaced with low V_{th} transistors in order to increase the performance. Both Header (PMOS M1 & M3) and Footer (NMOS M2 & M4) sleep transistors are used to implement power gating, whereas OR gate is used to implement clock gating. Both sleep signal and clock signal are used to transition to sleep mode. The inverter I2 is the extra circuitry added for data retention. The design metric used for sizing all the transistors is to maintain the same propagation delay $t_{c\text{-}q}$ (Clock-to-Q delay) as conventional D Flip-Flop. Inverter in the non-critical path such as I2, I3, and I5 are sized small to reduce the area. The transmission gate TG2 (high V_th) is sized small to weaken the feedback path to avoid overwriting node N1 by N3 during the transparent stage. Inverter I3 should be large enough so that during hold state, leakage current through transmission gate TG1 (low V_th) will not affect the state of node N1. Wider sleep transistors are used to reduce the performance degradation of the flip-flop.

5.2.1.2 Operation of mutoh MT-CMOS flip-flop

During active mode of operation, sleep signal is asserted high which turns ON the sleep transistors, and Mutoh Flip-Flop works as conventional D Flip-Flop. During sleep mode

(when there are no data transitions) clock is asserted high by the OR gate while the sleep signal is pulled to gnd to turn OFF all the sleep transistors. Data at node N2 is retained by cross -coupled inverters I2 and I3. They are high V_{th} transistors that are always connected to the true power supply. The major drawback of this circuit scheme is the large area overhead due to sleep transistors. Mutoh FF uses a large number of locally distributed high V_{th} sleep transistors instead of single centralized sleep transistor. As leakage current is directly proportional to the width of the transistor, wider sleep transistor also results in large leakage power consumption [21].

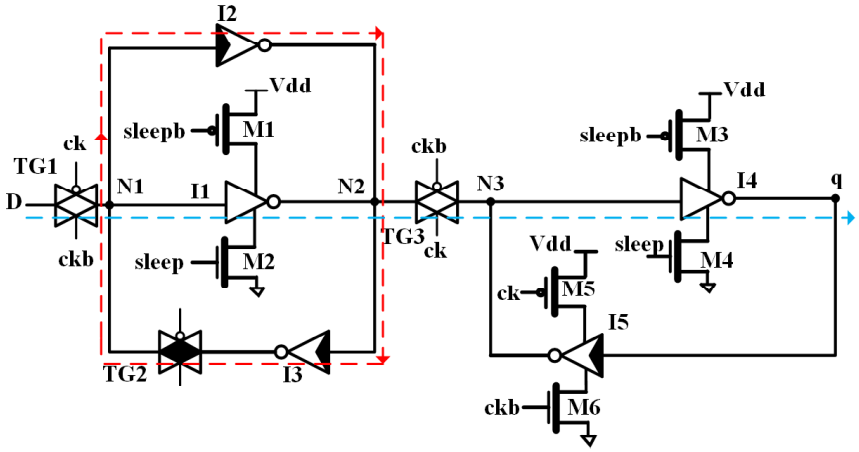


Figure 5.2: Mutoh MTCMOS State Retentive FF [14]

5.2.2 Balloon Flip-flop

5.2.2.1 Structure of balloon flip-flop

S. Shigemastu [2] proposed another MT-CMOS State Retentive Flip-Flop, which consists of additional data retention circuitry, a balloon circuit, and a switch to control data movement, as shown in Figure 5.3. Balloon circuit or retention cell consists of a transmission gate TG7 and cross-coupled inverters I5 and I6. The inverters I5 and I6 are made of high V_{th} transistors (shown with thick lines), which will always be connected to the supply rails. The transmission gate TG6 is made of high V_{th} transistors and acts as a switch that separates the retention cell from the node N3 of the main latch. The signals S1 and S2 control the reading and writing into the balloon circuit. A Sleep signal is used to control the operation of the sleep transistor. A centralized Footer (NMOS) is used to implement power gating, whereas AND gate is used to implement clock gating. All the transistors on the forward and feedback path are low V_{th} transistors, therefore, its clock-to-q delay is similar to low V_{th} D-FF. The balloon circuit is made up of high V_{th} transistor except for TG7. Since TG6 is OFF during active mode, node

N4 is floating. In order to avoid floating of node N4 during active period, TG7 is made low V_{th} so that the leakage currents will prevent the node N4 from floating.

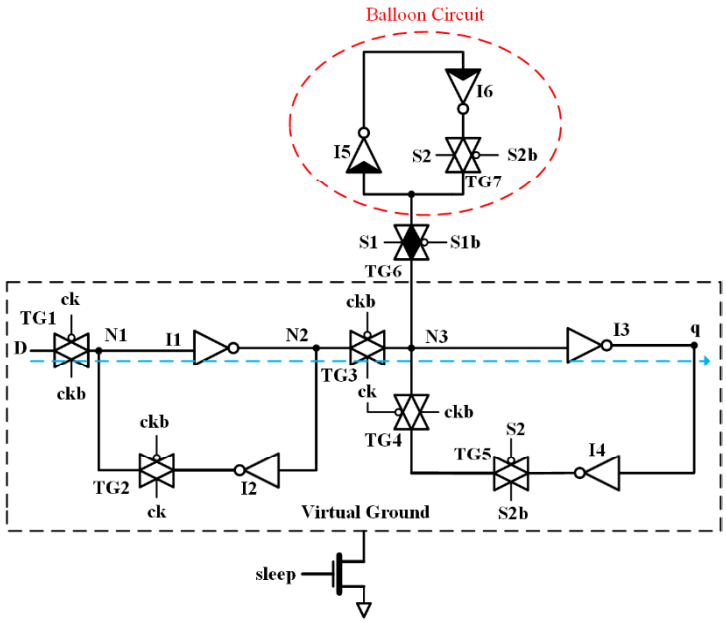


Figure 5.3: Balloon Flip-flop circuit

5.2.2.2 Operation of balloon flip-flop

Figure 5.4 (a) shows the four modes of operation: Active, Sleep-in, Sleep, Sleep-out, whereas values of control signals during these modes are illustrated by Figure 5.4 (b). In active mode, the balloon circuit is isolated from the main flip-flop. Transmission gate TG6 is turned OFF during the active period so as to reduce the capacitive load on the main circuit.

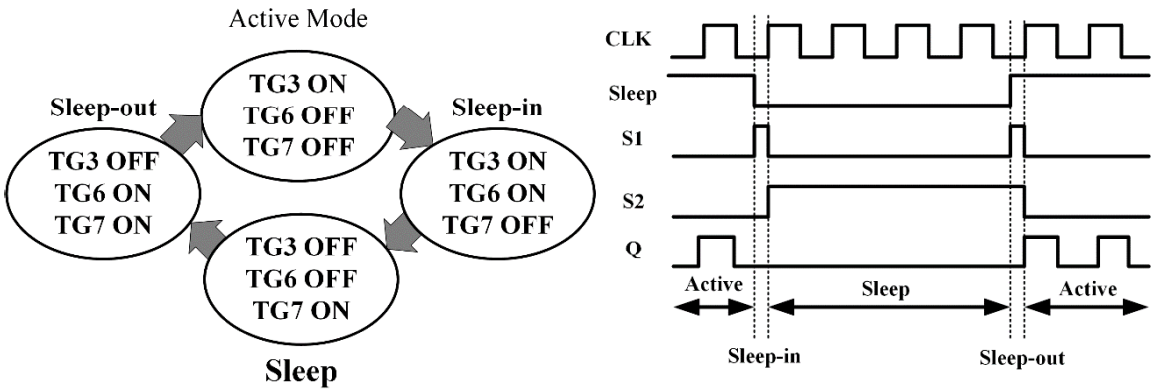


Figure 5.4: Operational mode and associated control signals for Balloon Flip-Flop

The sleep signal is asserted high so that the sleep transistor is turned ON and the circuit work as conventional D FF. Sleep-in mode corresponds to the transition mode between active and sleep mode, during which data at Node N3 moves to the balloon circuit. TG5 is turned off

during the sleep-in period so that the data at node N2 is not destroyed. In sleep mode, both sleep signal and clock are logic '0', and balloon circuits hold the data. Sleep-out mode is a transition mode between sleep mode and active mode in which data is transferred back to node N3. TG5 is turned OFF during the sleep-out period and, hence, the data stored in the memory cell is not destroyed by I4. The main drawback of balloon flip-flop is the increased complexity of signaling and large data restoration times.

5.2.3 Memory Flip-flop

5.2.3.1 Structure of memory flip-flop

Kursun and Jiao [14] proposed MT-CMOS state retentive flip-flop consisting of a memory cell connected to the slave stage through the two pass transistors M1 and M2, as shown in Figure 5.5. The memory cell consists of cross-coupled inverters (I4 & I5) and a transmission gate (TG4). It is similar to the 6T SRAM structure.

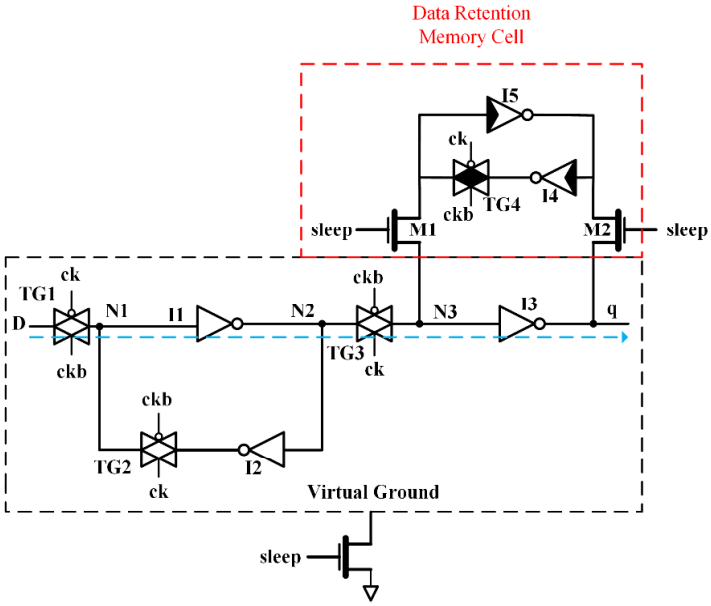


Figure 5.5: Memory Flip-Flop

A centralized NMOS transistor is used as a sleep transistor. The control signal used for state transition between sleep and active mode is only a single sleep signal. Hence, the complexity of signaling is much less compared to the balloon flip-flop. Another implementation shown in Figure 5.6, replaces pass transistor M1 by a transmission gate TG4 to avoid degradation of logic high through nmos pass transistor during the restore operation. Memory Flip-Flop forward and feedback paths are made up of low V_{th} transistors so as to maintain clock-to-q delay same as conventional D-FF. Data retention cell is made up of high V_{th} transistors to reduce the leakage during standby mode and since they do not form the critical path, their

high V_{th} does not affect the flip-flop speed.

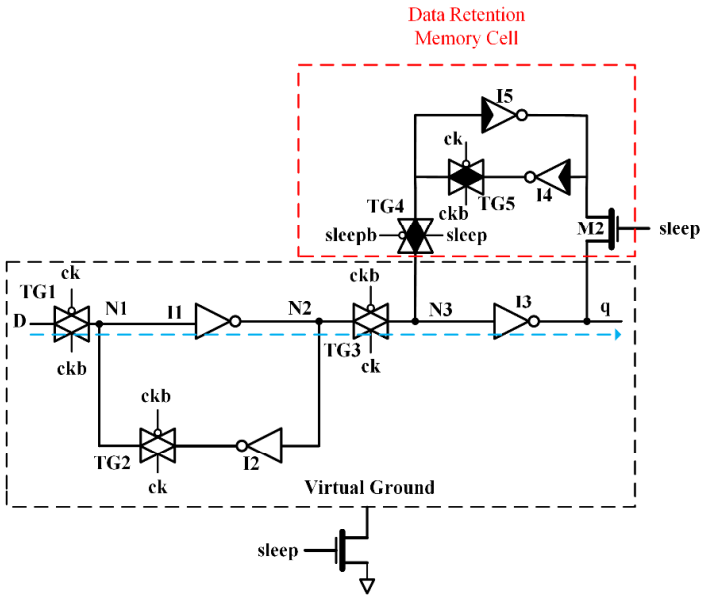


Figure 5.6: Memory TG Flip-Flop

5.3 Proposed State Retentive Hybrid D Flip-Flop

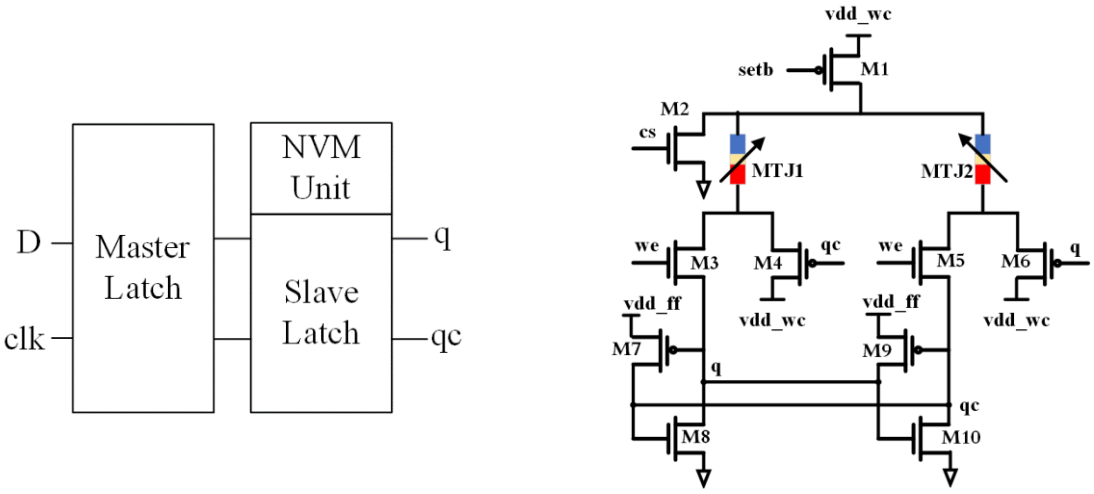
Although the above-mentioned state retentive circuits are able to effectively reduce the power consumption during standby mode while retaining the state yet zero power consumption is not possible due to 'Always ON' circuitry used in these FF designs. Zero leakage power during standby is possible by incorporating non-volatile element such as MTJ, which can retain the state without power supply. Therefore, we present two new circuit designs for state retentive hybrid flip-flop using magnetic tunnel junction (MTJ) device which can be completely switching OFF during idle mode while preserving the state in the MTJs.

5.3.1 Proposed State Retentive Hybrid Flip-Flop Circuit-I (HFF-I)

5.3.1.1 Structure of hybrid flip-flop (HFF-I)

The state retentive hybrid flip-flop design presented in this work is illustrated in Figure 5.7 (a). The hybrid FF designed with circuit-I approach comprises conventional master-slave flip-flop with non-volatility incorporated by NVM unit. NVM unit is connected to the cross-coupled inverter (M7-M10) of the slave latch, as shown in Figure 5.7 (b). It comprises two STT-MTJ devices (MTJ1 & MTJ2), two isolation transistors (M3 & M5) and rest of the circuit is used for selecting current polarity. The two MTJ devices are present in complementary form where MTJ1/MTJ2 in LRS/HRS represents logic '0' and MTJ1/MTJ2 in HRS/LRS represents

logic ‘1’.



(a) (b)

Figure 5.7: (a) Hybrid D Flip-Flop (b) NVM unit of FF-I connected to cross-coupled inverter of slave latch

5.3.1.2 Operational modes of HFF-I

The proposed hybrid FF-I has three modes of operation: Normal, Backup and Restore, as shown in Figure 5.8. The detail of each operation is presented in the following sub-sections.

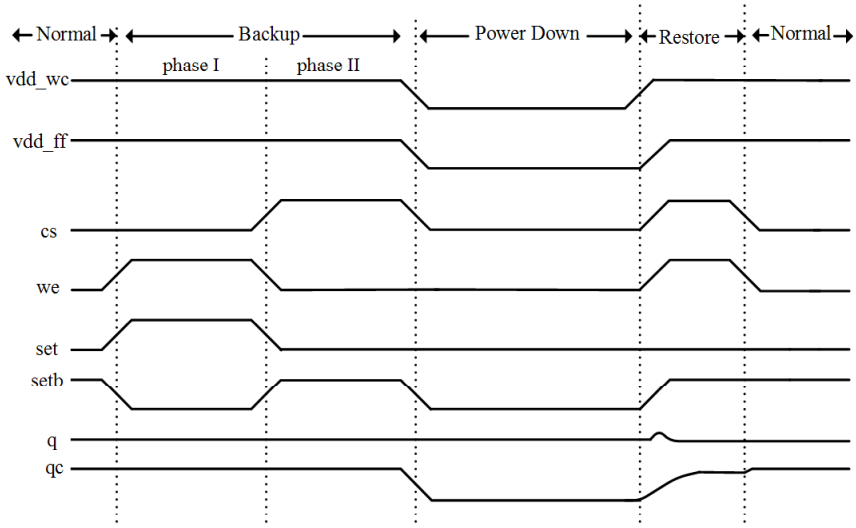


Figure 5.8: Operational waveform of hybrid Flip-Flop (HFF-I)

5.3.1.2.1 Normal operation

In the normal mode of operation, isolation transistors (M3 & M5) are turned OFF (as shown in Figure 5.9 by the shaded portion) to disconnect the NVM unit from the slave latch and HFF-I works as standard flip-flop.

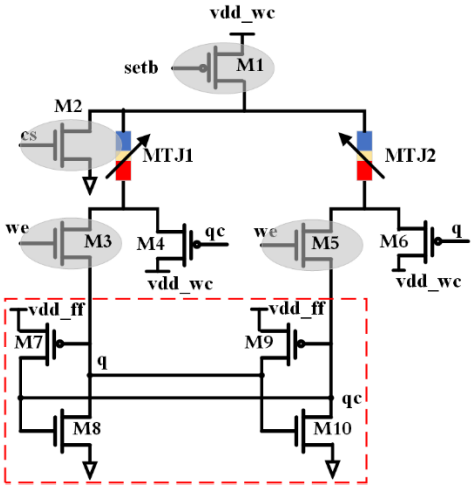
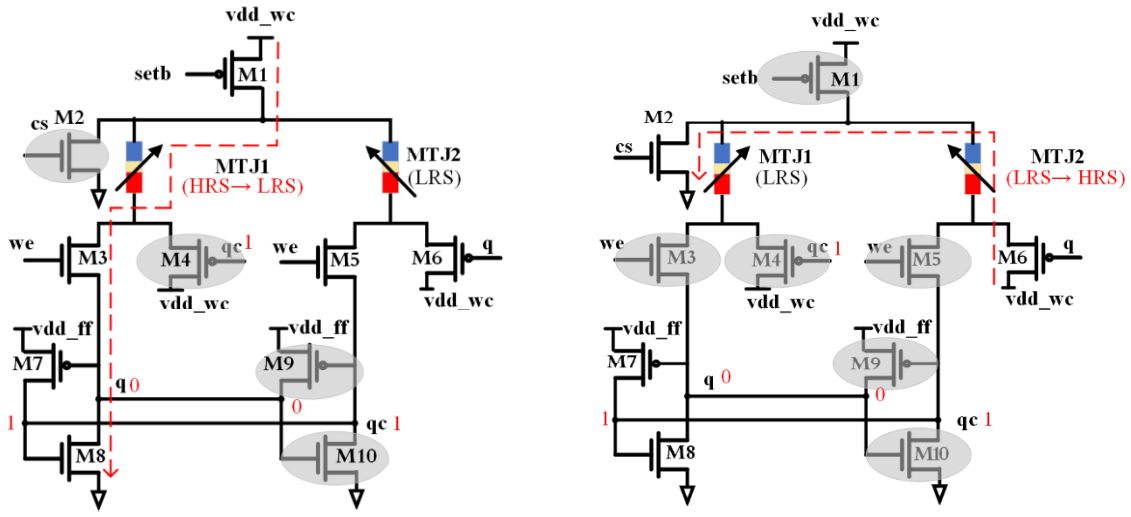


Figure 5.9: Proposed Hybrid Flip-Flop (HFF-I) in its normal mode

5.3.1.2.2 Backup operation

Figure 5.10 (a) presents phase I of the backup operation. At the start of the backup operation control signal (we=1 and setb=0) turns ON the isolation transistors and M1 thereby, connecting nodes (q & qc) with the MTJs (MTJ1 & MTJ2). The selection path M1-MTJ1 or M1-MTJ2 is determined by the value stored in q & qc.



(a) (b)

Figure 5.10: Backup operation of HFF-I circuit (a) Phase I of backup operation of HFF-I circuit (b) Phase II of backup operation of HFF-I circuit

A current flow through M1-MTJ1-M3-M8 when q/qc=0/1, and if the MTJ1 is in HRS, it is switched to LRS. On the other hand, a current flow through MTJ2 is prevented by maintaining same voltage across its terminals. Figure 5.10 (b) presents phase II of the backup operation, which starts by setting the control signal (cs) to logic high and pulling the control signals we

(write enable) and set to ground. Similar to phase I operation, the selection path M6-MTJ2 or M4-MTJ1 is determined by the nodes q & qc values. A current flow through M6-MTJ2-M2 when qc/q=1/0, and if MTJ2 is in LRS it is switched to HRS.

5.3.1.2.3 Restore operation

In restore mode, the application of control signals (we=1 and cs=1) forms a current divider path in the circuit. Current from M4 (M6) flows through two branches; MTJ1-M2 (MTJ2-M2) and M3-M8 (M5-M10), where the MTJ resistance state determines the magnitude of the current. If MTJ is in LRS, as MTJ1 in Figure 5.11, a large current passes through the MTJ1 and, a small dc current passes through M3-M8 resulting in a lower voltage at node q whereas, if MTJ is in HRS as MTJ2 in Figure 5.11, a small current passes through the MTJ2, and a large current passes through M5-M10 resulting in a large voltage at qc. With control signal write enable (we) pulled to gnd, nodes q & qc are brought to their full swing by cross-coupled inverter.

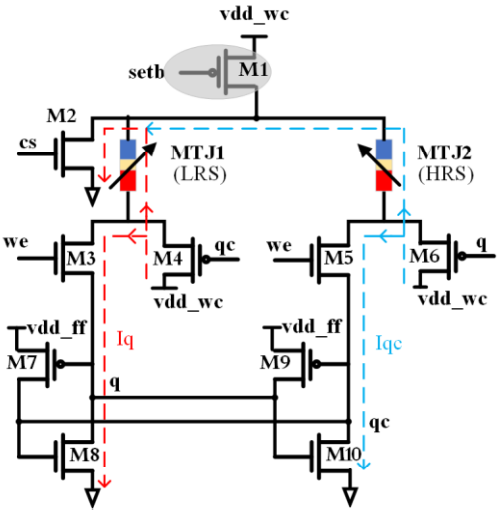


Figure 5.11: Restore operation of proposed hybrid flip-flop (HFF-I)

The above discussed state retentive hybrid flip-flop design is successful in achieving zero leakage power during idle mode, but a large number of control signals and their timing constraints increases the system complexity. Additionally, restore operation in hybrid flip-flop HFF-I depends on node voltage (q & qc). If the node voltages are not completely discharged during standby mode, any residual voltage will affect the restore operation. Therefore, another design of state retentive hybrid flip-flop (HFF-II) is presented, which uses a single control signal, and it has an additional advantage of performing the backup operation in a single step. Also, hybrid flip-flop HFF-II eliminates the dependency of restore operation

on node values by equalizing the nodes before the restore operation starts.

5.3.2 Proposed State Retentive Hybrid Flip-Flop Circuit-II (HFF-II)

5.3.2.1 Structure of hybrid FF Circuit-II (HFF-II)

Another hybrid flip-flop design is presented in Figure 5.12, which comprises conventional master-slave flip-flop with NVM unit. Its NVM unit consists of two isolation transistors (M5 & M6), two MTJs (MTJ1 & MTJ2), two NMOS (M2 & M3) and two PMOS (M1 & M4) pass transistor to determine the direction of current flowing through the MTJs. It also consists of equalization transistors (M11) between nodes q and qc which equalizes the node voltages when turned ON.

5.3.2.2 Operational modes of HFF-II

The proposed state retentive hybrid flip-flop HFF-II works in three operational modes as shown in Figure 5.13, Normal, Backup and Restore. The details of each operational modes are presented in the following sub-section.

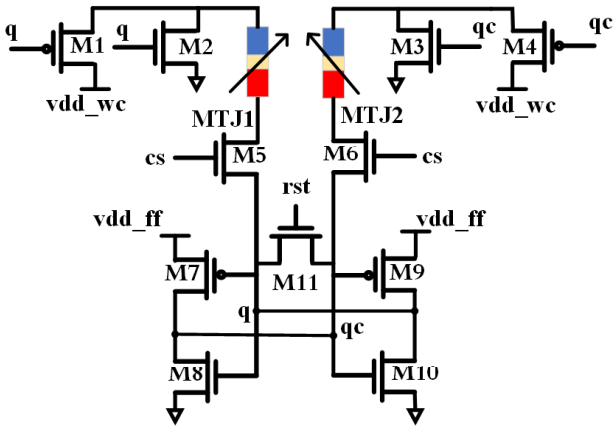


Figure 5.12: NVM unit of HFF-II connected to cross-coupled inverter of slave latch

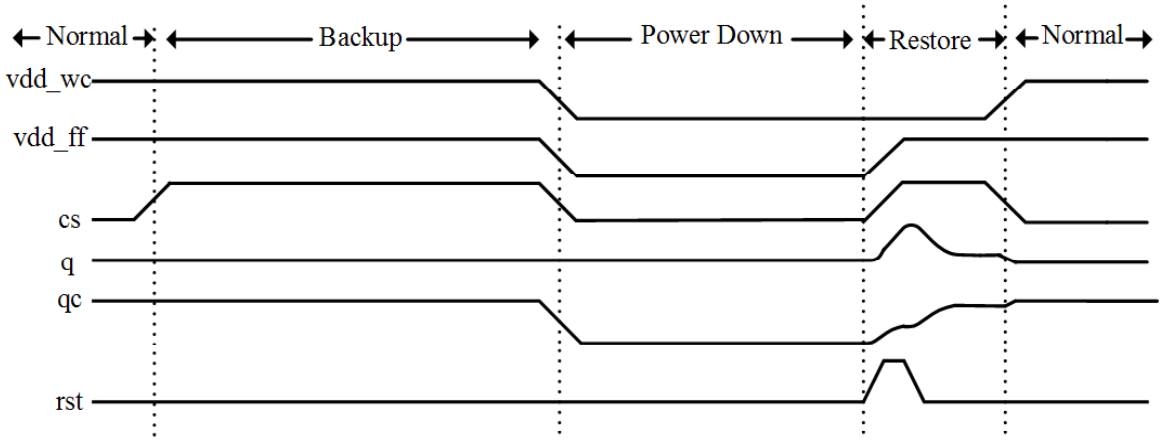


Figure 5.13: Operational Waveform of hybrid Flip-flop FF-II

5.3.2.2.1 Normal operation

In normal mode of operation, control signal cs is pulled to gnd thereby turning OFF the isolation transistors and disconnecting NVM unit from the main latch as shown in Figure 5.14. Control signal rst is also asserted low to disconnect q and qc therefore M7-M10 works as conventional cross-coupled inverter.

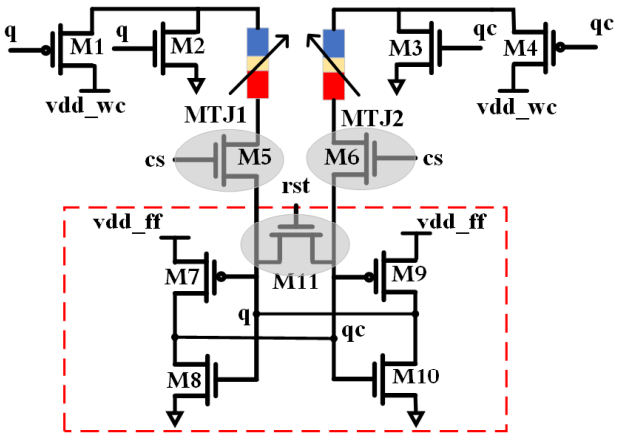


Figure 5.14: Normal mode of hybrid FF-II

5.3.2.2.2 Backup operation

Figure 5.15 presents the backup operation of hybrid flip-flop HFF-II circuit. It begins with control signal (cs) asserted high to connect MTJs to latch internal nodes while control signal (rst) remaining logic low. Direction of current through the MTJs is determined by the voltage value present at the nodes. If the node stores logic '0' (q=0) current from the PMOS pass transistor (M1) flows through MTJ (MTJ1) and the node (q) resulting in MTJ (MTJ1) switching from HRS→LRS whereas if the node stores logic '1' (qc=1) current from the node (qc) flows through MTJ (MTJ2) and NMOS pass transistor (M3) resulting in MTJ (MTJ2) switching from LRS→HRS.

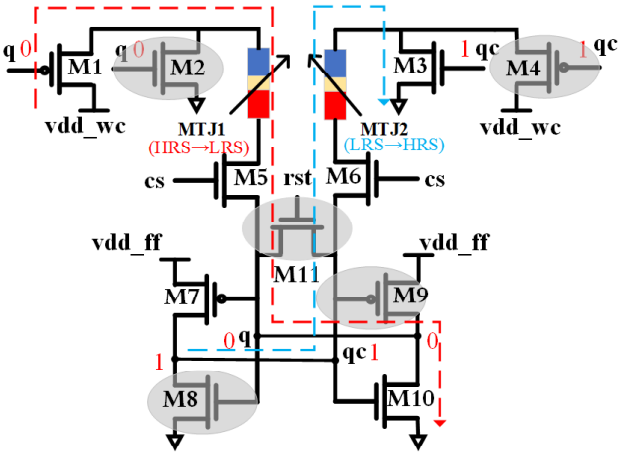


Figure 5.15: Backup operation of hybrid FF-II

5.3.2.2.3 Restore operation

In the restore mode, application of control signals (cs=1 & rst=1) enables q & qc to have differential discharge current flowing through MTJ1 (Iq) and MTJ2 (Iqc) as shown in Figure 5.16. The LRS (HRS) discharge path allows larger (smaller) current (Iq/Iqc) resulting in lower (higher) node voltage at q & qc which are brought to their full swing by cross-coupled inverter action.

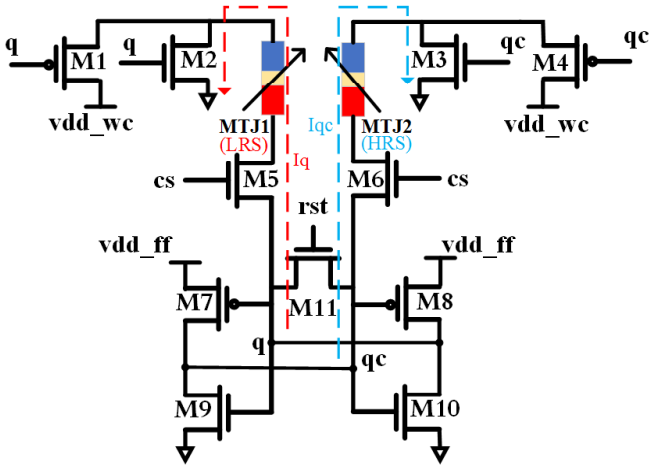


Figure 5.16: Restore operation of HFF-II

5.4 Simulation Result

To evaluate the performance of the proposed state retentive hybrid flip-flop we perform extensive simulations using SPICE simulator. The flip-flop circuits are designed using the CMOS FinFET and FD-SOI technology. All the structures are optimized in terms of speed and power. To achieve the same performance the clock frequency is fixed at 100MHz, and the circuit is operated with 10% duty cycle. Rise and fall times of all signals are also fixed to 100psec. The data stability, power dissipation and delay of different flip-flops are presented. The test circuit for simulation are presented in Figure 5.17. Methods for calculating power dissipation and propagation delay is same as described by Vlamidir [24]. Test Bench helps in realizing a realistic sequential circuit with buffer acting as clock and data signal load. Capacitive load at data and output is used for simulating fan out degradation.

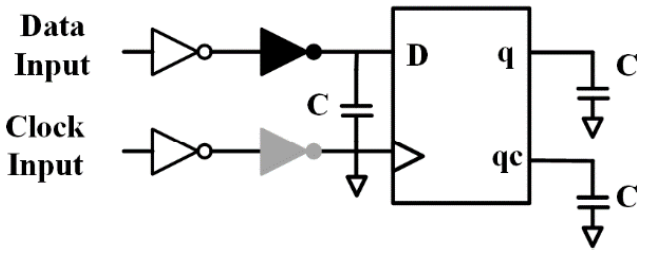


Figure 5.17: Test circuit for analyzing hybrid flip-flop

Power consumption is measured as given by equation (5.1) where V_{dd} is the power supply voltage and I_{dd} is the current through the power supply.

$$P = \frac{1}{T}\int_T V_{dd} I_{dd} \tag{5.1}$$

The total power consumption during active mode is due to clock, data and flip-flop itself. Local power dissipated by clock signal is measured by the portion of power dissipation by grey inverter driving (Figure 5.17) the input of latch. Similarly, local data power is portion of power dissipation by black inverter (Figure 5.17). Internal power dissipated by flip-flop also includes switching power by due to output capacitive load of FO4. To calculate only the portion of power dissipation on switching data/clock input capacitance power due to internal capacitance of buffer inverter is subtracted from the local clock/data power measured earlier. All the power measurement is conducted for data sequence with switching activity α varying from 0 to 1. Propagation Delay (t_{c-q}) calculation is performed in accordance with definition as stated by Unger and Tan [25]. It refers to time interval between clock edge and output q edge assuming that input D appears before clock edge to avoid any set up time violation.

5.4.1 Data recovery in various flip-flops

With implementation of power gating alone on standard D Flip-Flop data can be retained by flip-flop for period of few microseconds but if the standby duration is longer than few microseconds, state retentive flip-flops are required to preserve the data. Successful retention and recovery of data in the state retentive flip-flops are verified by the simulation results. Table 5.1, illustrates the data restoration times of each flip-flop design.

TABLE 5.1: DATA RESTORATION TIMES OF DIFFERENT STATE RETENTIVE FLIP-FLOP DESIGN

Data Restoration Times(psec)	
Mutoh Flip-Flop	74.6
Balloon Flip-flop	216
Memory Flip-Flop	53
Memory TG Flip-Flop	70
HFF-I	53.5
HFF-II	200 (equalization pulse duration) + 126

Memory FF requires very less time to restore the data. With sleep signal pulled to high, the pass transistors M1 and M2 in memory flip-flop turns ON, thereby quickly transferring data

stored in memory cell to N3 and Q. Mutoh FF design store the state of master therefore requires extra time to pass value of node N2 to Q. Balloon FF takes very long time when compared to other state retentive flip-flop. It is due to the state transition modes (sleep-in and sleep-out) occurring in between active and sleep mode which increases the storage as well as restoration times. HFF-II takes the largest data restoration time due to node equalization process. The duration of equalization pulse (rst signal) is taken as 200psec.

5.4.2 Power consumption by various flip-flops

The active and sleep mode power consumption of different flip-flops is analyzed in this sub-section. The simulations are done with a supply voltage of 0.9V and clock frequency of 100MHz. The total power consumption during active mode and leakage power dissipation during sleep/standby mode is measured at 27°C temperature. Table 5.2 illustrates the total power consumption during active mode.

TABLE 5.2: TOTAL POWER CONSUMPTION DURING ACTIVE MODE BY DIFFERENT STATE RETENTIVE FLIP-FLOPS

Total power consumption during active mode (uW)			
	CMOS	**FinFET**	**FD-SOI**
Mutoh FF	0.58	0.13	0.25
Balloon FF	0.88	0.10	0.248
Memory FF	0.94	0.11	0.27
Memory TG FF	0.69	0.10	0.26
HFF-I	2.8	1.4	0.95
HFF-II	1.5	0.70	0.813

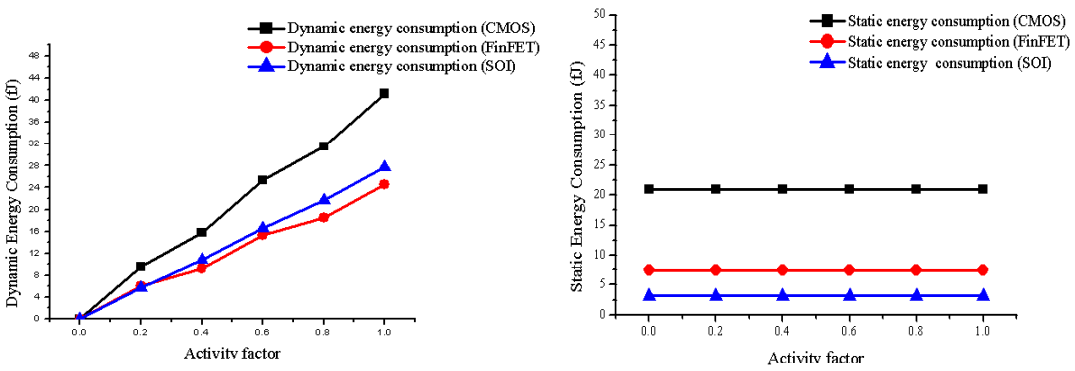
The Mutoh flip-flop design uses only one extra transistor (I2 in Figure 5.2) for data retention whereas the balloon circuit uses two transmission gates (TG6 & TG7) and a cross coupled inverter (I5 & I6 in Figure 5.3) therefore, power consumption of balloon circuit is 34% more than Mutoh FF. The Memory FF consumes the highest active mode power. This is because of the memory cell which is not isolated from the flip-flop during active mode. The increased parasitic capacitance leads to more power consumption during the active mode. The Memory FF power consumption during active mode increases by 38.2% and 6.3% when compared to Mutoh FF and Balloon FF respectively. Both hybrid flip-flops consume more power than conventional state retentive flip-flop due to NVM unit attached to the slave latch. The power consumption was evaluated for FinFET and FDSOI technology also. It was seen that both the

technology consumed lesser power compared to MOSFET technology. Large power saving is observed in conventional State Retentive Flip-Flops (77-88%) whereas only 50% power saving is observed for hybrid flip flop. Because in hybrid flip-flop HFF- I & II implementation with FinFET and FD-SOI, MTJ dimensions are not scaled therefore its switching current requirement remains same. Large size transistors are therefore used to maintain high current values.

To further analyze the energy consumption of proposed state retentive hybrid flip-flop during active mode, the HFF-I & HFF-II is simulated at different activity factor. Table 5.3 and 5.4 tabulates the static and dynamic energy consumption of HFF-I & HFF-II circuits for activity factor ranging from 0 to 1.

TABLE 5.3: ENERGY CONSUMPTION DURING ACTIVE MODE FOR HYBRID FLIP-FLOP (HFF-I) WITH RESPECT TO DIFFERENT ACTIVITY FACTOR

HFF-I						
Activity Factor	**Dynamic energy dissipation (fJ)**			**Static energy dissipation (fJ)**		
	CMOS	FinFET	FD-SOI	CMOS	FinFET	FD-SOI
0	0	0	0	20.95	7.43	3.18
0.2	9.6	6.05	5.8	20.95	7.43	3.18
0.4	15.79	9.24	10.82	20.95	7.43	3.18
0.6	25.4	15.29	16.62	20.95	7.43	3.18
0.8	31.6	18.48	21.76	20.95	7.43	3.18
1	41.2	24.53	27.72	20.95	7.43	3.18



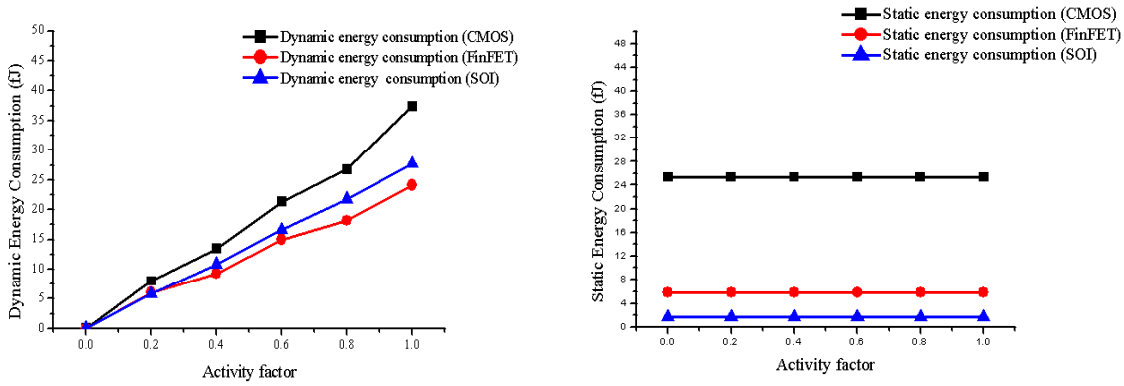
(a) (b)

Figure 5.18: (a) Dynamic and (b) Static energy consumption for the proposed hybrid flip-flop HFF-I

From Figure 5.18 and 5.19, it can be observed that the dynamic energy dissipation increases with increasing activity factor while static energy consumption remains almost same.

TABLE 5.4: ENERGY CONSUMPTION DURING ACTIVE MODE FOR HYBRID FLIP-FLOP (HFF-II) WITH RESPECT TO DIFFERENT ACTIVITY FACTOR

HFF-II						
Activity Factor	**Dynamic energy dissipation (fJ)**			**Static energy dissipation (fJ)**		
	CMOS	FinFET	FD-SOI	CMOS	FinFET	FD-SOI
0	0	0	0	25.4	5.9	1.82
0.2	8	5.9	5.8	25.4	5.9	1.82
0.4	13.4	9.24	11.6	25.4	5.9	1.82
0.6	21.3	15	17.4	25.4	5.9	1.82
0.8	26.8	18.2	23.2	25.4	5.9	1.82
1	34.7	24.1	29	25.4	5.9	1.82



(a) (b)

Figure 5.19: (a) Dynamic and (b) Static energy consumption for the proposed hybrid flip-flop HFF-II

Table 5.5 shows the leakage power consumption during sleep mode for different data retention flip-flops. For MOSFET technology the Mutoh FF consumes more leakage power due to the large size localized sleep transistors. The leakage power reduced by 70.9% for Balloon FF when compared to Mutoh FF. The leakage power also reduced by 5% compared to Memory FF. HFF - I & II have zero power consumption during standby mode as complete circuit is turned OFF. FinFETs and FD-SOI have leakage current one order lower than MOSFET, therefore the significant reduction in leakage power is observed.

TABLE 5.5: LEAKAGE POWER CONSUMPTION DURING SLEEP MODE BY DIFFERENT STATE RETENTIVE FLIP-FLOPS

Leakage power during standby mode (nW)			
	CMOS	**FinFET**	**FD-SOI**
Mutoh FF	196	1.412	0.6
Balloon FF	57	0.96	0.613
Memory FF	76	1.2	1.26
Memory TG FF	77	1.03	1.22
HFF-I	Zero because circuit is powered-down in standby mode		
HFF-II			

5.4.3 Delay of various flip-flops

The propagation delay of the different data retention scheme was analyzed and is tabulated in Table 5.6. Propagation is all the conventional state retentive flip-flop is maintained the same by different transistor sizing. Propagation delays of proposed hybrid flip-flops are increased when compared to conventional SRFF due to additional NVM unit.

TABLE 5.6: PROPAGATION DELAY CALCULATED FOR DIFFERENT STATE RETENTIVE FLIP-FLOPS

Propagation Delays (psec)	
Mutoh FF	18.5
Balloon FF	18.5
Memory FF	18
Memory TG FF	19.5
HFF-I	52
HFF-II	42

5.4.4 Comparison with state-of-the-art hybrid flip-flop

The proposed state retentive hybrid flip-flops are compared with existing CMOS based state retentive FF as well as hybrid FF based on emerging non-volatile devices such as non-volatile ferroelectric (FeRAM) and resistive device (RRAM). The Table 5.7 tabulate this comparison results of proposed work with state-of-the-art hybrid FF. Similar to Balloon and Memory flip-flop state saving technique, Moreau et al. [12] proposes a retentive flip-flop which uses an additional cross-coupled inverter pair controlled by clock gated signal.

TABLE 5.7: COMPARISON OF PROPOSED STATE RETENTIVE HYBRID FF WITH STATE-OF-ART STATE RETENTIVE FF

	Zero-Standby Power Dissipation	Store Time of NVE	Store Energy of NVE*	Area Overhead	CMOS Technology	Retention Technique
Moreau et al. [12]	No	-	-	6T	65nm	Retention Feedback
Kitagata et al. [13]	No	-	-	8T	65nm	Dual Mode Inverter
Kobayas-hi et al. [11]	No	-	-	8T	65nm	Dual Mode Inverter
Qazi et al. [26]	Yes	>100ns	~1pJ/bit	$22T+2C_F$	130nm	FeC
Bartling et al. [27]	Yes	>100ns	~1pJ/bit	$18T+4C_F$	130nm	FeC
Lee et al. [6]	Yes	<50ns	~100pJ/bit	15T+2R	65nm	Memristor
Chien et al. [28]	Yes	<50ns	~100pJ/bit	8T+2R	90nm	Memristor
This Work	Yes	<10ns	~0.02pJ/bit	7T+2MTJ	45nm	MTJ

* Store energy of the Non-Volatile Element (NVE): The amount of energy required to write a single bit into the embedded non-volatile element (FeC, Memristor or MTJ)

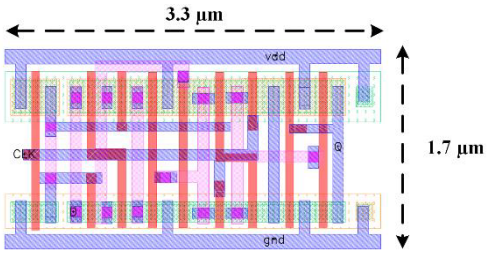
Since the circuit is only clock gated not power gated during standby periods, there is reduction in only dynamic power dissipation. Whereas Kitagata et al. [13] and Kobayashi et al. [11] uses power gating (PG) technique to reduce the static power dissipation and dynamic power dissipation during the standby mode. To prevent the loss of state during standby mode, Kitagata et al. [13] proposed a retentive flip-flop which have dual mode inverters that act as Schmitt trigger inverter during standby mode and conventional inverter during normal/active mode. Whereas, Kobayashi et al. [11] uses low voltage retentive operation mode during standby mode. It proposes a self-controllable voltage (SVL) block to adaptively change the voltage supply to the flip-flop i.e. Vdd during active mode and lower than Vdd during standby mode. However, all the aforementioned circuit are still not able to achieve zero standby power dissipation. Therefore, emerging non-volatile devices are used to completely eliminate the standby power dissipation. Qazi et al. [26] and Bartling et al. [27] proposed a hybrid flip-flip using non-volatile ferroelectric capcitor (FeC). The ferroelectric capacitor is one of the emerging non-volatile devices which uses remanent polarization of a ferroelectric thin film to store the data. However, it suffers from high operational voltage (>5 V), low write endurance (10^4 -10^5 cycles) and signal degradation upon scaling. Lee et al. [6] and Chien et al. [28] proposes a hybrid flip-flop based on emerging memristor device. The emerging memristor element has very low write endurance (10^6–10^9 cycles) which limits their usage in normally off applications.

With comprehensive consideration, STT-MTJ device seems to be an ideal candidate for low power applications such as IoT due to its low write currents (in uA range), greater writing endurance (>10^{12}), fast switching times (<10 ns) and compatibility with CMOS fabrication. The proposed MTJ device-based state retentive hybrid flip-flop is also compared with existing MTJ device-based hybrid flip-flop. The existing hybrid FF includes conventional CMOS master and hybrid slave latch, consisting of MTJ device and its write and read circuitry [29]–[32]. On similar concept, Jung et al. [32] designed a master slave D flip-flop with MTJ inserted in slave configuration. The circuit requires separate write circuit and pre-charge sense amplifier (PCSA) for storing and restoring the value from the MTJ. The post layout comparison results are tabulated in Table 5.8. The backup energy of Jung FF and hybrid FF-II are almost similar; however, the backup energy of hybrid FF-I is significantly higher than FF-II and Jung FF. This is because of two phase backup operation in which time required to store values in MTJs is twice the FF-I and Jung FF. The layout of proposed hybrid FF-I and FF-II is presented in Figure 5.20.

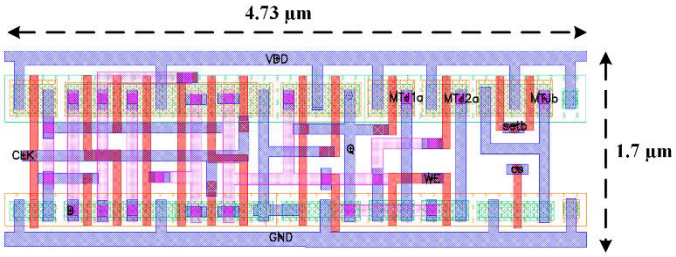
TABLE 5.8: COMPARISON OF PROPOSED HYBRID FLIP-FLOPS WITH EXISTING MTJ BASED HYBRID FLIP-FLOP

	Backup Energy (fJ)	Restore Energy (fJ)	Energy consumption during active mode		Area Overhead	Area (um^2)
			Dynamic Energy (fJ)	Static Energy (fJ)		
Jung FF [32]	579	33	38	43.94	25T + 2MTJ	32.1
HFF-I	893	27	27.18	29.94	6T + 2MTJ	8.041
HFF-II	613	24.5	30.3	28.35	7T + 2MTJ	7.82

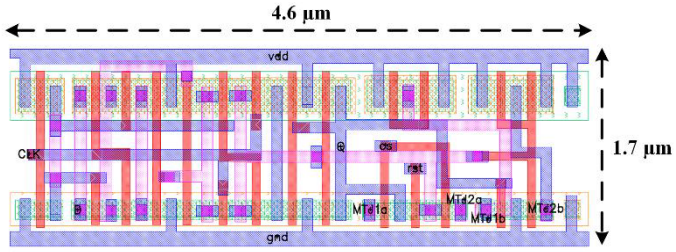
The total area for the proposed HFF-I is 8.041 um^2 (4.73um x 1.7um) and for the proposed HFF-II is 7.82 um^2 (4.6um x 1.7um) which is approximately 30% and 28% higher than the conventional D Flip-Flop. However, the area for the Jung FF is significantly higher than the HFF-I and HFF-II due to separate MTJ read and write circuitry. Because of separate MTJ read and write circuitry the energy consumption during active mode for Jung FF is also higher than HFF-I and HFF-II. Therefore, the proposed circuit is able to achieve lower power consumption during the active mode with minimum area overhead by eliminating the need of separate MTJ read and write circuitry.



(a)



(b)



(c)

Figure 5.20: Layout of (a) D Flip-Flop (b) Proposed hybrid HFF-I (c) Proposed hybrid HFF-II

5.5 Conclusion

Energy-overhead of existing state retentive flip-flop during long idle periods has to be decreased to improve the energy-efficiency of the batteryless devices. Therefore, in this work, we propose hybrid state retentive flip-flop using MTJ device as a potential candidate for ultra-low power application that offers zero leakage standby mode and quick wake ups. Reboot time of system is reduced from milliseconds to picoseconds by backing up data in MTJ device which ensures quick wake up. The proposed hybrid flip-flops (HFF-I & HFF-II) show successful data retrieval after wake up with data restoration time similar to conventional state retentive flip-flops. The 66-69% of active power overhead, 55-64% of delay overhead, and MTJ store/restore overhead for hybrid flip-flop can be compensated if the duration of standby mode exceeds few hundred of microseconds. Additional power saving is obtained by replacing CMOS technology with FinFETs and FD-SOI which results in 70-80% reduction of total power consumption. The proposed MTJ based hybrid flip-flops have lower power consumption, high write endurance and faster switching times when compared to hybrid flip-flop based on emerging ferroelectric capacitor and memristor elements. Also, the proposed circuit is able to achieve 25% lower dynamic power consumption and 40% lower static power consumption during the active mode with minimum area overhead compared to existing MTJ based hybrid flip-flop by eliminating the need of separate MTJ read and write circuitry.

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