CHAPTER 6

HYBRID ASYNCHRONOUS CIRCUIT DESIGN

6.1 Introduction

With the increasing demand for wearable devices, smart sensor nodes, and the emerging Internet of Things (IoT) systems in health-care, structural health monitoring & wireless sensor networks, it is expected that the number of IoT based systems will grow to 50 billion by 2025 [1]-[3]. Most of the current IoT systems are powered by batteries, which require frequent recharging or replacement. Researchers are working on cutting down the power requirement for IoT devices as the battery capacity is another bottleneck. One possible alternative to the battery capacity is harvesting energy from ambient sources. Recent studies on energy harvesting applications have proven to be quite promising for ultra-low power systems [4]-[6]. However, if the power supply goes off due to the non-availability of harvested power, data is not retained for the volatile circuits, and computation has to be re-initialized. Since power is a scarce commodity and system re-initialization is an energy-intensive process, the current design techniques are driven toward implementing a circuit with minimum energy possible and fair reliability.

In addition, the drastically increasing dynamic power dissipation due to the globally distributed clock in the state-of-the-art synchronous system is posing a serious challenge for the IoT application to meet the strong constraints of power consumption. Moreover, the clock distribution over a large number of blocks is becoming more and more challenging to manage. The fine-tuning of clock skew and jitter to ensure timing closure and proper functionality is also difficult to achieve at lower technology nodes. Furthermore, in such designs, while the worst-case delay path is computing, all the other paths remain active and consume static power. Since IoT systems stay idle for a long time, they consume a large amount of static power.

Addressing the above-mentioned challenges, in this work, we propose to combine the asynchronous architecture with the emerging non-volatile magnetic technology. An asynchronous circuit eliminates the clock tree, hence achieve a significant reduction in power consumption [7][8]. Moreover, it employs the event-based behavior and consumes power only if an event needs to be processed. Hence, the parts active consume energy while the rest of

the circuit automatically resort to standby mode, which further lowers the total power consumption [9]. Additionally, we adopt a re-initialization-free protocol to provide robustness against the unstable environment by making every localized memory element non-volatile using the emerging magnetic technologies, resulting in low-energy and low-latency wake-up. Figure 6.1 compares the percentage of computation done against power failures for Type I processor with volatile memory architecture and Type II processor with non-volatile memory architecture. Both the processors compute equally before the occurrence of the first power failure. However, sudden power failure causes the Type I processor to lose its state and begin from the initial point once power is restored, while the Type II processors have its state retained in local non-volatile elements and can resume from the point of interruption after power restoration.

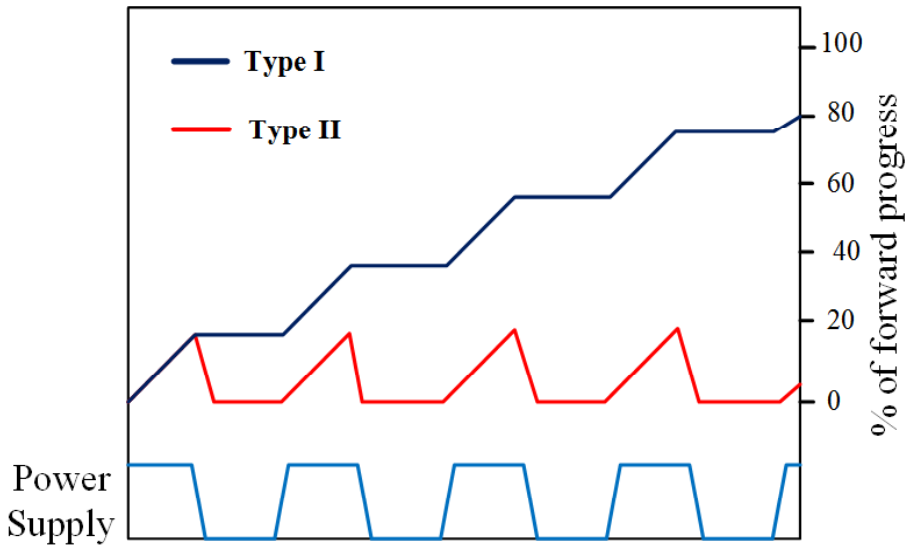

Figure 6.1: Percentage of computation done by different processors against power failures

This work aims to design a low-power asynchronous circuit with data retention capability to provide resilience against sudden power failures. Therefore, we first develop a non-volatile hybrid basic asynchronous block such as c-element by incorporating the emerging magnetic device into the volatile conventional c-element. Various volatile c-element designs are explored and compared in terms of power consumption and delay to select the best possible candidate for the design of hybrid c-element. The non-volatile hybrid c-element is developed by modifying the selected volatile c-element using the magnetic tunnel junction (MTJ) device. Furthermore, we implement a novel hybrid half-buffer using the designed non-volatile hybrid c-element.

6.2 State-of-the-Art Asynchronous Circuit

The basic building block of most of the asynchronous circuits is the c-element, where it creates synchronization among different blocks of the circuits. The truth table of the c-element is given in Table 6.1 which shows that the output follows the input when both input have same value, otherwise it retains the previous state [11].

TABLE 6.1: TRUTH TABLE OF C-ELEMENT

A	B	Z_n
0	0	0
0	1	Z_{n-1}
1	0	Z_{n-1}
1	1	1

$Z_n = AB + (A+B) Z_{n-1}$

We discuss three different implementations of c-element introduced by Martin [12], Sutherland [11], and Van Berkel [13]. The static implementation of the c-element proposed by Martin [12], shown in Figure 6.2, is designed using back-to-back connected inverter, also known as staticizer, which stores the data when the input does not have a similar logic. It requires proper sizing of inverters for reliable operation. The feedback inverter is kept weak compared to the driving inverter to prevent race condition at node c_bar.

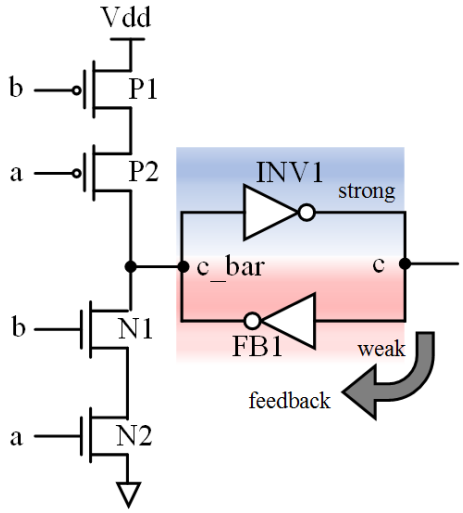

Figure 6.2: Martin's weak feedback c-element

Another implementation of the c-element, shown in Figure 6.3, was proposed by Sutherland [11]. The circuit is ratioless, i.e., sizing of transistor does not affect the operation of the circuit. In this implementation, transistors N3, N4, and N5 are used to provide the necessary feedback

for holding the state of the transistor when input values don't match.

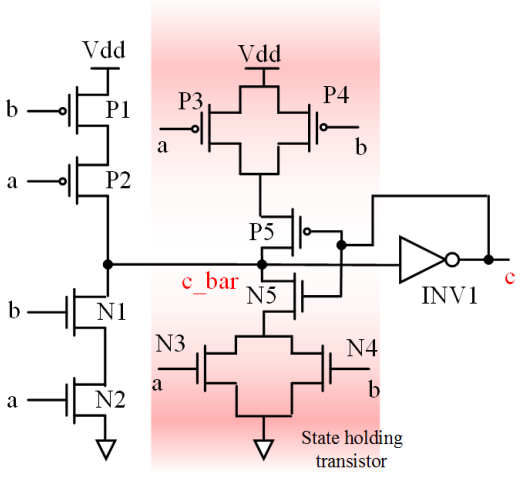

Figure 6.3: Sutherland c-element

Van Berkel [13] also proposed a c-element, as shown in Figure 6.4, which did not require any feedback inverter to hold the states of the transistor instead, it uses feedback conducting path of three transistors in the pull-up network (P3, P4 &P5) or pull-down network (N3, N4 & N5). It is also ratioless and symmetrical with respect to inputs as it provides the same pull-up and pull-down resistance when switching action happens.

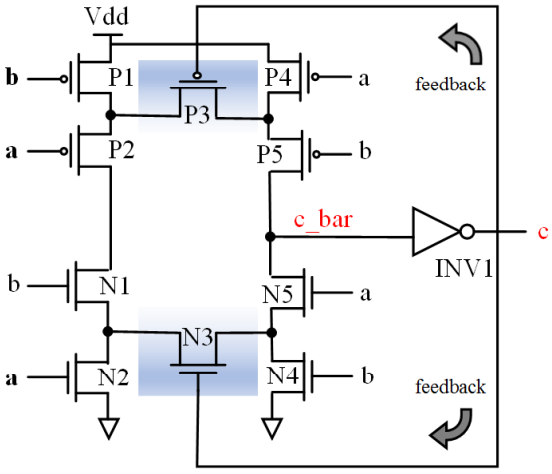

Figure 6.4: Van Berkel c-element

6.3 Proposed Hybrid Asynchronous Circuit

This section presents the design details of the proposed hybrid c-element and hybrid half-buffer where we modify their volatile counterparts using emerging magnetic tunnel junction device.

6.3.1 Proposed Hybrid C-Element

Our objective is to attain non-volatility in the primitive part of the asynchronous system by emerging magnetic tunnel junction (MTJ) device. Hence, we present design of a non-volatile hybrid c-element, as shown in Figure 6.5. The circuit consists of a conventional volatile c-element embedded with an MTJ device and its processing circuitry. The data in the MTJ is read or written by the processing circuitry, which consists of transistors (P7, N3, N4, N5 & N6) controlled by (Az), (wr), and (rd) control signals [18]. To ensure sufficient current passes through the MTJ during the backup operation, the width of the transistor N5 is kept large. On the other hand, the minimum width transistors are used for N3 and N4 as the restore operation is destructive in nature. The non-volatile hybrid c-element has three operational modes: normal mode, backup mode, and restore mode.

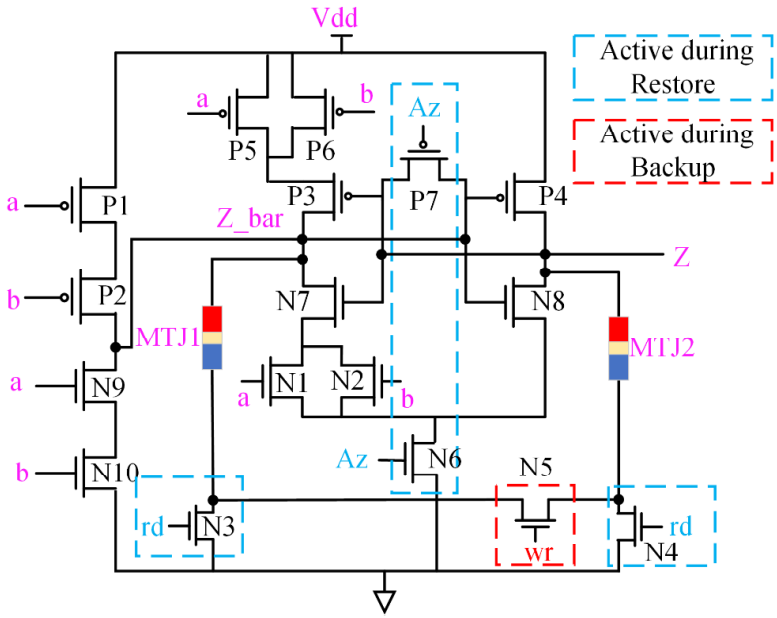

Figure 6.5: Proposed hybrid C-Element

6.3.1.1 Normal mode

In this mode of operation, the proposed hybrid c-element works as a conventional volatile c-element. During normal mode, the status of the control signals is (Az)=1, (rd)=0 and (wr)=0, which disconnect the processing circuitry from the main circuit. The output is driven high for both the input high and driven low for both the inputs low. Otherwise, the circuit holds the previous value.

6.3.1.2 Backup mode

When power starts to fall below a threshold value, the backup operation is initiated by asserting write control signal (wr) high, which turns ON the transistor N5. The other

transistors in the processing circuitry (N3, N4 & P7) remain OFF as the control signals (rd) and (Az) are still at '0' and '1', respectively. Since writing into the MTJ is an asymmetric operation, i.e., time required to flip the state of MTJ from LRS to HRS requires more time than HRS to LRS transition. Therefore duration of the backup operation depends on LRS to HRS transition time of the MTJ [19]. During backup operation for case 1, where Z=1 and Z_bar=0, current flows from MTJ2 to MTJ1 via N5, as shown in Figure 6.6. Similarly, for case 2, where Z=0 and Z_bar=1 current flow from MTJ1 to MTJ2 via N5. If the current flowing through the MTJ exceeds the critical switching current of the MTJ, the MTJ flip its states resulting in successful backup operation.

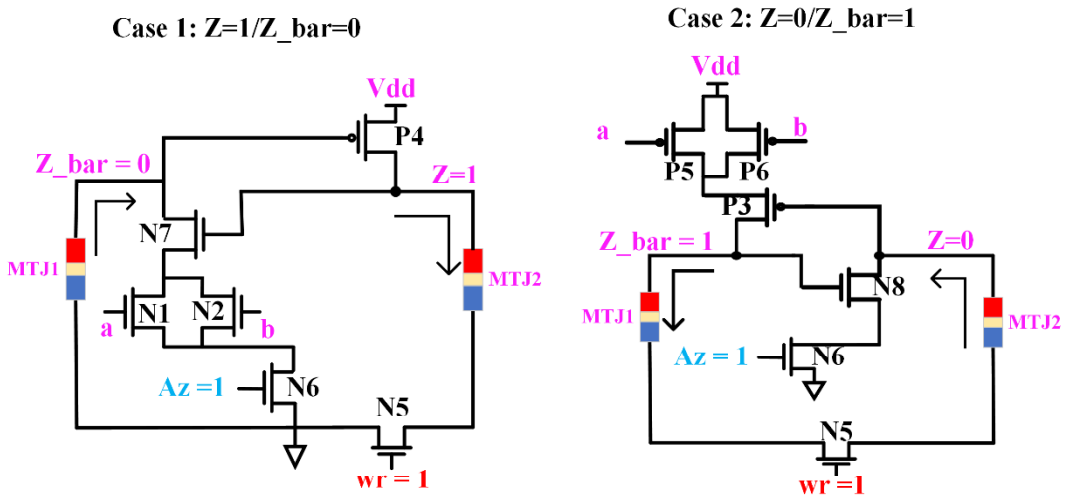

Figure 6.6: Backup operation - storing logic '1' and logic '0' into the MTJ

6.3.1.3 Restore mode

After the power outage, the restore operation is performed to resume the execution from the point of interruption. During the restore operation, the control signal (Az) is asserted low to bring the two output nodes Z and Z_bar to a common voltage level. Next, the control signal (rd) is asserted high, which turns ON the transistor N3 and N4 of processing circuitry, as shown in Figure 6.7. At the same time, transistor P7 is turned OFF by asserting control signal (Az) high. The turning ON of transistor N3 and N4 allows current to flow from nodes Z and Z_bar to ground through MTJs. As the MTJ are in complementary states, more current flows through MTJ having low resistance state and less current flows through the MTJ having high resistance state resulting in the formation of differential voltage across Z and Z_bar. After a small delay, the control signal (rd) is asserted low. The differential voltage at the nodes Z and Z_bar is translated to full voltage level using the cross-coupled inverters. The outputs are now restored back to the values stored before the power failure occurred.

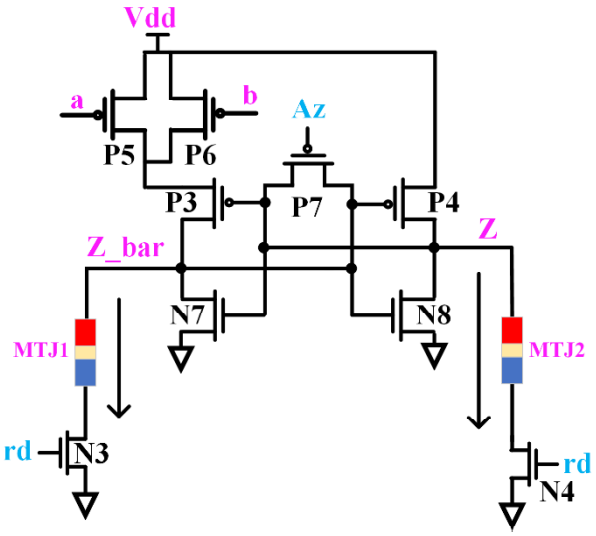

Figure 6.7: Restore operation

6.3.2 Proposed Hybrid Half-Buffer

Figure 6.8 shows a conventional CMOS-based weak conditioned half-buffer based on dual-rail logic. L and R show the Left and Right environment of the volatile half-buffer where L denotes the sender and R denotes the receiver stage. The volatile half-buffer is designed with inputs (In0, In1), output (Out0, Out1), and enable signals: request (req) and acknowledge (ack). The half-buffer normally remains in its reset state, which implies the status of input and output rails (In0, In1, Out0, and Out1) are kept low while the status of the control signal (req) and (ack) are kept high. When data arrives on the left environment, the corresponding input In(x) is asserted high. This event on the input rail results in corresponding output Out(x) to go high, and control signal (ack) to go low. As soon as the acknowledge signal (ack) is asserted low, input In(x) and request signal (req) is pulled to gnd. With request signal (req) asserted low, the output Out(x) is pulled to gnd, and acknowledge signal (ack) is pulled to Vdd. The cycle completes when the request signal (req) is asserted to logic high [20].

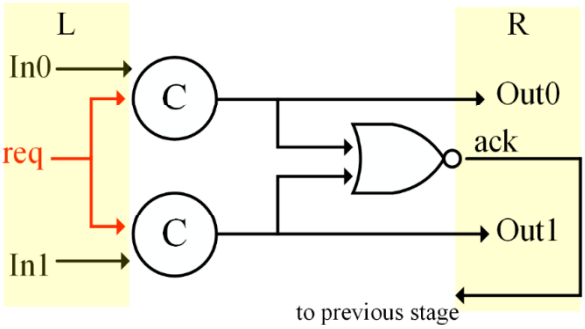

Figure 6.8: Conventional Half-Buffer [20]

The hybrid half-buffer cannot be realized from volatile half-buffer simply by replacing volatile c-element with proposed hybrid c-element. As the during restore operation of hybrid c-element, it is observed that the nodes Z and Z_bar are equalized close to logic '1'. As a result, the output is misinterpreted, resulting in both the output rails being in a high state. However, according to the dual-rail protocol, both the rails cannot have logic '1' simultaneously. Therefore, to avoid the propagation of this invalid state to the output of half-buffer, a gating mechanism is needed during the restore operation. This gating mechanism is implemented using a standard AND gate, as shown in Figure 6.9, which ensures reliable restore operation. Also, the introduction of AND gates results in increased load at the output of the c-element. Due to which the sensing circuitry of non-volatile c-element charges/discharges the internal node capacitance at a slow rate. Therefore, the sizing of the sensing circuitry is increased to compensate loading effect due to the addition of AND gates.

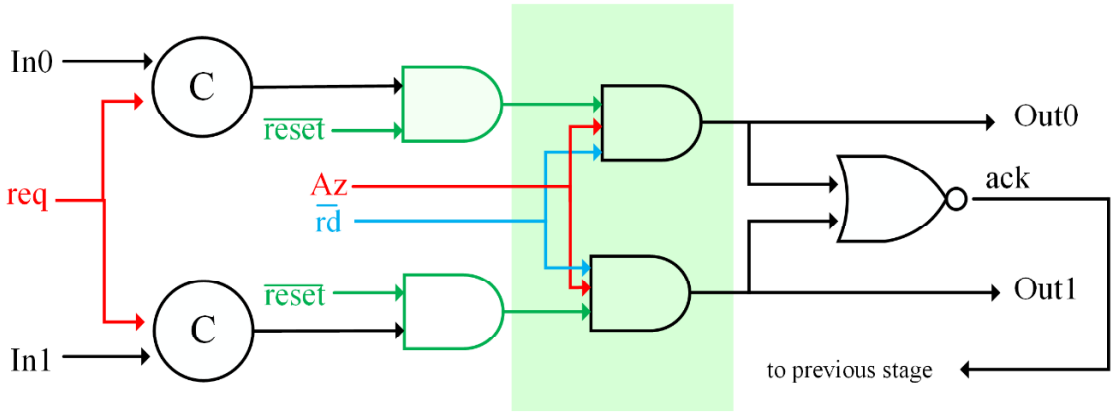

Figure 6.9: Proposed non-volatile hybrid half buffer

6.4 Simulation Results and Discussion

In this section, the proposed hybrid c-element and hybrid half-buffer are validated using extensive simulations performed on the SPICE circuit simulator. The hybrid c-element is designed by modifying the volatile c-element. Therefore, various aforementioned volatile c-element are compared in terms of power dissipation to select the best possible candidate for low power applications. The transistor sizing of these various c-elements are discussed in Ref. [24], according to which Martin's weak feedback c-element is the only one dependent on the W/L ratio of the two cross-coupled inverters while the other two are size-independent. Table 6.2 tabulates the power dissipation, rise time, and fall time of all three implementations of the c-element. The results are calculated at two different power supplies 1.2V and 0.75V.

TABLE 6.2: SIMULATION RESULTS OF DIFFERENT VOLATILE C-ELEMENT

C-Element	VDD	Total Power Dissipation (nW)	Rise Time (psec)	Fall Time (psec)
Van Berkel's [13]	1.2V	218.4	6.2	7.6
	0.75V	77.03	14.53	15.10
Sutherland's [11]	1.2V	187.2	11.95	10.66
	0.75V	65.97	23.45	25.94
Martin [12]	1.2V	102.2	9.1	8.7
	0.75V	30.73	26.16	36.14

From the obtained simulation results, it is observed that Martin's weak feedback c-element has the lowest power consumption amongst the three implementations. However, its design consists of a weak inverter, which doesn't work properly for sub-micron technology. Therefore, Sutherland's implementation is selected for designing hybrid c-element as it provides low power operation without compromising stability. The proposed non-volatile hybrid c-element is compared with its volatile counterpart (Sutherland c-element), and the comparison results at power supply of 1.2V are summarized in Table 6.3. Figure 6.10 plots the simulation waveform of the proposed non-volatile hybrid c-element with all its operational modes. The simulation begins with a backup operation (region 1) in which logic '1' at node Z and logic '0' at Z_bar are stored into the MTJ1 and MTJ2, respectively. Similarly, to evaluate the proposed hybrid non-volatile half buffer, it is also compared with its volatile counterpart. Table 6.4 summarizes the performance comparison results evaluated at 1.2V power supply.

TABLE 6.3: PERFORMANCE COMPARISON OF VOLATILE AND NON-VOLATILE HYBRID C-ELEMENT

	Energy consumption during different modes (J)				Propagation Delay (ns)
	Normal Mode (fJ)	Standby Mode (fJ)	Backup Mode (pJ)	Restore Mode (pJ)	
Volatile c-element [11]	0.792	0.576	-	-	0.042
Non-volatile Hybrid c-element	5.04	0	9.9	1.08	0.155

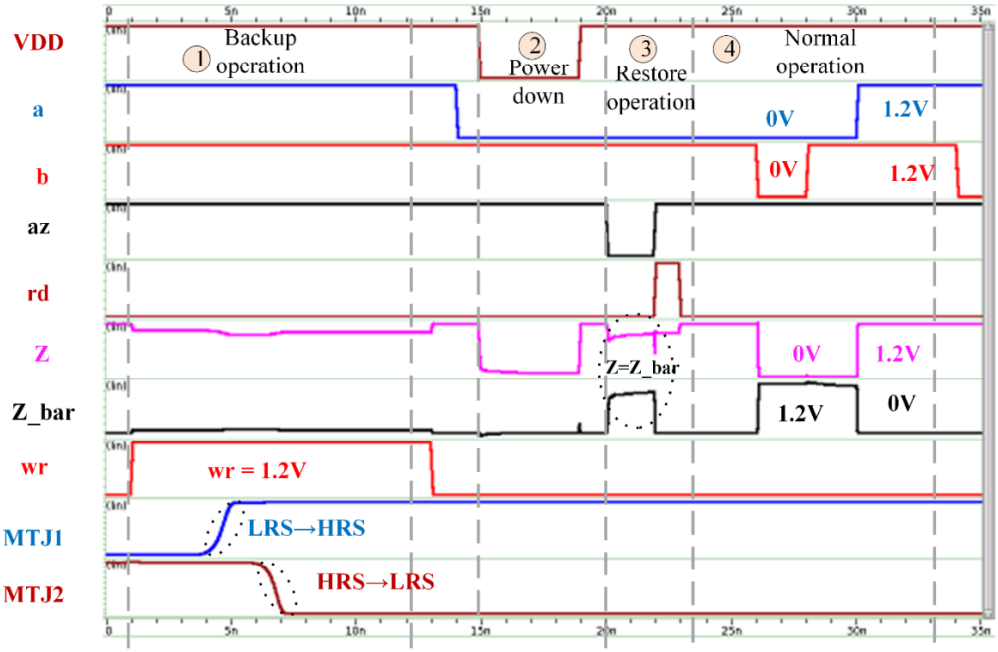

Figure 6.10: Simulation waveform of proposed hybrid c-element

In the proposed non-volatile hybrid half-buffer, energy consumption during standby mode is zero as opposed to volatile circuit because the system is turned off during idle mode with data retained by locally embedded MTJ. Also, energy consumption during normal operation is increased due to increased transistor sizing in proposed non-volatile design to allow large MTJ switching current. Figure 6.11 plots the simulated waveform of the proposed non-volatile hybrid half-buffer similar to hybrid c-element. The circuit functions efficiently in all three operation modes with region 1 plotting the backup operation storing the outputs of both the non-volatile c-elements. After the power outage (region 2), a restore operation is performed to successfully loads the value from the MTJs to the output rail (region 3). Next, region 4 plots the normal operating mode of hybrid half-buffer.

TABLE 6.4: ENERGY CONSUMPTION BY VOLATILE AND NON-VOLATILE HYBRID HALF-BUFFER

	Energy Consumption during different modes				**Propagation Delay (ns)**
	Normal Mode (fJ)	**Standby Mode (fJ)**	**Backup Mode (pJ)**	**Restore Mode(pJ)**	
Volatile half buffer [20]	11.52	37.44	-	-	0.45
Non-volatile hybrid half buffer	64.35	0	355.2	92	0.47

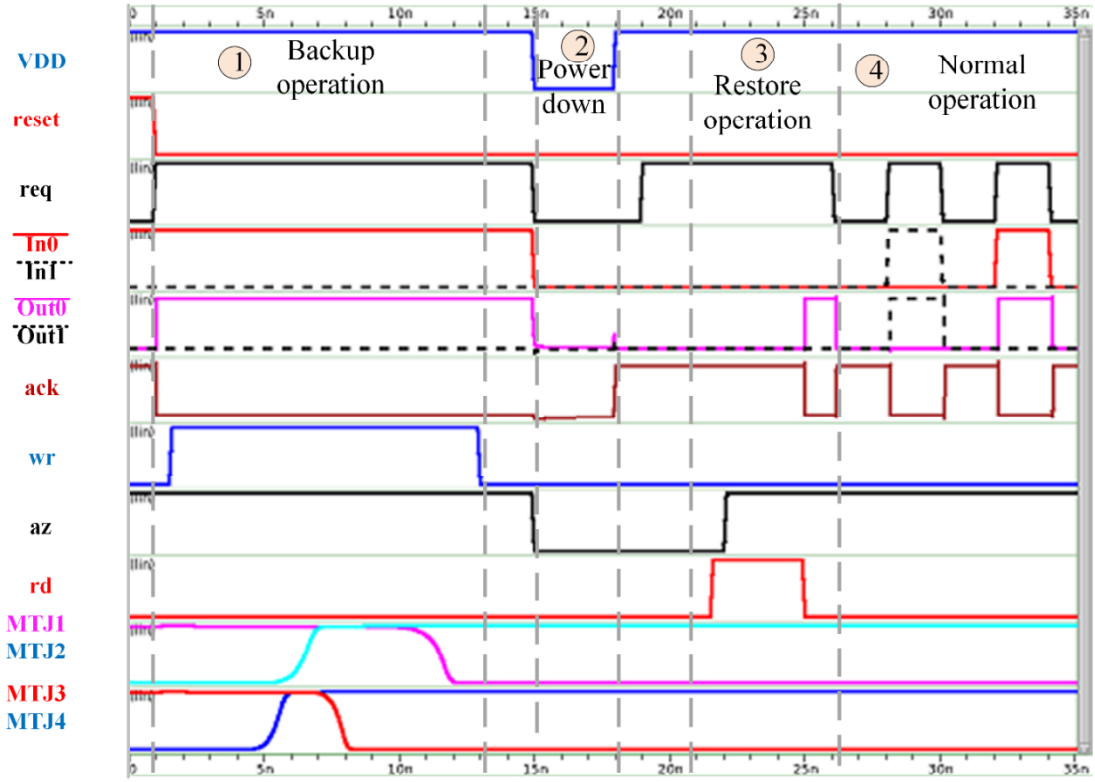

Figure 6.11: Simulation waveform of proposed hybrid half-buffer

6.5 Conclusion

In this work, hybrid asynchronous circuits have been presented to overcome the challenges faced by the state-of-the-art synchronous systems in energy-autonomous applications. The hybrid asynchronous design offers lower power consumption due to the following reasons: 1) elimination of the clock, 2) zero standby power consumption. Moreover, the non-volatile nature of the proposed design offers greater immunity against power failures. The non-volatility is introduced in the basic asynchronous blocks such as c-element by modifying the volatile c-element using emerging non-volatile magnetic device. Therefore, we first explore different implementations of volatile c-element. Based on a comparative analysis of the various implementations of c-element, Sutherland c-element is selected for the non-volatile hybrid version of c-element as it offers lower power consumption without affecting circuit stability. Further, we also propose a novel design of non-volatile hybrid half-buffer by utilizing the proposed hybrid c-element. The proposed hybrid half-buffer prevents transmission of invalid state to the next stage in dual-rail circuit. Moreover, it offers immunity against sudden power outages by preserving the data in the MTJ device. The proper functionality of the proposed hybrid designs has been verified by the extensive simulation results. The proposed designs are also compared with their volatile counterparts, and the

energy overhead and delay overhead for the hybrid circuits can be compensated if the duration of power down exceeds a few hundred microseconds.

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