

# Table of Contents

<b>Abstract.....</b>	<b>i</b>
<b>Acknowledgements.....</b>	<b>iii</b>
<b>List of acronyms.....</b>	<b>iv</b>
<b>Table of contents.....</b>	<b>v</b>
<b>List of figures.....</b>	<b>viii</b>
<b>List of tables.....</b>	<b>x</b>
<b>Chapter 1. Introduction.....</b>	<b>1</b>
1.1 FPGAs in VLSI design and verification flow .....	1
1.2 High-level synthesis .....	3
1.3 Motivation behind the work.....	4
1.4 Objectives of this work.....	5
1.5 Organization of this thesis.....	6
1.6 Concluding remarks.....	7
<b>Chapter 2. Literature review .....</b>	<b>8</b>
2.1 High-level synthesis in VLSI design.....	8
2.2 Advantages and limitations of HLS .....	10
2.3 Concepts of HLS optimization .....	11
2.4 Prior works in the area of HLS optimization .....	17
2.5 HLS optimization directives in MATLAB HDL coder.....	18
2.6 HLS optimization directives in Vivado HLS.....	19
2.7 Gaps in existing research.....	23
2.8 Concluding remarks.....	24

<b>Chapter 3. Optimization techniques based on HLS directives.....</b>	<b>.25</b>
3.1 Bandpass digital signal processing filter design (HDL coder).....	25
3.2 QPSK modulator design and implementation (HDL coder).....	28
3.3 MIPS processor core (HDL coder).....	31
3.4 Encryption and cryptography algorithms: AES (Vivado HLS).....	35
3.5 YOLO v2 deep learning algorithm (Vivado HLS).....	47
3.6 Concluding remarks.....	55
<b>Chapter 4. Application-specific bit width for intermediate data nodes : method and results</b>	<b>56</b>
4.1 Introduction to ASBWIDN method .....	56
4.2 Detailed description of the methodology.....	57
4.3 Bandpass DSP filter design, implementation, and optimization.....	60
4.4 Sobel edge filter design, implementation, and optimization.....	62
4.5 Harris corner detector design, implementation, and optimization.....	69
4.6 Digital down converter for software defined radio applications : design, implementation, and optimization .....	75
4.7 Advanced encryption standard for automotive applications : design, implementation, and optimization .....	82
4.8 Concluding remarks.....	88
<b>Chapter 5. Test application: RADAR signal processor for automotive applications.....</b>	<b>.89</b>
5.1 Introduction to RADAR signal processor application.....	89
5.2 Prior works for RADAR signal processor implementation.....	91
5.3 RADAR signal processor and verification framework.....	91
5.4 Model simulation and verification results.....	94
5.5 HLS optimization results for RADAR signal processor.....	96
5.6 Results comparison with literature.....	99
5.7 Concluding remarks.....	101
<b>Chapter 6. Conclusion and future directions.....</b>	<b>102</b>
6.1 Major contributions of the work .....	103
6.2 Limitations and Future directions .....	107

<b>References.....</b>	<b>110</b>
<b>Appendix.....</b>	<b>121</b>
<b>List of publications.....</b>	<b>126</b>
<b>Brief biography of candidate .....</b>	<b>128</b>
<b>Brief biography of supervisor .....</b>	<b>129</b>
<b>Brief biography of co-supervisor .....</b>	<b>130</b>