Chapter 2. Hard Switched SPWM Inverter

2.1 Introduction

SPWM voltage source inverters, especially those intended for UPS application, are generally operated at switching frequency well above fundamental, in order to increase the distance between the desired and the lowest undesired spectral components. The inverter performance is also determined by the PWM switching scheme [Aziz 2004]. With the availability of faster power switching devices, the present trend is to increase the switching frequency of operation to meet the objective. This results in distortion in the output voltage wave shape when the inverter is operated at high switching frequencies due to finite switching times of the device used. Distortion is also sensitive to output current levels and also due to presence of snubber and parasitic inductances. Lower order harmonics such as 3^{rd}, 5^{th} and 7^{th} are introduced in a single phase inverter and the amount of distortion becomes significant when the switching frequency is increased [Evans 1987, Bowes 1996, Manjunath 1985].

The power switching device is selected based on the power rating of the inverter. The hybrid Darlington switches are used in low voltage and medium power applications, MOSFET switches in low power applications and IGBT switches in medium to high power applications. This chapter presents inverter performance analysis with hybrid Darlington and IGBT as power switches.

2.2 Inverter Performance with Hybrid Darlington Switches [Kumar 2001, 2007(1)]

Fig.2.1 shows an SPWM inverter made of hybrid Darlington transistors. The inverter uses an RCD snubber with optimum design. The inverter power circuit also takes into account the parasitic wiring inductance. Control pulses for the switches are obtained

by SPWM-stored waveform technique. The idealized voltage wave shapes are shown in Fig.2.2.

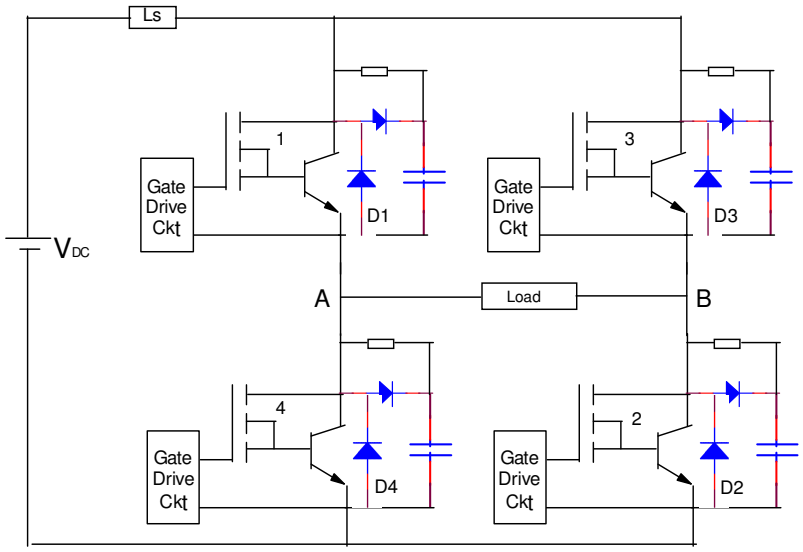

Fig.2.1. Single Phase PWM Inverter Employing Hybrid Darlington

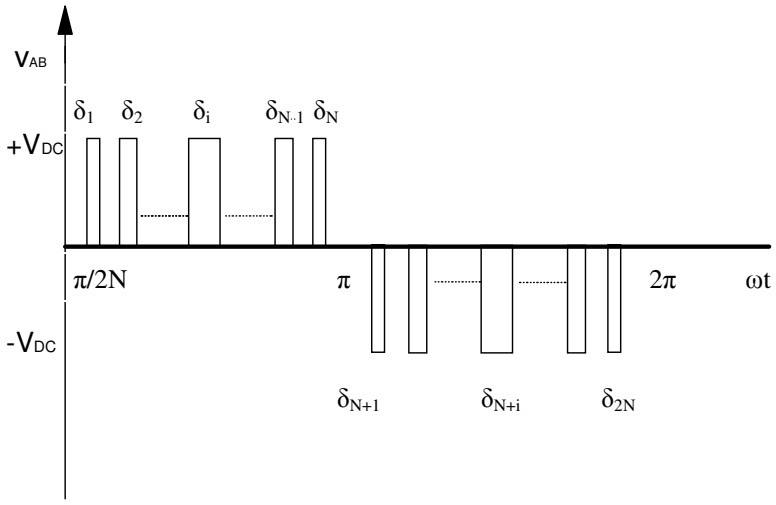

Fig.2.2 The SPWM output voltage waveform

The output voltage v_{AB} consists of N number of pulses per half cycle whose centers are equally spaced with respect to each other with a spacing of $\Delta=\pi/N$ radians. The width of i^{th} pulse

in radians is proportional to the sine of the argument at the centre of the pulse [Huang 1980, Pitel 1981]. The i^{th} pulse is at a distance, $X_i = (2i-1)\pi/2N$ radians from $\omega t=0$. With sinusoidal pulse width modulation the width of the i^{th} pulse in radians for a modulation index M less than 1 is given by

$$\delta_i = M\Delta \sin\{(2i-1)\pi/2N\} \tag{1}$$

Since the inverter output pulse train is an odd periodic function possessing half wave symmetry, the output voltage v_{AB} can be represented by Fourier series as

$$v_{AB} = \sum_{n=1}^{\infty} A_n \sin n\omega t \tag{2}$$

Where A_n is the amplitude of the n^{th} harmonic component and $\omega = 2\pi/T$. A_n is given by,

$$\begin{aligned} A_n &= \frac{2}{\pi}\int_0^{\pi} v_{AB}(\omega t)\sin(n\omega t)\, d(\omega t) \\ &= \frac{4V_{DC}}{n\pi}\sum_{i=1}^{N}[\{\sin n\Delta(i-1/2)\}\sin n\delta_i/2] \end{aligned} \tag{3}$$

Where, V_{DC} is the dc link voltage.

2.2.1 Estimation of distortion

The inverter circuit analysis presented here includes the dead time inserted between the turn ON and turn OFF intervals of the two switches in a phase leg. The dead time is a function of the switching times of the devices used and the safety margin taken into account. The switch output terminal voltage with snubber [McMurray 1980] and analysis of reverse recovery phenomenon in inverter of a freewheeling diode form the basis of the analysis presented here.

Analysis during Turn ON of switch1:

Fig. 2.3(a) to Fig. 2.3(d) show the current paths in the inverter at various instants after the switch is turned-on. Prior to turn-on of switch1, load current is freewheeling through diode D4 and switch 2 as shown in Fig. 2.3(a).

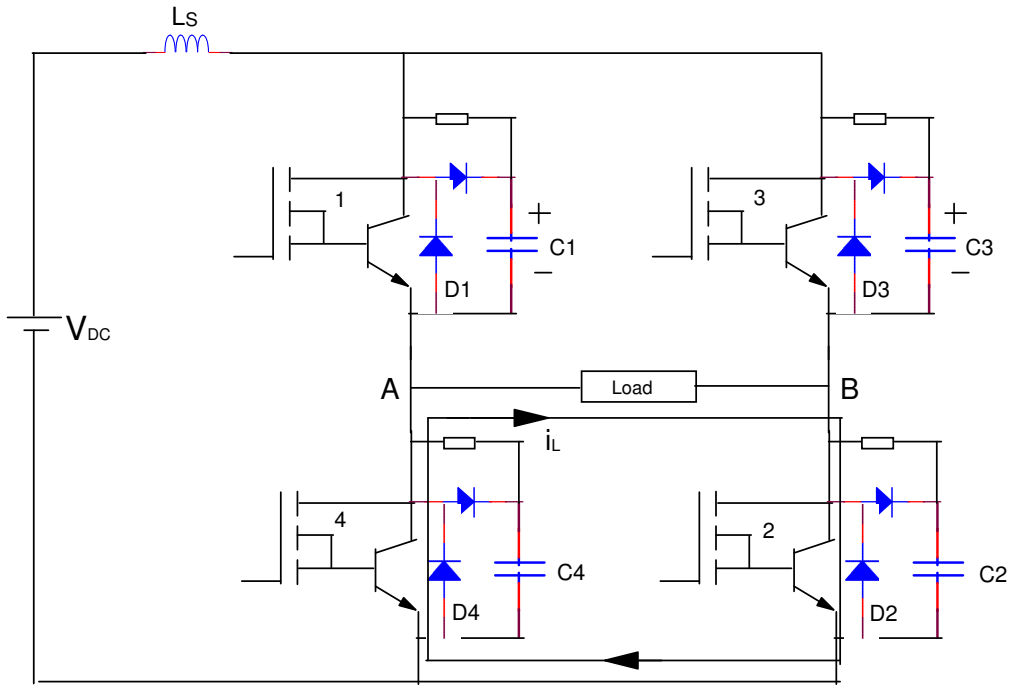

Fig.2.3 (a) The load current is freewheeling through diode D4 and switch 2

When switch1 is turned-on load current starts flowing through it and capacitor C1 discharges with current i_{C1}. Diode D4 current starts decreasing. This mode of operation is shown in Fig. 2.3(b).

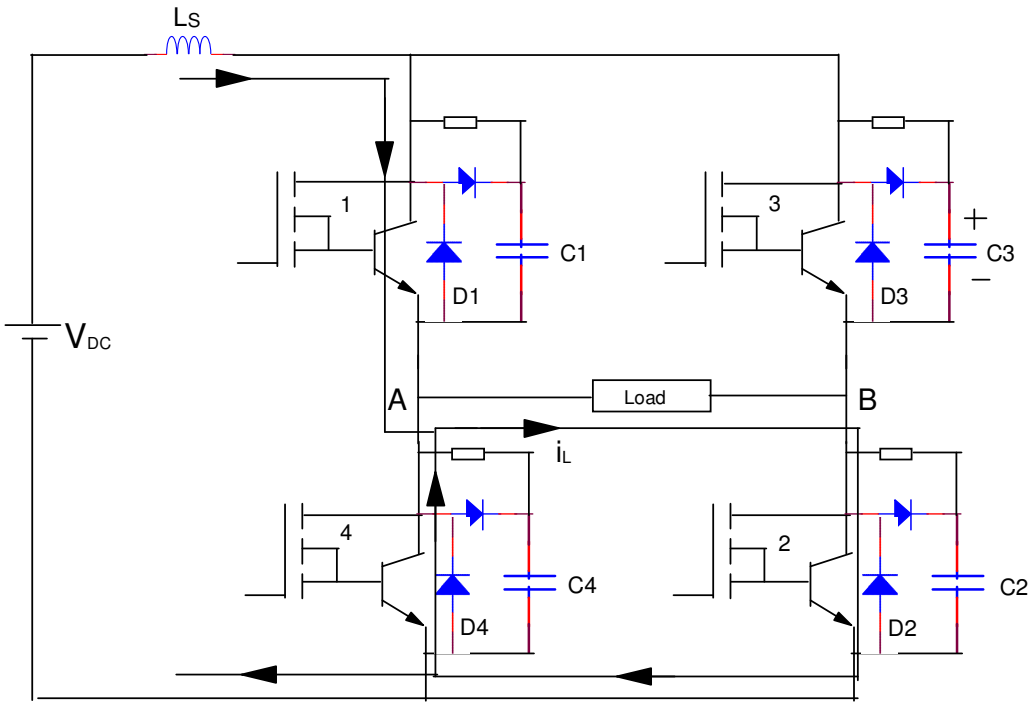

Fig.2.3 (b) Switch1 starts conducting the load current with diode D4 and switch2 are ON

Fig. 2.3(c) shows the load current conducting through switch1 and switch2 with reverse recovery current of diode D4. Fig. 2.3(d) shows the operating mode when diode current i_{D4} is fully recovered and now the load current is conducing through switch1 and switch2.

Theoretical waveforms for these modes are shown in fig. 2.4. Switch1 is turned-on at time t_0 and at t_5 the capacitor C4 completely loses its excess charge and load voltage V_{AB} return to dc link voltage V_{DC}.

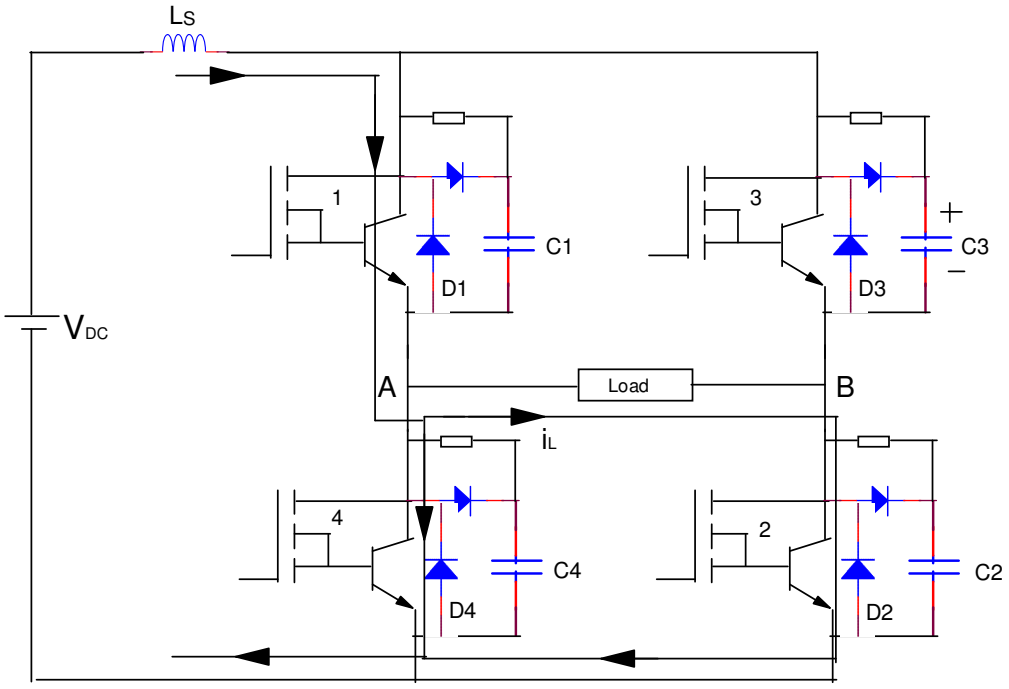

Fig.2.3 (c) Switch1 is conducting the load current with reverse recovery current in diode D4 and switch2 is ON

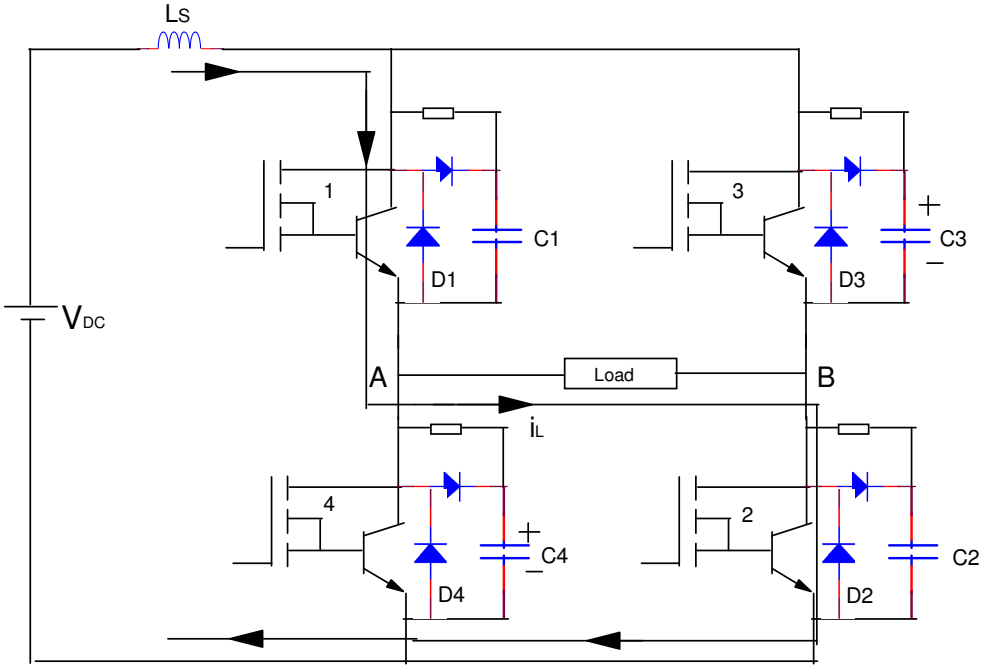

Fig.2.3 (d) Switch1 and switch2 are conducting the load current

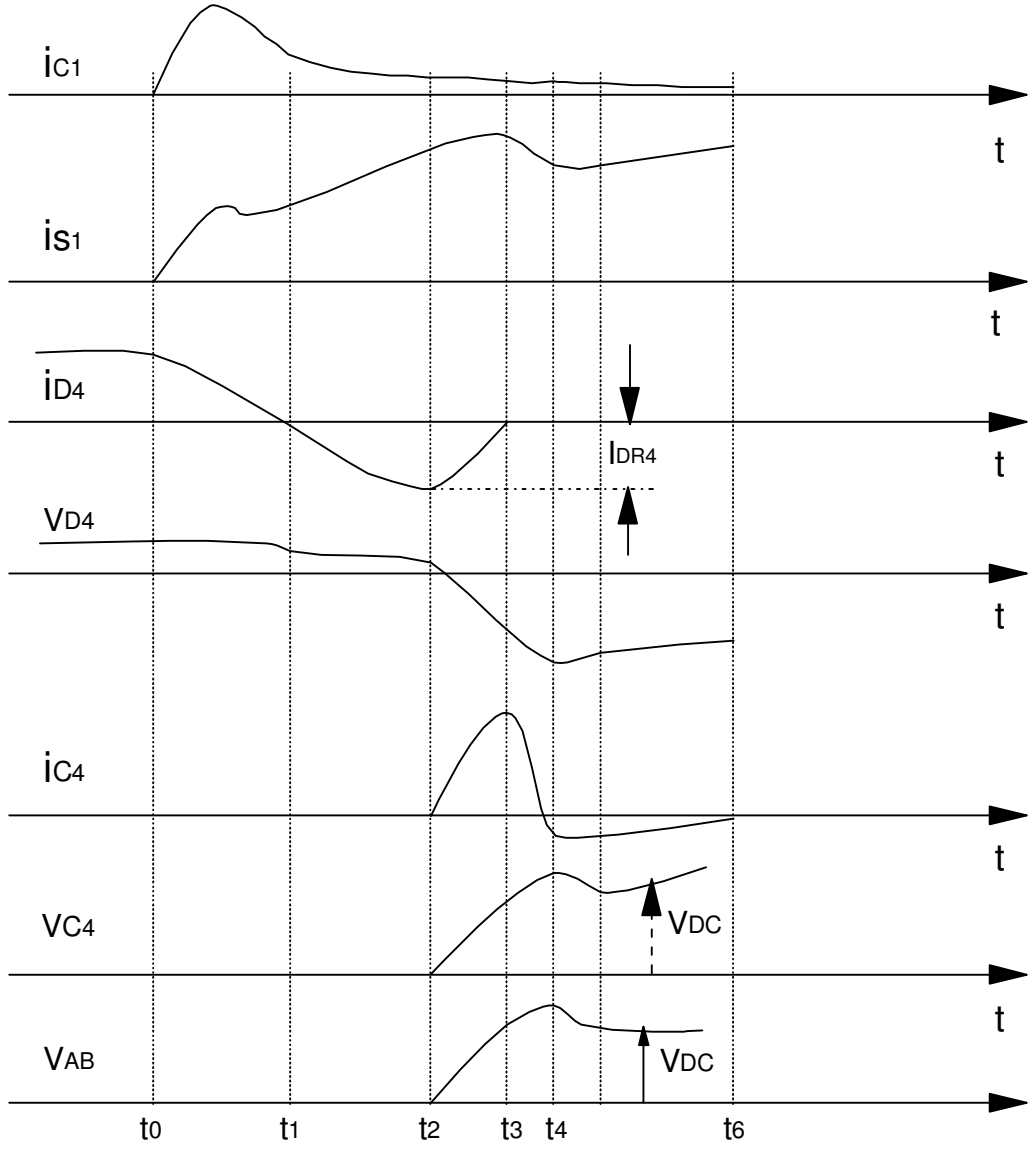

Fig.2.4 Waveforms of current and voltage in the circuit during turn-on of switch1 in a switching cycle

Fig.2.4 shows the associated current and voltage waveforms during turn ON of switch1 in the switching cycle, where V_{AB} is the voltage waveform at the inverter output.

The load voltage starts rising after a delay of

$$t_d = \{\frac{I_{DR4} + i_L}{V_{DC}}\} L_S \tag{4}$$

Where I_{DR4} is the peak reverse recovery current of diode D_4 and i_L is the load current value during that pulse. (4) Indicates that the delay time in the output voltage is due to the peak reverse recovery current in D_4 and i_L, the instantaneous load current. The load current itself in a half cycle varies sinusoidally. If $i_L = I_L \sin\omega t$, then, the delay time during the turn ON of a switch

$$t_{d_{ON}} = \frac{(I_{DR4} + I_L \sin \omega t) L_S}{V_{DC}} + t_{ds} \tag{5}$$

Where, t_{ds} is the delay time of the switch itself.

Thus for L_s = 5μH, V_{DC} = 100 V, I_L =10A (peak) and I_{DR4} of 2A and t_{ds} = 0.3 μS,

$t_{dON\ max}$ = 0.9 μS.

The worst case rise time of the load voltage pulse is due to the interaction of snubber capacitor and L_s given by

$$t_r = \frac{\pi}{2}\sqrt{L_S C} \tag{6}$$

With L_S = 5μH , C = 0.1μF (used), t_r = 1.1μS.

The above analysis indicates that the delay can be minimized by using a soft fast recovery diode for freewheeling and low turn ON delay devices. The stray inductance has to be minimized in order to minimize t_{dON} and t_r. A fast turn OFF switch minimizes the value of C and in turn reduces t_r.

Analysis during Turn OFF of switch1:

Fig. 2.5 (a) to Fig.2.5 (d) show the current path in the inverter circuit during turn-off of switch1. Fig. 2.5(a) shows the initial condition before switch off when the load current is flowing through switch1 and switch2.When the gate signal is removed from switch1, current starts decreasing through the switch and starts increasing through snubber diode and capacitor C1. This is shown in Fig. 2.5(b). Fig. 2.5(c) shows the current path when the entire load current is flowing through snubber diode and C1.

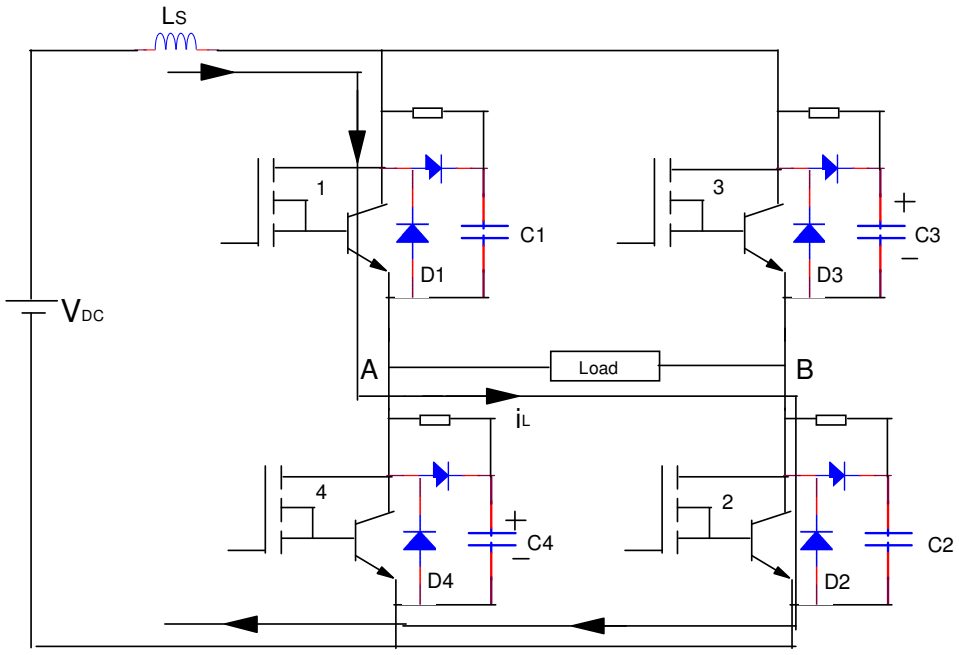

Fig. 2.5(a) Current is flowing through switch1 and switch2

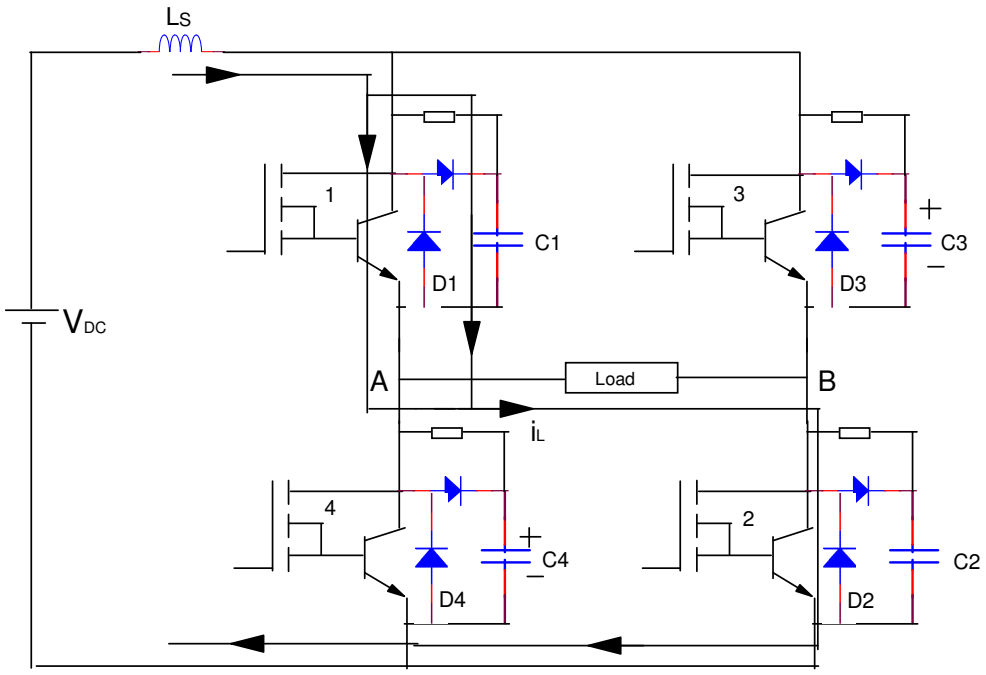

Fig. 2.5(b) Current in switch1 starts decreasing and current starts increasing through C1

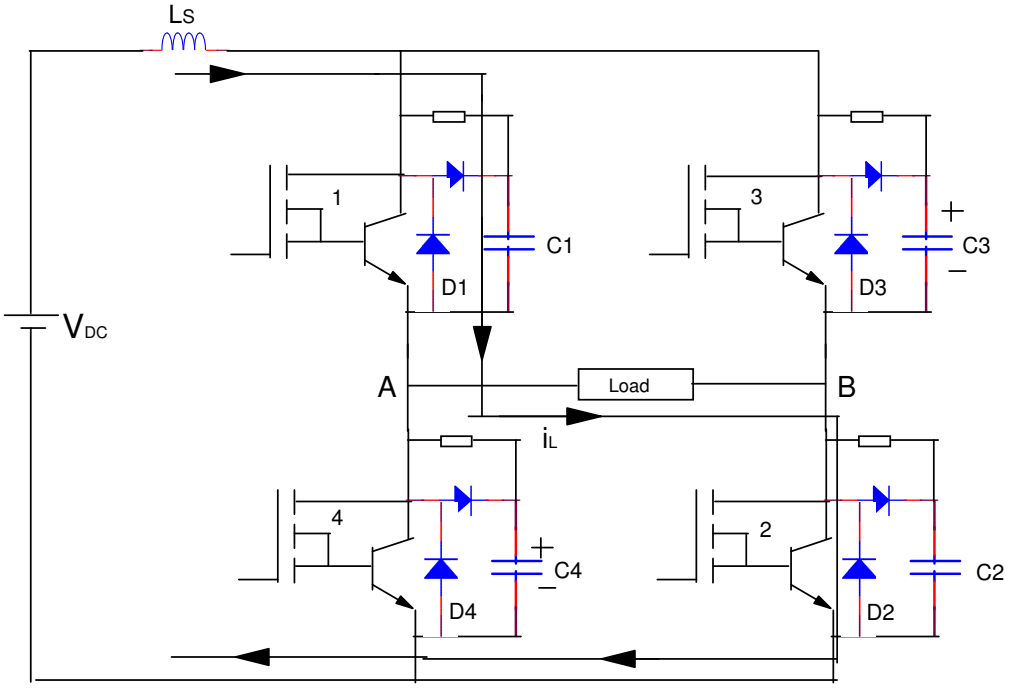

Fig. 2.5(c) Switch1 is off and all the current is flowing through C1

Fig. 2.5(d) shows the current path when the load current is freewheeling through diode D4 and switch2 and excess charge is removed from the capacitor C1.

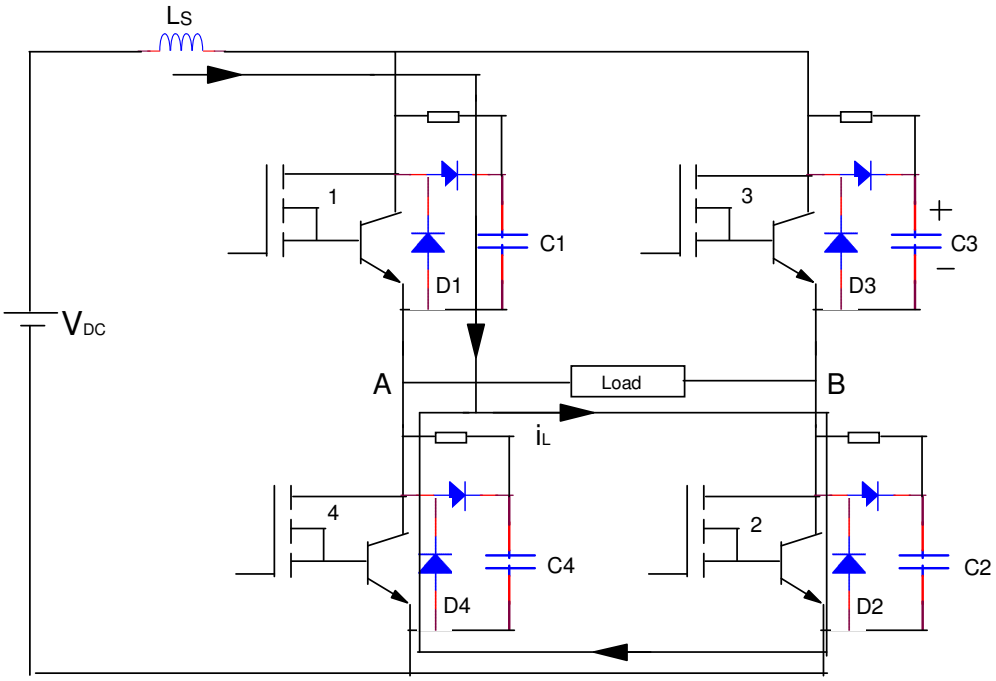

Fig. 2.5(d) Load current is freewheeling through switch2
and diode D4 and excess charge is removed from C1

Theoretical waveforms at different instants during turn-off of switch1 are given in Fig. 2.6. Prior to the instant t_0 switch1 is supplying the load current with current paths and snubber capacitor voltage polarities as shown in fig 2.5(a). At t_0, the gating pulse to switch1 is removed and switch1 goes through storage time till t_1. At t_1, the switch1 current starts decreasing. The switch current is assumed to fall linearly from t_1 to t_2 as shown in Fig. 2.6

The delay in the fall of load voltage pulse as seen from Fig 2.6 is equal to

$$t_{fall} = (t_{dd} - t_s) + (t_4 + t_3) \qquad (7)$$

Where, t_{dd} is the dead time between the gating ON instant of switch4 and the instant of removal of gating pulse for switch1.

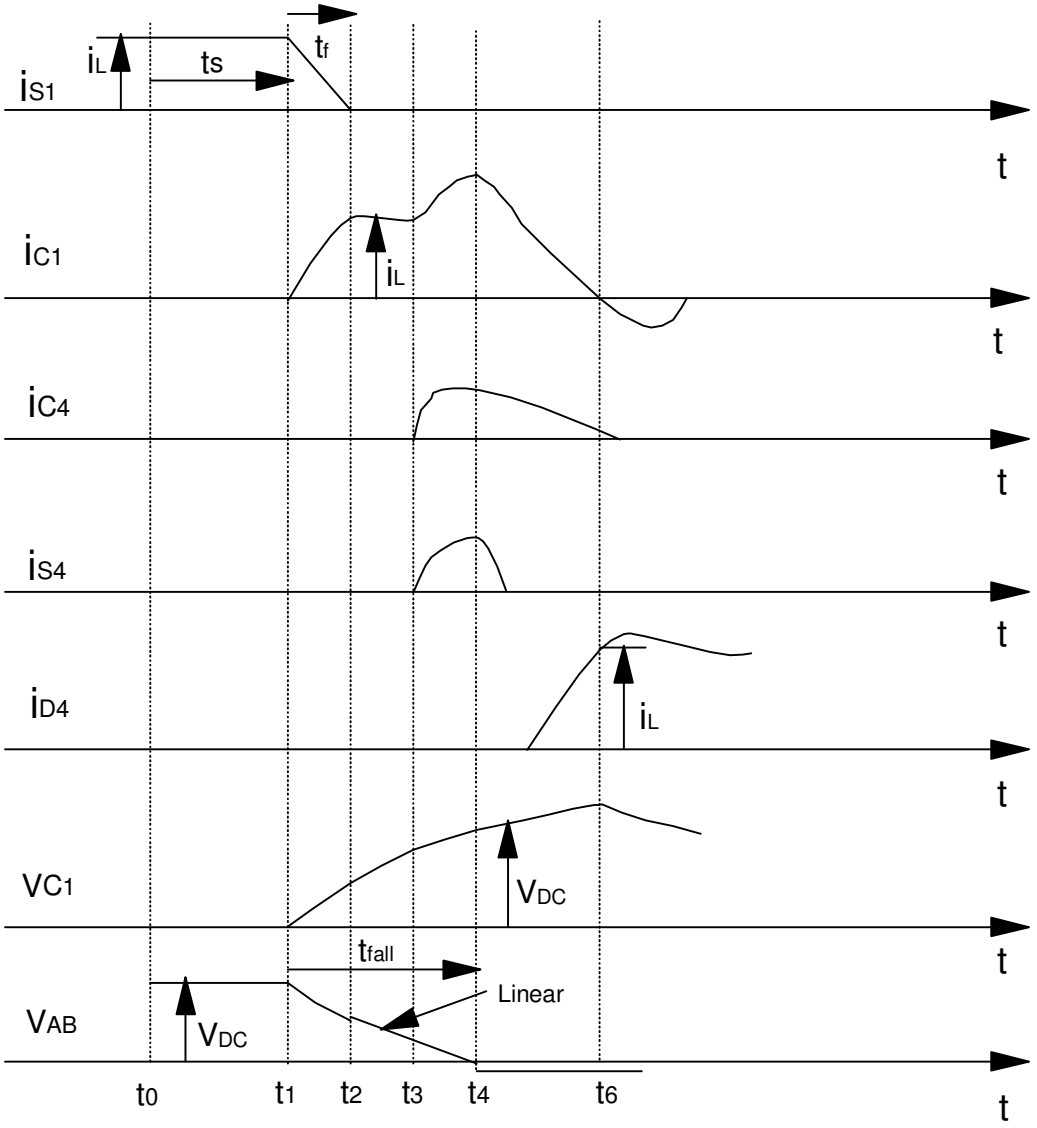

Fig.2.6 Waveforms of current and voltage in the circuit during turn-off of switch1 in a switching cycle

The effect of dead time on output voltage can be found from [Jeong 1991, Kerkman 2003]. The worst case delay time is equal to t_{dd}, the dead time. This is because near zero load current values V_{C1} practically does not change until t_3. Hence the load voltage also does not fall appreciably till t_3. The capacitor charges resonantly from t_3 to t_4 as switch 4 turns ON at t_3 and hence the load voltage V_{AB} falls off only during t_3 to t_4 to zero. The fall time is shorter at light loads and at zero load is equal to

$$t_{fall} = \frac{\pi}{2}\sqrt{L_s C} \tag{8}$$

At full load for an optimum snubber

$$t_{fall} = t_f \tag{9}$$

Thus for L_s = 5μH, C = 0.1μF and measured t_s = 0.75μS and t_f = 0.5μs, for zero load current and t_{dd} = 2μs, t_{doff} = 2μS.

At a load current of 10A with measured t_s = 0.7μS, estimated value of t_{doff} = 0.75μs and t_{fall} = 1.1μS. The fall time of the output pulse at 10A load current is estimated to be

t_{fall} = 0.5μS.

Fig.2.7 and Fig.2.8 show the output voltage pulse rise and fall respectively near zero load current and 10A load current. The output pulse rise and fall times, theoretical and experimental are given in Table 2.1 at load currents of 0A and at 10A.

Fig.2.7. Rise of Output Voltage Pulse at Output currents of (a) 0A (b) 10A

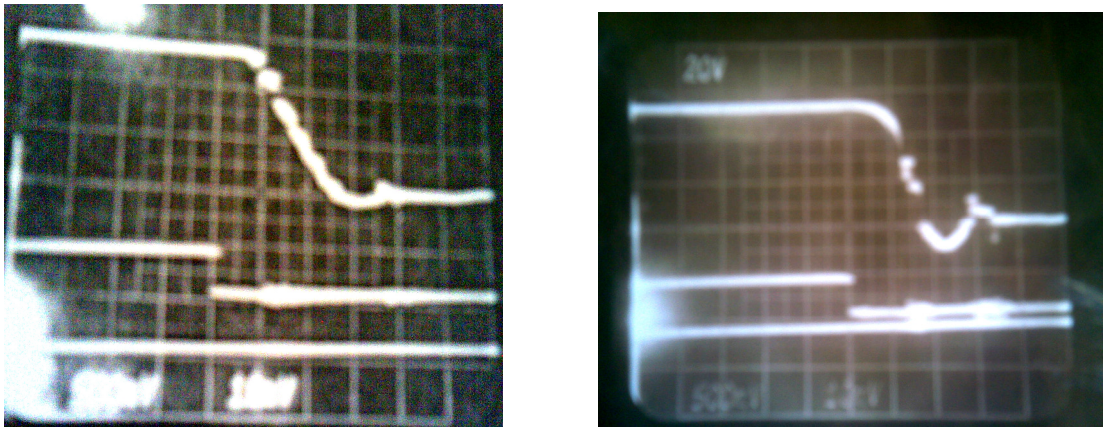

Fig.2.8. Fall of Output Voltage Pulse at Output currents of (a) 0A (b) 10A

2.2.2 Effect of waveform distortion on spectral component

In this analysis it is assumed that the output voltage pulses have linear rise and fall and that the rise time and fall time are equal. This is justified if the switching frequency is not too high. The overshoot and undershoot as can be seen in Fig. 2.7 and Fig.2.8 is neglected.

Table2.1
Output Pulse Rise and Fall Time at no load and at rated load current (0.7pf lag, Z_{load}=7.5Ω)
(Theoretical and Experimental)

Load current	Theoretical Delay Time (μS)				Experimental Delay Time (μS)			
	Rise	Fall	ON	OFF	Rise	Fall	ON	OFF
0 Amp	1.1	1.1	0.3	2	1.5	1.5	0.25	1.0
10 Amp	1.1	0.5	0.9	0.75	1.5	0.6	1.0	0.85

Fig. 2.9 shows a pair of pulses at the output of the inverter. The inverter output voltage consists of several such width modulated pulses.

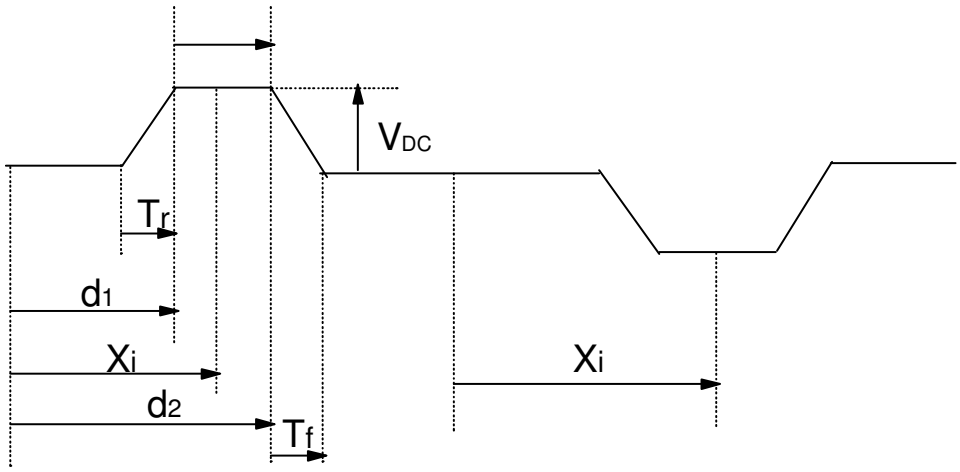

Fig.2.9. A Pair of Pulses at the Output of the Inverter (actual)

The output spectral components can be determined by Fourier series. The waveform of Fig. 2.9 is an odd periodic function possessing half wave symmetry. The Fourier series components A_n and B_n for the pulse train composed of several such pulses is given by

$$A_n = \frac{2V_{DC}}{\pi T_r n^2}[\sin nd1 + \sin nd2 - \sin n(d1 - T_r) - \sin n(d2 - T_r)] \quad (10)$$

$B_n = 0$

Where,

$$d_1 = X_i - \frac{\delta_{ia}}{2} \ radians$$

$$d_2 = X_i + \frac{\delta_{ia}}{2} \ radians$$

T_r = rise and fall times in radians,

δ_{iact} = actual width of the pulse without slopes.

Theoretical and experimental results of values of harmonic amplitudes in the inverter output at modulation index of 0.75 are given in Table 2.2 for 10 kHz and 20 kHz switching frequencies. The computed results were obtained by setting,

$T_r = 2\mu s$, $\delta_{iact} = (\delta_i - Tr/2)$ sec.

Where δ_i is given by (1) for M = 0.75.

Table2.2
Harmonic Amplitudes in the Inverter Output (theoretical and experimental)
With inclusion of switching slopes as percent of the fundamental at modulation index of 0.75, f_s= switching frequency, f_1=fundamental frequency

Harmonic Order	10 kHz System		20 kHz System	
	Theoretical	Experimental	Theoretical	Experimental
3	0.57	0.9	1.11	1.25
5	0.33	1.9	0.66	1.0
7	0.23	0.85	0.463	0.7
f_s-3f_1	16.2	17.5	16.8	16.5
f_s-f_1	43.9	45	42.7	40.0
f_s+f_1	43.1	42.5	41.9	39.5
f_s+3f_1	16.8	20	17.0	16.5

The difference between the experimental and theoretical results appears to be due to the variation of storage time and fall time in a fundamental period due to sinusoidal distribution of current pulses. Thus, at high switching frequencies, as the values of $\Delta = \pi/N$ decreases, the value of T_r becomes comparable to Δ and hence the output spectrum deviates more from the ideal. The low order harmonics are difficult to filter off and when such an inverter is to be used for UPS system, the switching frequency must be selected based on this criterion, as lower order harmonics contribute to the THD significantly. Thus, when a device is selected for a given rating of an inverter, with certain switching times, it dictates the selection of snubber capacitor C.

The power circuit has certain wiring inductance or may have snubber inductor included. The dead time used results in a particular delay time. The choice of freewheeling diode influences the delay time. The rise and fall times are affected by L_s and C. The dead time itself is dependent on switching times of the device and so on. In addition, the variation of output current in a half cycle also influences the delay time. These factors make the output pulse width different from the ideal value in addition to causing rise and fall times other than zero. Therefore it can be concluded from this, that there exists an optimum switching frequency above which it only serves to increase the low order harmonics for a given device, hence rating. The waveforms approximated here and analyzed are equally applicable to soft switching inverter [Divan 1986, Vahid 2004]. However, in soft switching inverters with PWM, the slopes are more prominent when inductance is used and a higher limit on switching frequency is further reduced compared to hard switching inverters, as it introduces more low order harmonic amplitudes.

2.3 Dead time circuit suitable for low cost inverter [Kumar 2007(1)]

Thus it is clear from the previous discussion the importance of dead time circuit. Now if dead time is generated using R and C components and gates or mono shots as shown in Fig. 2.10 and Fig.2.11, the dead time is affected by the component tolerance. Further CMOS ICs are only suitable for generating this type of dead time. Even though TTL monoshots can be used, these are more susceptible to noise. For the circuit of Fig. 2.10, TTL IC cannot be used. The switching time of the CMOS ICs and the threshold voltage vary with supply voltage. Hence while using these types of circuits; high

precision components must be used in order to ensure constancy of dead time. This is particularly true if MOSFETs are used as switching devices and switching frequency is above 50 kHz. This can be explained from the point of view that as the switching frequency increases large number of pulses near the zero crossing of the voltage wave will have very small width pulses and hence a small change in the width of the pulse is expected to result in a very significant increase in the lower order harmonics which are particularly difficult to filter off.

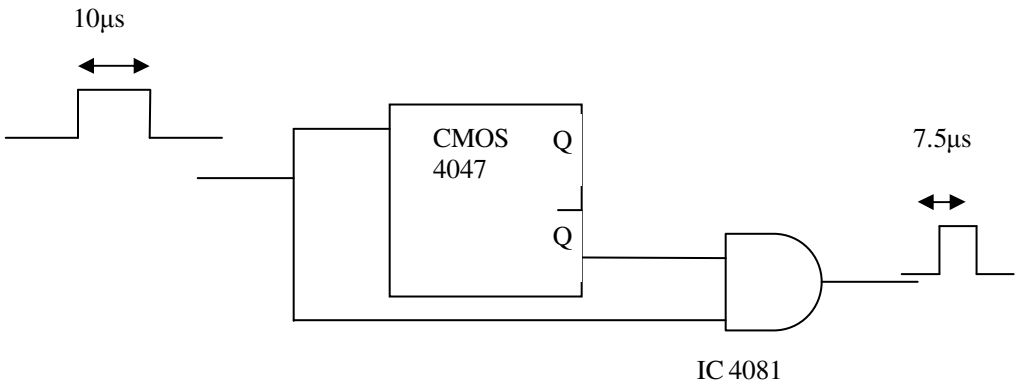

Fig.2.10. Circuit for Dead Time Generation Using CMOS IC

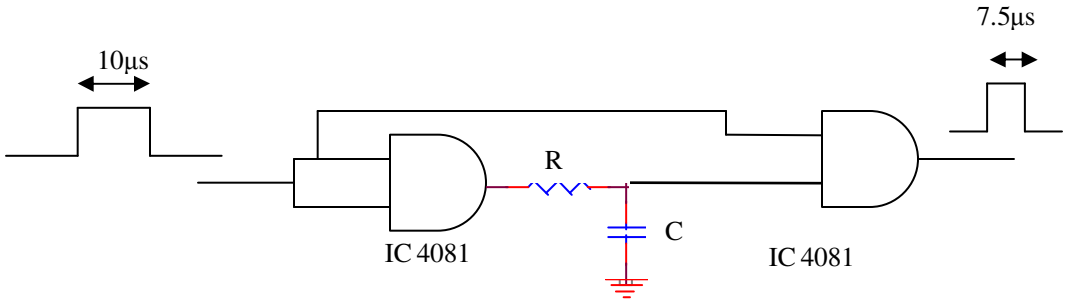

Fig.2.11. Circuit for Dead Time Generation Using R and C

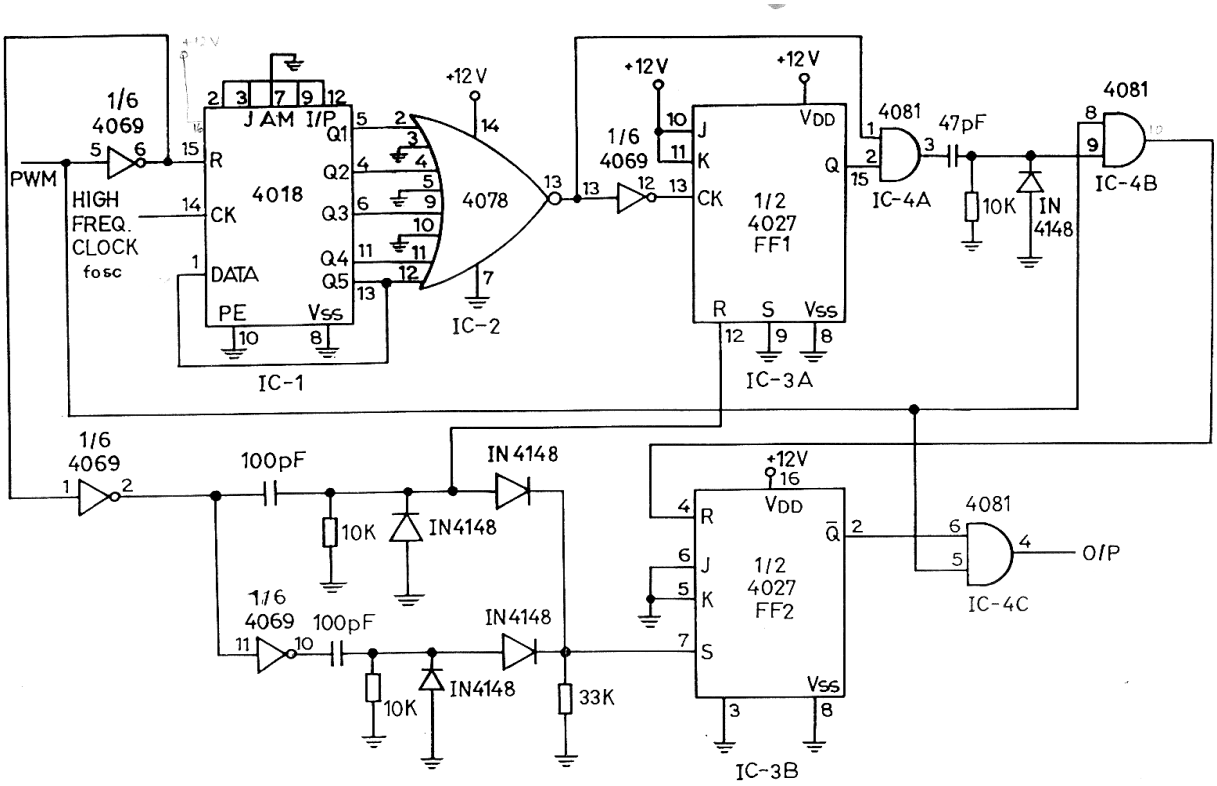

Fig.2.12. Digital Dead Time Circuit

Fig.2.12 shows a dead time circuit developed for this work which does not depend on the tolerance of components. This is particularly suitable when the dead time is between 3-10 µs. This circuit requires a high frequency clock which can be made available in the system at any point.

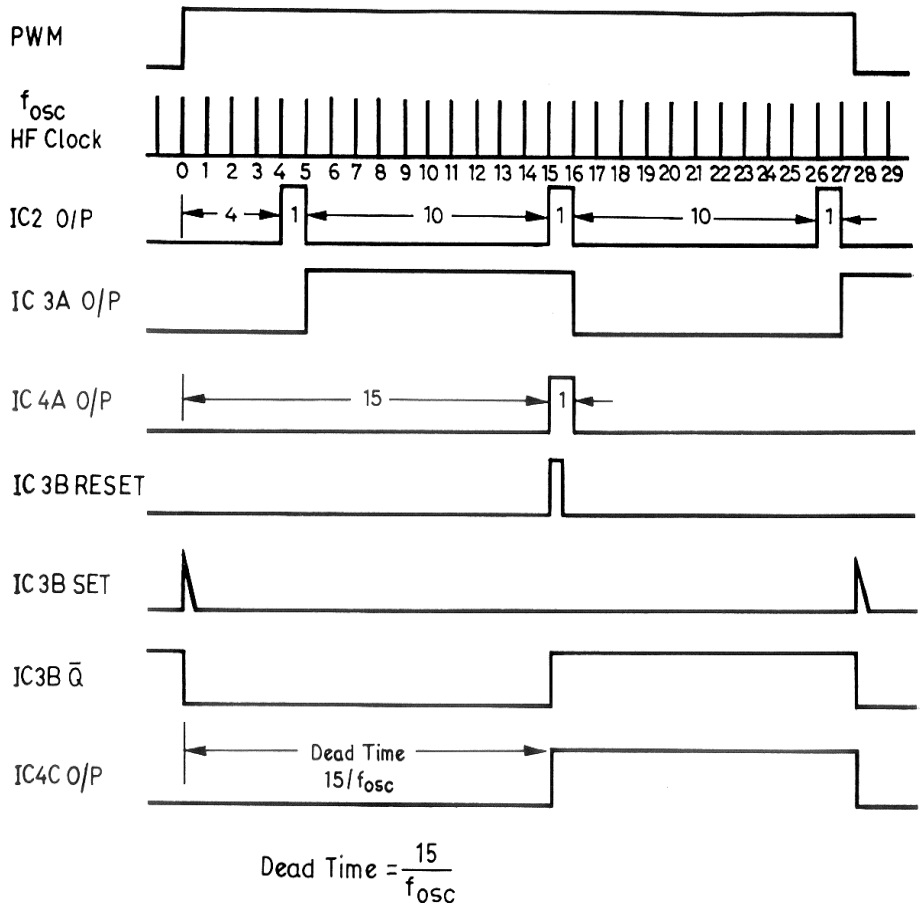

Fig.2.13. Waveforms at Various Points of a Digital Dead Time Circuit

Fig.2.13 shows the waveforms of this circuit at various points in the circuit. The waveforms from the actual circuit are shown in Fig. 2.14.

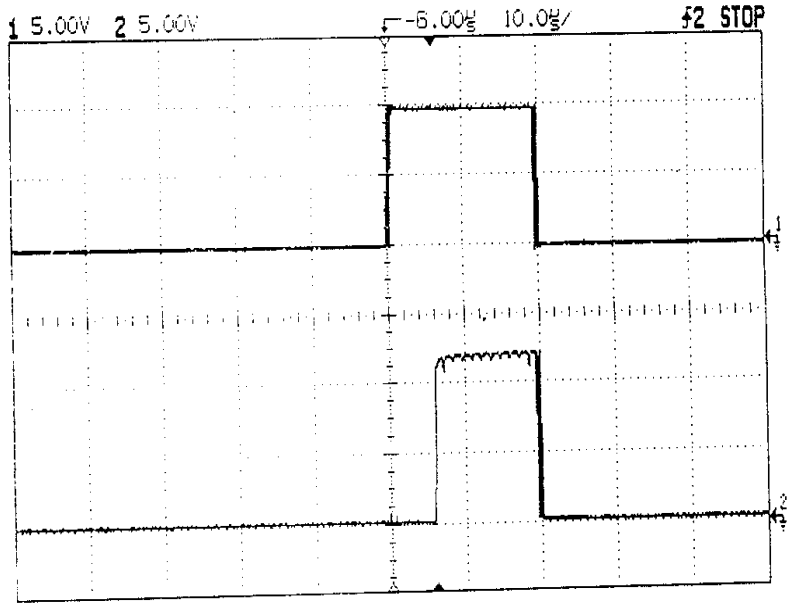

Fig.2.14. Actual Waveform at Input and Output of the Digital Dead Time Circuit

This circuit has the advantage that by varying the clock, the dead time can be generated to suit any device preferably which has switching times more than 1μs. This circuit can be easily hybridized.

2.3.1 Uses of dead time circuit for PWM generation

To generate sinusoidally pulse width modulated signal from dead time generator circuit, the PWM signal in Fig.2.12 can be replaced by a low notch width signal and f_{osc} is obtained from a VCO whose voltage input can be a sinusoidal signal. This can simplify the control circuitry for the generation of sinusoidally pulse width modulation. The conventional SPWM scheme using EPROMS and other digital circuits used in

programmed waveform PWM generation can be replaced by the above mentioned circuit. The circuit can be used in closed loop with inverter to generate sinusoidal PWM output voltage.

Another use of dead time circuit of Fig. 2.12 is that, since, the dead time depends on the frequency of f_{osc} (dead time = $15/f_{osc}$), by reducing the f_{osc} , the dead time can be increased. This strategy can be adopted in the event the short circuit occurs in the inverter output. By decreasing the dead time, pulse width is reduced to limit the short circuit current, and can be used for current control.

2.3.2 Effect of driver circuit delays on the output pulse

Very often the driver circuit has delays in the range of 0.5μs to 2μs depending on the device to be driven from it. Thus if a 5μs pulse is produced by the control circuit and the driver circuit has 1μs delay during pulse rise and 2μs delay during pulse fall, the resulting output pulse of the driver has its width increased by 1μs. Thus, when the switching frequency is high, a large number of pulses will have very small widths, which is expected to alter the low order harmonics, if this inaccuracy is included.

2.4 Inverter Performance with IGBT Switches

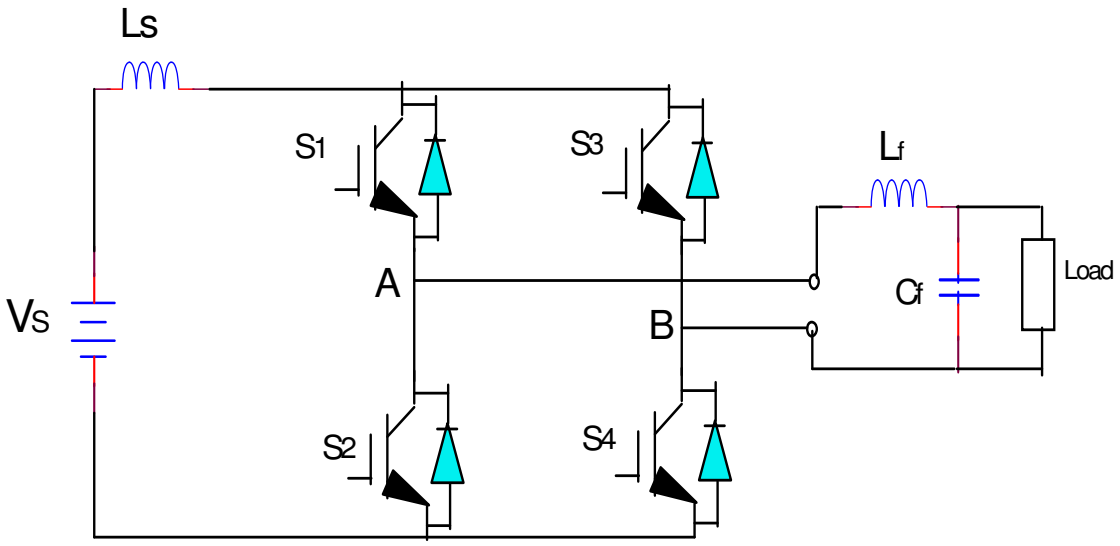

Fig.2.15 SPWM inverter with IGBT switches

Fig.2.15 shows a single phase SPWM voltage source inverter (VSI) topology with IGBT switches. The dc voltage Vs is assumed to be constant in magnitude. The magnitude and frequency of ac output voltage is achieved by various pulse width modulation schemes of the inverter switches. For the designed inverter, the sinusoidal pulse width modulation scheme is used to obtain the desired output voltage. In this control scheme a sinusoidal control signal at desired frequency is compared with a triangular waveform. The triangular waveform V_{tri} is at switching frequency f_s, which establishes the frequency at which the inverter switches are switched. The sinusoidal control signal $V_{control}$ is used to modulate the switch duty ratio and has a frequency f_1, which is the desired fundamental frequency of the inverter output voltage. The amplitude modulation ratio of the output voltage m_a is defined as

$$m_a = \frac{V_{control}}{V_{tri}} \tag{11}$$

The frequency modulation ratio m_f is defined as

$$m_f = \frac{f_s}{f_1} \tag{12}$$

The block diagram of PWM with unipolar voltage switching scheme is shown in Fig.2.16

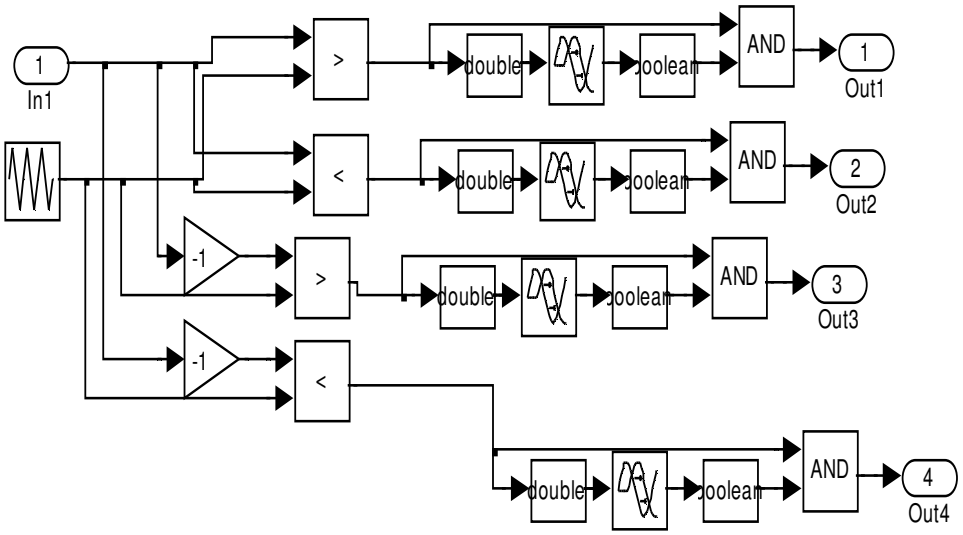

Fig.2.16 Control pulses with unipolar voltage switching for SPWM inverter switches

In this scheme, the switches in the two legs of the inverter are controlled separately by comparing V_{tri} with $V_{control}$ and -$V_{control}$ respectively.

The comparison of $V_{control}$ with the triangular waveform results in the following logic signals to control the switches in first leg:

$V_{control} > V_{tri}$: S_1 is gated on and $V_{AN} = V_s$

$V_{control} < V_{tri}$: S_2 is gated on and $V_{AN} = 0$

The comparison of $-V_{control}$ with the same triangular waveform results in the following logic signals to control the switches in the second leg:

$-V_{control} > V_{tri}$: S_3 is gated on and $V_{BN} = V_s$

$-V_{control} < V_{tri}$: S_4 is gated on and $V_{BN} = 0$

The control pulses for switches obtained with unipolar switching scheme are shown in Fig. 2.17. In this type of PWM scheme, when a switching occurs, the output voltage changes between zero and $+V_s$ or between zero and $-V_s$ voltage levels. The peak of the fundamental frequency component in the output voltage is given by:

$$v_{o1} = m_a V_s \qquad (m_a \leq 1.0) \tag{13}$$

The harmonics in the inverter output voltage waveform appears as sidebands, centered around the switching frequency and its multiples, that is, around m_f, $2m_f$, $3m_f$ and so on. In unipolar switching scheme the harmonics are centered around $2m_f$ and their multiples. The location of harmonics at higher frequency reduces the size of output filter components and makes the inverter control faster.

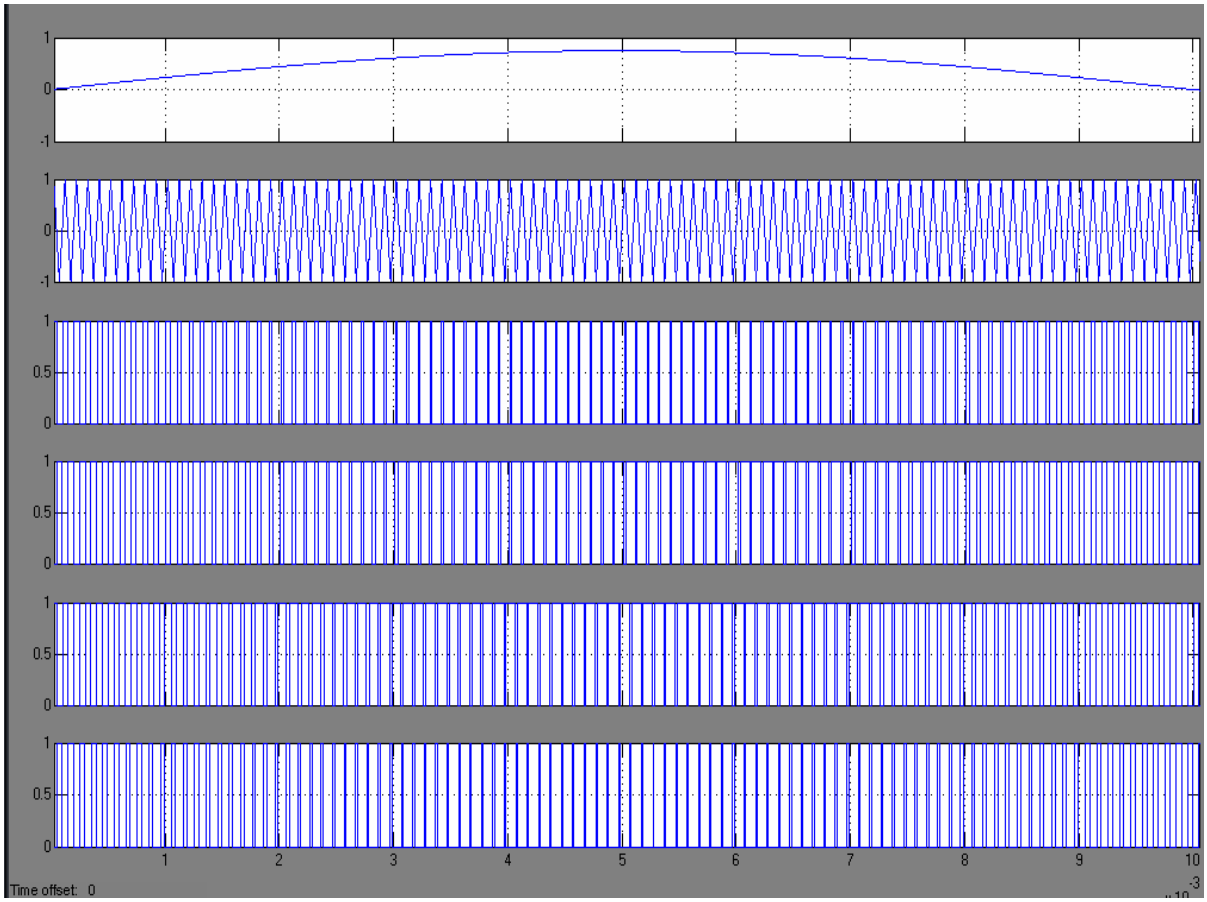

Fig.2.17 Generation of SPWM signals for switches with sine-triangle comparison

The frequency spectrum of the voltage V_{AB}, with the unipolar switching scheme at a switching frequency f_s =10 kHz is shown in Fig.2.18.

The harmonics in the inverter output voltage waveform V_{AB} around $2f_s$, $4f_s$ and $6f_s$, are shown in Fig.2.19, Fig.2.20, and Fig.2.21 respectively. The dc link voltage is 100V.

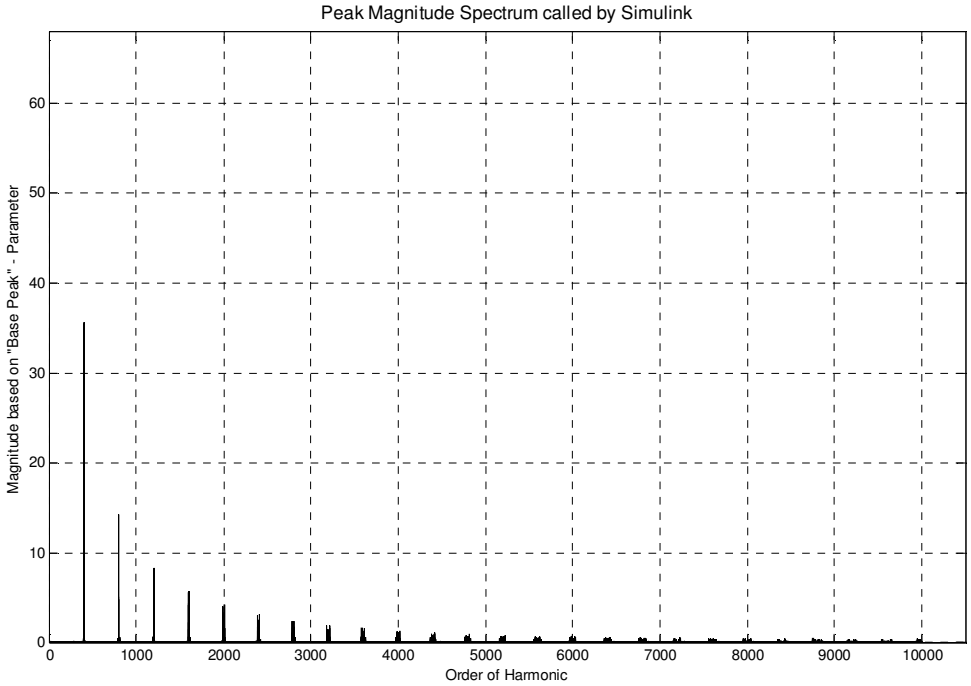

Fig.2.18. Frequency spectrum of V_{AB} (magnitude is in volts, m_a =0.75)

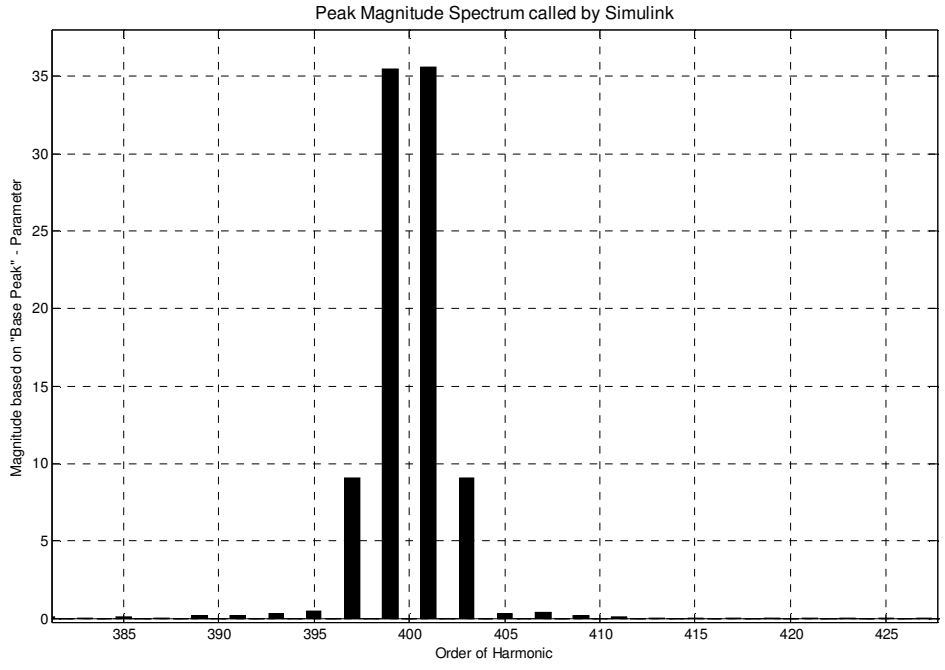

Fig. 2.19 Harmonic spectrum of V_{AB} around $2f_s$ (magnitude is in volts, m_a =0.75)

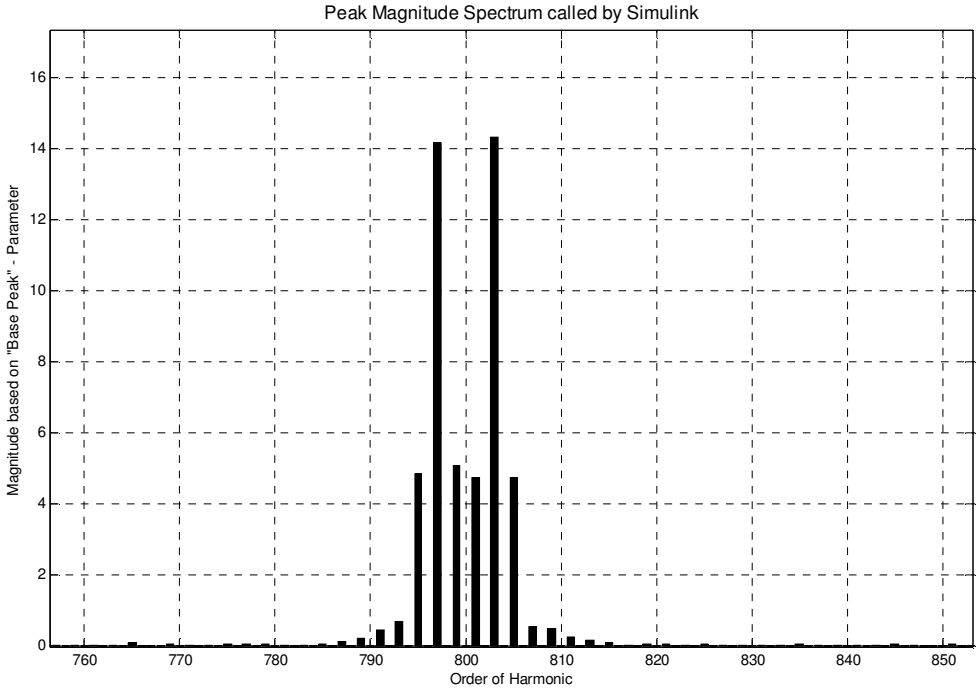

Fig.2.20 Harmonic spectrum of V_{AB} around $4f_s$ (magnitude is in volts, m_a =0.75)

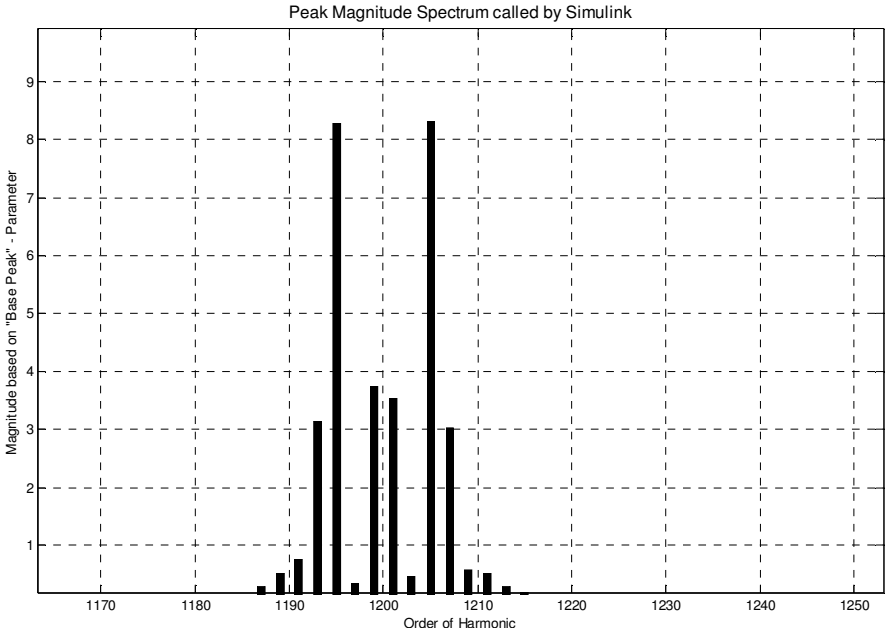

Fig. 2.21 Harmonic spectrum of V_{AB} around $6f_s$ (magnitude is in volts, m_a =0.75)

Lower order harmonics generated at this switching frequency is shown in Fig.2.22.

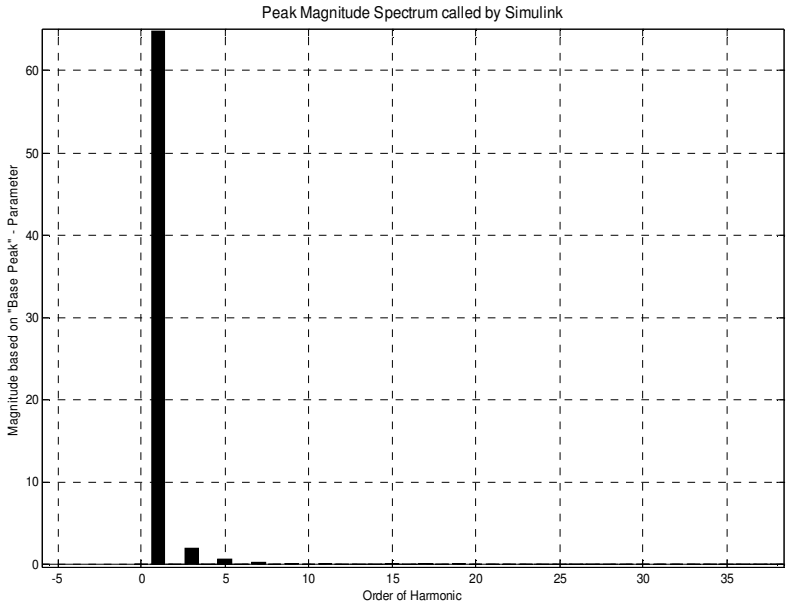

Fig.2.22 Lower order harmonics of V_{AB} (magnitude is in volts, m_a =0.75)

As the pulse rise and fall times are influenced by the source inductor L_s and the capacitor C, in addition to the pulse overshoot and undershoot, it is particularly important to minimize any stray inductance in the circuit, between dc link and the devices, between device and device and between the device and snubber components. The overshoot in the pulses for the designed inverter is shown in Fig.2.23.

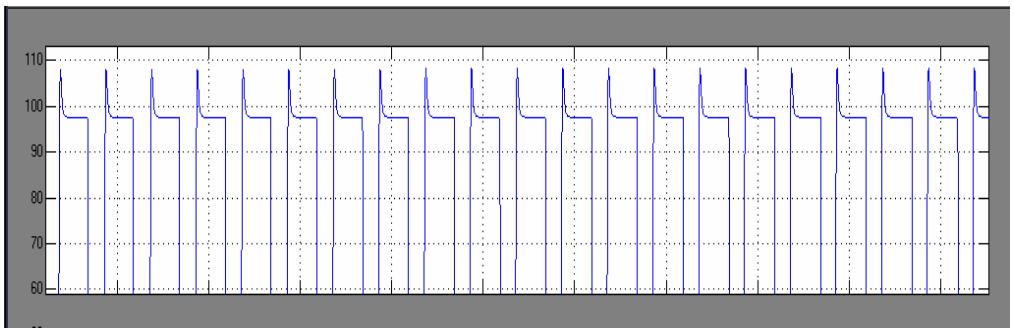

Fig.2.23 Overshoot of voltage V_{AB}(magnitude is in volts, m_a =0.75, I_L= 10A, f_s =10kHz)

2.5 Filter Design

To keep the total harmonic distortion (THD) less than 3% at load, the output filter components L_f and C_f are designed. Filter inductor is designed such that about 1-2% of output nominal voltage drops across the filter inductor at the rated load current. It is given by

$$I_{rms} \times 2\pi f \times L_f = 0.01 \times V_{rms}(no\,\min al) \tag{14}$$

Taking resonant frequency as 1/6th of twice the switching frequency f_s , the filter capacitor is designed using the expression given by

$$\frac{1}{2\pi\sqrt{L_f C_f}} = \frac{1}{6}(2f_s) \tag{15}$$

Also, value of the filter capacitor is adjusted taking into account the effect of load and the worst case harmonic content in the inverter output, so as to get a THD of less than 3% at load. The frequency spectrum of load voltage is shown in Fig.2.24.

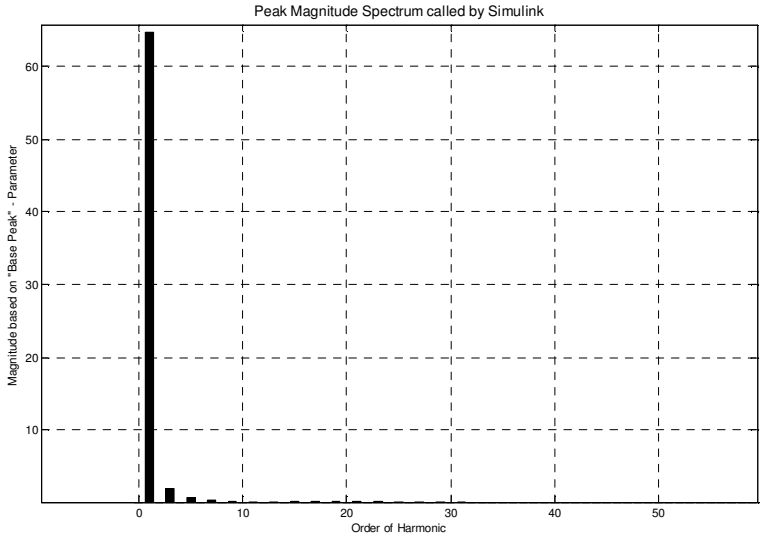

Fig.2.24 Frequency spectrum of output voltage (magnitude is in volts, m_a =0.75, m_f =200)

The inverter output voltage V_{AB} with load voltage and current with a suitable filter design is shown in Fig.2.25. The total harmonic distortion is 2.97%, which is within the specified limit. The harmonic content is shown in table 2.3.

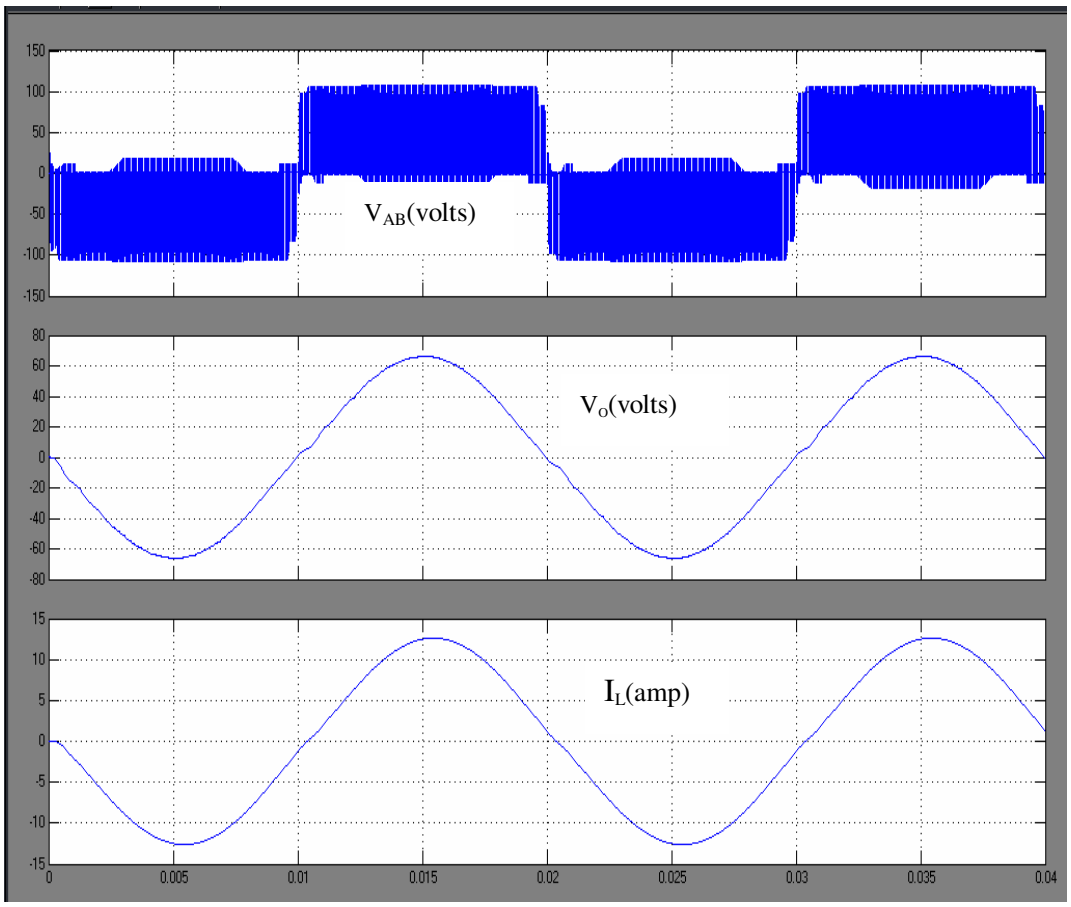

Fig.2.25 Load voltage and current waveforms with inverter output voltage V_{AB}

Table 2.3
Frequency spectrum magnitude of V_{AB} in terms of % of fundamental (m_a =0.75, m_f =200)

Harmonic order	Magnitude
3^{rd}	2.7
5^{th}	1.2
7^{th}	0.3
$2f_s$-1	54.9
$2f_s$+1	54.1
$2f_s$-3	13.9
$2f_s$+3	14.17
$4f_s$-1	7.9
$4f_s$+1	6.79
$4f_s$-3	21.53
$4f_s$+3	22.02

2.6 Output Voltage Control with Variation in Modulation Index

The modulation index of the control signal is adjusted such that the rms output fundamental voltage is equal to

$$V_o \approx \frac{V_{DC} - 2\times V_{SW} - V_L}{\sqrt{2}} \times m_a \tag{16}$$

Where, V_{DC} is the dc link voltage, V_{SW} is the switch drop at full load which is generally 1 to 2 volts, V_L is the average inductor voltage (about 1% of the filter output voltage), m_a is the modulation index (MI).

Block diagram for the proposed method is shown in Fig.2.26

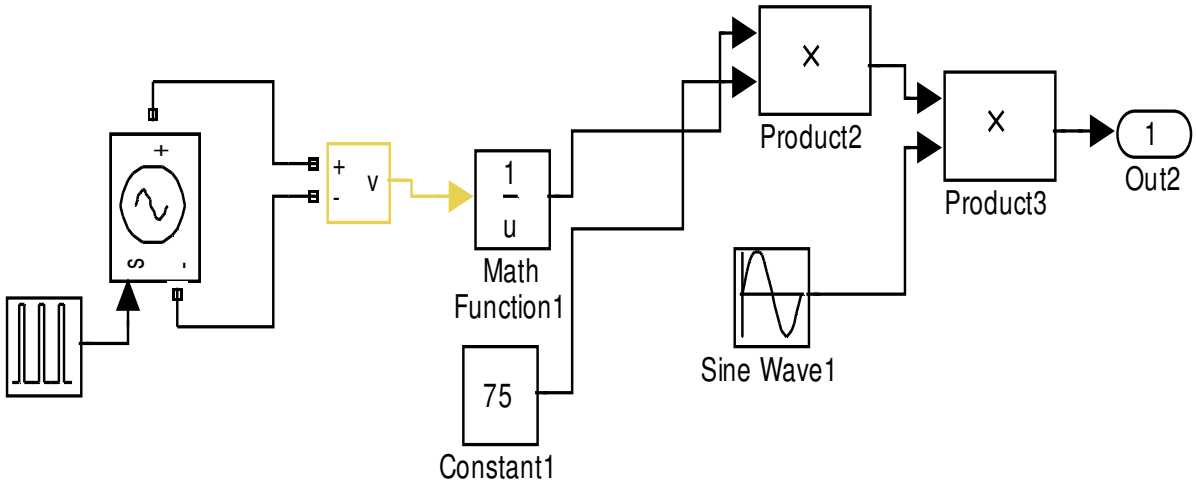

Fig.2.26 Control Scheme for Voltage control using MI

Output voltage and current waveforms with V_{AB} for SPWM inverter with control and without control are shown in Fig.2.27 and Fig.2.28 respectively. With this method the output voltage sensing and implementation of PI controller is dispensed with.

This control strategy responds almost instantly, as seen from the output voltage waveform with control.

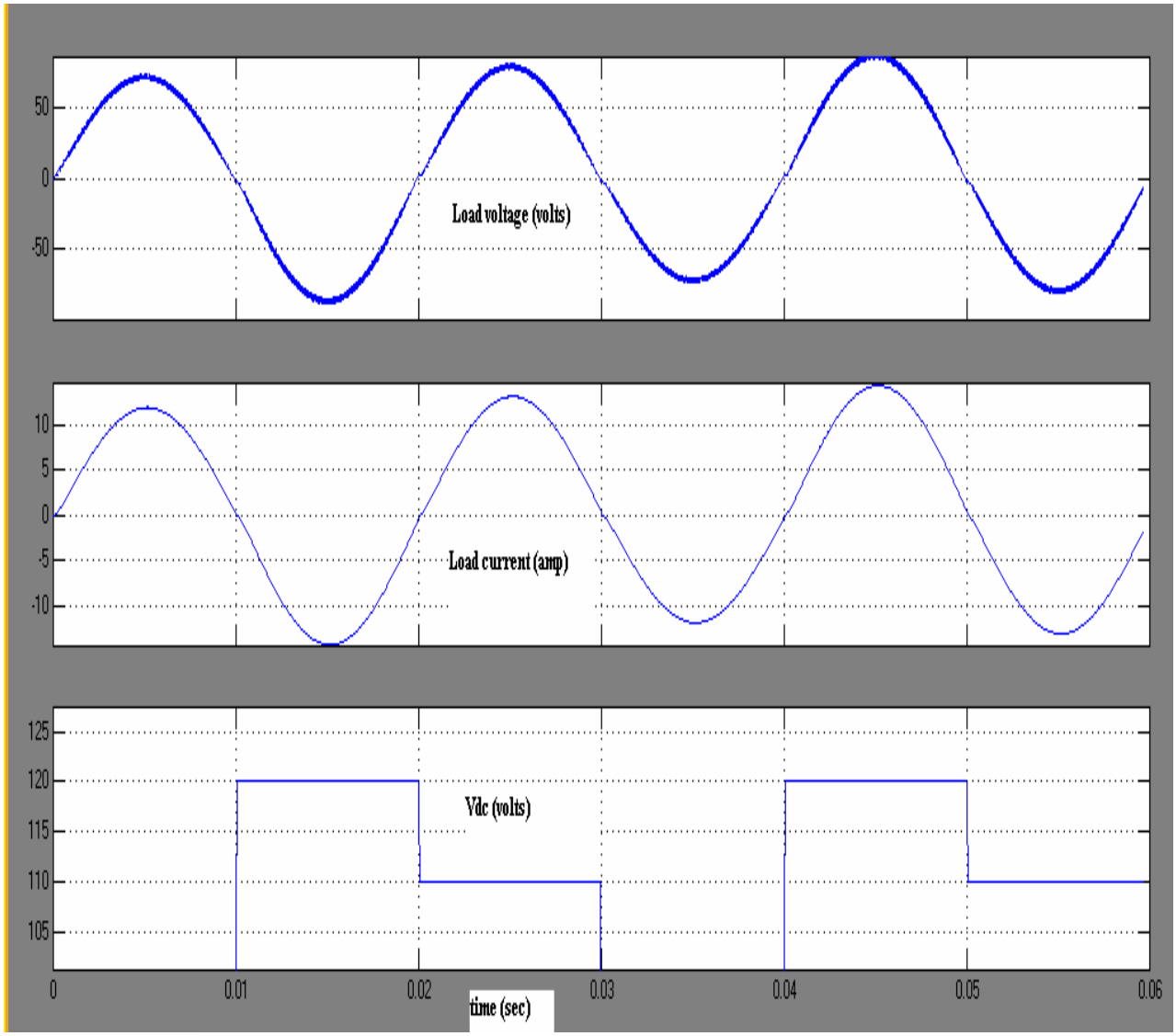

Fig. 2.27 Load voltage and current waveform with change in input (V_{DC}) without control

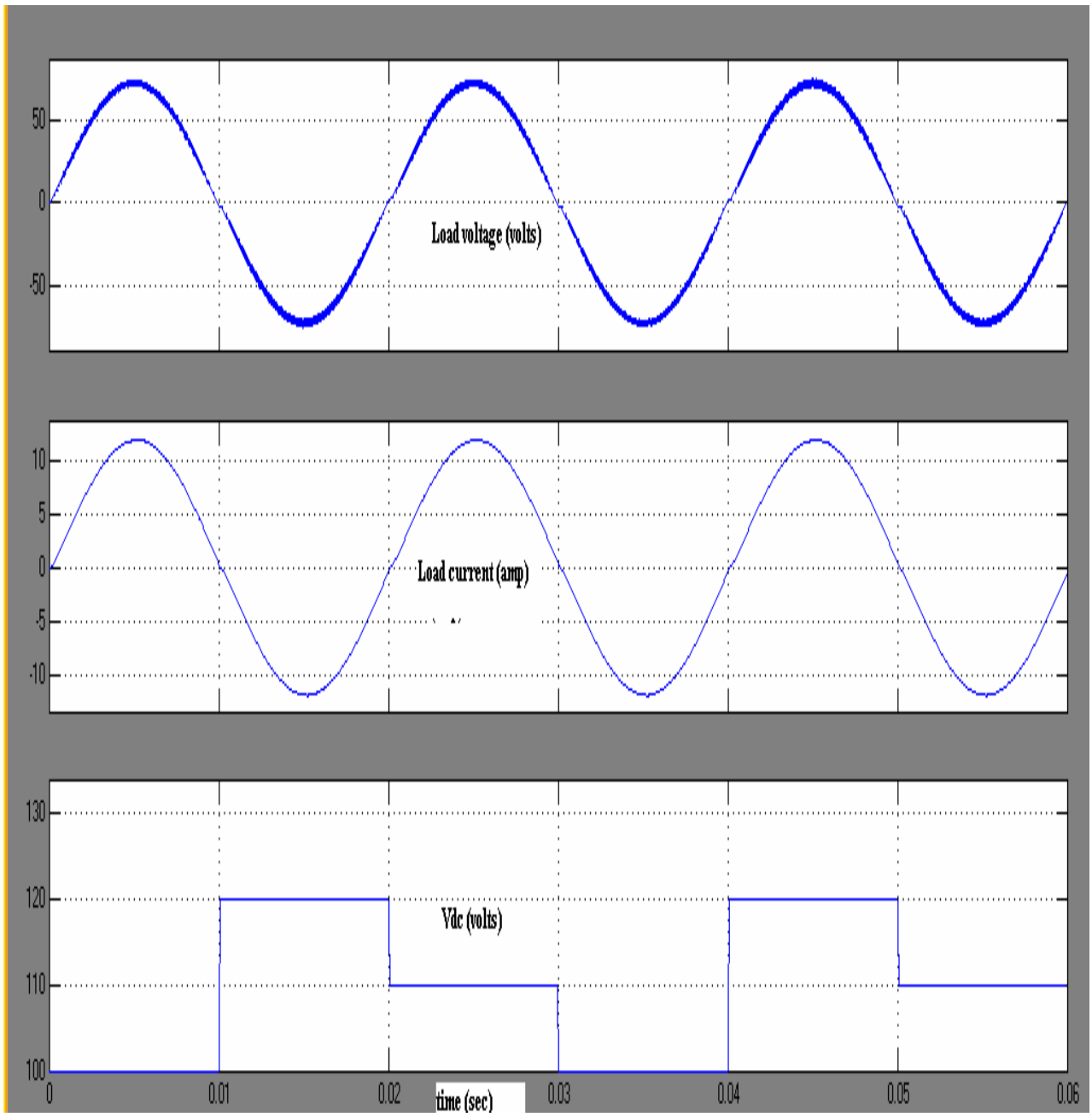

Fig.2.28 Load voltage and current waveform with change in input (V_{DC}) with control

2.7 Parameters for the designed SPWM inverter

V_{DC} = 100V

Modulation Index (MI) = 0.75

Switching frequency (f_s) = 10 kHz

Frequency of load voltage = 50 Hz

L_s = 5µH

Snubber Resistance = 22Ω

Snubber Capacitance = 0.1µF

Load current I_{load} = 10 A(rms); R_{load} = 5Ω, L_{load} = 1mH

Inverter Output Voltage (V_{AB}) parameters:

Rise time t_{rise} = 1.3µs at I_L = 10A.

Fall time t_{fall} = 0.9µs at I_L = 10A.

Voltage Overshoot = 8V

Voltage Undershoot = 2.2V

IGBT Device Parameters:

R_{on} = 0.001Ω, L_{on} = 1nH

Forward Voltage (V_f) = 1V

Current Fall Time (t_f) = 0.5µS

Current tail Time (T_t) = 1µS

Output Filter Parameters:

Filter Inductor L_f = 225µH

Filter Capacitor C_f = 10µF

2.8 Conclusions

Two topologies of SPWM inverters, one using Hybrid Darlington switches and other using IGBT switches are discussed. Former utilizes stored SPWM waveform as the control pulse for its switches and later the sine-triangle comparison method to generate control pulses for its switches. Rise and fall time with voltage overshoot and undershoot of the inverter output voltage V_{AB} is measured in both the cases and it is found that some variations are there due to different switching times of both the switches. Output filter is designed to keep the THD less than 3%. Lower order harmonics and harmonics at side-bands are seen from the frequency spectrum in both cases and it is found that they are nearly equal. The sine-triangle comparison method has an advantage over stored SPWM technique with respect to the side-bands of the harmonic components. In stored SPWM technique, the side-band occurs around f_s and its multiples but in sine-triangle comparison it occurs around 2fs, leading to smaller size of output filter components.

A simple control scheme using modulation index variation is presented to control the variation in output voltage. Also, the dead time circuits suitable for different types of devices are presented.