Chapter 5. Experimental Results and Discussion of ZVT Topology

5.1 Introduction

A single phase SPWM inverter discussed in chapter2 is designed and an experimental set-up is established to verify the design to achieve an output voltage with a total harmonic distortion less than 3%. Spectrum of output voltage with different filter capacitor values is presented to see the effect of filter parameter on the output voltage distortion. Unipolar switching scheme is used for the switching instants of the MOSFET switches.

To verify the concept of resonant snubber based soft-switching technique, an experimental set-up for a ZVT converter with reduced voltage and current rating is presented. It demonstrates zero-voltage turn-on in one pair of switches. Control pulses for main and resonant snubber branch switches were generated using available IC LM555 and LM 3525. For isolation purpose pulse transformer with suitable pot core and turns ratio is designed. IGBTs are chosen as main and auxiliary switches with low current ratings. Also suitable diodes for auxiliary branch were selected to reduce the reverse recovery problem.

5.2 Single-phase SPWM Inverter

Fig. 5.1 shows a single phase full bridge inverter topology with output filter and an R-L load. S1-S4 are the main switches and V_D is the source voltage. Inverter output voltage V_{AB} is shown in Fig. 5.2.

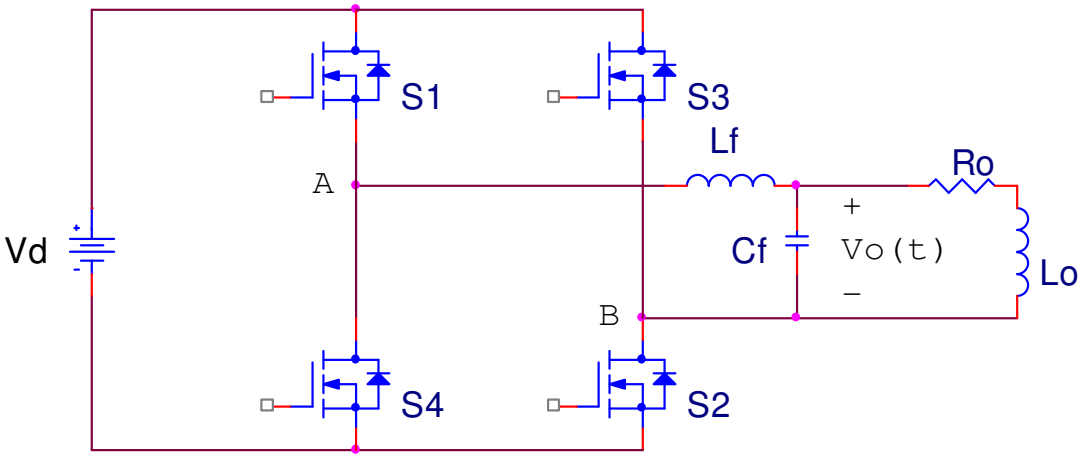

Fig. 5.1 Single-phase SPWM Inverter

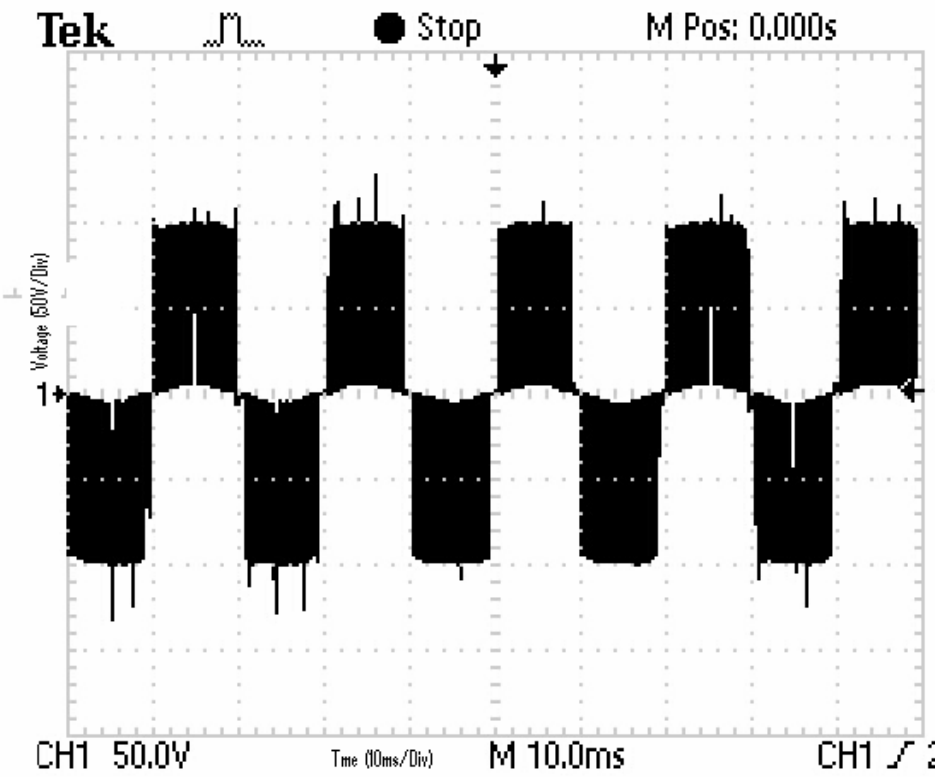

Fig. 5.2 Inverter output voltage V_{AB}

Switching Signals

Switching signals for the switches S1-S4 are generated by comparing a sinusoidal signal (modulating signal) of 50 Hz with a triangular signal (carrier signal) of high frequency. The frequency of triangular signal is chosen as 10 kHz for the experiment. Fig. 5.3 shows sine and triangle signals generated by IC 8038 for a modulation index of 0.8. Gate pulses for switches S1, S2 and S3, S4 are shown in Fig. 5.4 and Fig. 5.5 respectively.

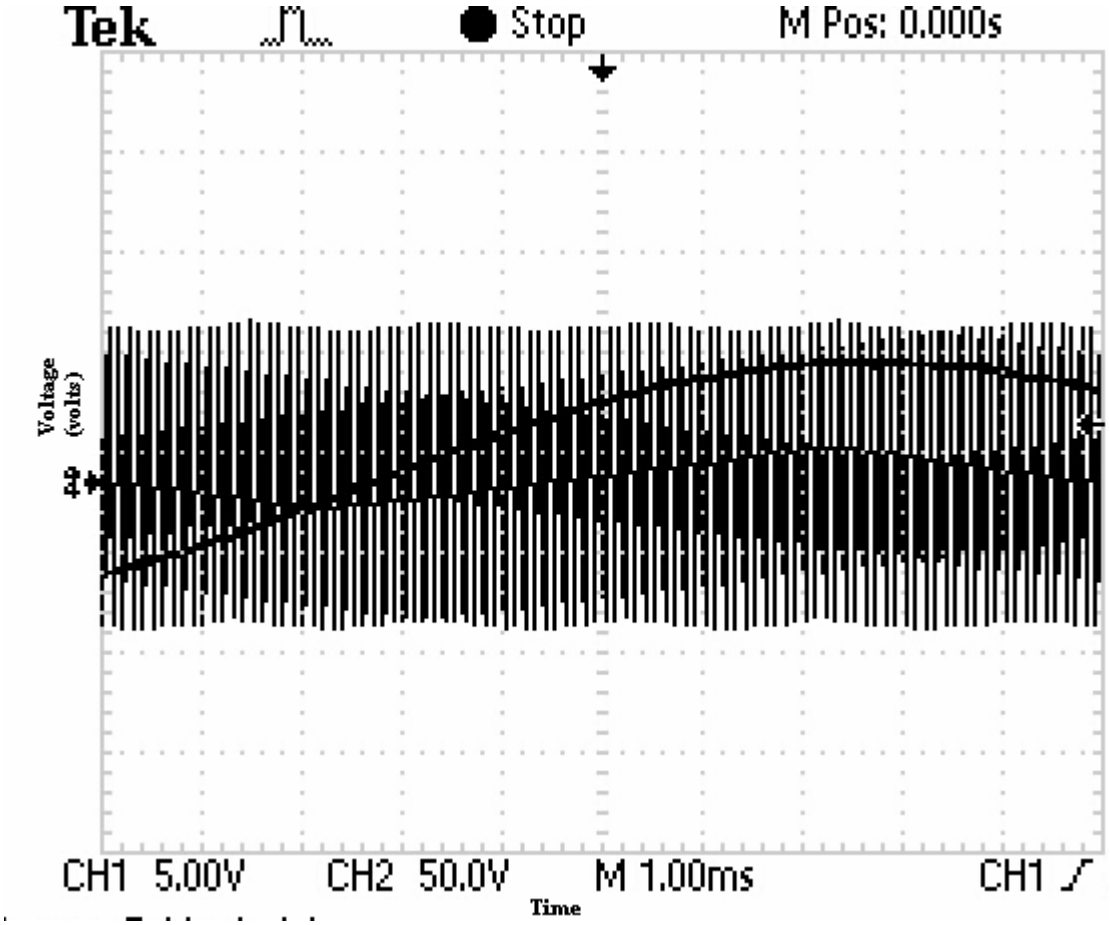

Fig. 5.3 Sine and Triangle signals for a Modulation index of 0.8

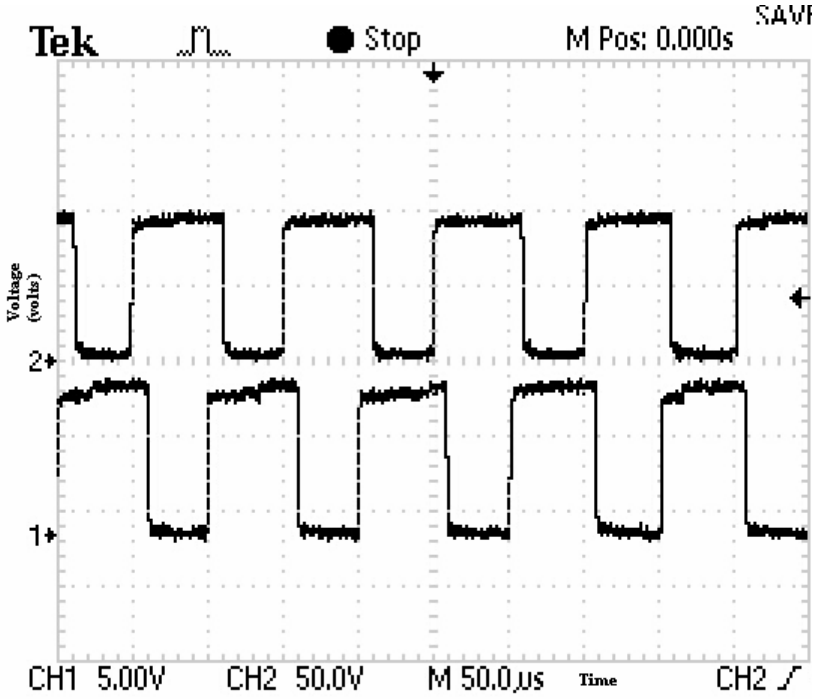

Fig. 5.4 Gate pulses for switches S1, S2

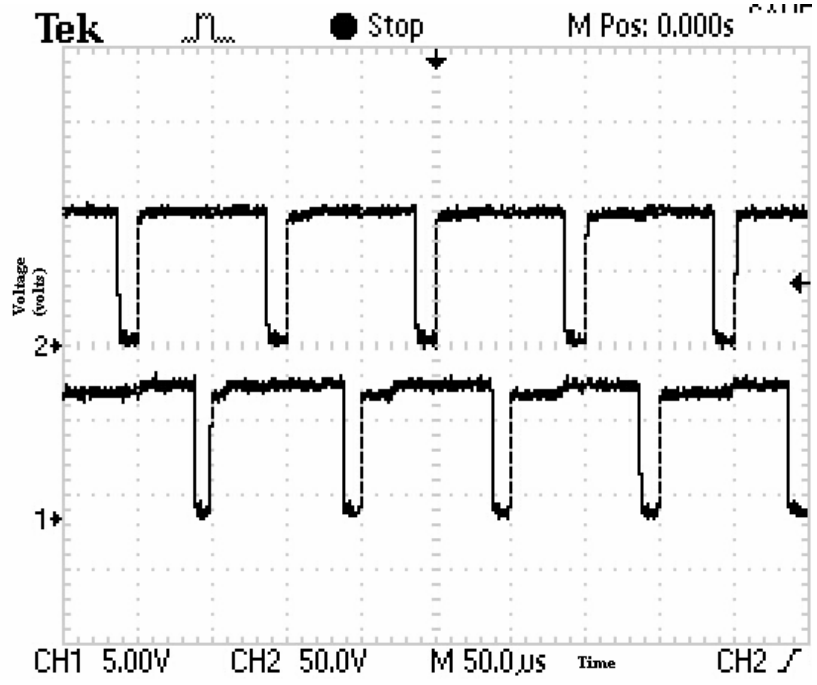

Fig. 5.5 Gate pulses for switches S3, S4

Output Voltage and Harmonic Spectrum

Load voltage for an R-L load with a current of 2A (rms) is shown in Fig. 5.6. Output filter is designed to keep the THD less than 3%. Lower order frequency spectrums at various values of output filter capacitances are shown in Fig. 5.7, Fig. 5.8 and Fig. 5.9. The spectrum shows that the specified value of THD is achieved at a higher value of filter capacitor than the theoretical one.

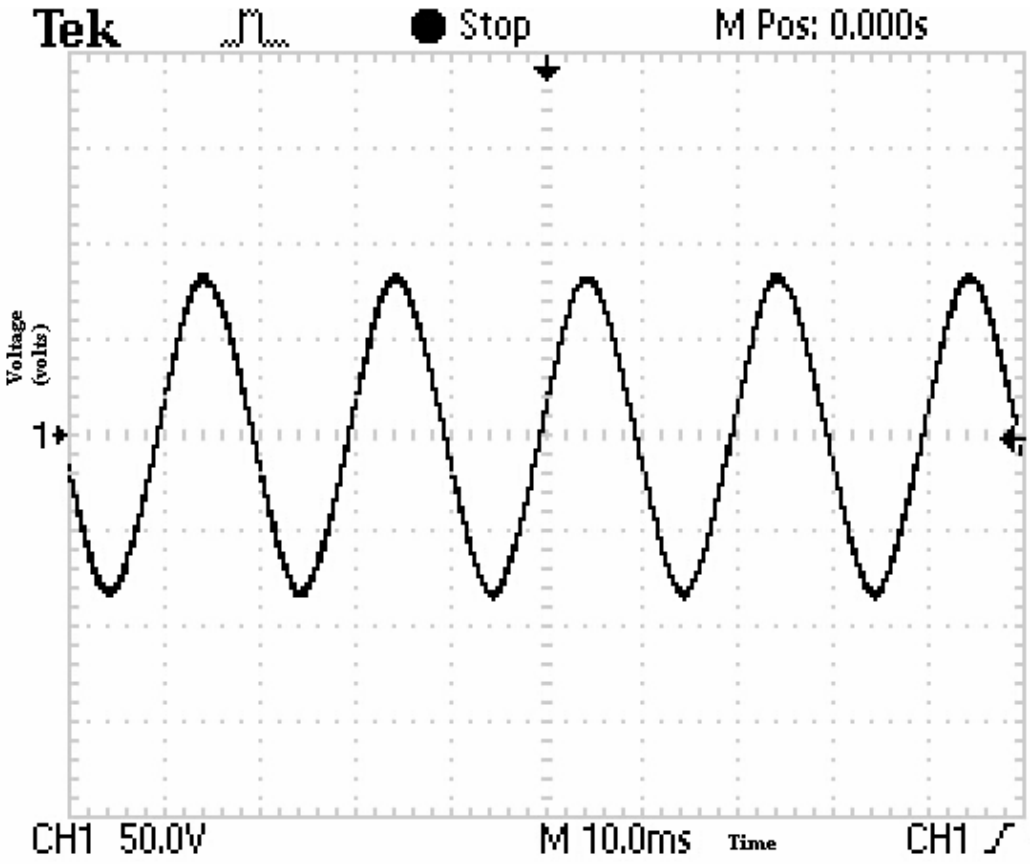

Fig. 5.6 Load voltage

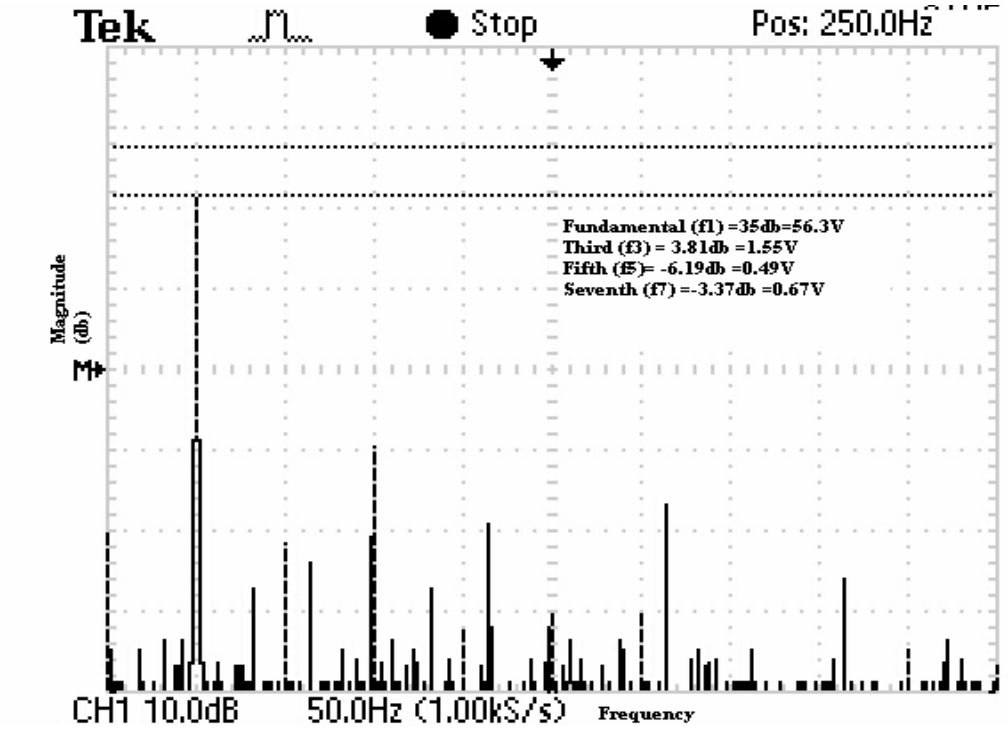

Fig. 5.7 Frequency spectrum at filter capacitor of 5μF

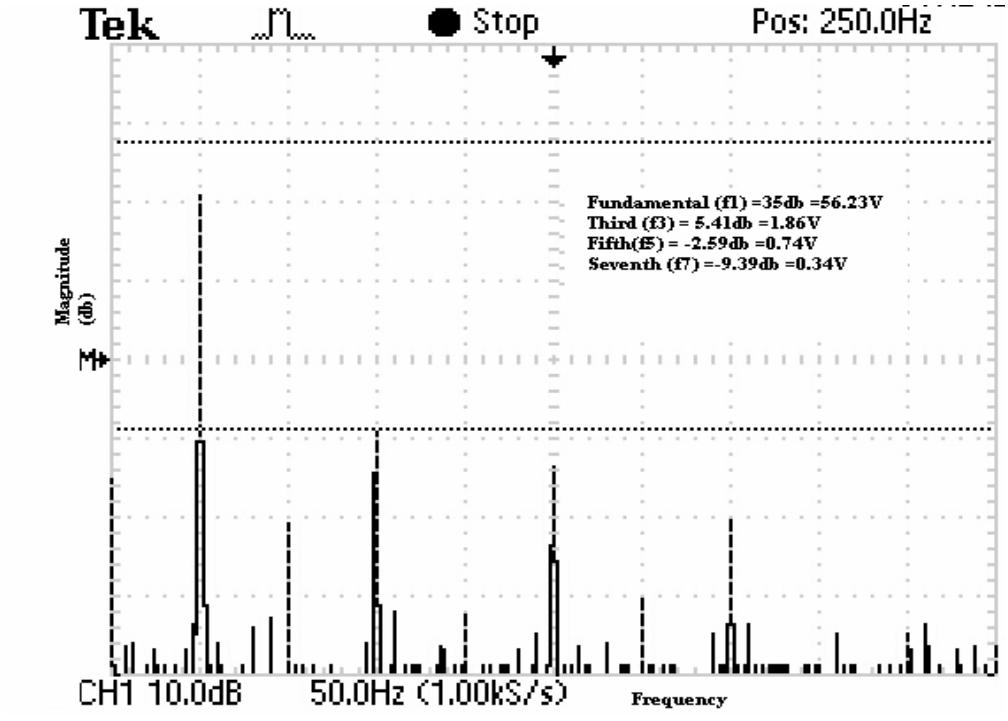

Fig. 5.8 Frequency spectrum at filter capacitor of 4μF

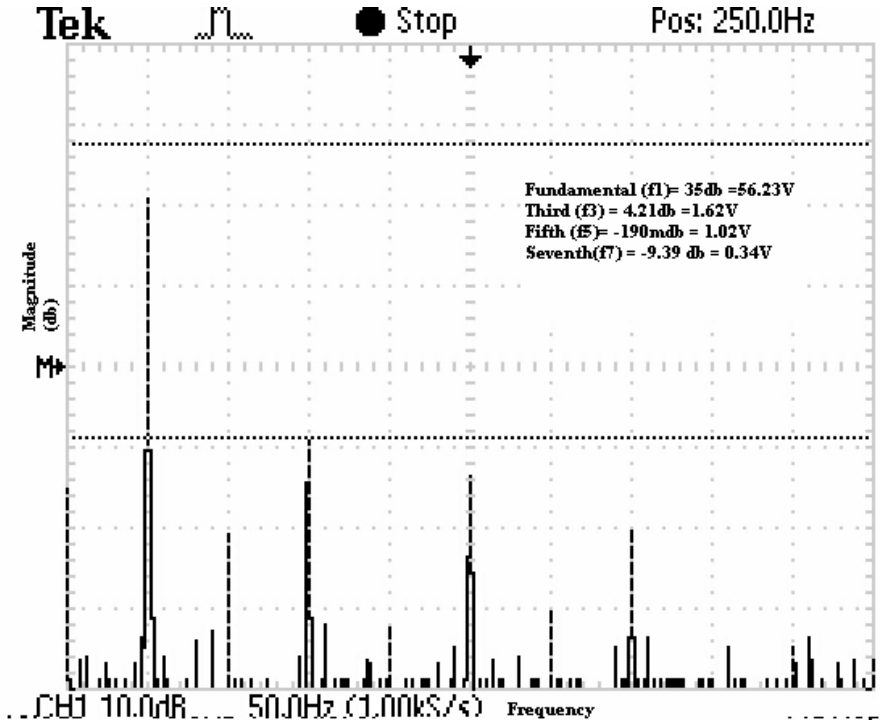

Fig. 5.9 Frequency spectrum at filter capacitor of 4μF

Table 5.1
Harmonic order of load voltage

Filter Parameter	Harmonic order (% of fundamental)		
L_f (μH) , C_f (μF)	3rd	5th	7th
400, 5	2.75	0.08	1.19
400, 4	3.31	1.31	0.06
400, 3	2.88	1.81	0.08

The frequency spectrum at $2f_s$ and its multiple is shown in Fig. 5.10.

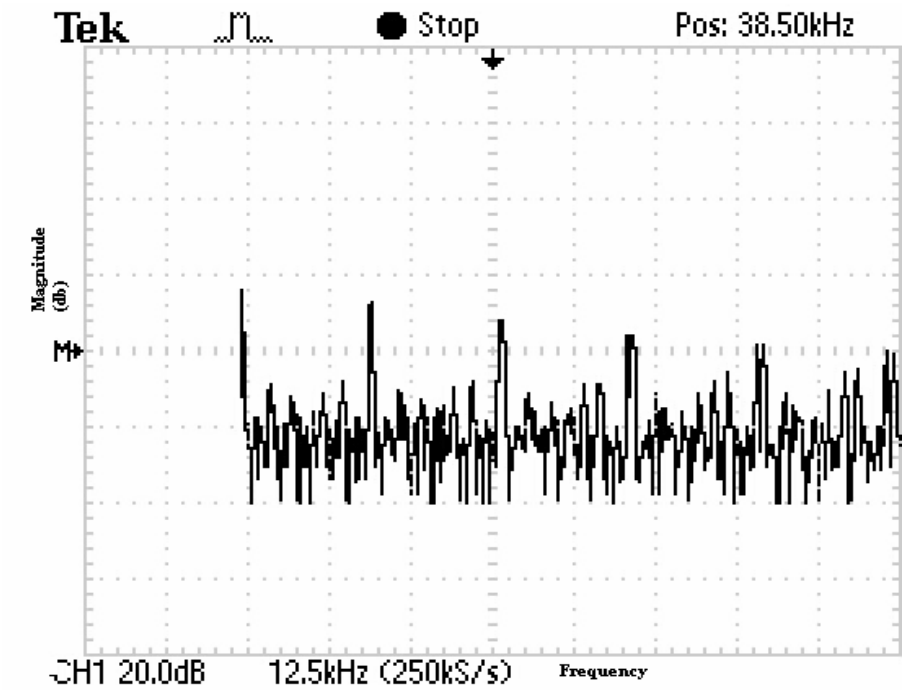

Fig. 5.10 Frequency spectrum of V_{AB} at $2f_s$, and its multiple (without filter)

5.3 Experimental Details:

5.3.1 Control Circuit:

Sine and triangular wave generation: Using IC 8038 both sine and triangular waveforms are generated.

The frequency of the waveform is given by

$$f = 0.15/RC$$

Selecting suitable values of resistor and capacitor, a sine of 50 Hz and a triangle of 10 kHz can be generated. Pin configuration for IC 8038 is given in Fig. 5.11

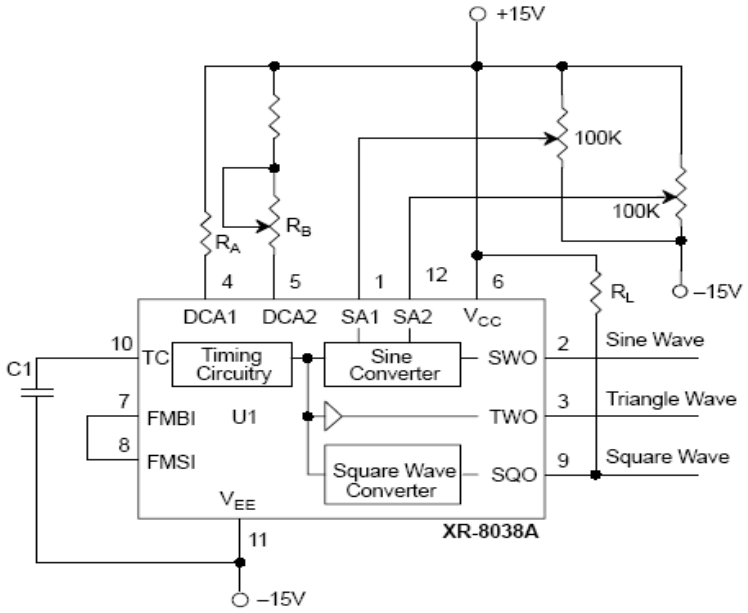

Fig. 5.11 Pin configuration of IC 8038

Comparator:

The comparator produces the SPWM signal by comparing the sine and the triangle signals. Fig 5.12 shows the schematic circuit of LM311 comparator.

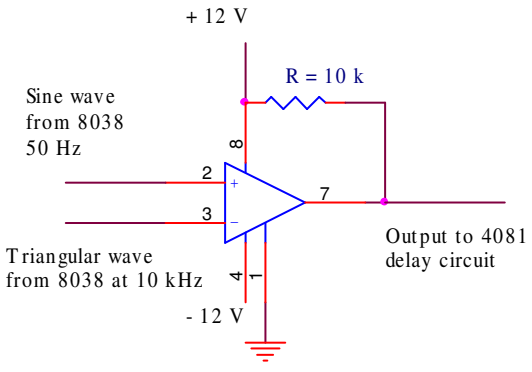

Fig. 5.12 LM311 Comparator

Dead Time Circuit:

A dead time of around 1μs is introduced using a dead time circuit shown in Fig. 5.13.

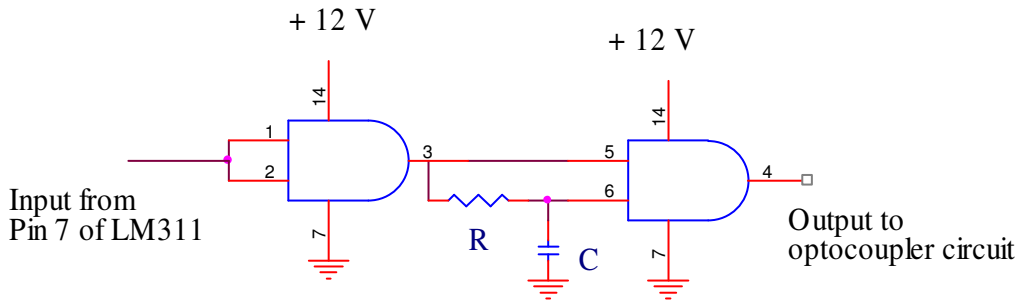

Fig. 5.13 Dead time circuit (R = 330 Ω, C = 0.01 μF)

Inversion of Sine Wave:

IC 4069 is used for the inversion of sine wave shown in Fig. 5.14

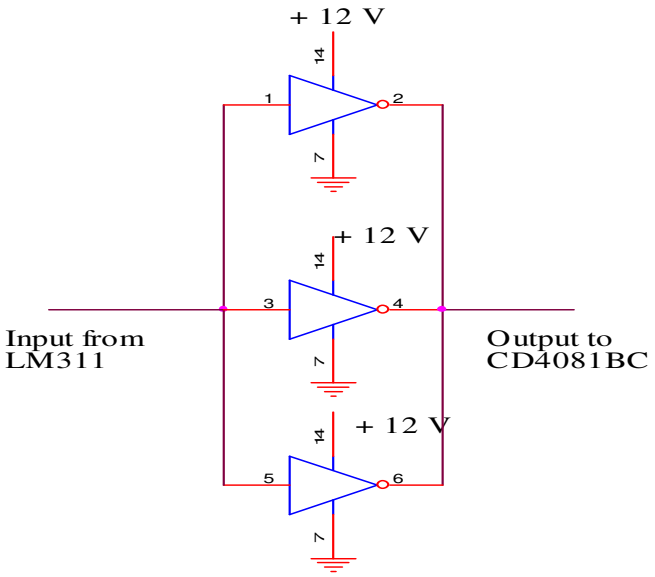

Fig. 5.14 NOT gate for PWM inversion

Driver Circuit:

A driver circuit using an optocoupler is shown in Fig. 5.15.

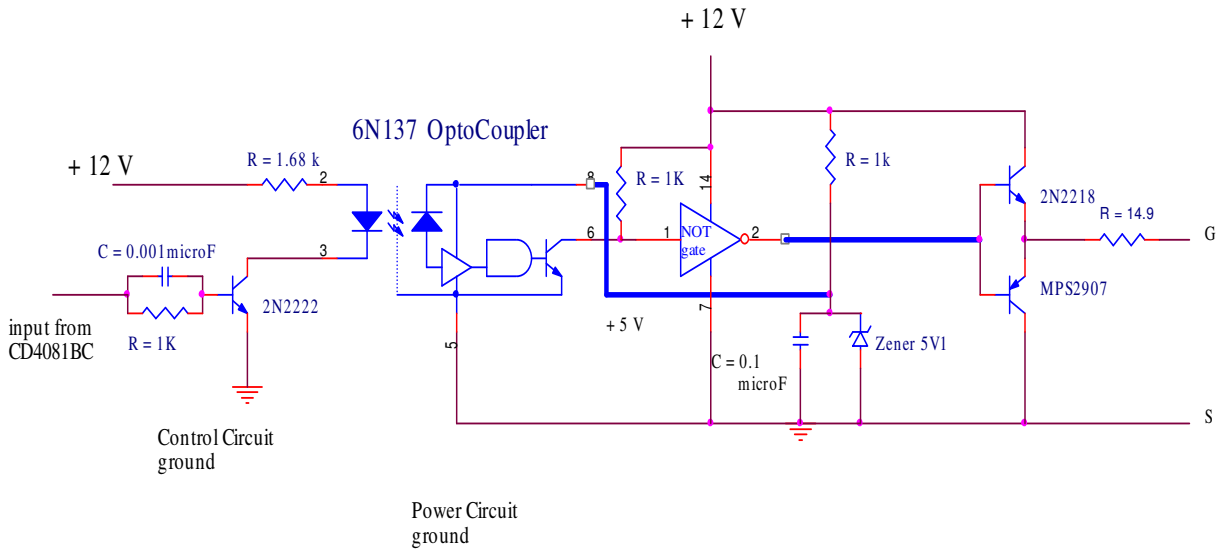

Fig.5.15. Gate driver circuit for MOSFET switches

5.3.2 Experimental Data:

Source Voltage (V_D) = 100V

Load Current 2A (rms)

Output Filter Parameter: L_f = 400µH; C_f = 4µF

Snubber parameters: R=22Ω: C=22nF

Switches (S1-S4): MOSFET (IRF 460)

5.4. ZVT Topology

A MATLAB/SIMULINK model of resonant snubber based soft-switching topology is shown in Fig. 5.16. For the analysis purpose IGBT and diode models are taken from the library of SIMULINK (SimPowerSystems/Power Electronics).

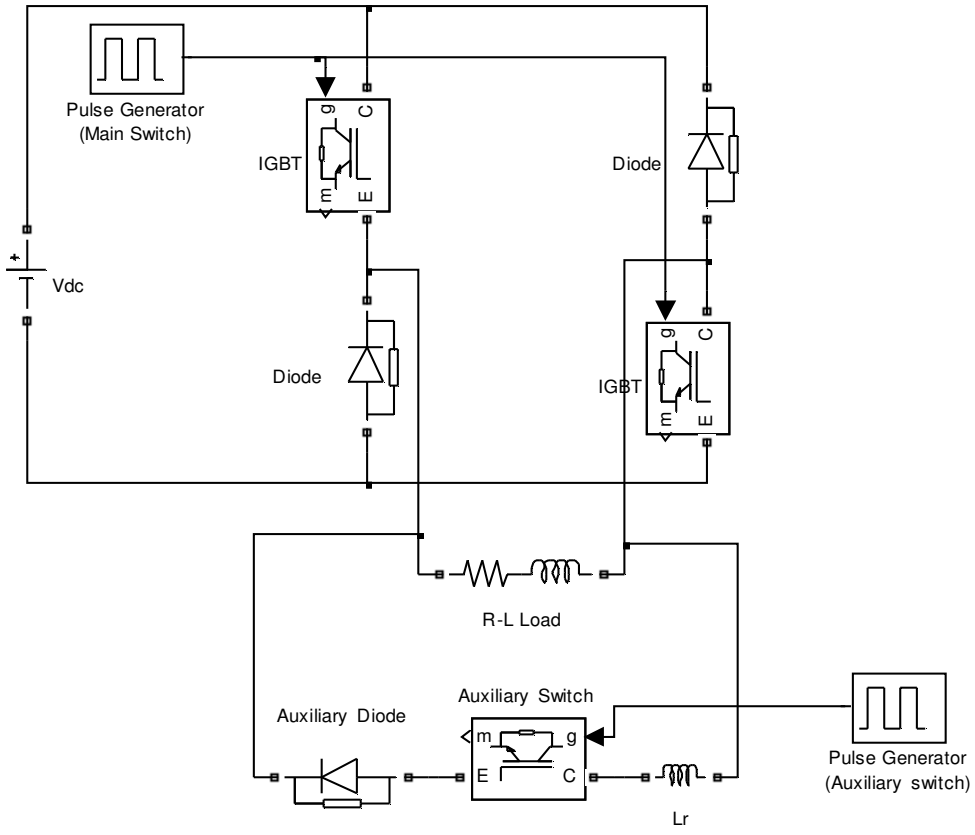

Fig. 5.16 Resonant snubber based soft-switching topology

Soft-switching for the main switches (IGBT) is achieved by connecting an auxiliary branch parallel to the load. Auxiliary branch consists of an auxiliary switch connected in series with resonant inductor and an auxiliary diode.

Detailed operating principle and design methodology for inverter topology is discussed in chapter3. Here, to achieve the zero voltage switching during turn-on for one leg of the main switches, a ZVT converter topology is first simulated using SIMULINK and then it is experimentally verified. Experimental results validate the design and simulation results obtained. Experimental results are carried out under reduced voltage and current rating due to laboratory constraints.

5.4.1 Simulation Results

Device voltage and device current for the main switches during hard switched turn-on condition is shown in Fig. 5.17.

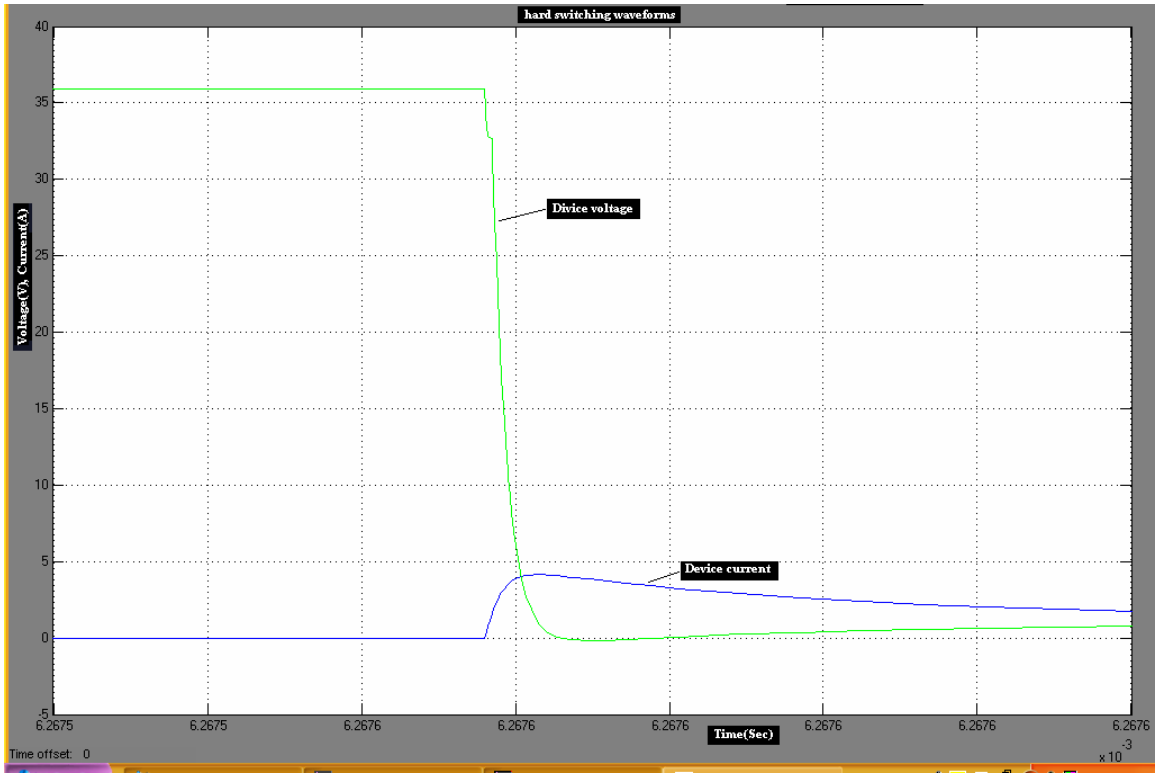

Fig. 5.17 Device voltage and current for the main switches during hard switching (turn-on)

Overlap between voltage and current during turn-on can be easily seen which gives rise to turn-on switching losses. To reduce this overlap, an auxiliary branch is connected in parallel to the load which creates zero-voltage condition during turn-on. Fig. 5.18 shows the gate pulses for main and auxiliary switches with device voltage and current during turn-on for ZVT.

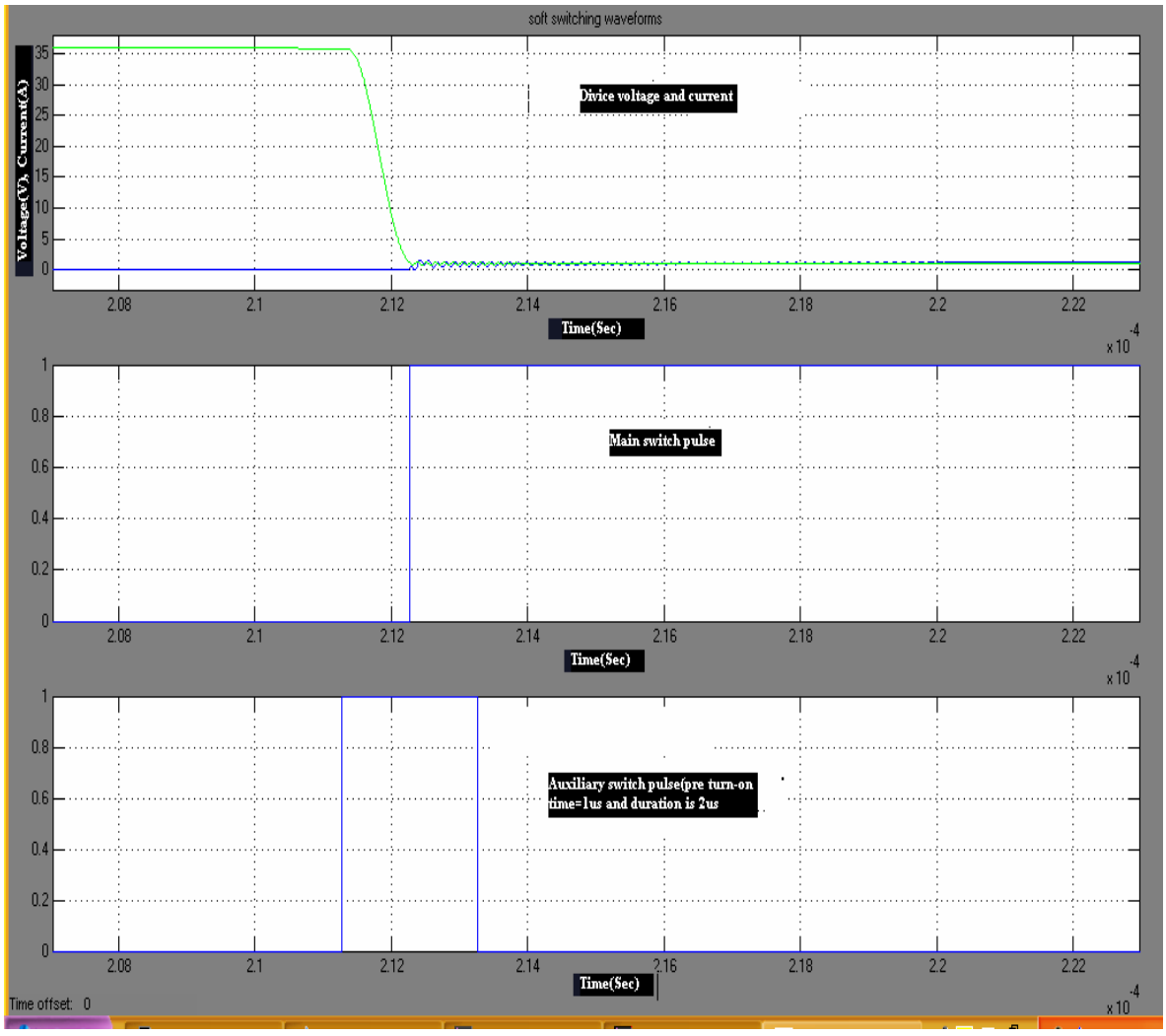

Fig. 5.18 Device voltage and current with main switch and auxiliary switch pulse (turn-on)

The pre turn-on time for the auxiliary switch pulse is calculated to be 1μs and duration of auxiliary pulse is 2μs.

The build up of current in the resonant inductor when the auxiliary switch is turned-on is shown in Fig. 5.19. The peak resonant inductor current is limited to a specified value by proper selection of resonant inductor (L_r) and resonant capacitor (C_r) value.

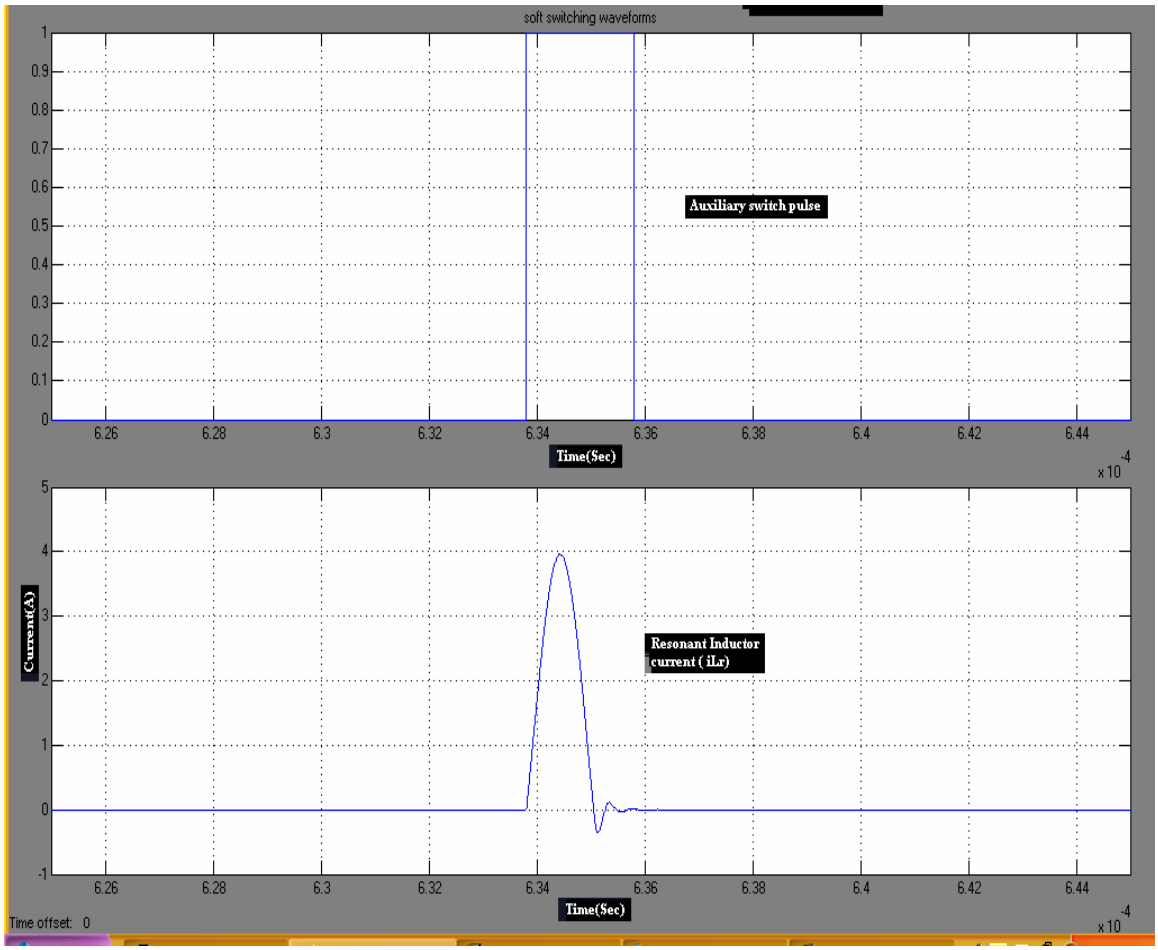

Fig. 5.19 Resonant inductor current build up when auxiliary switch is on

When the resonant inductor current becomes equal to the load current resonance starts and device voltage swings to zero at the end of resonant period. This transition of device voltage with resonant inductor current is shown Fig. 5.20.

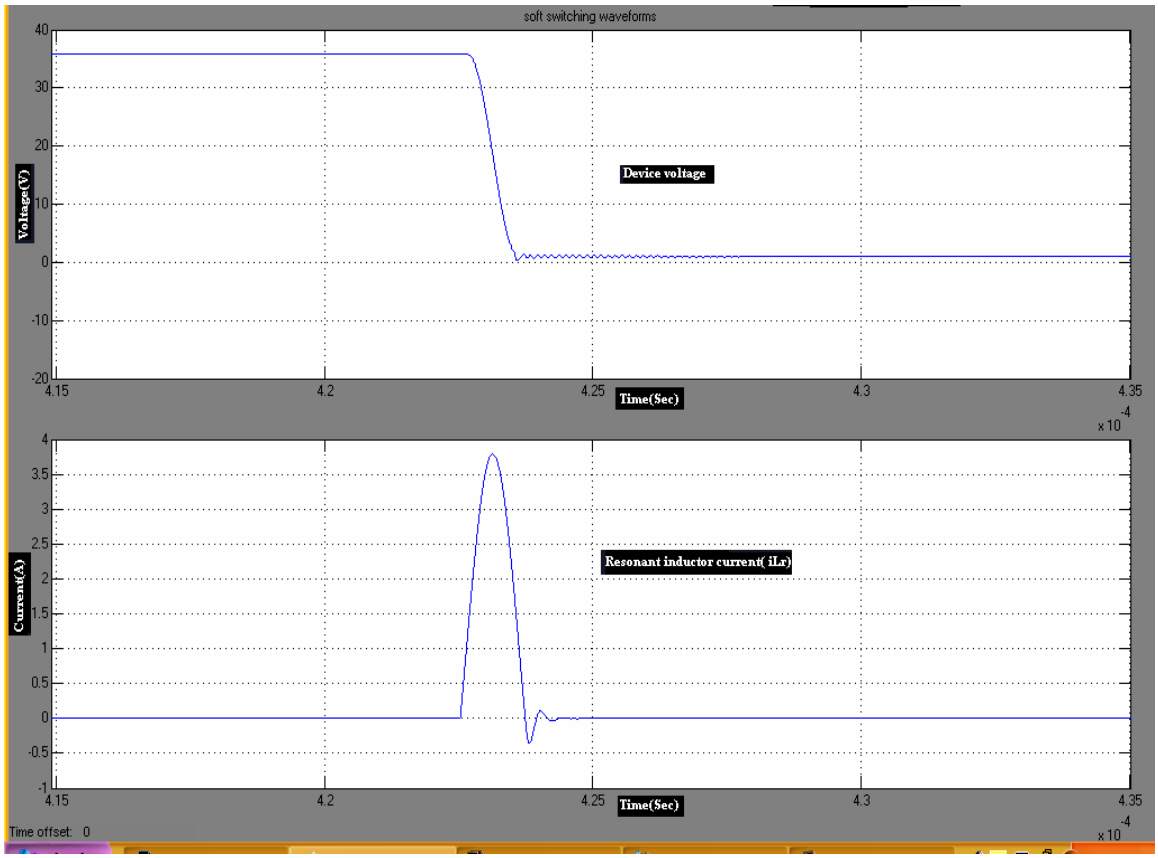

Fig. 5.20 Device voltage and resonant inductor current

Device voltage and device current for the main switches under zero voltage condition is shown in Fig.5.21 and in Fig.5.22., a closer view of the switching waveform under zero voltage condition is shown.

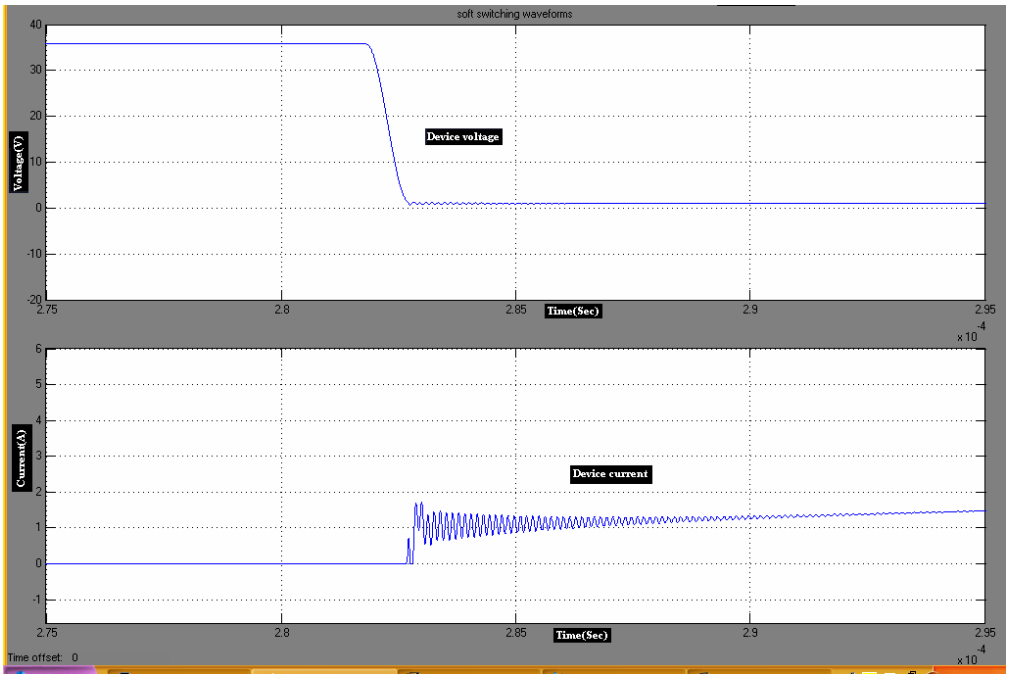

Fig. 5.21 Device voltage and device current under zero voltage condition

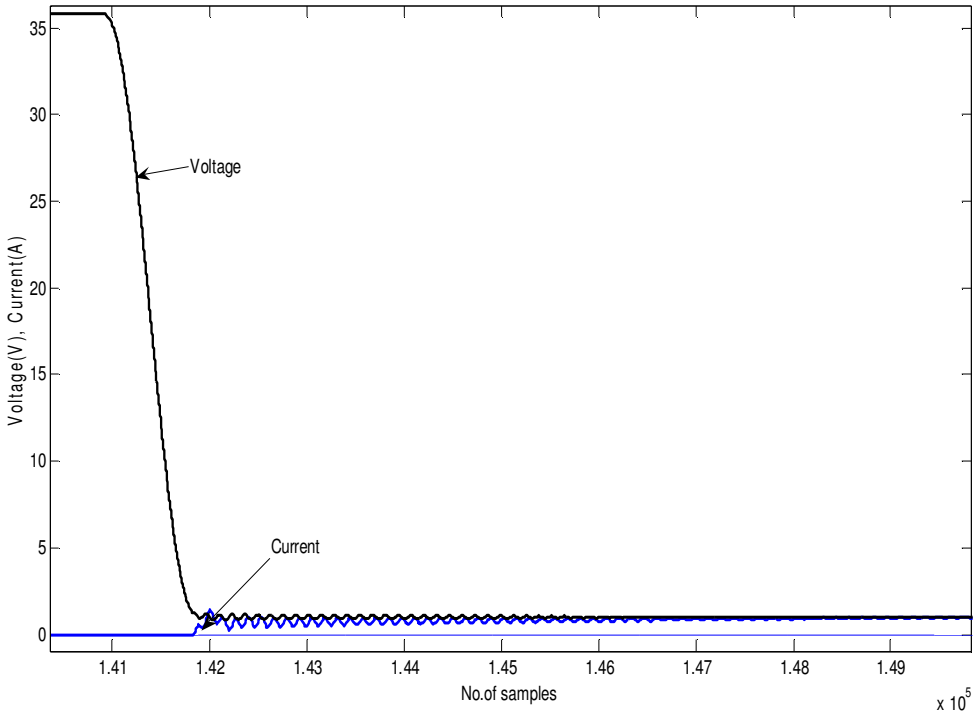

Fig. 5.22 Device voltage and device current under zero voltage condition (closer view)

Device voltage and device current waveforms of Fig. 5.21 and Fig.5.22 clearly show a drastic reduction in the overlap between them and hence reducing the switching loss.

Load voltage and load current waveforms are shown in Fig.5.23. This is to show a continuous load current for a selected value of resistance and inductance as a load.

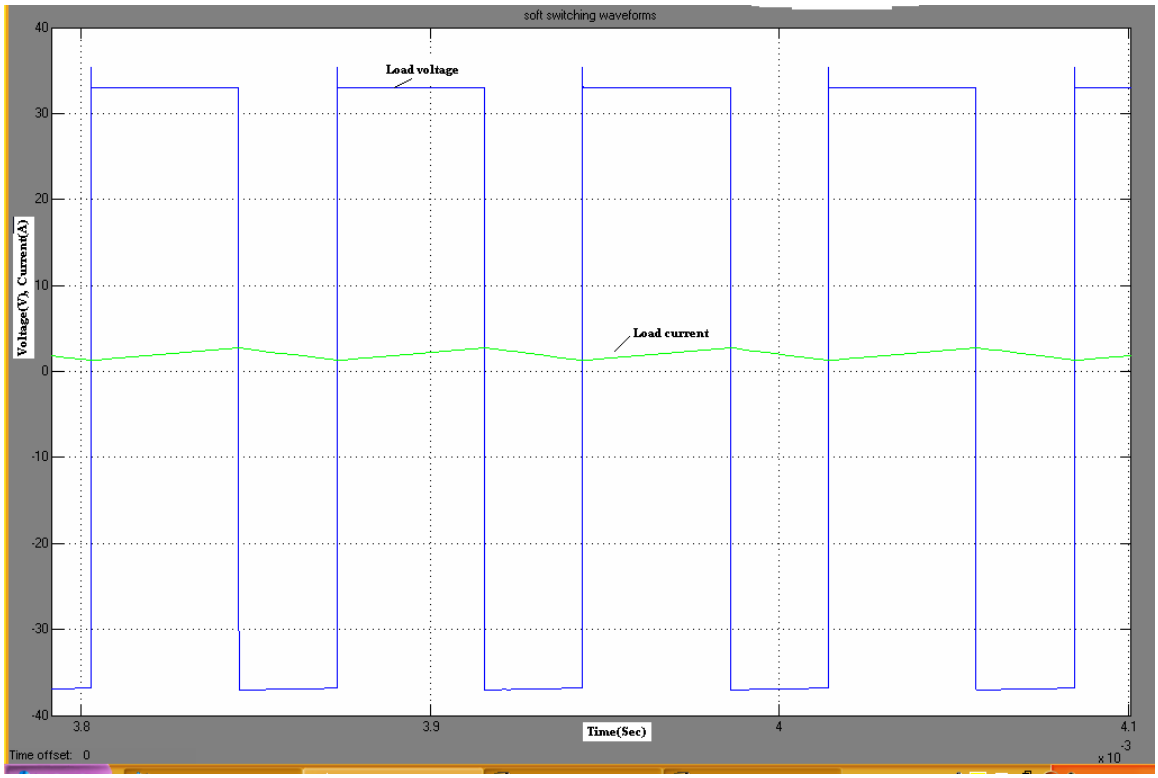

Fig. 5.23 Load voltage and load current

5.4.2 Experimental Results

Fig.5.24 shows the ZVT topology for the experimental verification. S1 and S2 are the IGBT switches which undergo zero voltage transition to achieve soft switching.

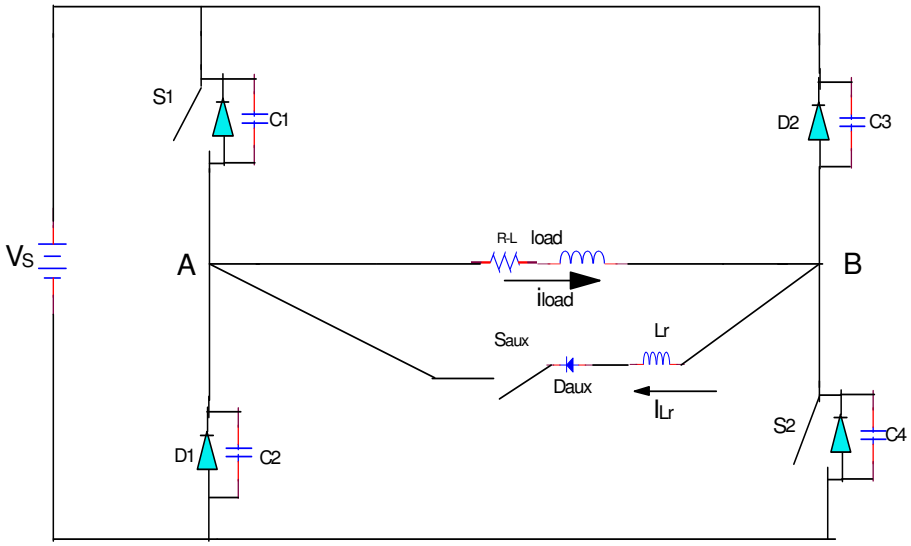

Fig.5.24 ZVT Topology for experimental verification

Combination of resistance and inductance were chosen as the load current was made continuous. Resonant capacitor and inductor values were designed to meet the ZVT condition.

Switching Transition

Hard Switching

Firstly the experimental set-up was built to see the hard switching waveforms of IGBT switches. Switching waveforms were captured using Tektronics TDS 1002B DSO, 60MHz, which are shown in Fig.5.25.

It shows device voltage and current overlap during transition. There is considerable overlap between voltage and current waveforms during switching which results in switching loss. This gives a measure of switching loss during turn-on. To remove the voltage spike and oscillation, a snubber consisting of resistance and capacitance was placed across the devices.

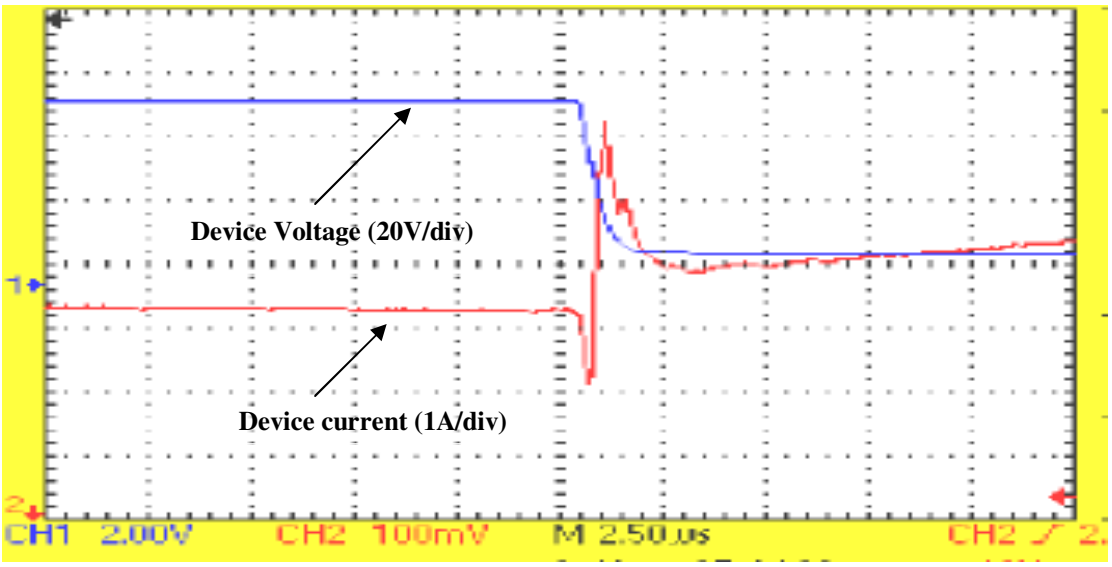

Fig. 5.25 Device voltage and current during turn-on for hard-switching

Soft-Switching

To verify the simulation results and design concept of ZVT topology, an experiment with resonant branch is conducted. Fig. 5.26 shows the gate pulses for main and auxiliary switches.

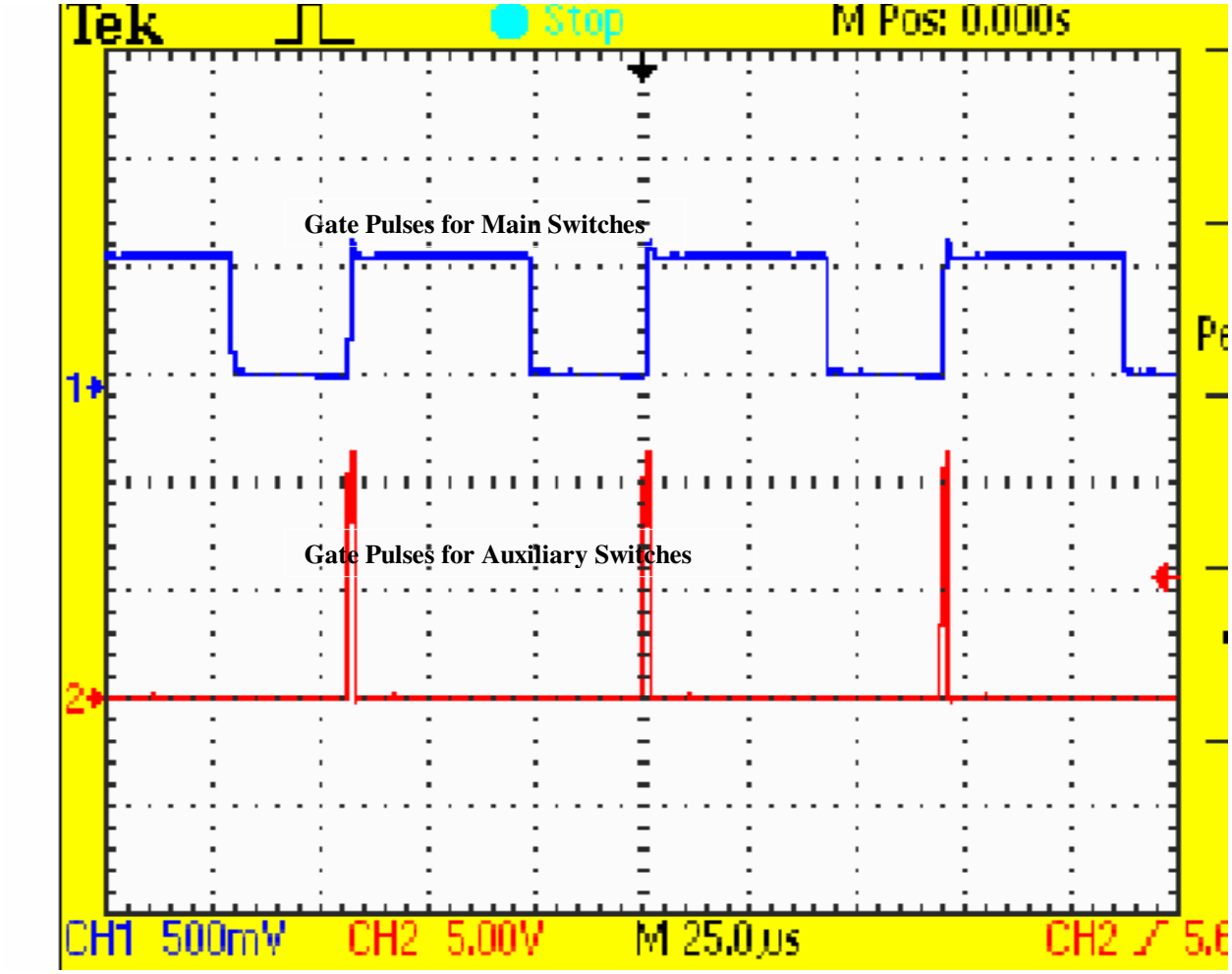

Fig. 5.26 Gate pulses for main and auxiliary switches

Main pulse duty cycle was decided by the load current and auxiliary pulses were adjusted accordingly. As is seen from the waveforms, the duration of auxiliary pulses are very small and require precise width and time at which they are supposed to turn-on the auxiliary switch. Pre turn-on time of the auxiliary switch and delay time of the main

switches are calculated with design equations. Fig. 5.27 shows main and auxiliary switch pulses with calculated pre turn-on and delay time.

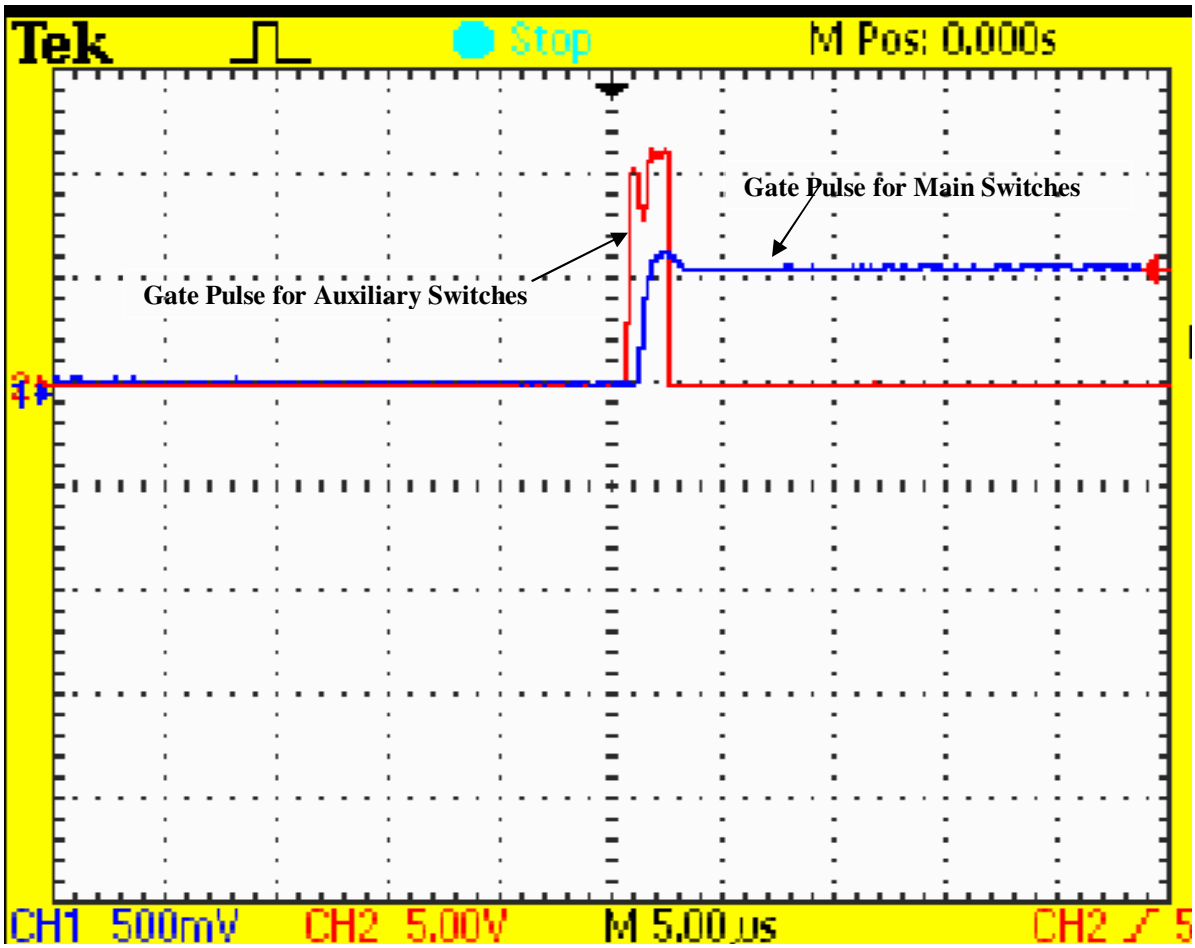

Fig. 5.27 Gate pulses for main and auxiliary switches with pre turn-on and delay time

Auxiliary switch gate pulse and resonant current are shown in Fig.5.28. The resonant duration is decided by the snubber capacitor and resonant inductor value.

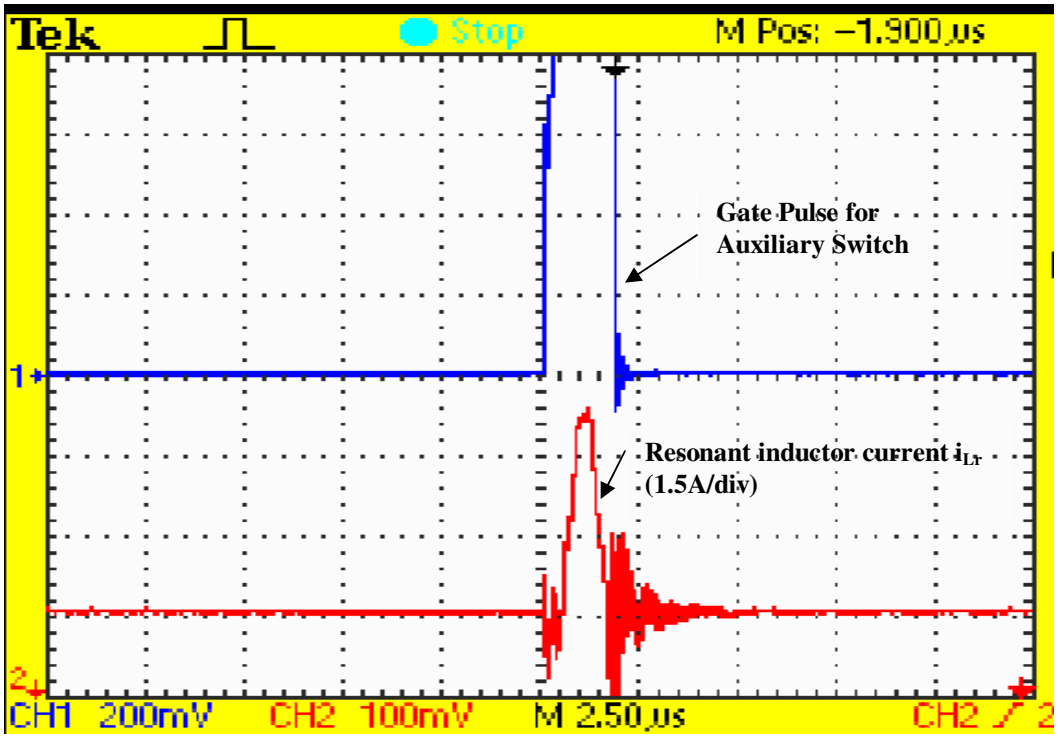

Fig. 5.28 Auxiliary gate pulse and resonant current

Fig. 5.29 shows the resonant inductor current during switching transition. The resonant inductor current builds up linearly to the load current value, resonates and then falls linearly after the resonant switch is turned-off.

The ringing in the resonant inductor current is due to the auxiliary diode reverse recovery. A saturable inductor may be placed to remove the ringing. The peak resonant current is limited by the designed value of snubber capacitor and resonant inductor.

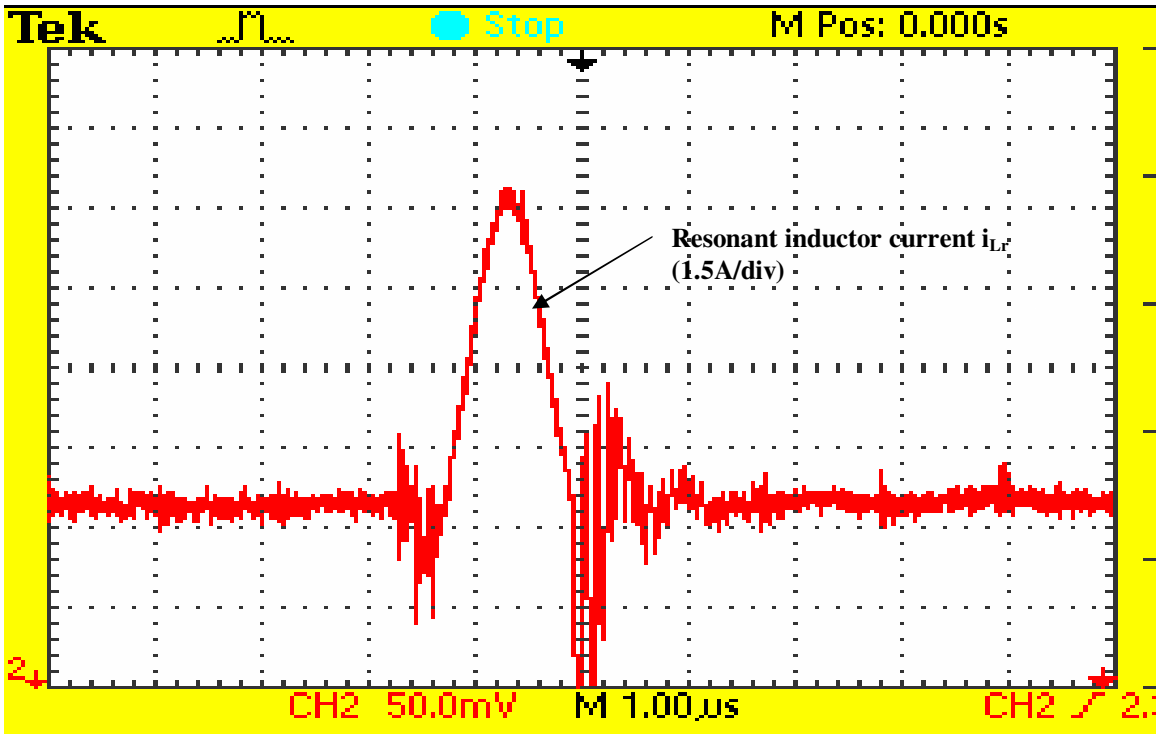

Fig.5.29 Resonant inductor current with ringing

Fig. 5.30 shows device voltage and resonant inductor current. This clearly shows how the device voltage is brought to zero with resonating branch. When the resonant inductor current reaches the load current value, snubber capacitor and resonant inductor transfer energy and start oscillating. The resonance pulls the device voltage to zero creating ZVT condition and hence soft switching.

Device voltage and current waveforms during turn-on for soft switching condition is shown in Fig. 5.31. The overlap between voltage and current waveforms during turn-on is almost zero. This is the zero voltage transition condition where the device is turned-on to reduce the switching loss and to minimize the EMI. The transition of device voltage from source voltage to zero voltage is smooth and it occurs before the current starts

building through the device. The switching loss reduces drastically as found by the actual data for instantaneous power loss calculation.

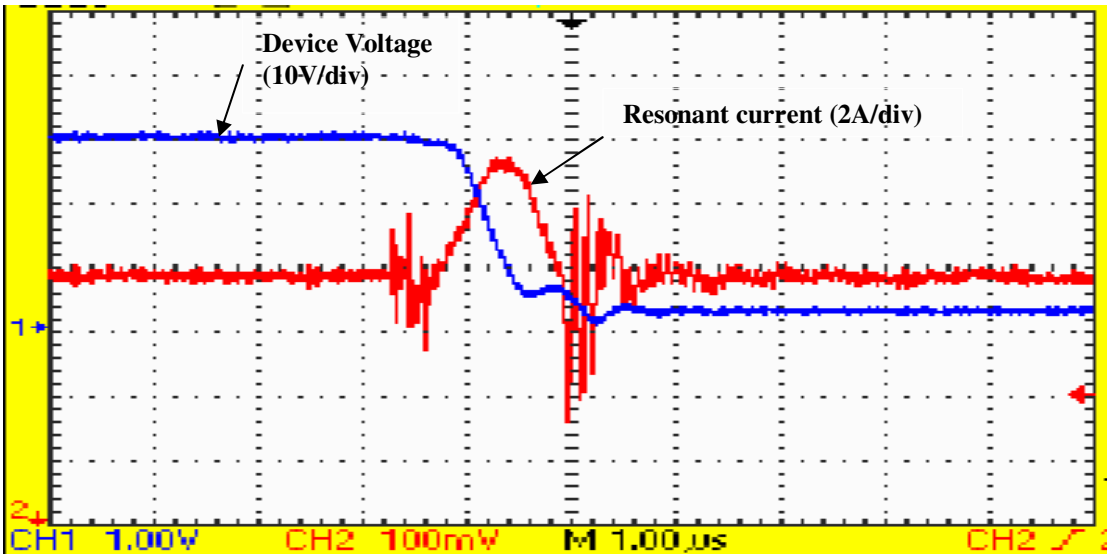

Fig.5.30 Device voltage and resonant current showing ZVT condition

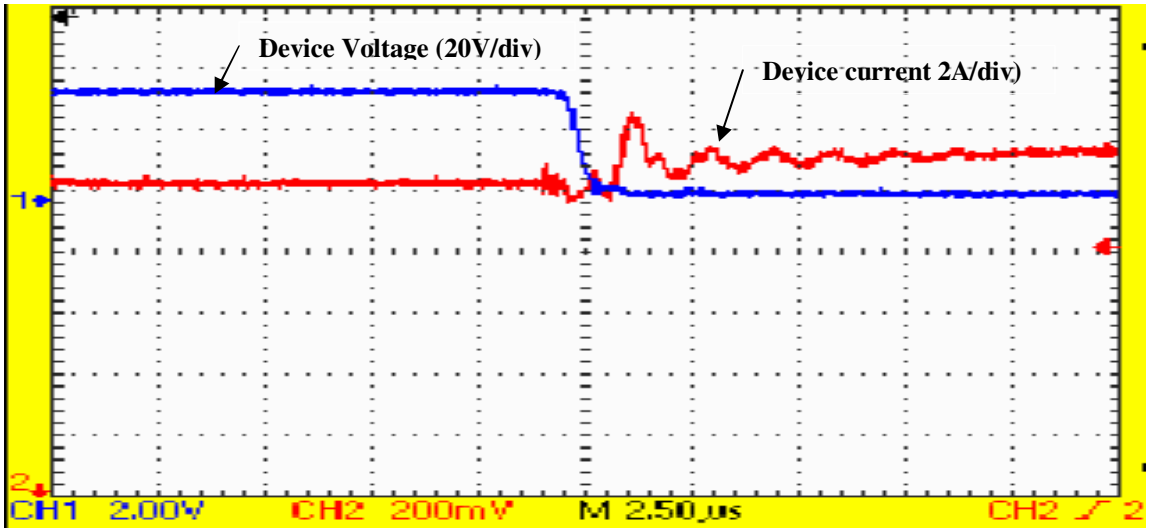

Fig.5.31 Device voltage and current under soft-switching condition

Load voltage and current are shown in Fig. 5.32. It shows a continuous current with negative slope and positive slope during turn-off and turn-on respectively.

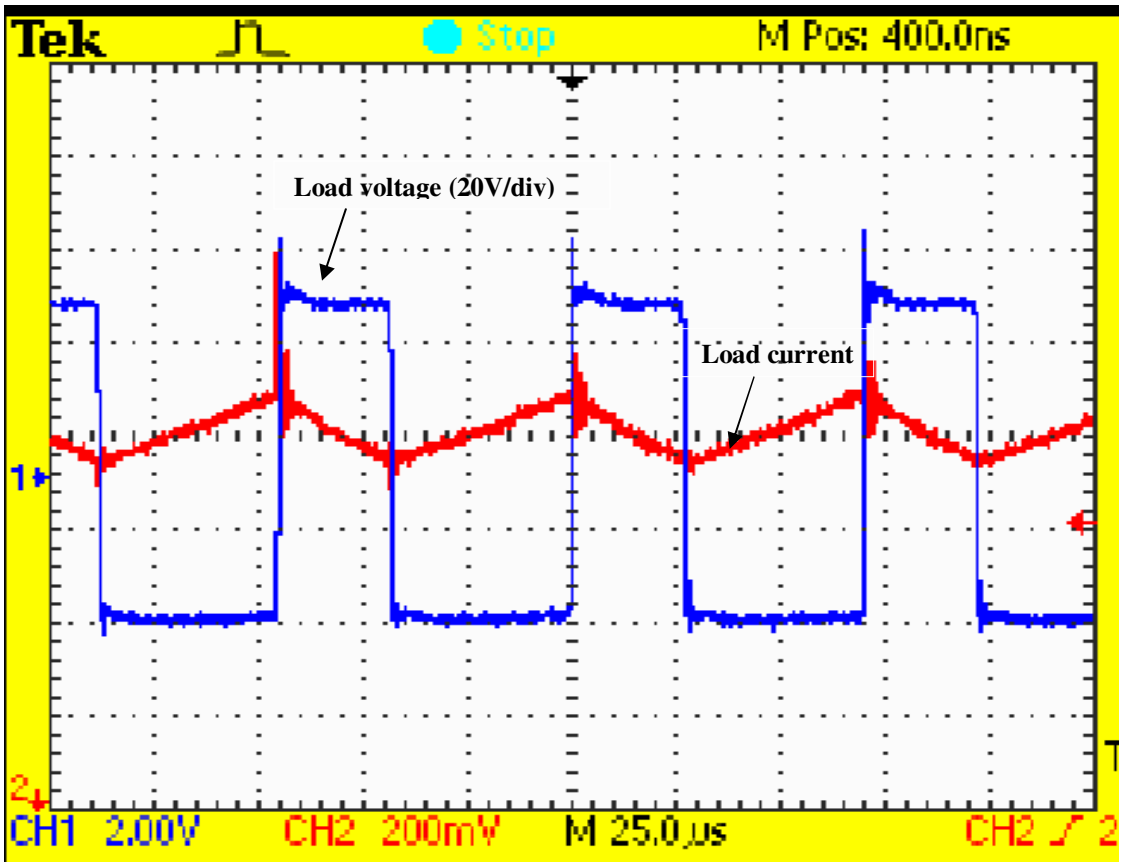

Fig. 5.32 Load voltage and current

5.5 Instantaneous Power

A method for measurement of instantaneous power and energy losses in static switching devices using real data obtained by data acquisition system during different operating intervals was first proposed by [Locci 1988].

The instantaneous power with a view to characterizing the losses in the different intervals of switching cycle (turn-on delay, rise time, on-state, turn-off delay, fall time, off state) was measured by acquiring data with sampling rate available at that time. With advancement in signal processing tools and large memory size of data acquisition systems, it is possible to analyze frequency based features of switching transients in addition to the instantaneous power loss calculation. Experimental voltage and current waveforms during hard-switching and soft-switching conditions are shown in this section. Corresponding instantaneous power waveforms are also shown for both cases. Next section discusses instantaneous power calculation using wavelets and frequency content of transients during switching.

5.5.1 Hard Switching

Experimental waveforms obtained for device voltage and device current during hard switched condition is used to plot the instantaneous power. Fig. 5.33 shows device voltage and current during hard switching condition. Instantaneous power corresponding to these waveforms is shown in Fig.5.34.

5.5.2 Soft switching

Experimental waveforms obtained for device voltage and device current during soft switched condition is used to plot the instantaneous power. Fig. 5.35 shows device voltage and current during soft switching condition. Instantaneous power corresponding to these waveforms is shown in Fig.5.36.

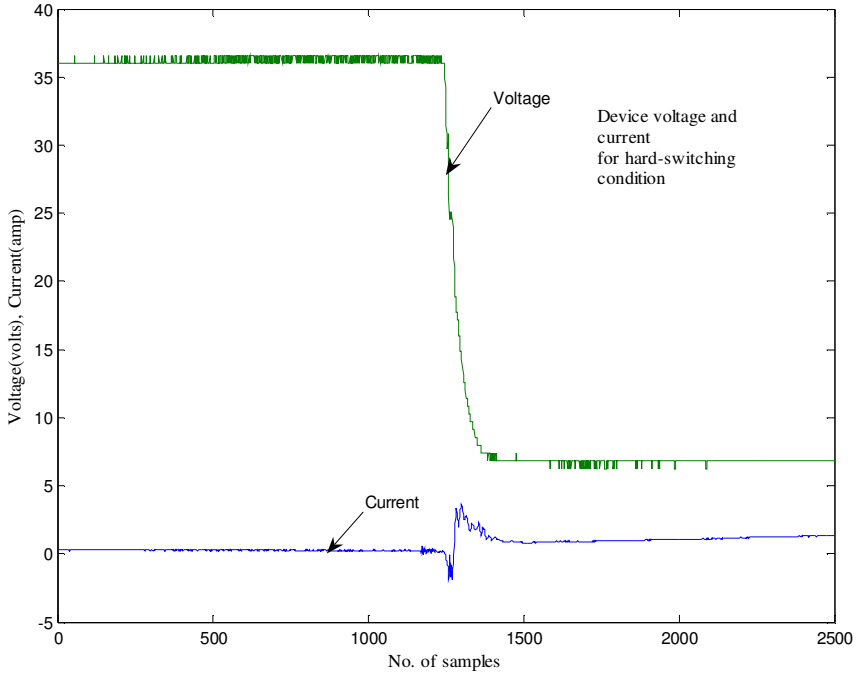

Fig. 5.33 Device voltage and current during hard switching condition

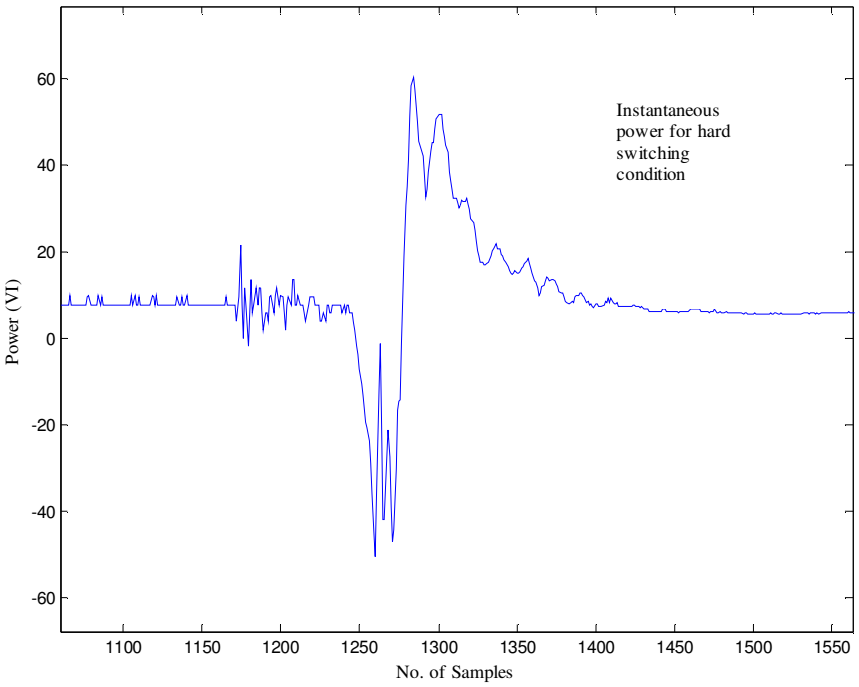

Fig. 5.34 Instantaneous power during hard switching condition

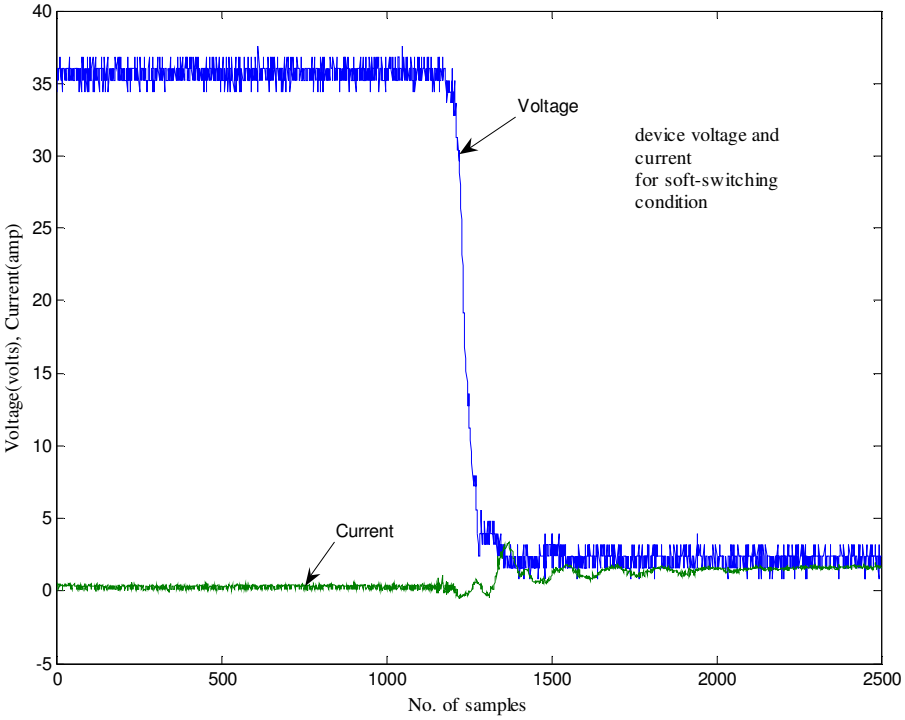

Fig. 5.35 Device voltage and current during soft switching condition

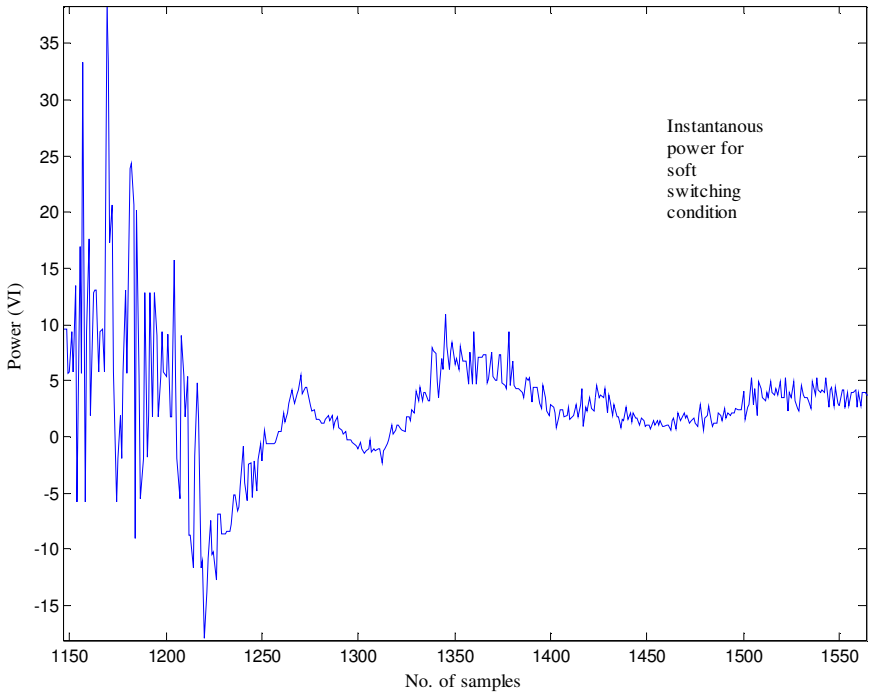

Fig. 5.36 Instantaneous power during soft switching condition

5.6 Wavelet Based Power Loss Analysis

Wavelet based method for power loss calculation in a soft switching converter, using multi resolution analysis (MRA) is discussed in this section. MRA is used to decompose voltage and current signals in sub-band frequencies. The power loss is calculated in each sub-band by multiplication of current and voltage wavelet coefficients. The detail and approximate wavelet coefficients of current and voltage waveforms during hard switching are shown in Fig. 5.37 and Fig. 5.38 respectively.

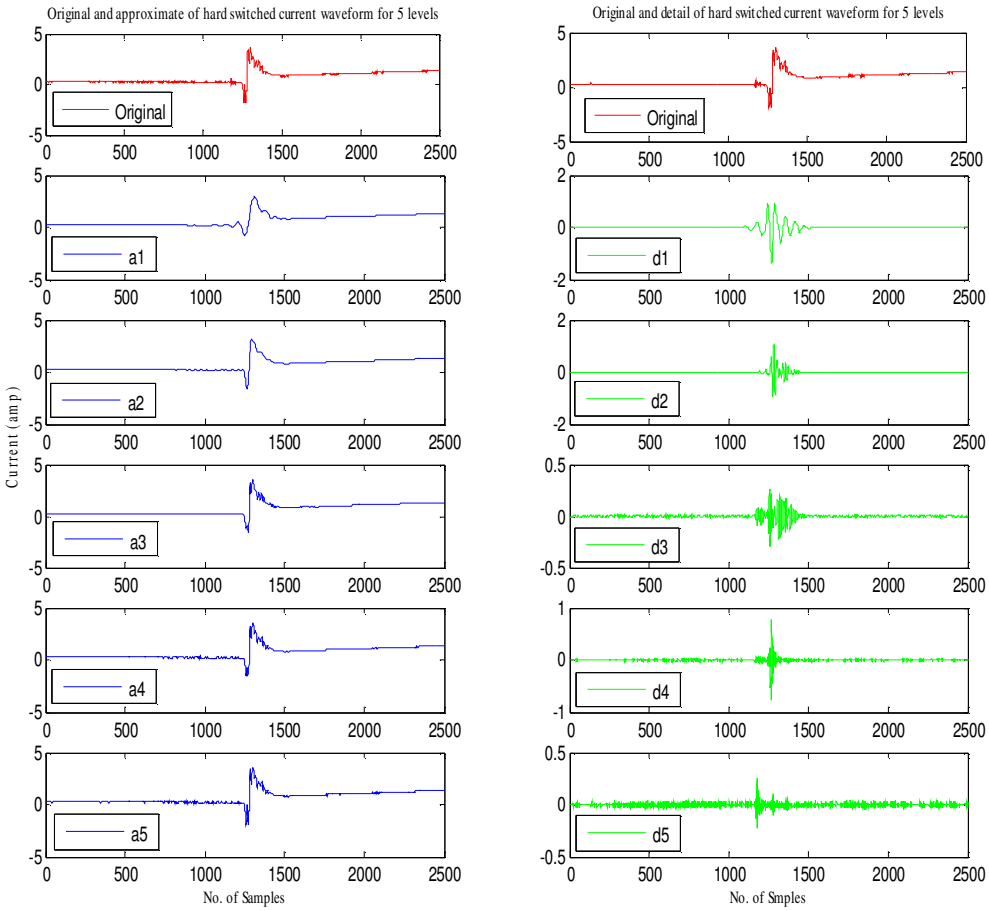

Fig. 5.37 Detail and approximate wavelet coefficients of hard switched current waveform in five frequency sub bands

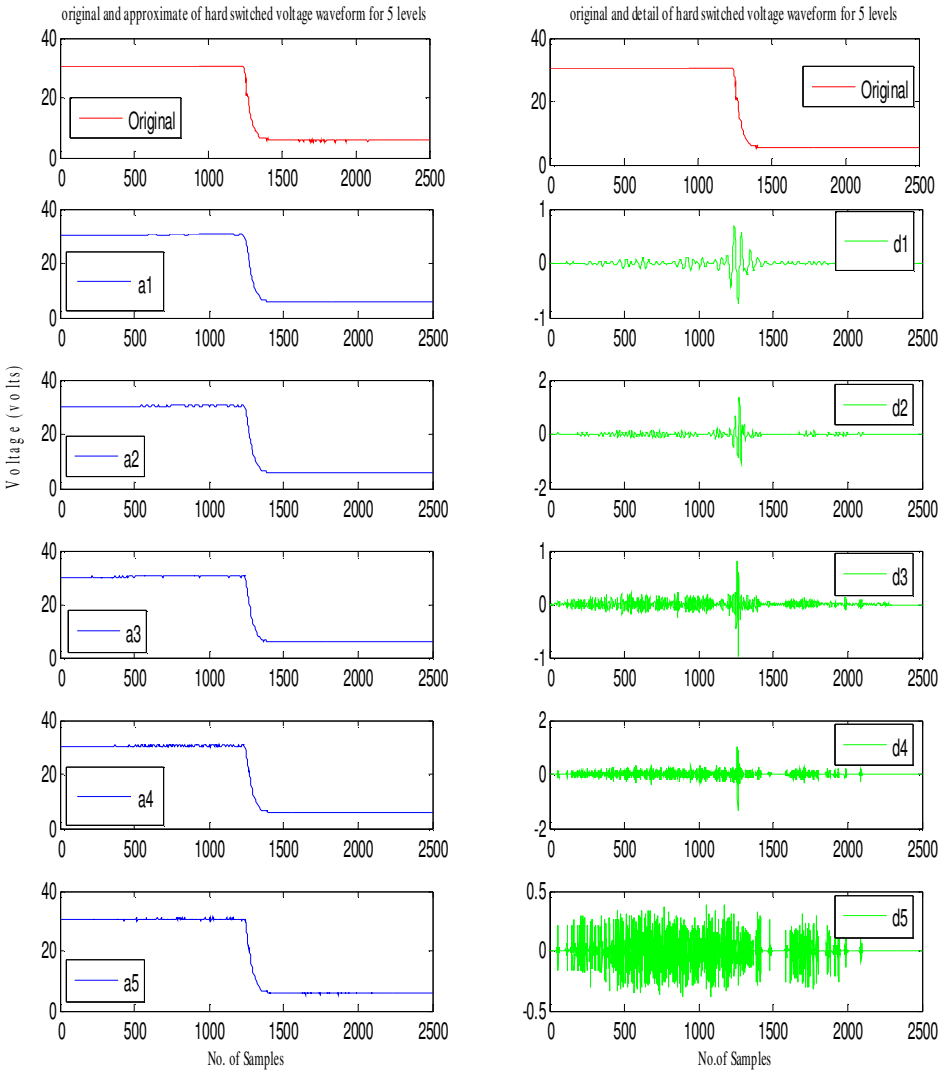

Fig. 5.38 Detail and approximate wavelet coefficients of hard switched voltage waveform in five frequency sub bands

This gives us an idea about the magnitude of frequency content in each sub-band for current and voltage waveforms during transient region. This is an added advantage of wavelet based analysis.

The detail and approximate wavelet coefficients of current and voltage waveforms during soft switching are shown in Fig. 5.39 and Fig. 5.40 respectively.

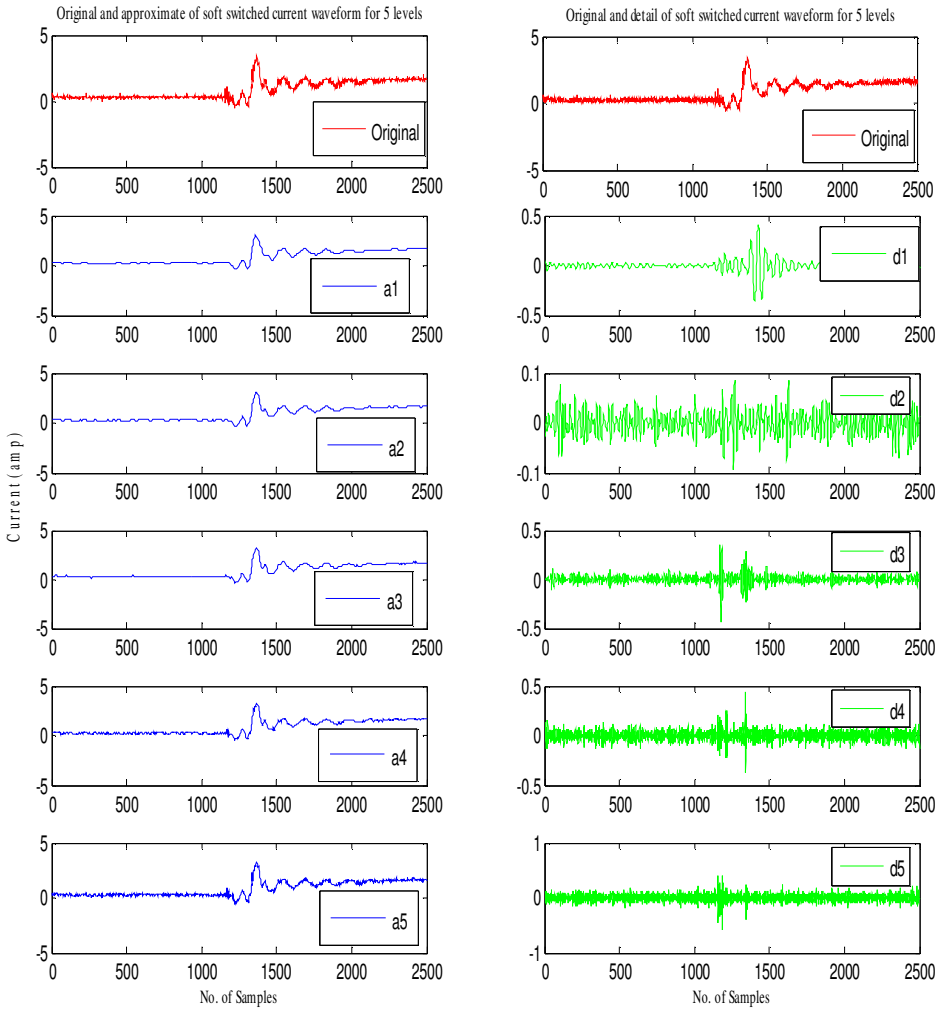

Fig.5.39. Detail and approximate wavelet coefficients of soft switched current waveform in five frequency sub bands

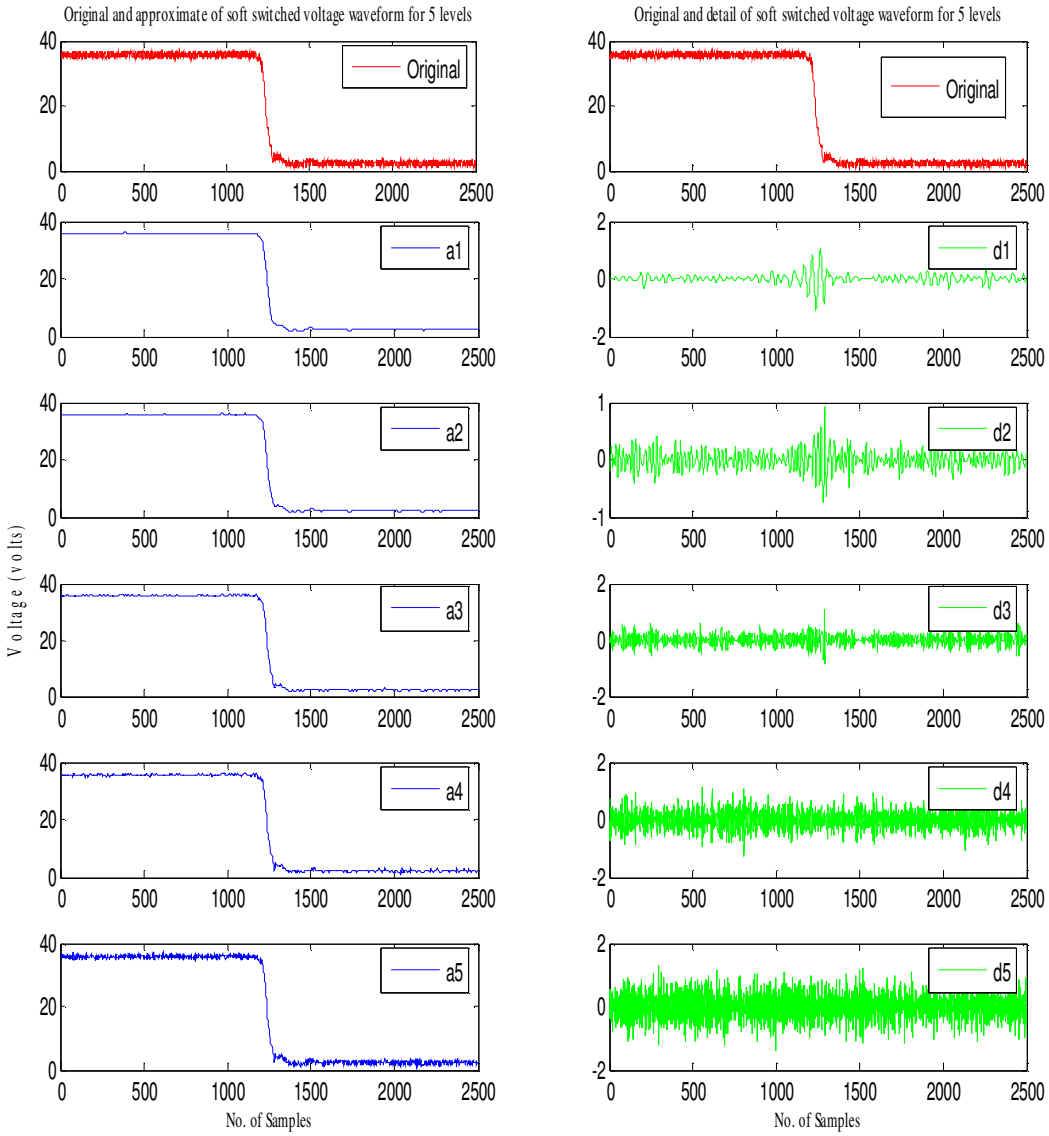

Fig.5.40. Detail and approximate wavelet coefficients of soft switched voltage waveform in five frequency Sub bands

Power loss calculated from wavelets for entire region as shown in table 5.2. Power loss during turn-on for hard-switched and soft-switched conditions is given in table 5.3 and table 5.4 respectively.

Table 5.2
Power Loss Calculation in Five frequency Bands for Entire Region

	Average Power loss(watt)						
Mother Wavelet	Level 1		Level 2	Level 3	Level 4	Level 5	Total Power
	Approximate	Detail					
Db1	7.2470	-0.0032	5.0755e-004	-0.0044	1.2018e-004	1.3296e-004	7.2401
Db2	7.4248	-0.0033	-0.0072	-0.0014	-1.9367e-004	1.7997e-004	7.4129
Db10	8.6680	0.0131	-0.0041	-0.0019	2.0464e-004	1.2709e-004	8.6754
Db20	10.1517	0.0102	-0.0060	-4.9657e-004	6.3986e-004	-3.7025e-005	10.1560
Db35	12.1717	0.0093	-0.0048	-5.6460e-4	3.8897e-4	-4.0005e-5	**12.1760**

Table 5.3
Power loss calculation during transient region for hard switching (watt)

Mother wavelet	Level 1	Level 2	Level 3	Level 4	Level 5
db1	8.8466	8.8505	8.8849	8.8849	9.1040
db2	8.8319	8.8563	8.9564	9.3009	10.0608
db10	8.7253	8.9337	9.7295	11.6869	**15.6243**
db20	8.6073	9.0150	10.4902	13.7818	20.4615
db35	8.4635	9.1668	11.3625	16.0576	25.2756

Table 5.4
Power loss calculation during transient region for soft switching

Mother wavelet	Level 1	Level 2	Level 3	Level 4	Level 5
db1	0.2081	0.1891	0.1531	0.1531	0.1531
db2	0.3909	0.7713	1.5461	3.0329	6.0037
db10	1.1279	2.6715	5.3094	10.2235	19.1118
db20	**1.3110**	2.9566	5.6160	10.1960	18.4125
db35	0.0212	-0.1516	-0.3817	-0.7247	-1.0843

Highlighted powers in table 5.2, table 5.3 and table 5.4 are the powers which are matching with the power calculated by the captured data from the oscilloscope. Here the power loss is calculated using different mother wavelet functions. The entire region of observation is divided into three regions namely on-state region, transient region and off-state region. It is found that the power calculated in on-state and off-state is same for different mother wavelets. It matches with the power calculated by experimental data in low frequency bands since the frequency content in on-state and off-state is low. For transient region, higher scale and mother wavelets with higher filter coefficients are needed. It is clearly seen from the table that the power loss calculated by wavelets and by instantaneous value for transient region matches at fifth level decomposition and with db20 and db35 mother wavelets. The calculation also shows that the power loss for soft-switching condition is very less during transient region.

5.7 Experimental details

5.7.1 Gate Pulse Generation Circuit

Fig. 5.41 and Fig. 5.42 show the gate pulse generation circuit for auxiliary and main switches respectively. The component values are given below the figures.

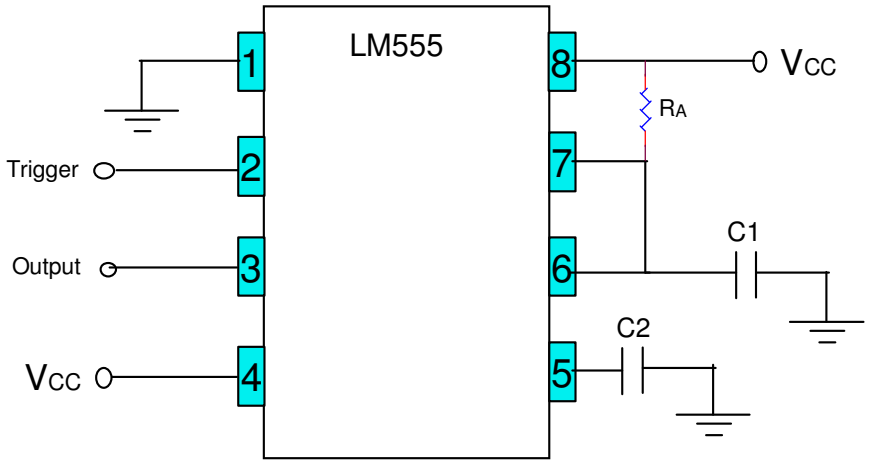

Fig. 5.41 Circuit for gate pulse generation of auxiliary switch

R_A=1kΩ; C1 = 0.001μF; C2 = 0.01μF; V_{CC} = 15V

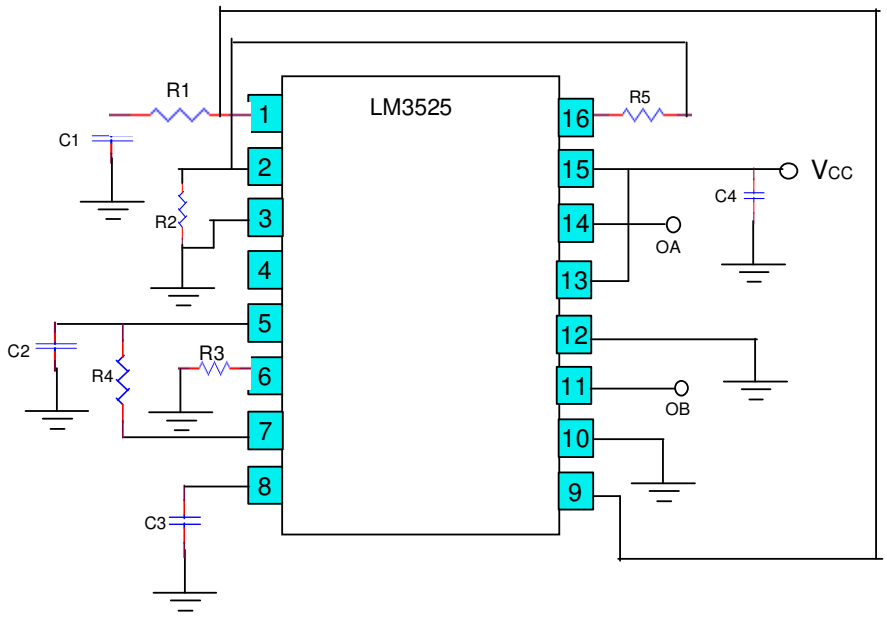

Fig. 5.42 Circuit for gate pulse generation of main switches

R1 = 18kΩ; R2 = 2.2kΩ; R3 = 2.2kΩ; R4 = 100 Ω; R5 = 1kΩ; C1 = 0.01μF; C2 = 0.001μF; C3 = 22nF; C4 = 0.1μF;

5.7.2 Gate Driver Circuit

Gate driver circuits using pulse transformer (PT) for main and auxiliary switches are shown in Fig. 5.20 and Fig. 5.21 respectively. Component names and values are given below the Figures.

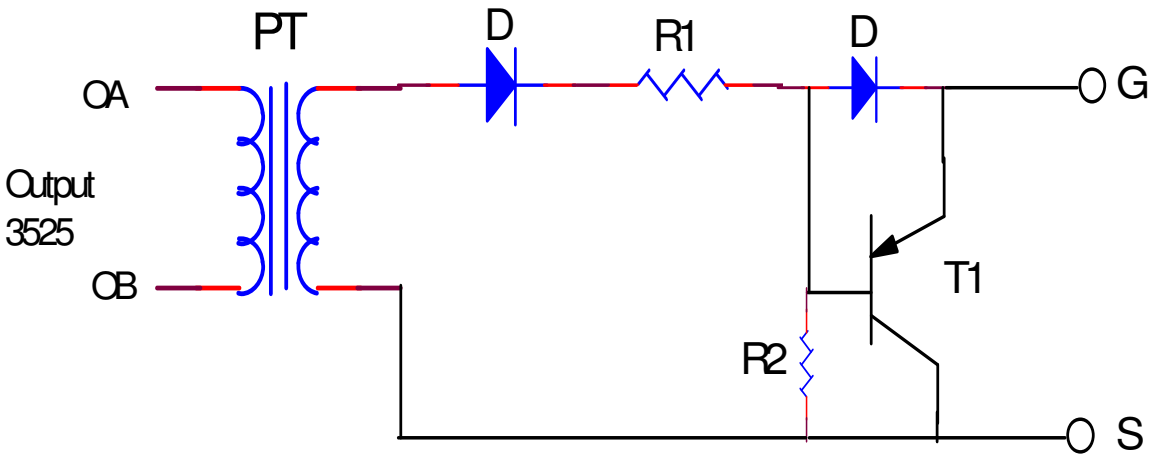

Fig. 5.43 Gate driver Circuit using pulse transformer for main switches

D is IN 4148; T1 is BC 177; R1 = 22Ω; R2 = 470Ω; PT is a pulse transformer with pot core of 30/19, with 30 turns in the primary and 20 turns in the secondary winding.

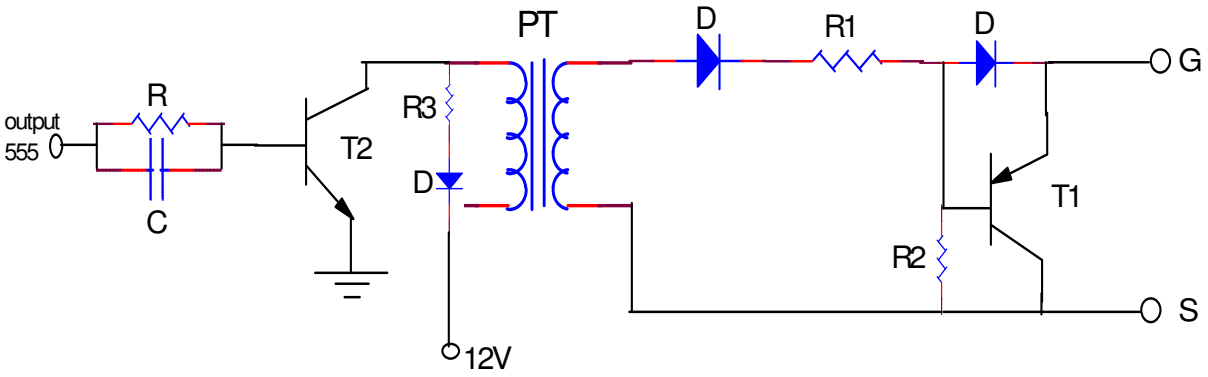

Fig.5.44 Gate driver Circuit using pulse transformer for auxiliary switch

D is IN 4148; T1 is BC 177; R1 = 10Ω; R3 = 1kΩ; T2 is 2N 2218; R = 1kΩ; C = 0.01μF;

5.8 Experimental data

V_{dc} = 35V; Load (R-L) = 2.5Ω and 0.8mH;

Main pulse frequency = 14.2 kHz; Duty cycle = 60%; delay time = 1μs;

Auxiliary pulse width = 2μs; Pre turn-on time = 1μs;

Snubber Capacitor (hard-switch) = 1nF; Snubber resistor (hard-switch) = 22Ω;

Snubber Capacitor (soft-switch) = 22nF; Resonant inductor = 4μH;

Main and auxiliary switches IGBT IRG4PC30U

(V_{CES} = 600V; I_C = 12A; t_r = 9.6ns; t_f = 150ns; t_d(off) = 120ns;)

Main Diodes PFR856 Fast recovery diode with

(V_{RRM} = 600V; I_F(avg) = 3A; t_{rr} = 150ns;)

Auxiliary branch diode MR854 Fast recovery diode with

(V_{RRM} = 600V; I_F(avg) = 3A; t_{rr} = 100ns;)

5.9 Conclusions

Experimental results are presented for a single phase SPWM inverter to verify the design to meet a THD of less than 3% for load voltage. Frequency spectrum of load voltage is observed for both lower order and higher order harmonics.

Simulation results of a ZVT converter topology are verified from laboratory prototype with reduced voltage and current ratings. It achieves soft-switching for one pair of switches. Snubber capacitor and resonant inductor values are selected with design equations and corresponding pre turn-on time for auxiliary switch and delay time for main switch is calculated. Waveforms from both hard and soft switched converters are presented. It seen that near ZVT condition is met.

Wavelet based method for switching power loss calculation is discussed and verified for on-state, off-state and transient region with the data obtained from experiment. The analysis during transient region in terms of frequency content in different frequency bands is also presented.