

References

- [Abnous 1996] A. Abnous and J. Rabaey, "Ultra-low-power domain-specific multimedia processors," VLSI Signal Processing, Vol. 9, pp.461-470, Oct. 1996.
- [Atkin 1970] D. E. Atkin, "Design Of arithmetic UNITS OF Illiac III: Use of redundancy and higher radix method," IEEE Trans. on Computer, Vol. C-19, No. 8, pp. 720-733, Aug. 1970.
- [Avizienis 1961] A. Avizienis, "Signed-digit number representation for fast parallel arithmetic," IRE Trans. Electron. Computer, Vol. EC-10, pp. 389-400, Sept. 1961.
- [Balsara 1996] Poras T. Balsara and David T. Harper, "Understanding VLSI bit serial multiplier," IEEE Trans. on Education, Vol. 39, No. 1, Feb. 1996
- [Baugh 1973] C.R. Baugh, and B.A. Wooley, "A two's complement parallel array multiplication algorithm," IEEE Trans. Computers, Vol. 22, No. 12, pp. 1045-1047, Dec. 1973.
- [Blanken. 1974] P.E. Blankenship, "Comments on 'a two's complement parallel array multiplication algorithm," IEEE Trans. Computers, Vol. 23, pp. 1327, 1974.
- [Booth 1951] A.D. Booth, "A signed binary multiplication technique," Quarterly J. Mech. Appl. Math, Vol. 4, Part 2, pp. 236-240, 1951.
- [Bui 2002] Hung Tine Bui, Yuke Wang, and Yingtao Jiang, "Design and analysis of low power 10-transistor full adder using novel XOR-

- XNOR gates,” IEEE Trans. On Circuits And Systems-II: Analog And Digital Signal Processing, Vol.49, No.1, pp. 25-30, Jan. 2002.
- [Cattloor 2000] F. Cattloor, *Unified Low-power Design Flow for Data-dominated Multimedia and Telecom Applications*, Kluwer Academic Publishers, 2000.
- [Chan 1992] Pak K. Chan, M. D. F. Schlag, C. D. Thomborson and V. G. Oklobdzija, “Delay optimization of carry-skip adders and block carry-lookahead adders using multi-dimensional dynamic programming,” IEEE Trans. on Computers, special issue on Computer Arithmetic. Vol. 41, No. 8, pp. 920-930, Aug. 1992.
- [Changyeh 2000] Wen-Changyeh and Chein-wei Jen, “High-speed Booth encoded parallel multiplier design,” IEEE Trans. On Computers, Vol. 49, No. 7, pp. 692-701, July 2000.
- [Chien 2001] C. Chien, *Digital Radio Systems on a Chip: A Systems Approach*. Kluwer Academic Publishers, 2001.
- [Choi 2001] K. Choi and M. Song, “Design of a high performance 32*32-bit multiplier with a novel sign select Booth encoder,” in Proc. 2001 IEEE Int. Symp. Circuits and Systems, Vol.2, pp.701-704, May 2001.
- [Dadda 1965] L. Dadda, “Some schemes for parallel multipliers,” *Alta Frequenza*, Vol. 34, pp. 349-356, March 1965.
- [Edamatsu 1988] H. Edamatsu, T. Taniguchi, T. Nishiyama and S. Kuninobu, “A 33 MFLOPS floating-point processor using redundant binary

- representation,” in *ISSCC Dig. Tech. Papers*, pp. 152-153, Feb. 1988.
- [Ercegovac 1987] Milos Ercegovac and Tomas Lang, “On the fly conversion of redundant to conventional representation,” *IEEE Trans. on Computers*, Vol. C-36, No. 7, pp. 895-897, July 1987.
- [Gnana. 1985] R.Gnanasekaran, “A fast serial-parallel binary multiplier”, *IEEE Trans. Computer*, Vol. C-34, No. 8, pp. 741-744, Aug. 1985.
- [Goto 1992] Gensuke Goto, Tomio Sato, Masao Nakajima, and Takao Sukemura, “A 54X54 regular structured tree multiplier,” *IEEE J. Of Solid State Circuits*, Vol.27, No.9, pp. 1229-1236, Sept. 1992.
- [Goto 1997] Gensuke Goto, Atsuki Inoue, Ryoichi Ohe, Shoichiro Kashiwakura, Shin Mitarai, Takayuki Tsuru and Tetsuo Izaw, “A 4.1 ns compact 54X54 -bit multiplier utilizing sign-select Booth encoders,” *IEEE J. Of Solid-State Circuits*, Vol.32, No.11, pp. 1676-1682, Nov. 1997.
- [Harata 1987] Y. Harata, Y. Nakamura, H. Nagese, M. Takigawa, and N. Takagi, “A high-speed multiplier using a redundant binary adder tree,” *IEEE J. Solid-State Circuits*, Vol. 22, pp. 28-34, Feb. 1987.
- [Hennesy 2000] John L Hennesy and David A Patterson, *Computer architecture a quantitative approach*, Morgan Kaufmann Publication. San Francisco, Inc.2000.
- [Hoon 2002] Sang-Hoon Lee, Seung-Jun BAE, and Hong-June PARK, “A compact radix-64 54x54 CMOS redundant binary parallel

- multiplier,” IEICE Trans. Electron., Vol. E85-C, No. 6, pp.1342-1350, June 2002.
- [Hsiao 1998] Shen-Fu Hsiao, Ming-Roun Jiang, and Jia-Sien Yeh, “Design of high-speed low-power 3-2 counter and 4-2 compressor for fast multipliers,” IEE Electronics Letters, Vol. 34, No. 4, pp. 341-343, Febr. 1998.
- [Khoo 1999] K-Y. Khoo, Z. Yu, and A.N. Willson, “Improved-Booth encoding for low-power multipliers,” in Proc. 1999 IEEE Int. Symp. Circuits and Systems, Vol.1, pp.62-65, May 1999.
- [Kim 2001] Yum Kim, Bang-Sup Song, John Grosspietsch, and Steven F. Gilling , “ A carry-free 54b x 54b multiplier using equivalent bit conversion algorithm, ” IEEE J. Of Solid State Circuits, Vol. 36, No.10, pp. 1538-1544, Oct. 2001.
- [Kim 2003] Yum Kim, Bang-Sup Song, John Grosspietsch, and Steven F. Gilling, “ Correction to a carry-free 54 b X 54 b multiplier using equivalent bit conversion algorithm,” IEEE Journal of Solid-State Circuits, Vol. 38, No. 1, pp. 159160, Jan. 2003.
- [Kuninobu 1987] S. Kuninobu, T. Nishiyama, T. Edamatsu, T. Taniguchi, and N. Takagi, “Design of high speed MOS multiplier and divider using redundant binary representation,” In Proc. 8th Symp. Computer Arithmetic, Italy, pp. 80-86, May 1987.
- [Ling 1981] H. Ling, “High-speed binary adder,” IBM J. Res. Develop., Vol. 25, No. 3, pp.156--166, May 1981

- [Makino 1996] Hiroshi Makino, Yasunobu Nakase, Hiroaki Suzuki, Hiroyuki Morinaka, Hirofumi Shinohara, and Koichiro Mashiko, "An 8.8-ns 54 x 54-Bit multiplier with high speed redundant binary architecture," *IEEE J. Of Solid State Circuits*, Vol.31, No.6, pp. 773-783, June 1996.
- [Oberman 1997] S.F. Oberman and M. J. Flynn, "Design issues in division and other floating point operations," *IEEE Transactions on Computers*, Vol. 46, No. 2, pp. 154 -161, Feb. 97.
- [Ohkubu 1995] Nario Ohkubu, Makoto Suzuki and Toshinobu shinbo, "A 4.4 ns CMOS 54x54-b multiplier using pass-transistor multiplexer," *IEEE J. Of Solid-State Circuits*, Vol.30, No. 3, pp. 251-257, March 1995.
- [Oklobdzija 1996] V.G. Oklobdzija, D. Villeger, and S.S. Liu, "A method for speed optimized partial product reduction and generation of fast parallel multipliers using an algorithmic approach," *IEEE Trans. Computers*, Vol. 45, No. 3, pp. 294-305, Mar. 1996.
- [Oppen. 1999] A. V. Oppenheim and R. W. Schaffer, *Discrete-Time Signal Processing*. 2nd edition, Prentice Hall, 1999.
- [Parhi 2001] K. Prasad and K.K. Parhi, "Low-power 4-2 and 5-2 compressors," *Proc. of 2001 Asilomar Conf. on Signals, Systems and Computers*, Pacific Grove, CA, USA, Vol. 1. pp 129-133, Nov. 2001.
- [Rubinfeld 1975] L. P. Rubinfeld, "A proof of the modified booth's algorithm for multiplication," *IEEE Trans. on Computers*, Vol. 24, No. 10, pp. 1014-1015, Oct. 1975.

- [Rulling 2003] Wolfgang Rulling, "A remark on carry-free multiplication," IEEE J. Of Solid State Circuits, Vol.38, No.1, pp. 159-160, Jan. 2003.
- [Saleh 2001] H. I. Saleh, A. H. Khalil, M. A. Ashour, and A. E. Salama, "Novel serial parallel multipliers", IEE Proc-circuits Devices System, Vol. 148, No.4, pp. 183-189, Aug. 2001.
- [Sam 1990] H. Sam and A. Gupta, "A generalized multibit recoding of two's complement binary numbers and its proof with application in multiplier implementations," IEEE Trans. Computer, Vol.39, No.8, pp.1006-1015, Aug. 1990.
- [Santoro 1989a] M. Santoro and M. A. Horowitz, "A pipelined 64x64-bit iterative multiplier," IEEE Journal of Solid-State Circuits, Vol. 24, No. 2, pp. 487-493, April 1989.
- [Shalem 1999] R.Shalem,E. John and L.K.John , "A novel low power energy recovery full adder cell," in Proc. IEEE Great Lakes VLSI Symp., pp. 380-383, Feb. 1999.
- [Shams 2002] Ahmed M. Shams, Tarek K. Darwish and Magdy A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 10, No. 1, pp. 20-29, Feb. 2002.
- [Shen 1978] D. T. Shen and A. Weinberger, "4-2 carry-save adder implementation using send circuits," In IBM Technical Disclosure Bulletin, pp. 3594-3597, February 1978.

- [Song 1991] P.J. Song and G. De Micheli, "Circuit and architecture trade-of for high-speed multiplication," IEEE J. Solid-State Circuits, Vol.26, pp.1184-1198, Sept. 1991.
- [Stelling 1996] P. Stelling and V. G. Oklobdzija, "Design strategies for optimal hybrid final adders in a parallel multiplier," Special issue on VLSI Arithmetic, Journal of VLSI Signal Processing, Kluwer Academic Publishers, Vol.14, No.3, December 1996.
- [Takagi 1984] N. Takagi, H. Yasuura and S. Yajima, "A VLSI-Oriented High-Speed Multiplier Using Redundant Binary Adder Tree," IECE Japan, Vol. J66.d, pp. 683-690, June 1984.
- [Takagi 1985] N. Takagi, H. Yasura and S. Yajima., "High-speed VLSI multiplication algorithm with a redundant binary addition tree," IEEE Transactions on Computers, C-34(9): 217-220, Sept. 1985.
- [Toshiba] 130-nano meter silicon process technology library, Toshiba.
- [Twaijry 1997] H. A. Al-Twaijry, "Area and performance optimized CMOS multipliers," Ph.D. dissertation, Stanford University, Aug. 1997.
- [Vassiliadis 1991] Stamatis Vassiliadis, Eric M. Schwarz and Baik Moon Sung, "Hard-wired multipliers with encoded partial products," IEEE Trans. Computers, Vol. 40, No. 11, pp. 1181-1197, Nov. 1991.
- [Villegger 1993] D. Villegger and V. G. Oklobdzija, "Analysis of Booth encoding efficiency in parallel multipliers using compressors for reduction of partial products," Proceedings of the 27th Asilomar Conference on Signals, Systems and Computers, pp. 781-784, 1993.

- [Wallace 1964] C.S. Wallace, "A suggestion for a fast multiplier," IEEE Trans. Computers, Vol. 13, pp. 14-17, Feb. 1964.
- [Wang 2003] Qi Wang and Yousef R. Shayan, "A versatile signed array multiplier suitable for VLSI implementation," in proc. IEEE CCECE 2003, Vol. 1, pp 199-202, May 2003.
- [Wein. 1981] A. Weinberger, "4:2 carry-save adder module," IBM Technical Disclosure Bull., Vol.23, Jan. 1981.
- [Yannick 2000] Dumonteix Yannick and Mehrez Habib, "A family of redundant multipliers dedicated to fast computation for signal processing," IEEE International Symposium on Circuits and Systems (ISCAS 2000), Geneva, Switzerland, May 2000.