A 7-cell, Stackable, Li-ion Battery Monitoring and Balancing System for Electric and Hybrid Vehicles

THESIS

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CERTIFICATE

This is to certify that the thesis entitled, A 7-cell, Stackable, Li-ion Battery Monitoring and Balancing System for Electric and Hybrid Vehicles and submitted by Veeresh Babu Vulligaddala ID No. 2010PHXF0703H for award of Ph.D. of the Institute embodies original work done by him/her under my supervision.

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Abstract

Battery monitoring systems are a critical aspect of electric and hybrid electric vehicles. A stacked IC approach is used to interface with high voltages. In this thesis, a stackable cell monitoring device which can monitor 7 cells per IC has been designed, fabricated and evaluated for performance. The IC has a 12-bit SAR ADC to measure individual cell voltages and temperature. The measured accuracy of these voltages is less than 4.5 mV which corresponds to 0.1% of the maximum cell voltage of 4.5 V. The reference voltage with respect to which cells are to be balanced, is obtained by a separate reference generation block in the IC. In order to meet the accuracy requirements of the ADC which is a part of the design, a piecewise-linear curvature corrected bandgap circuit has been designed and implemented. Using the reference provided by this bandgap, a 4.5 V reference is generated with an absolute accuracy of 0.05%.

Simultaneous comparison is introduced in the design, in which cell voltages are compared with a reference to identify cells that require balancing. This comparison takes place at the same time for all the cells in the design. An intelligent digital algorithm has also been developed in this design, this eliminates the need for cell voltage measurement during each balancing cycle thereby reducing the volume of data transferred between the stacked ICs and host microcontroller. The communication between ICs in a stack is achieved by cyclic redundant synchronous bi-directional voltage mode level shifting circuit. Power requirement for the internal blocks is provided by the On-chip 3 V and 5 V LDOs. The design also incorporates balancing switches which are conventionally implemented as external devices, thereby reducing the complexity. The design supports both active and passive balancing and has a quiescent current of 17μA.

For precise estimation of state of charge of individual cells, accurate current sensing/measurement is required. This requirement demands it to be implemented as a separate IC. Accurate current measurements are made possible by precision reference voltage across a temperature range. In this thesis, a design of an on-chip precision bandgap reference with digitally calibrated technique is also presented and described. The bandgap is trimmed for temperature and magnitude and is calibrated digitally. Experimental results show a maximum of 0.06 % variation in the bandgap output for a temperature range of -40 °C to 100 °C at a power supply voltage of 3.3 V.

The design of cell balancing and monitoring IC is fabricated in 0.35 μm triple-well 5V HV CMOS process with drain extended MOS high voltage devices. Experimental results confirm, a typical on-resistance value of the balancing switch as 8 Ω. Absolute accuracy of 2 mV is achieved for reference voltage and balancing experiments show a final balancing accuracy of 4.5 mV. Communication between the stacked ICs has also been verified.

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Abbreviations

EV	Electric Vehicle
HEV	Hybrid Electric Vehicle
FCEV	Fuel Cell Electric Vehicle
SC	Switched Capacitor
SOC	State of Charge
BMS	Battery Management System
IC	Integrated Circuit
CAN	Controller Area Network
PVT	Process Voltage Temperature
PTAT	Proportional To Absolute Temperature
BJT	Bipolar Junction Transistor
ADC	Analog to Digital Converter
DAC	Digital to Analog Convertenductor
PGA	Programmable Gain Amplifier
DC	Direct Current
AC	Alternate Current
HV	High Voltage
PCB	Printed Circuit Board

Physical Constants

Boltzmann constant	k	=	$1.380\ 648\ 52\ \times 10^{-23}\ \mathrm{m}^2\ kg\ \mathrm{s}^{-2}\ \mathrm{k}^{-1}$
elementary charge	q	=	$1.602\ 176\ 62\ \times 10^{-19}$ coulombs

Chapter 1

Introduction

There has been a rapid increase in the research on the alternative energies in the past decades. Most promising technologies for the future needs have been identified as Electric vehicles (EV) and Hybrid electric vehicles (HEV). Primary source of energy for EV is battery and vehicle propulsion is controlled by electric motor. HEV uses both conventional as well as electric drive-train to optimize the fuel consumption. Configurations used in HEV are Series-HEV, Parllel- HEV and Series/Parallel-HEV [13]. Fuel cell hybrid electric vehicle (FCHEV) uses fuel cells and battery to support energy requirements. Fig. 1.1 shows different alternative vehicle configurations.

In addition to EV and HEV, micro hybrid and mild hybrid vehicles are gaining traction owing to their simplicity in design and cost compared to HEVs and EVs. Micro and mild hybrid vehicles use 48 V (DC) supply voltages to accommodate the needs of electrification in passenger vehicles. Introduction of 48 V in cars, in addition to conventional 12 V system, reduces CO_2 emissions by 15% [14].

Micro hybrid, mild hybrid and hybrid electrical vehicles need batteries to store the energy. Electrochemical batteries and cells are categorized as primary(non-rechargeable) and secondary

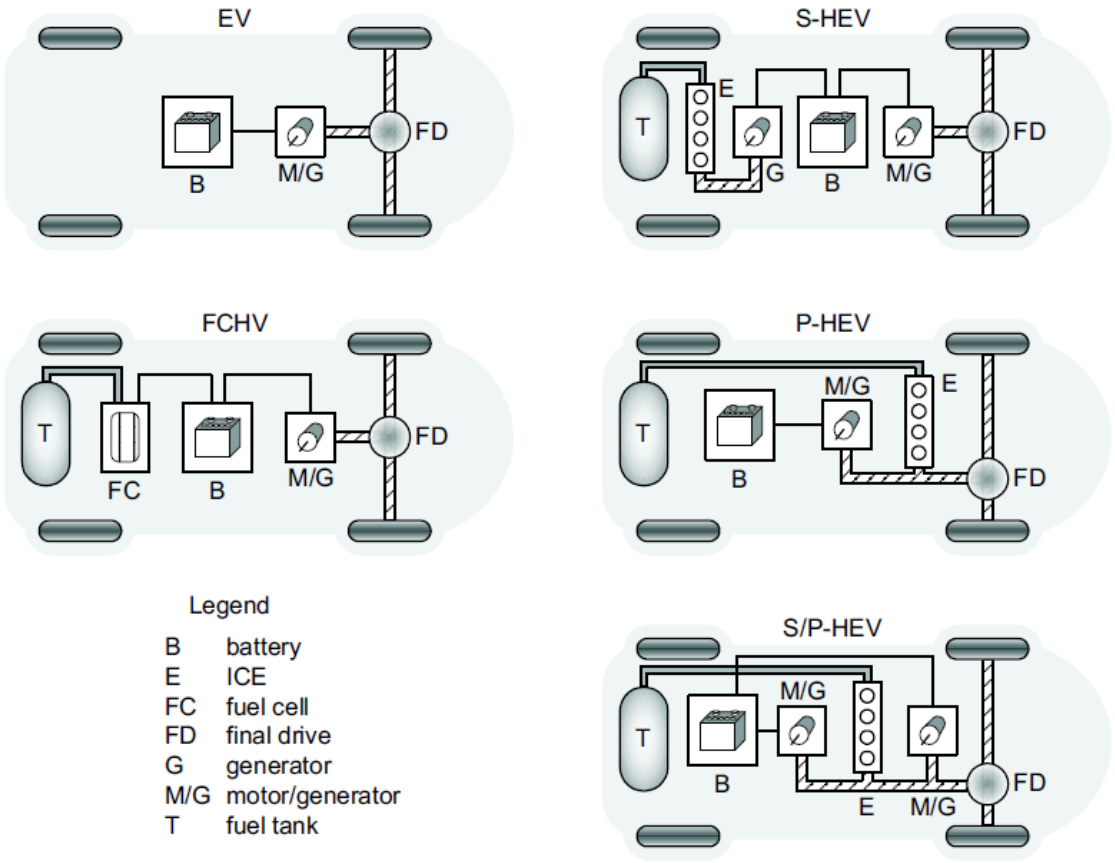

FIGURE 1.1: Alternate vehicle configurations[1]

(rechargeable), based on their electrical rechargeable capability. Usually secondary batteries are used for EV, HEV, portable power tools and portable electronics.

Various battery technologies have been compared in the Table 1.1 [11]. Lead acid batteries are used in all the conventional automotive vehicles because they are safe. Li-ion batteries are better in comparison to other battery chemistries in terms of weight to storage capacity, however, they can pose safety hazards. With proper care, Li-ion batteries are more attractive choice for EVs, HEVs and portable power tools.

Power requirement for EV is based on the range it can travel for a single charge and for HEV it is based on the range extension. A mild hybrid vehicle's power requirements are of the order of 10 KW and the same for EV is about 80 KW [15]. To accommodate these power requirements

TABLE 1.1: Comparison table of different battery technologies [11]

				Li-ion		
Specifications	**Lead Acid**	**NiCd**	**NiMH**	**Cobat**	**Manganese**	**Phospate**
Specific Energy density(Wh/kg)	30-50	45-80	60-120	150-190	100-135	90-120
Internal Resistance(mΩ/V)	<8.3	17-33	33-50	21-42	6.6-20	7.6-15.0
Cycle life(80% discharge)	200-300	1,000	300500	5001,000	500-1,000	1,000-2,000
Fastcharge time(hrs.)	8-16	1 typical	2-4	2-4	1 or less	1 or less
Overcharge tolerance	High	Moderate	Low	Low	Low	Low
Seff-discharge/month(room temp.)	5-15%	20%	30%	<5%	<5%	<5%
Cell voltage	2.0	1.2	1.2	3.6	3.8	3.3
Charge cutoff voltage(V/cell)	2.40(2.25 float)	Full charge indicated by voltage signature	Full charge indicated by voltage signature	4.2	4.2	3.6
Charge cutoff voltage (V/cell, 1C)	1.75	1	1	2.5-3.0	2.5-3.0	2.8
Peak load current	5C	20C	5C	>3C	>30C	>30C
Peak load current (best result)	0.2C	1C	0.5C	<1C	<10C	<10C
Charge temperature	-20 - 50 °C	0 - 45 °C	0- 45 °C	0- 45 °C	0- 45 °C	0- 45 °C
Discharge temperature	-20 - 50 °C	-20 - 65 °C	-20 - 60 °C	-20 - 60 °C	-20 - 60 °C	-20 - 60 °C
Maintenance requirement	3 - 6 months (equalization)	30 - 60 days (discharge)	30 - 60 days (discharge)	None	None	None
Safety requirements	Thermally stable	Thermally stable, fuses common		Protection circuit mandatory		
Time durability				>10 years	>10 years	>10 years
In use since	1881	1950	1990	1991	1996	1999
Toxicity	High	High	Low	Low	Low	Low

with the same gauge wiring higher voltages are required. A 250A capable wiring system requires a voltage ranging from 48 V to 400 V, which is obtained by stacking several Li-ion cells [16]. For some applications stacked ultra-capacitors can serve the purpose. A typical li-ion cell voltage is about 3.6 V and maximum cell voltage can be 4.5 V [17]. To support 48 V for a mild-HEV, 14 series connected Li-ion cells are required and for EVs to realize 400 V about 100 stacked cells are needed.

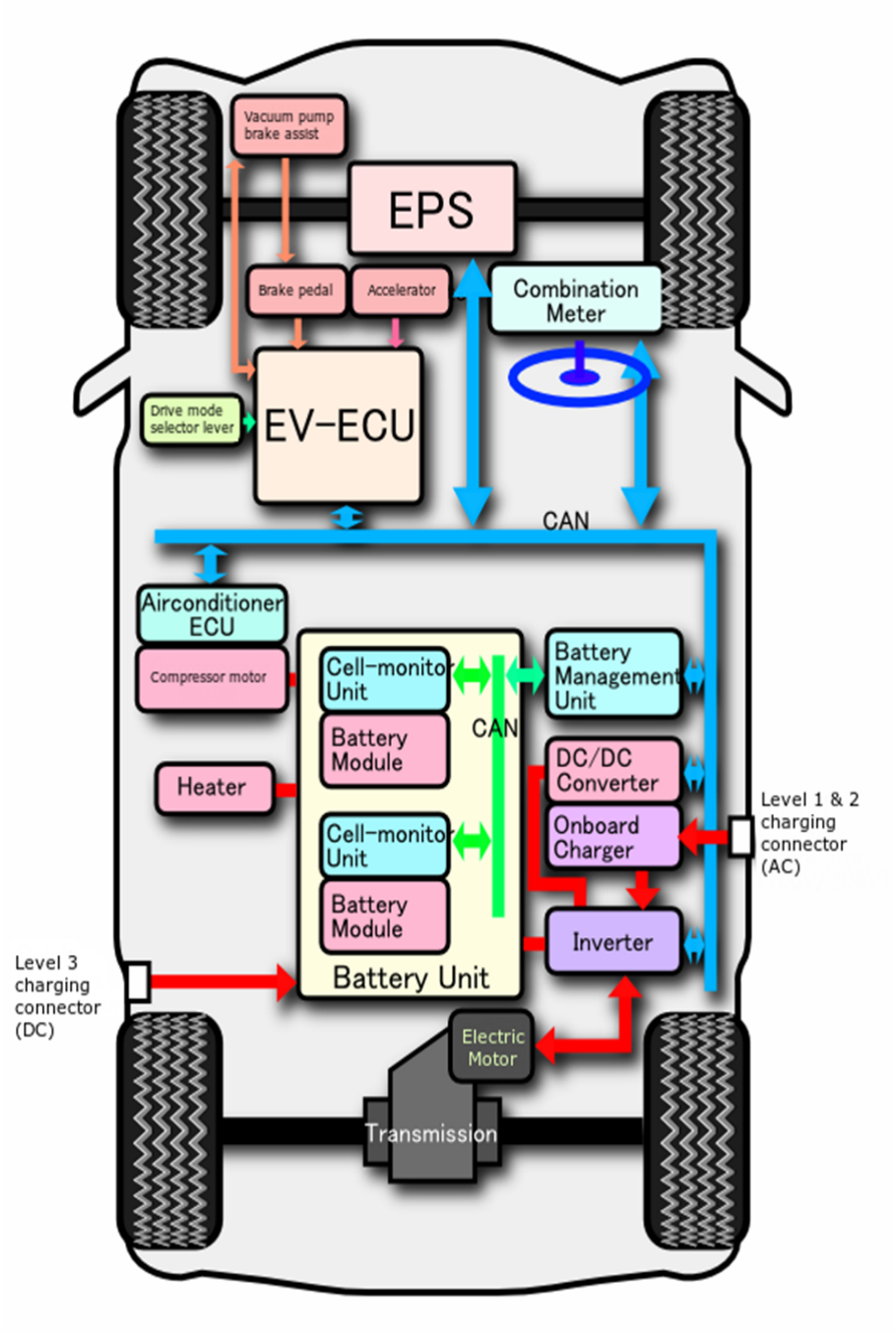

FIGURE 1.2: Mitsubishi i-MiEV's System Diagram [2]

To ensure smooth operation of Li-ion cells, their State of Charge (SOC) is measured. Research on SOC suggests [18] that a cell charged to 100% SOC or discharged to 0% SOC degrades quickly. Therefore, Li-ion cells need to be managed to ensure that these cells do not reach either 100% or 0% SOC level. Based on the accuracy and reliability of battery management system (BMS), cells can be charged and discharged between 90% to 10% or 70% to 30%. SOC provides most important information and it should be estimated precisely. Battery management systems are used mainly to estimate the SOC of the battery pack. Fig. 1.2 shows the Mitsubishi i-MiEV's system diagram, it is evident that, battery unit and battery management unit are critical components of the complete system.

In order to obtain detailed information about SOC, integrating accurate sensors into the battery-monitoring system is essential. Following sensors are required to measure SOC of a battery pack

- Voltage
- Current
- Temperature

Most battery manufacturers stack individual Li-ion cells that are well matched with respect to parameters like capacity, efficiency and internal resistance. Differences in temperature mission profiles of the individual cells are one of the major reasons that causes the parameters of a given cell to drift as it ages. This difference is shown to be significant even in active temperature conditioned battery packs[19]. To over come these differences and maintain cells within the specified parameters, an efficient battery monitoring and cell balancing system is required. Balancing in a given stack is achieved either via active balancing or passive balancing[20], as the former redistributes the energy while the latter dissipates the excess energy.

1.1 Motivation

As discussed earlier, battery management systems play a vital role in EV and HEVs. Intelligent BMS helps in improving the battery performance and adds safety. Accurate measurement of cell voltage and current is very critical for BMS. Complexity associated with level shifting the cell voltages to a standard CMOS voltage levels of 3 V or 5V and designing high voltage circuits using CMOS technologies is a challenging task. Also, battery management system for electric vehicles is not possible on a single IC owing to high voltages involved. Depending on process technology of the manufacturer, the number of cells monitored by a single IC varies between 6 and 12. Thus, a BMS for an EV requires several ICs to be stacked. This poses design challenges like communication between the ICs, the need for synchronisation etc. In battery management systems available in the literature[6]-[8], voltage of each cell is converted to a digital value using analog-to-digital converter (ADC). This value is then transmitted to the on-board microcontroller after every conversion. Because of the number of cells monitored by an IC and the number of ICs stacked in a system, the amount of data transmitted by the BMS to the on-board microcontroller is significant, requiring high speed communication. In most cases, device to device communication is implemented with external isolators which however is an expensive solution. The microcontroller then compares these cell voltages with a reference voltage and decides the cells to be balanced and communicates the same to the balancing device. The cells are then balanced with the help of external components, which include transistors, capacitors, resistors and transformer-based isolators. The number of external components required for balancing ranges between 24 to 59 and this makes the design of such balancing system complex and expensive.

Further, accurate current measurement is essential for precise estimation of SOC of a given cell. In order to measure current accurately, precision reference voltage is required. Therefore a BMS

with robust communication, least number of external components for balancing, precise bandgap reference circuit to facilitate accurate measurements is essential.

This thesis focuses on reducing the complexity and cost optimization as well as improving the robustness of the BMS. This is achieved by reducing the number of external components used, the volume of data transferred internally and improving the accuracy of measurement system.

1.1.1 Organization of the Thesis

This thesis is organized as follows: Chapter 1 gives a brief introduction to the work and identifies the need for BMS. Chapter 2 gives an overview of BMS with a focus on battery monitoring and balancing methods. Chapter 3 explains the novel bandgap reference design for current sensing circuit, while in Chapter 4, cell monitoring and balancing architectures are discussed. Implementation of the proposed system is detailed in Chapter 5. Chapter 6 details and analyses the experimental results while conclusions are drawn in Chapter 7.

Chapter 2

Overview of Battery management system

As discussed in the last chapter, battery management system is an essential part of EV, HEV and power tools to improve the battery life and runtime cost. Li-ion cells are the best choice for these applications owing to their energy density. Li-ion technology is very sensitive to charging and discharging [18], [12] and results in hazardous situations when overcharged. Fig. 2.1 shows the safe operating range of a Li-ion cell. During charging, if the cell voltage exceeds upper voltage limit, typically 4.2 V, then higher currents could flow causing lithium plating and overheating. If the Li-ion cell discharges below the specified lower limit, typically 2.5 V, it can result in progressive breakdown of the electrode. In this work, maximum cell voltage is taken as 4.2 V and lower limit as 2.5 V. These thresholds might vary a little bit based on the chemistry of the cell.

Operating temperatures for the Li-ion cells should be carefully controlled, otherwise excessively high and low temperatures could cause irreversible damage. Safe operating temperatures for Li-ion cells are between -20 °C and 60 °C with thermal runaway occurring at extremely high temperatures. While voltage and temperature effects are not apparent immediately, their

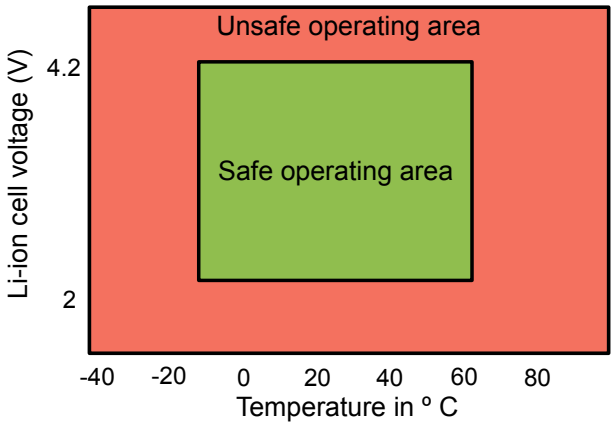

FIGURE 2.1: Li-ion cell safe operating range

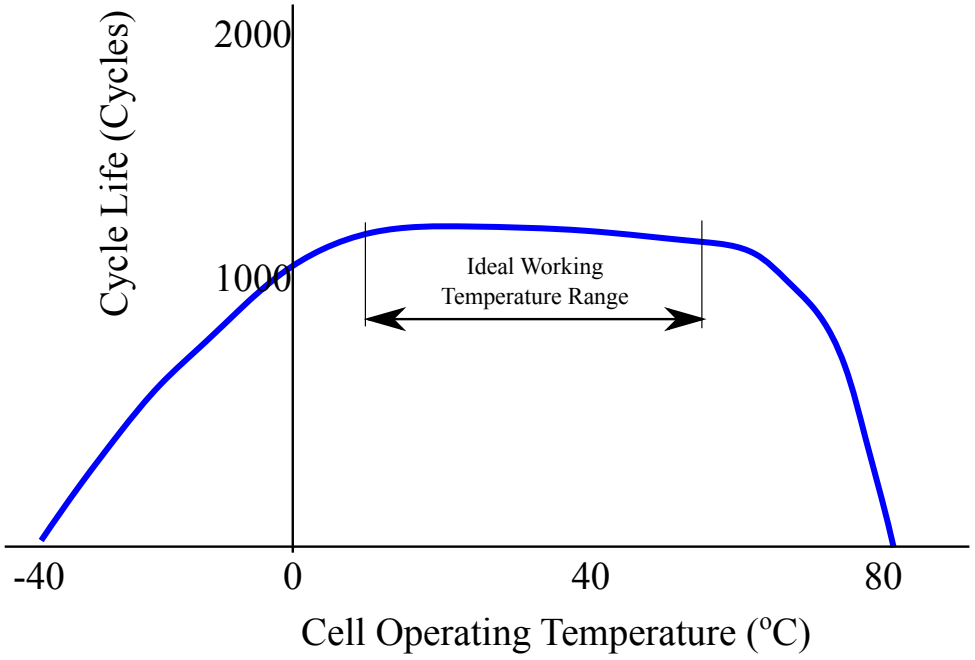

FIGURE 2.2: Li-ion cell cycle live with temperature

cumulative effect may cause life time degradation. Fig. 2.2 shows that the cycle life of Li-ion cell reduces below 10 °C and above 60 °C.

As discussed in the previous chapter, several (about 100) individual Li-ion cells are stacked to achieve the desired voltage for an EV. In such a stacked system, it is not enough to monitor just the stack voltage. This is because, unmonitored individual cells might reach their upper (4.2 V) and lower threshold value (2.5 V) during charging and discharging respectively and result in unsafe conditions. Hence, individual monitoring is mandatory for the safety of a stacked Li-ion

cell battery pack.

Individual cells should be closely matched to same SOC to utilize complete stack capacity. This is better understood with the help of an example. While being charged, assume one cell in a battery pack reaches 4.2 V with all other cells at much lower voltages. This causes the charging to be stopped to prevent thermal runaway of the cell charged to 4.2 V even though all the other cells are at lower voltages. Similarly, during discharging, if one of the cells in a pack reaches 2.5 V, load is disconnected from the entire pack, resulting in under-utilization of energy. To avoid the above mentioned scenarios, balancing between the cells is required and this will help in improving the stored energy, life of the battery pack and cost. A variety of battery management systems have been proposed and discussed in [12] [21] [22] [23].

BMS carries out the following set of functions:

- Data acquisition
- Cell balancing
- Communication with all battery components
- Safety management
- Thermal management
- Ability to control battery charging and discharging
- Ability to determine and predict the state of the battery

A typical battery management system is shown in Fig. 2.3. Safety is one of major concerns in a Li-ion cell BMS. In case of overcharge, deep discharge and extreme temperatures, battery is protected by switching off the load current by disabling the emergency battery disconnect switch. As discussed earlier in this chapter, the operational temperature for Li-ion batteries is

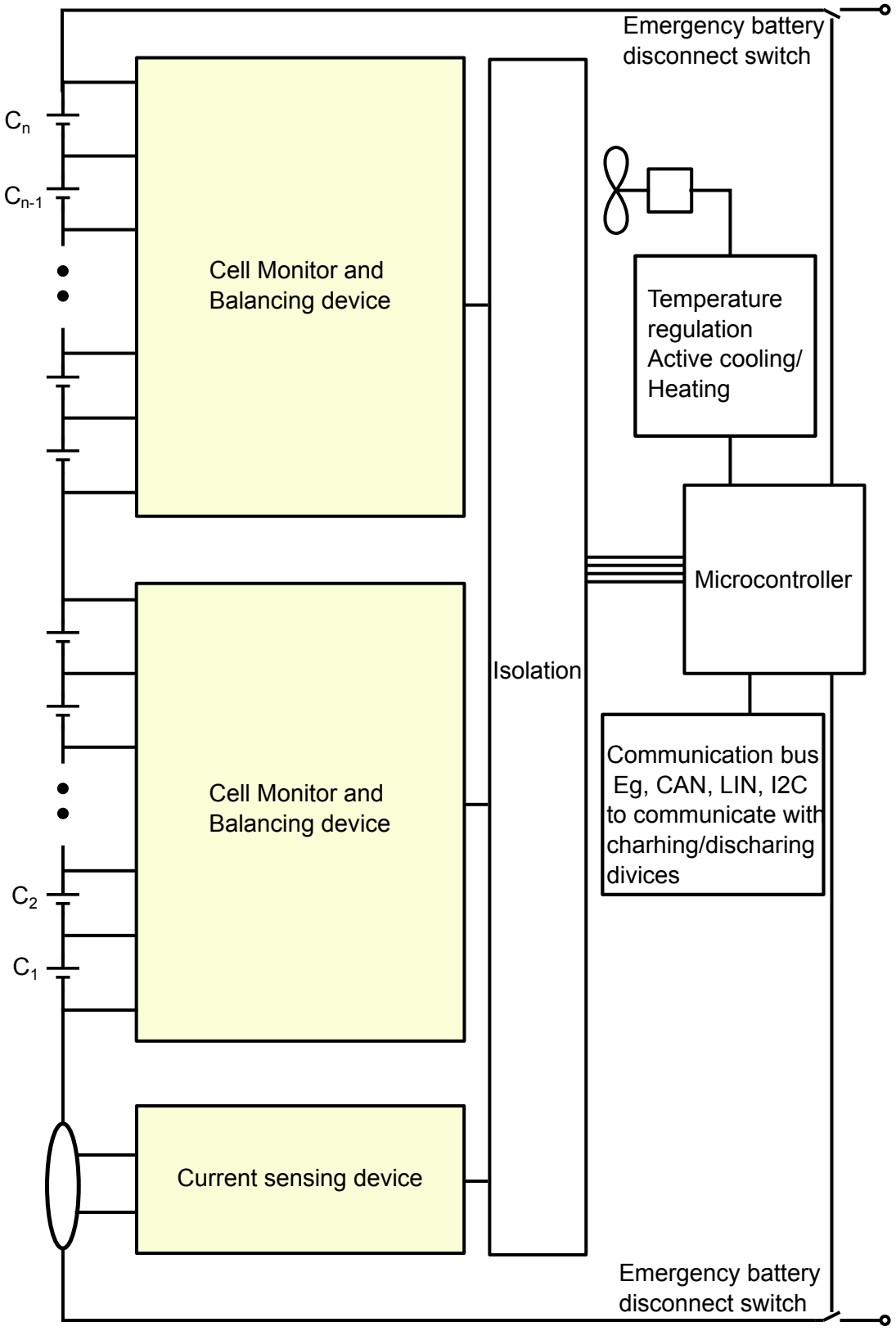

FIGURE 2.3: Typical battery management system

between -20 °C to 60 °C. Battery pack is maintained in this range by regulating the temperature with active cooling and heating mechanisms. In conventional BMS, communication between balancing devices and microcontroller is implemented using isolators.

As mentioned earlier, the focus of this work is on cell monitoring, measurement, balancing and communication between the stacked devices. The following sections of this chapter focus on each of these aspects in detail.

2.1 Monitoring and Measurement

Measurement of the following parameters is essential for BMS.

- Current (I)
- Voltage (V)
- Temperature (T)

Accurate measurement of V, I and T is required for a precise estimation of the state of charge (SOC) of the battery. In addition to measuring these parameters, under and over threshold voltages are also detected to protect the battery pack from over charging and deep discharge. In most of the BMS architectures, cell voltage monitoring and balancing is implemented as one device and current measurement as a separate device. Since the current flowing through the stack is same throughout, having a current measurement circuit in each IC increases the cost of the system. Dynamic range and accuracy requirements of current measurements are more stringent compared to cell voltage measurement. Hence a separate IC is preferred for current measurement as shown in Fig. 2.3.

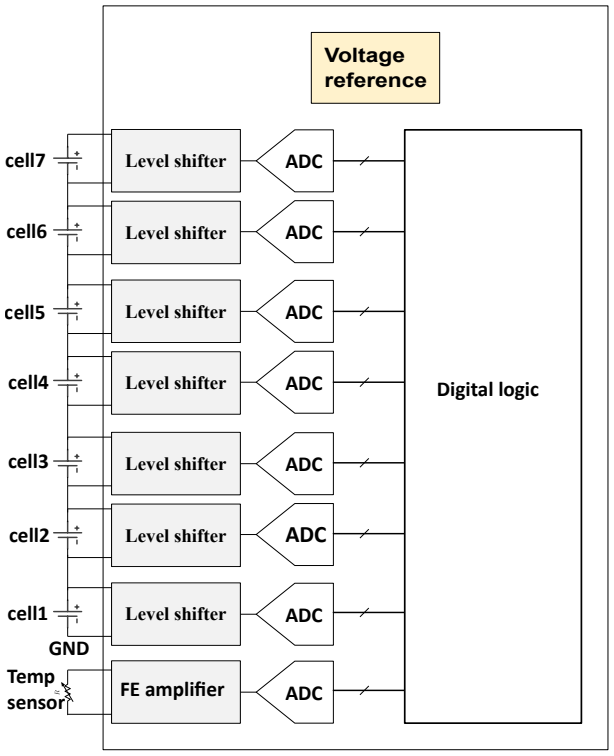

FIGURE 2.4: A typical cell monitoring system

A typical cell monitoring device is shown in Fig. 2.4, which contains level shifters and ADCs to convert cell voltages to equivalent digital codes [6]. A detailed description of level shifters and ADCs is provided in Chapter 4. Temperature of the cell pack is one of the critical parameters on which the safety of the entire BMS depends. Hence, temperature measurement is also a part of cell monitoring device. Thermistor based temperature sensors are most commonly used for BMS applications. The number of temperature sensors per cell stack is decided based on the architecture of BMS.

In addition to level shifters and ADCs, accurate reference voltage is also required for the ADC. Accuracy of the reference voltage is based on the overall measurement accuracy and typically a cell voltage measurement accuracy of 0.1% is required. This sets the initial accuracy of reference voltage to be less than 0.05%.

2.1.1 Current measurement

There are many current sensing techniques available in the literature such as resistor based sensing, hall effect based sensing and current transformer based sensing etc [24]. A current sensing resistor(shunt resistor) is the most widely used technique, that converts current to voltage by inserting a resistor in the current path. The advantages of using the sensing resistor are low cost, high accuracy and capability to measure both AC and DC currents. Power dissipation and loading effect are the major disadvantages of these sensing resistors, which however can be reduced by using a sensing resistor of small value. There are two techniques for current measurement using sensing resistor viz, high side current sensing and low side current sensing .

In high side current sensing, shunt resistor is connected between positive (+ve) terminal and of the battery load as shown in Fig. 2.5. Advantage of high side current sensing is that, placement of the shunt can be anywhere in the battery supply node to load. Main disadvantage of this implementation however is high input common mode voltage and as a result a necessity arises for level shifting of the input signal.

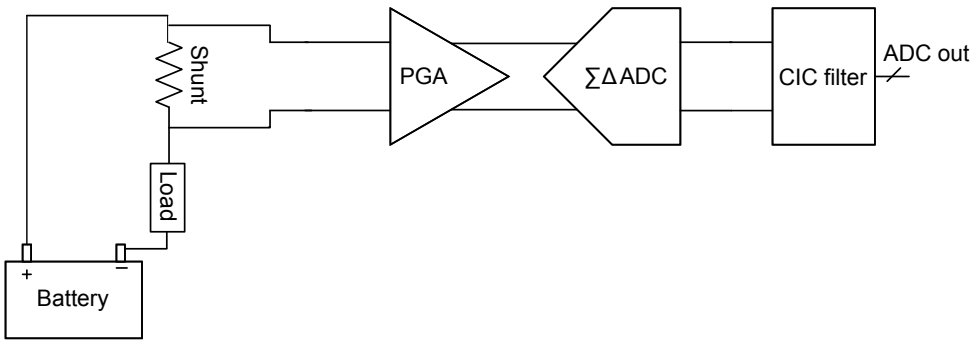

FIGURE 2.5: High side current measurement circuit

In low side current sensing, the shunt resistor is connected to negative (-ve) terminal of the battery and ground as shown in Fig. 2.6. In automotive applications, low side current sensing is popular because of its low cost, lower input common mode and a single supply. Major

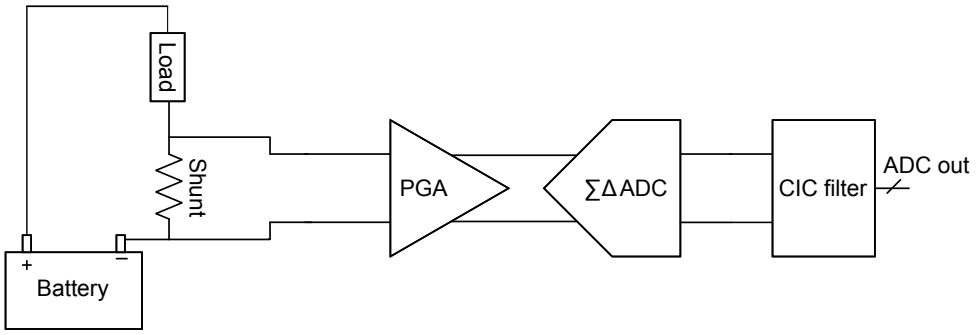

FIGURE 2.6: Low side current measurement circuit

disadvantage of this implementation is that, shunt resistor should be shorted to -ve terminal of the battery which poses significant area constraints.

In EV and HEV, based on the operation of the vehicle, current ranges from low currents of the order of 10 mA to permanent high currents of the order of 600 A and peak currents of up to 1500 A, which have to be measured with a precision of 0.1 and 0.5% respectively (1500 A range) [25]. Low side current sensing is a better choice for measuring these currents using a shunt resistor of 100 $\mu\Omega$ in order to reduce I^2R losses. With these shunt resistor and current ranges, measurement systems require a sensor interface with a measurement range of >100mV and with a resolution of better than 1μV. To accommodate these large input dynamic range, a programmable gain amplifier is required and to obtain the resolutions of less than 1μV, high resolution ADC (most applications demand 16-bit) is required. To measure currents with an accuracy of 0.1% to 0.5%, a precision bandgap with less than 0.1% is required over temperature. In this thesis, a precision bandgap is designed to monitor low side current sensing.

2.2 Cell Balancing

In a stacked battery system, the weakest cell decides the overall capacity of that battery pack, while number of full charging cycles decides the life of Li-ion cells. To prolong life time and

ensure maximum capacity utilization of a battery stack, it is essential that all the cells in a stack are maintained at the same SOC.

Individual cells that have matching SOC values (less than 3%) are usually stacked together to form a pack. However, over a period of time, SOC of each cell varies because of differences in self-discharge, temperature, internal resistance etc., of each cell. In automotive applications, if cells are not well balanced, additional capacity is used up affecting the mileage of the vehicle. This adds additional weight and cost to the vehicle.

Thus it is necessary to carry out cell balancing in a series stacked battery pack. Different balancing methods have been proposed in the literature and these can be classified as [20]

- Passive balancing
- Active balancing

In passive balancing, cells are balanced by dissipating energy into a resistor. Active balancing is achieved using different methods such as switched capacitor, switched inductor or converter. Different methods used for cell balancing are studied in[3],[4], [26],[27],[28].

2.2.1 Passive balancing

This is a simple method wherein the cell with lowest voltage is identified after measuring the voltages of all the cells and the excess voltage is dissipated using a shunt resistor. Two topologies are used in passive balancing as shown in Fig. 2.7. Parallel charge shunt is shown in Fig 2.7(a), where cell and shunt resistor are connected in parallel through a switche from $cts1$ to $cts4$. Individual as well as multiple cells can be discharged by controlling the switches. Fig 2.7(b) shows multiplexed shunt, in which a single shunt resistor is used to discharge cell voltages.

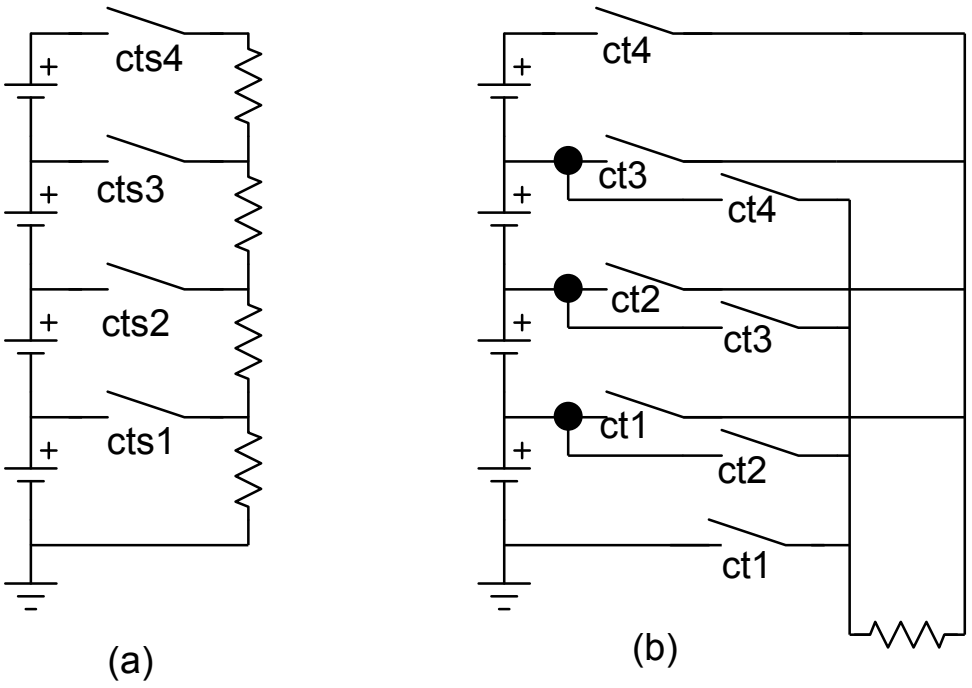

FIGURE 2.7: Passive balancing topology

2.2.2 Active balancing

In active balancing, the voltage or capacity of each cell is measured initially, after which an average voltage or capacity is calculated. Then the cells that have the highest deviation from this average value are identified. The cells with lowest voltage measured are then recharged while the cells with highest voltage are discharged.

Further, active balancing can be categorized into

- Capacitor based
- Transformer/converter based

Various such techniques are proposed and reviewed in [3],[4],[26],[27],[28]. Out of which few are discussed in detail here.

A mechanism that removes charge from a given cell, stores it and then delivers the same to another cell is called charge shuttling cell balancing. A most popular example of this mechanism

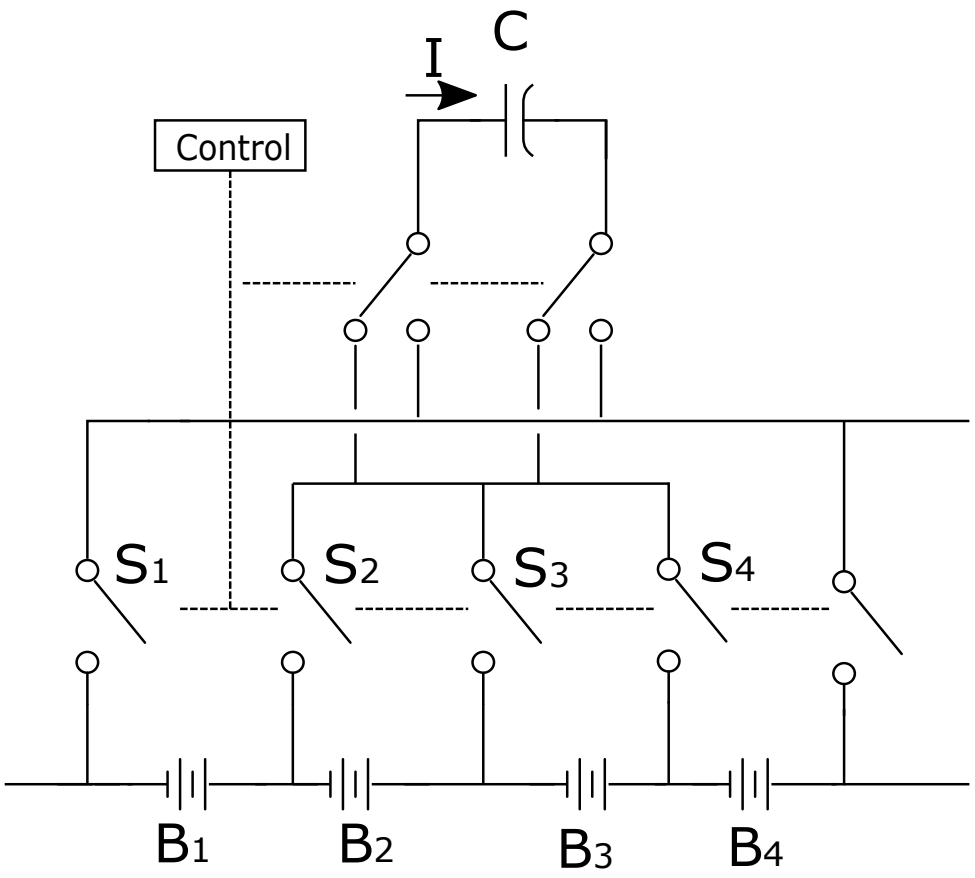

FIGURE 2.8: Flying capacitor charge shuttling method

is flying capacitor shown in Fig. 2.8. This method facilitates charging of the capacitor from the cell with highest voltage and discharge it selectively to a cell with lowest voltage. This method takes short time in balancing the cells, however employs large number of switches resulting in heavy energy dissipation.

A cascade charge shuttling method is shown in Fig.2.9. This method takes longer to charge cells with low voltage from cells with high voltage if they are placed on the opposite ends in a pack because the charge needs to go through every cell resulting in time and efficiency penalties. While this method is not useful for HEV applications, it is suitable for EV applications. Another active balancing method is energy converting method.

Fig. 2.10 shows the multi-winding transformer balancing topology. The "shared transformer" topology of this multi-windings transformer has a single magnetic core with one primary

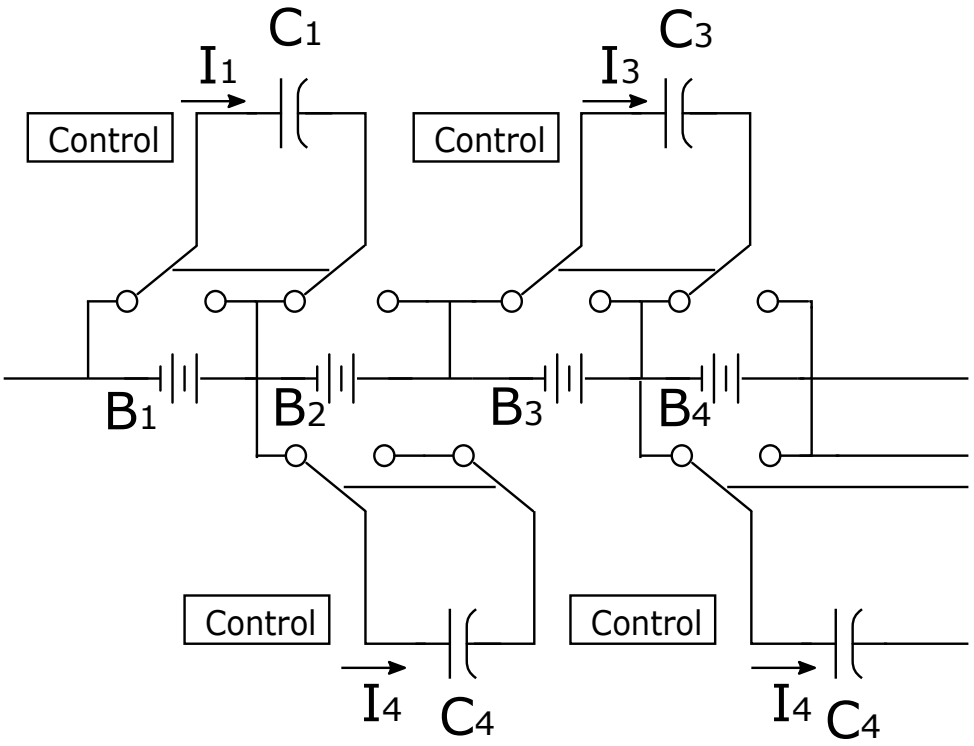

FIGURE 2.9: Balancing using Charge shuttling

winding and multiple secondary windings [3], one for each cell. Fig. 2.10 shows the two circuit configurations namely, flyback and forward configurations. In the flyback structure, when the switch connected to the primary side is on, some energy gets stored in the transformer. When the switch is off, this energy is transferred to the secondary. With the help of the diode(s), most of the current induced in the secondary is provided to the cell(s) with lowest value. In the forward structure, when there is a difference in voltage levels of cells, the switch connected to the cell with highest voltage is activated. This enables transfer of energy between this cell and the others through the transformer and antiparallel diodes of the switch. This configuration is however complex and expensive and also has a saturation problem.

Synchronous switching bidirectional flyback converters are used to achieve active cell balancing for a given target cell and is shown in Fig. 2.11 [4]. Assume the weakest cell in the pack is identified as cell2 and it needs to be charged. First, the switcher S_P is turned on applying the entire pack voltage to the primary winding which stores energy in the transformer's magnetizing

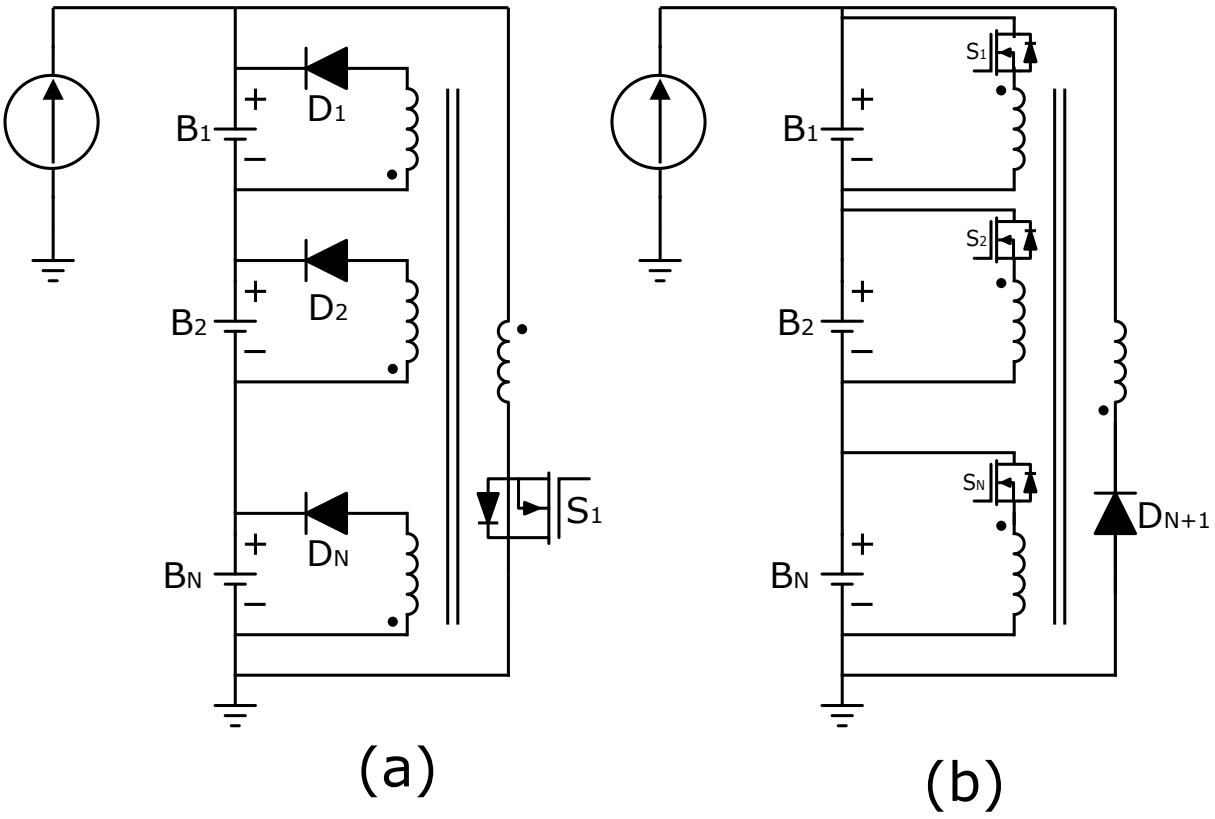

FIGURE 2.10: Balancing using Multi secondary windings transformer, (a) Flyback (b) forward structure [3]

inductor. When the switcher Sp is turned off, the MOSFET S_2 associated with the cell2 (the weakest cell in our case) is turned on and the energy stored in the transformer is transferred to cell2. This extends the run time of the battery pack by ensuring that the weakest cell does not reach the end of discharge earlier, compared to the other cells. This operation therefore achieves cell balancing by transferring energy from the pack to the required cells. On the other hand, a requirement for shifting energy from a strong cell to the entire pack might also occur. With no cell balancing mechanism, the process of charging is stopped when one cell attains maximum voltage even when rest of the cells are not fully charged. Suppose cell N_1 has been detected as the cell with highest voltage in the battery pack. The energy from cell N_1 has to be discharged and redistributed into the pack, the MOSFET S_{N1} is turned on first resulting in a connection between the winding and cell N_1 and the energy from this cell is then stored as magnetic field in the winding. As soon as the MOSFET S_{N1} is off, MOSFET Sp is turned on, which is connected

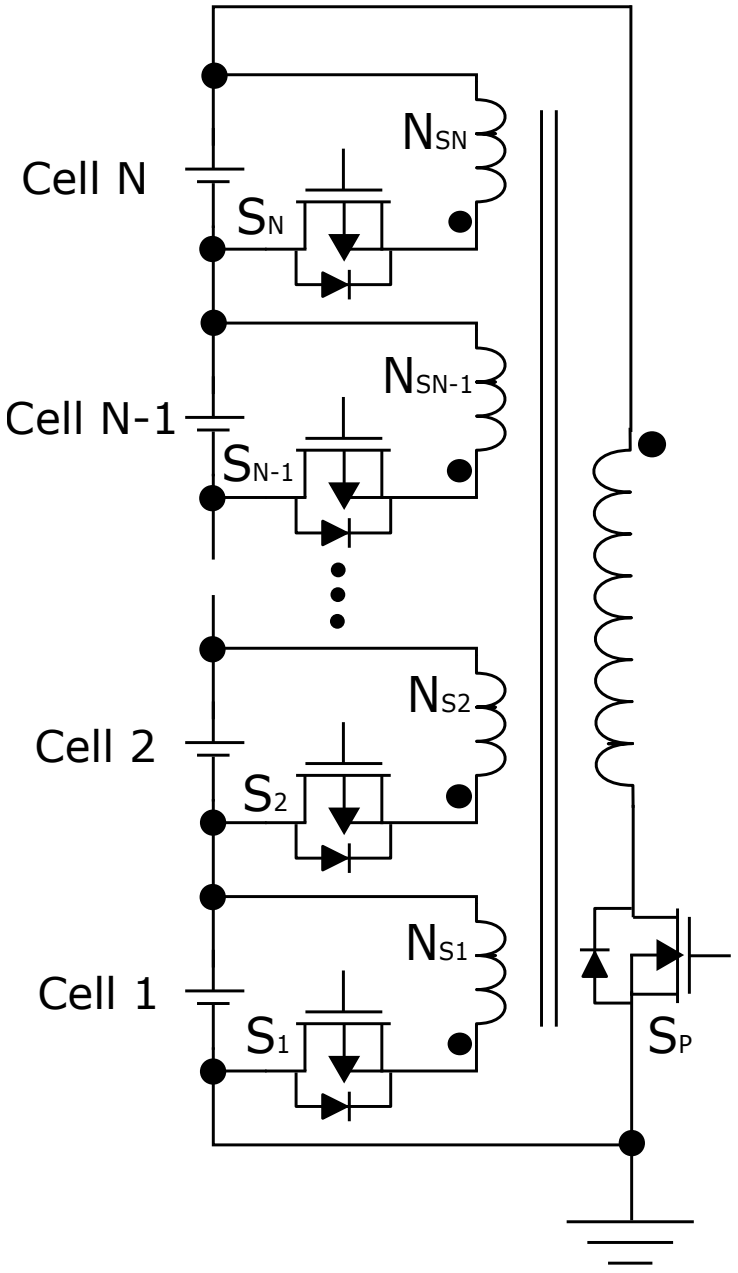

FIGURE 2.11: Active balancing using synchronous bidirectional flyback converter [4]

to the primary winding. This results in energy stored in the magnetic field to be redistributed to the entire pack via the primary winding.

A comprehensive comparison of the active and passive balancing techniques discussed above is provided in Table 2.1.

TABLE 2.1: Comparison of Active and Passive balancing techniques [12]

	Topology		Pros	Cons
Passive	Multiplexed Charge Shunt		Cheap, simple	0% Efficiency, very slow
	Parallel Charge Shunt		Cheap, simple, fast	0% Efficiency, trade-off between speed and generated heat
Active	Module-to-Cell		Relatively simple	Switch network, High isolation voltage of the DC/DC
	Cell-to-Cell	Distributed	Moderate efficiency	Bulky, Complex control
		Shared	Moderately fast	Switch network
	Cell/module bypass		High balancing efficiency	High current switches,Complex to implement
			Very fast and flexible	Decrease battery efficiency during normal operation

2.3 Communication between stacked devices

A data link that monitors the performance, logs data, provides diagnostics and/or set system parameters may be used to provide the communication function of a BMS. Alternatively, it may also be provided by a channel that carries system control signals. The communications protocol to be used is determined by the application of the battery. To ensure smooth and proper operation of the vehicle, the BMS in EVs must communicate with motor controller and the upper vehicle controller. Two major protocols are used by the BMS for communication: (i) through the data bus or (ii) through controller area network (CAN) bus. RS232 connection and EIA-485 (also called the RS485 connection) are included in the data buses. CAN bus is the industry standard for on-board vehicle communication and is commonly used in EV application.

Communication between stacked ICs needs to have a proper isolation from the ground as the common mode voltage for each IC in a given stack is different and is implemented with galvanic isolation or daisy chain. Fig. 2.12 shows the implementation of galvanic isolation between the stacked devices. It uses signal transformers such as ethernet LAN magnetics, which are ideal for providing the isolation needed. LAN transformers are usually bulkier and expensive and to provide proper isolation and a trade-off should be made between safety, size, cost and signal integrity.

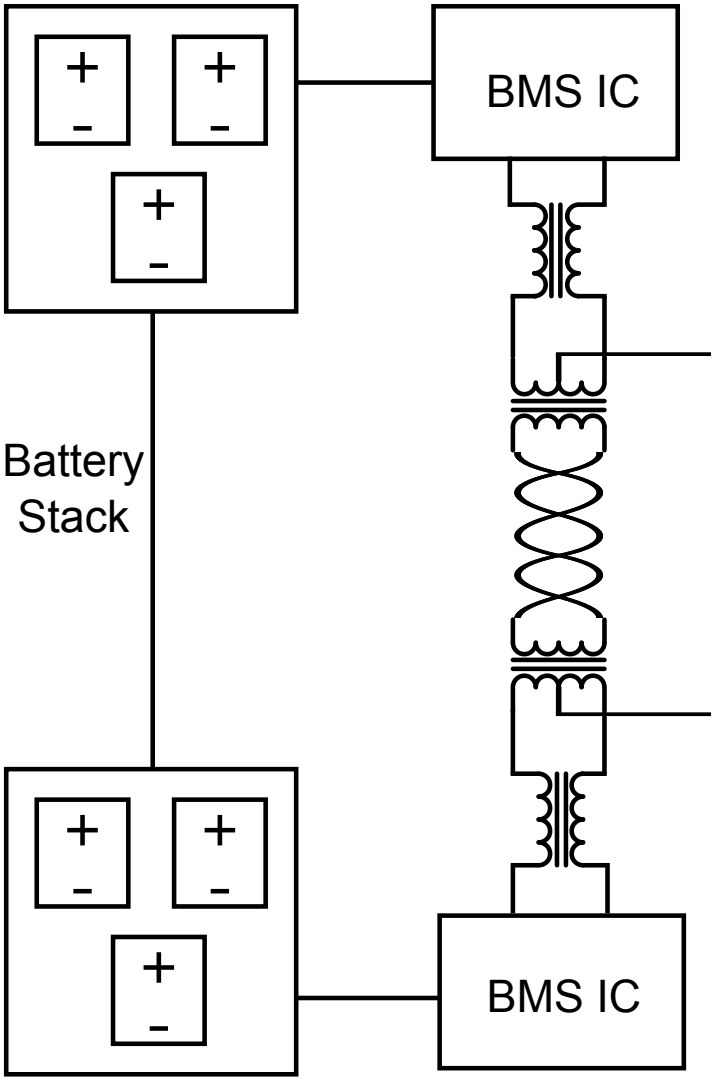

FIGURE 2.12: Communication between stacks using galvanic isolation [5]

Most common implementation with Galvanic isolation is using CAN Communication between the models and vehicle CAN bus. Fig 2.13 shows one of these implementations. There are however several combinations possible with this communication architecture.

Another implementation of stack to stack communication is with daisy chain presented in [6], [8], [29]. The communication between ICs in the stack which avoids the usage of expensive isolators discussed above is required to reduce the overall cost of BMS.

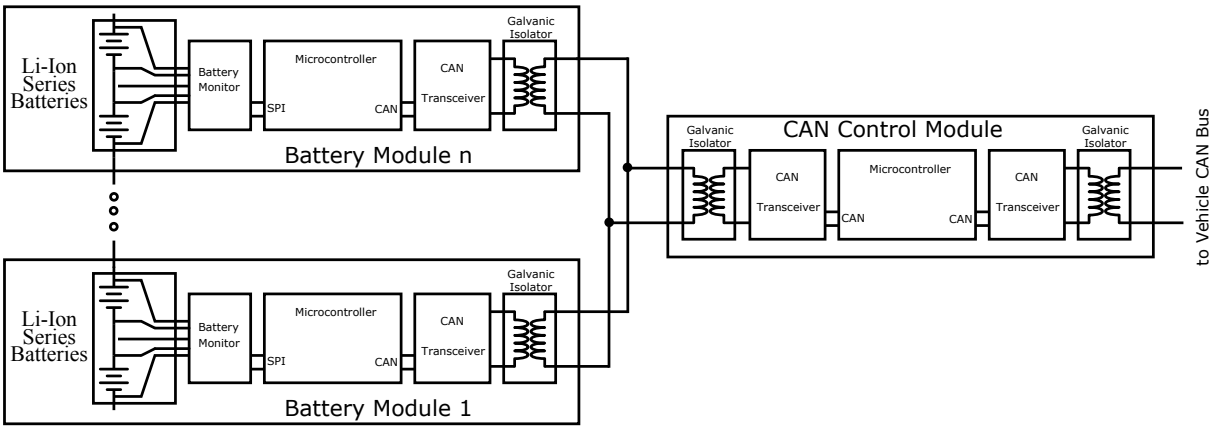

FIGURE 2.13: Communication between stacks using isolated CAN

2.4 Proposed BMS solution

The emergence of functional safety standard ISO26262 [30] has resulted in increased time and effort in designing automotive systems. The effort required to ensure this compliance is even more tough in case of lithium based BMS which involves high-end processors and complex software. A typical cell monitoring system which provides individual cell voltages includes complex software and communication between sensors and host microcontroller. To prove that such system complies with the ISO26262 functional safety standard has been a great challenge to automotive manufacturers.

Customary cell monitoring approach today involves measurement of each cell voltage followed by communicating this data to a host microcontroller in real time. The controller then makes use of this data into useful information like SOC, SOH and safe operating area analysis of the cells, using a complex software.

This approach has drawbacks in the form of requirement of complex software and high speed data communication. Noise effects and interference present in the engine compartment must be overcome during the transmission of cell voltage values to the microcontroller, while also coping change from a high-voltage to a low-voltage domain. The cost and complexity of the system is increased by the peripheral components like shields and isolation couplers.

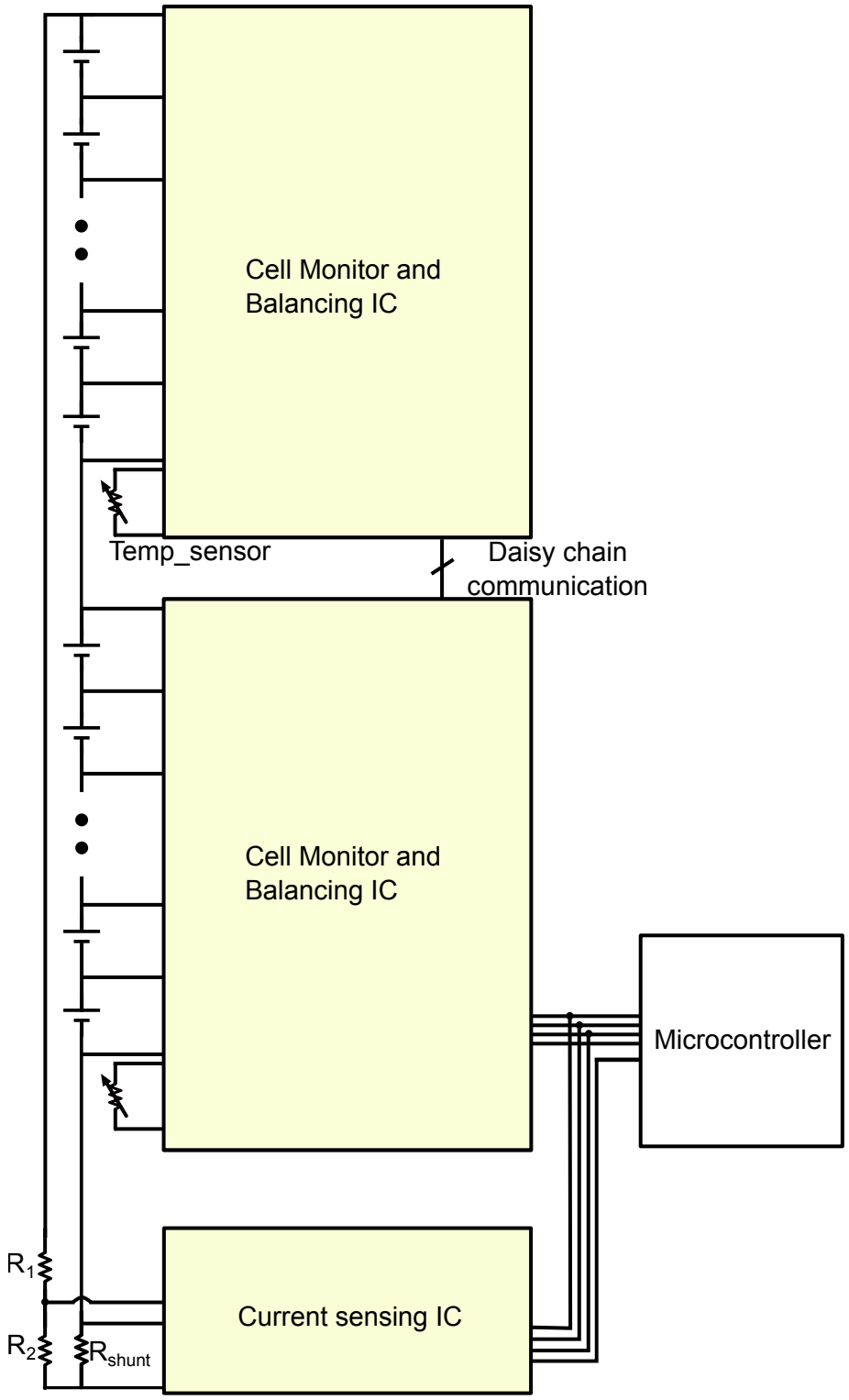

FIGURE 2.14: Proposed battery management system

In the proposed solution, the BMS uses both pack monitor and cell monitoring systems. Voltage and current at the level of entire battery are monitored by the pack monitor. The proposed battery monitoring system is shown in Fig. 2.14. The voltage of each individual cell and their temperatures at selected locations is handled by a cell monitoring IC. The measured battery voltage is compared with an aggregate of measured cell voltages to validate the BMS is functioning properly. Because such verification is based on measurement systems that are fully independent, it validates the entire measurement signal path from the sense wire to the software. This results in a more comprehensive validation than possible with conventional architectures where functional safety compliance is implemented at individual ICs.

2.5 Conclusion

This chapter discussed the need for separate devices for cell monitoring and balancing as well as current sensing. Different current sensing methods have been discussed and the requirement of designing an accurate bandgap was highlighted. The measurement accuracies required by these designs were also discussed. Different balancing methods have been detailed, advantages and disadvantages of each method were discussed. The need for communication between stacked ICs without isolators was also emphasized. Proposed battery management system to monitor cell voltages and pack voltage has been discussed.

Chapter 3

Bandgap reference design for Low side current sensing

3.1 Introduction

In BMS applications, current sensing is essential for estimation of accurate SOC. Low side current sensing is preferred over other techniques due to low cost, lower input common mode and a single supply. A conventional low-side current sensing of a battery is shown in Fig. 3.1. Shunt resistor converts current to voltage, which is amplified by a programmable gain amplifier (PGA). A sigma delta ADC then converts this amplified voltage to an equivalent digital code. In sigma delta modulator (SDM), input and reference are sampled on to input capacitors in the first phase of the clock while the second phase is used for error integration [31]. Most of the output of CMOS bandgap reference are high impedance nodes and are not suitable to drive switching loads [32], such as the input capacitors of SDM present in the circuit. This problem is overcome by driving the switched capacitor nodes with reference buffers [33] as shown in Fig.3.1. However, these reference buffers require additional area, power and also introduce additional

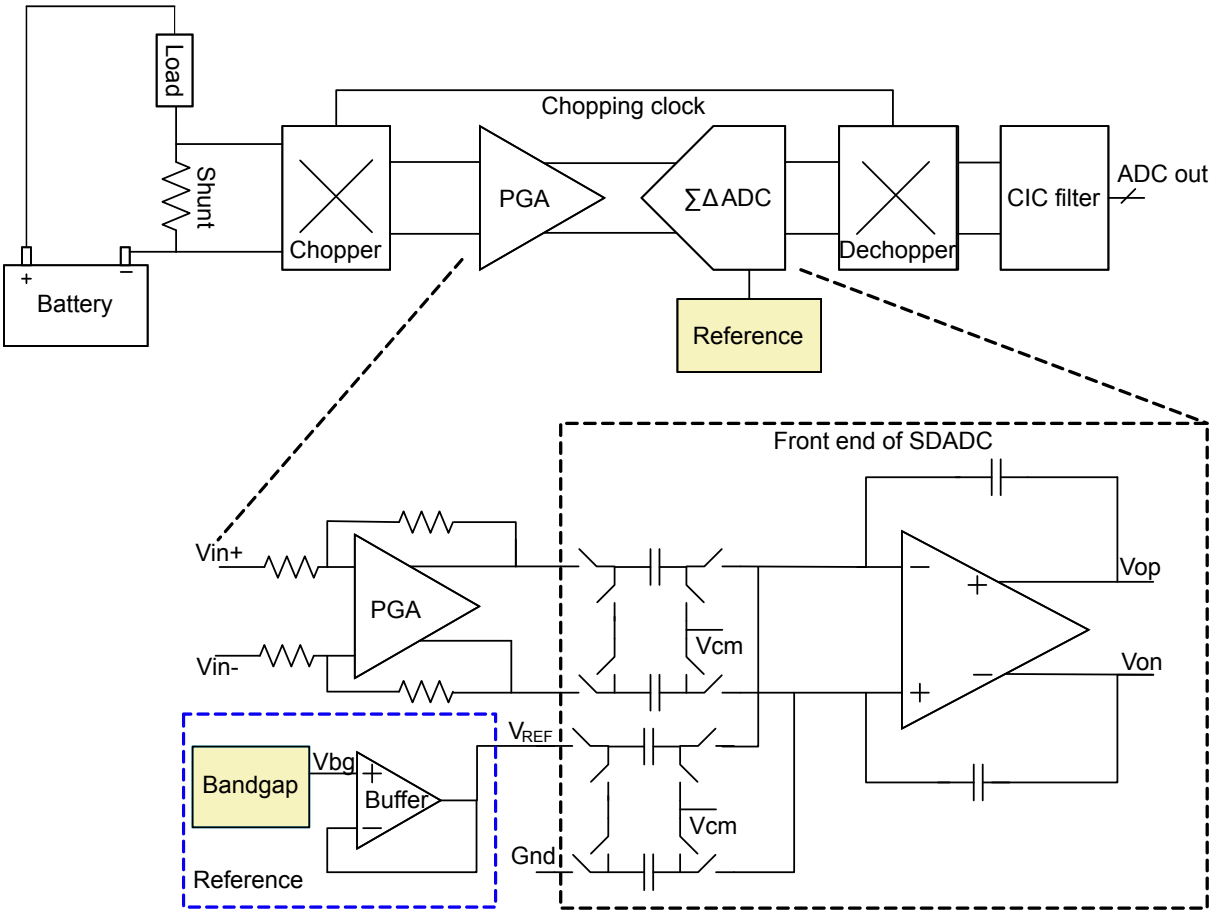

FIGURE 3.1: Low side current measurement of battery and signal path front end with SDADC

errors such as offset and its drift over temperature. Hence it is essential to design an accurate reference across process, voltage and temperature (PVT) to reduce measurement errors in ADCs.

Accurate references are generated with the help of digitally corrected bandgap references [34] and digitally assisted bandgap references [35]. However, digital implementation in both these designs consumes significant area. In the proposed measurement system, bandgap reference is trimmed for temperature and magnitude and the correction of residual curvature is achieved using polynomial curve fitting. Correction based on the coefficients of the polynomial is implemented digitally on a microcontroller. The bandgap reference designed in this work is a part of low-side current sensing application and provides accurate reference for the high precision 16-bit sigma-delta ADC. Further, this bandgap does not require additional buffer as required in conventional switched capacitor (SC) circuits.

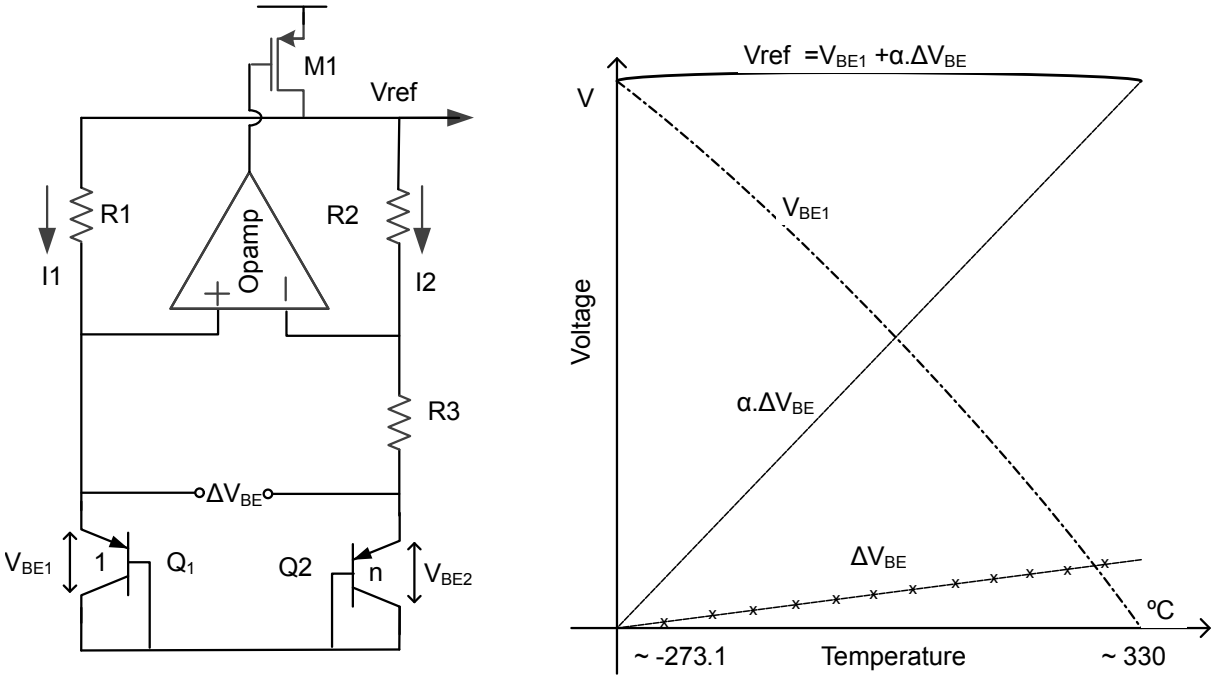

FIGURE 3.2: Typical Bandgap reference

3.2 BANDGAP REFERENCE

A conventional bandgap reference circuit is shown in Fig. 3.2[3]. A bandgap reference voltage is generated by adding two voltages that have complementary temperature coefficients with appropriate multiplication constants. The positive and negative temperature coefficients are generated with standard bipolar junction transistors (BJTs). The diode voltage drop across the base emitter junction, V_{BE} of a bipolar junction transistor (BJT), changes Complementary To Absolute Temperature (CTAT). When two BJTs are operated with unequal current densities and areas, the difference in the base emitter voltages, ΔV_{BE} of the transistors, is Proportional To Absolute Temperature (PTAT)[33, 36, 37].

The equation governing PTAT is given by

$$V_{BE} = V_T \ln(\frac{I_C}{I_S}) \tag{3.1}$$

where I_C is the collector current determined by bias circuit and I_S is transistors saturation

current. Saturation current of BJT has a strong temperature dependency and base-emitter voltage has a negative temperature coefficient given by

$$\frac{\partial V_{BE}}{\partial T} = -1.5mV/^{\circ}K \tag{3.2}$$

$$\Delta V_{BE} = V_T \ln mn \tag{3.3}$$

where V_T is given by

$$V_T = \frac{kT}{q} \tag{3.4}$$

where, k is Boltzmann's constant, T is the absolute temperature, q is the electron charge and m, n are the ratios of the current and area densities of the two BJTs respectively.

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} = 0.087mV/^{\circ}K \tag{3.5}$$

To match the temperature coefficient of V_{BE} and ΔV_{BE}, a multiplication factor α is chosen such that numerically both PTAT and CTAT coefficients are same.

$$\frac{\partial V_{BE}}{\partial T} = -\alpha \frac{\partial \Delta V_{BE}}{\partial T} \tag{3.6}$$

where α can be determined by

$$\alpha = \frac{1.5}{0.087} = 17.2 \tag{3.7}$$

The reference voltage generated, V_{REF} is governed by the equation given below

$$V_{REF} = V_{BE} + \alpha.\Delta V_{BE} \tag{3.8}$$

where α = R1/R2 is the gain, implemented with resistor ratio and V_{BE} is the base emitter voltage of the BJT.

3.2.1 Proposed Bandgap Circuit

Variations in any bandgap reference voltage are mainly due to three parameters: process, temperature and supply. The proposed design attempts to demonstrate the minimization of these variations to achieve the required accuracy. Fig. 3.3 illustrates the complete bandgap circuit including start up circuit, bias circuit to generate PTAT and bandgap core. Start-up circuit helps to start the bandgap to a stable operating point by considering slow and fast power supply ramps.

In the bias circuit shown in Fig. 3.3, MP_1 and MP_2, MN_1 and MN_2 are designed to have the same current in both the branches by sizing the PMOS and NMOS transistor pairs equally. Since the W/L values and currents are same in MN_1 and MN_2, the gate to source voltages of both NMOS transistors are equal. This forces equal voltages at nodes A and B. Also, voltage drop across the BJT Q_1 is V_{BE1} and the voltage drop across the Q_2 BJT is V_{BE2}. These two voltages are not equal because BJTs have different areas with Q_2 occupying eight times more area compared to that of Q_1. The current through the resistor R_0 is given by

$$I = \frac{\Delta V_{BE}}{R_0} \tag{3.9}$$

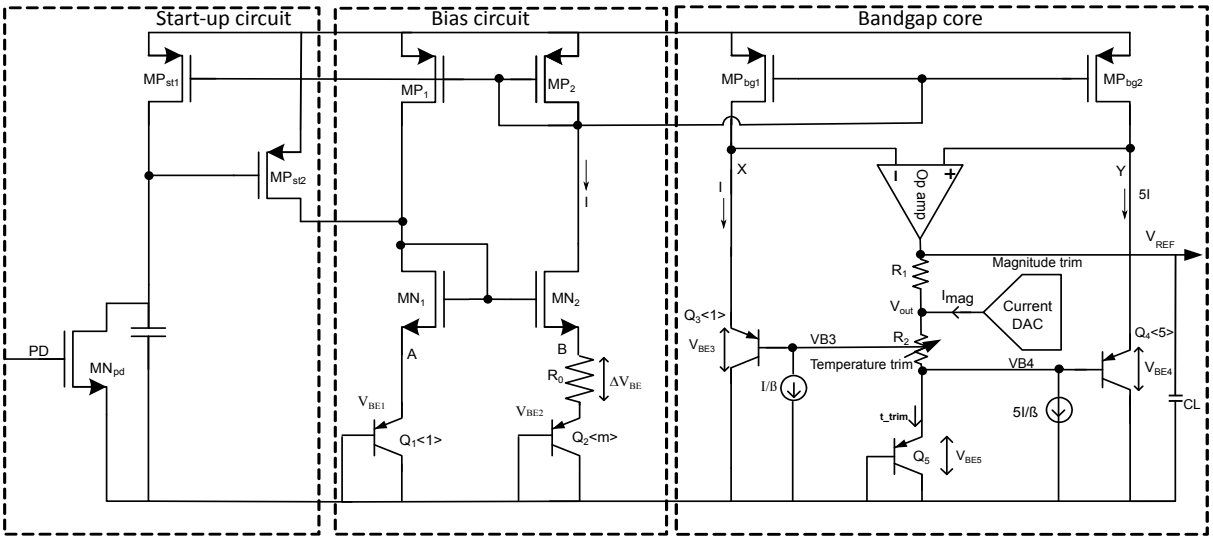

FIGURE 3.3: Schematic of proposed bandgap circuit

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln m \tag{3.10}$$

where V_T is given in Eq. (3.4) and m is the ratio of the areas of the BJT's $Q_1$and Q_2.

$$I = \frac{kT \ln m}{qR_0} \tag{3.11}$$

The above equation shows a supply independent current through the resistor R_0 and is directly proportional to the absolute temperature.

3.2.2 Design of bandgap core

Bandgap core in Fig. 3.3 shows the circuit of the bandgap reference with trim blocks implemented. The supply independent PTAT currents of I and $5I$ are mirrored in to the BJTs, where the area of Q_4 is 5 times that of Q_3. By using these currents, large ΔV_{BE} is realized with less number of BJTs (only 5). If the branch currents of these two BJTs are same, then to achieve the same current densities in both these BJTs, their areas have to be in the ratio of 1:25. Therefore, by using a current of $5I$ in Q_4, its area is brought down by 5 times. A high gain operational

amplifier (Op-amp) forces the same voltages at nodes X and Y. The base nodes of Q_3 and Q_4 are biased by using the supply independent PTAT currents of I/β and 5I/β respectively, where β is the current gain of the transistor. By biasing the bases with base current with a ratio of $1/\beta$, reduces the dependency of process spread associated with β

Bandgap reference, V_{REF}, is taken at the output of the Op-amp, while bandgap voltage is the sum of the base to emitter voltage (V_{BE5}) of Q_5 and voltage drop across resistors R_1 and R_2. Part of R_2 is connected between base nodes of BJTs Q_3 and Q_4 which generates a PTAT voltage. By adjusting R_2, a portion of the PTAT voltage changes in the bandgap output which compensates for the temperature variations.

From Fig. 3.3 it can be found that current in the output branch of the bandgap is given by

$$I_{t\_trim} = \frac{V_{BE3} - V_{BE4}}{R_2} \tag{3.12}$$

and the bandgap output voltage is given as

$$V_{REF} = V_{BE5} + I_{t\_trim}R_2 + (I_{t\_trim} \pm I_{mag})R_1 \tag{3.13}$$

The operational amplifier is designed to drive the switched capacitive loads which helps in avoiding the usage of an additional buffer to drive ADCs.

Simulation results of the bandgap in typical corner is shown in Fig. 3.4, which shows the curvature of the bandgap. Fig. 3.5 shows the simulated output of bandgap across the corners, which shows a large variation across temperature and process corners. Such variation explains the need for a trimming circuit.

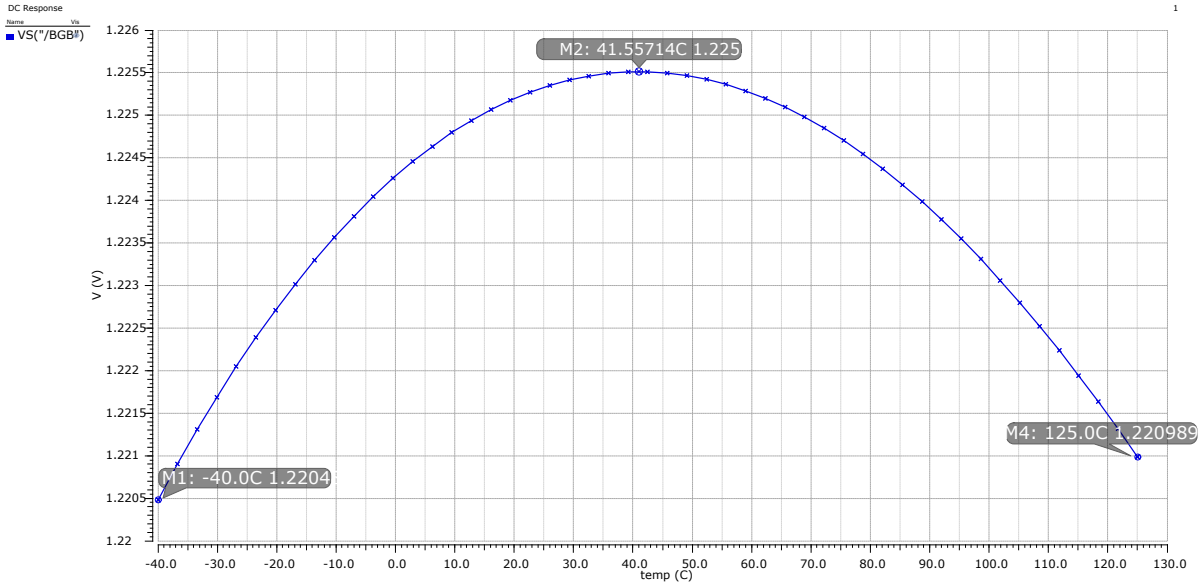

FIGURE 3.4: Simulation results bandgap output in typical corner

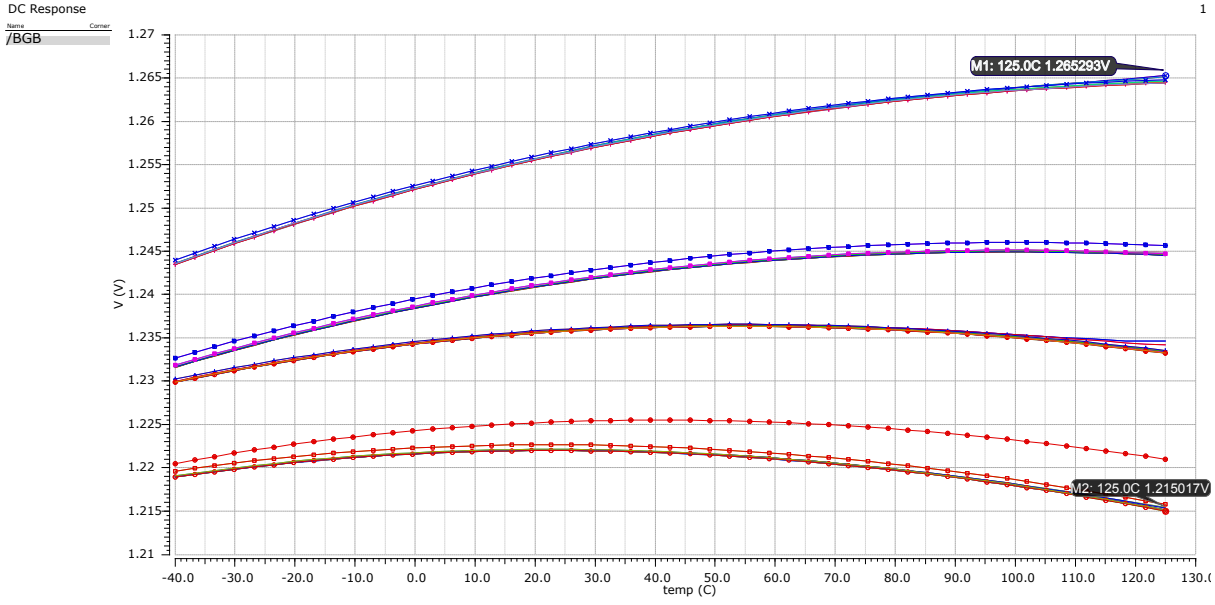

FIGURE 3.5: Simulation results bandgap output across the corner

3.2.2.1 Design of temperature trimming block

Temperature trimming circuit is shown in Fig. 3.6, where PTAT current flows though R_2. It is connected between base nodes of Q_3 and Q_4 which are VB3 and VB4 respectively. R_2 is implemented with a sum of 32 equal series connected resistors (R_T). The value of R_2 is changed by the trim code, which results in a change in PTAT current. The change in current flowing

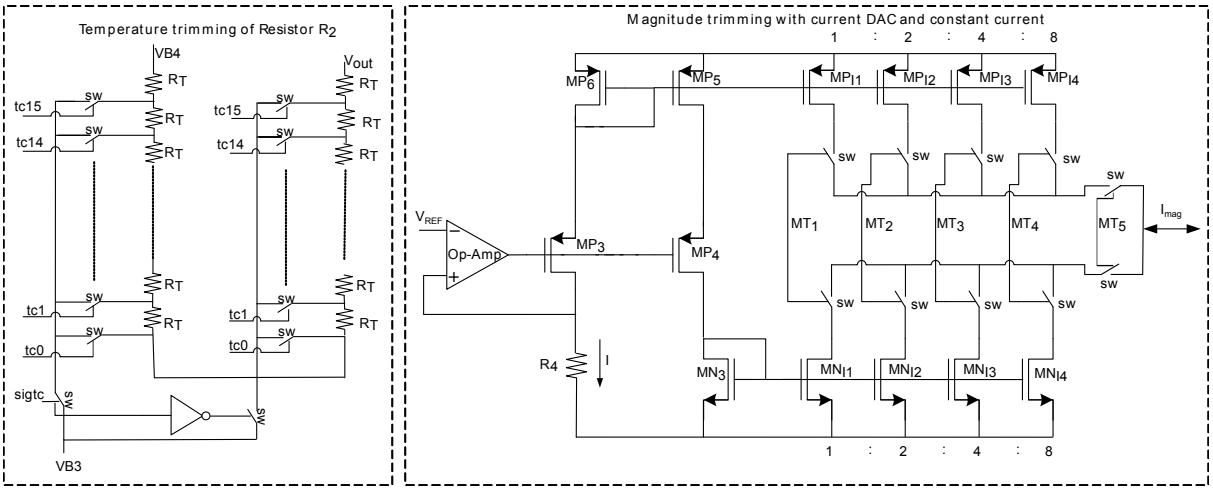

FIGURE 3.6: Schematic of temperature and magnitude trim circuits

through a part of R_2 causes a change in PTAT voltage, in turn changing the value of bandgap reference voltage and its variation across a temperature range.

PTAT voltage at the output of the bandgap reference can be increased or decreased with most significant bit (MSB), which is "sigtc" of the trim bits shown in Fig. 3.6. The resistance R_2 connected between the bases of Q_3 and Q_4 can be changed by controlling the switches with decoder output control signals tc0 to tc15. The value of the unit resistor is 40 Ω to compensate for the total variation of bandgap across the process and temperature with the trim bits. Layout of the temperature trim circuit is very critical because of very small unit resistors. The contact resistance and the routing resistance of the circuit are optimized to get less than 0.1 Ω to minimize the trim step to step variation.

Fig. 3.7 shows the simulation results of bandgap output with respect to temperature for all the trim codes. It is evident that, some of the codes are CTAT in nature while some are PTAT. As shown in Fig. 3.4 and Fig. 3.5, bandgap voltage in a typical corner is constant over temperature compared to other corners. The trim codes shown in Fig. 3.7 can now be used to compensate temperature variation of the bandgap voltage across corners.

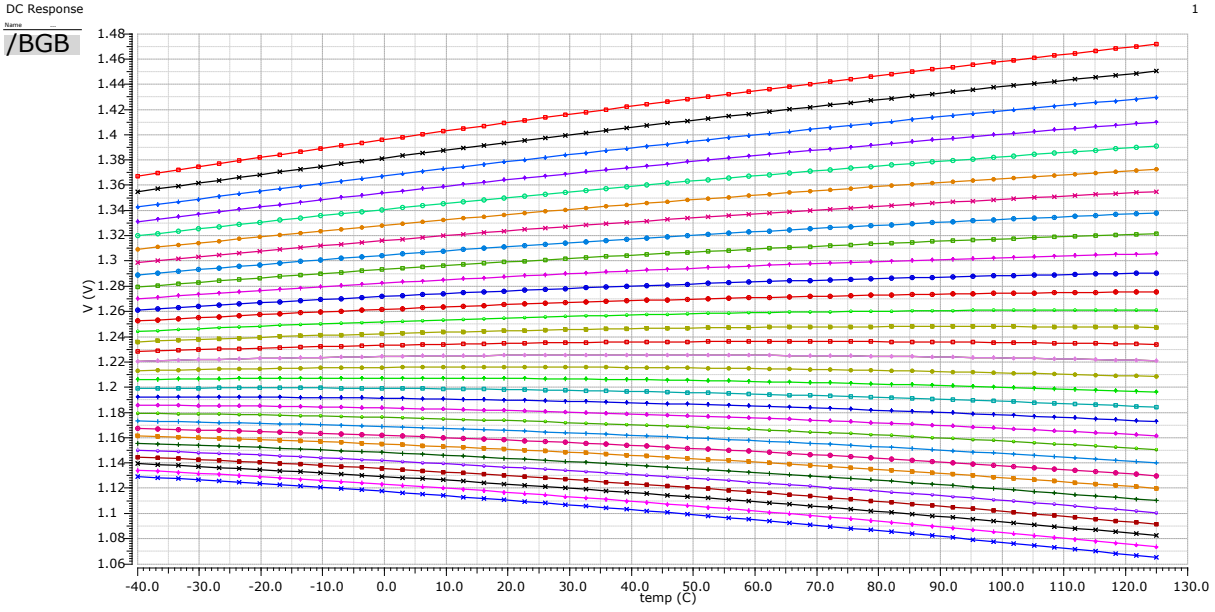

FIGURE 3.7: Simulation results of V_{REF} voltage across different temperature trim codes for complete temperature range

3.2.2.2 Design of magnitude trimming block

Absolute magnitude of bandgap reference varies from sample to sample even after compensating for temperature variations. This creates a need for magnitude trimming circuit which is shown in Fig. 3.6. Initial accuracy of the bandgap voltage is achieved by sourcing or sinking a constant current (I_{mag}) through resistance R_1 in the output of the circuit. In this trimming circuit, the bandgap voltage, V_{REF} is used to generate the constant current. A two stage operational amplifier is used in unity gain feedback to generate constant current I_{CONST} and is given by

$$I_{CONST} = \frac{V_{REF}}{R_4} \tag{3.14}$$

This constant current is mirrored into 4 PMOS and 4 NMOS transistors in a binary weighted ratio of 1 : 2 : 4 : 8 respectively as shown in the Fig. 3.6. One end of the control switches is connected across the drain of the transistors and the other end of is shorted together separately for PMOS and NMOS transistors. These two shorted terminals are connected to each other by

using two more control switches. The sourcing or sinking of current (I_{mag}) in the resistor R_1 is controlled by MSB (MT_5) of the trim bits which control magnitude of the current (I_{mag}).

The current flowing through the resistor R_2 is fixed and defined by the two base voltages of Q_3 and Q_4. The current flowing through the resistor R_1 is the combination of the currents I_{t_trim} and I_{mag}. If the current in the magnitude trimming block is a sourcing current, then the bandgap reference voltage is given by

$$V_{REF} = V_{BE5} + I_{t\_trim}R_2 + (I_{t\_trim} - I_{mag})R_1 \tag{3.15}$$

If it is a sinking current, it is given by

$$V_{REF} = V_{BE5} + I_{t\_trim}R_2 + (I_{t\_trim} + I_{mag})R_1 \tag{3.16}$$

To increase or decrease the bandgap voltage after temperature trim, the current I_{mag} can be adjusted by using the appropriate trim bits (MT_1 to MT_5). The value of the magnitude trim step size is given by

$$\Delta V_{BE} = R_1 I_{mag} \tag{3.17}$$

Since matching between devices is critical to reduce offsets, extreme care is taken during the layout to match the devices.

3.2.3 Trimming and calibration

To reduce variation of proposed bandgap reference, two temperature trimming circuits for temperature variation and a magnitude trimming circuit for process variation have been implemented. Temperature trimming is performed by collecting the bandgap reference values at -20 °C and at

60 °C for all trim-codes and finding the best trim code for which reference has least variation across temperature. Magnitude trimming is performed to get the reference of 1.22 V for process variation at room temperature. This magnitude trimming has no effect on temperature variation of the bandgap because the current used for absolute trim is a constant current pumped into the resistor. Similar poly resistors are used to generate the trim current and to trim the absolute value of the reference voltage at the output of bandgap.

A simple PTAT based internal temperature sensor is implemented in this design. Since temperature is a slow varying signal, it is multiplexed with voltage channel to save area required by the additional ADC. Temperature is measured at an interval of 10 msec which can be programmed based on application.

Compensation factor is provided with a polynomial equation of K_{comp} = A·T^2 + B·T + C. Where $K_{comp}$is the compensation factor for V_{REF} drift over temperature and is normalized to 1 at room temperature. T is the measured temperature from internal temperature sensor and A, B and C are the coefficients of the polynomial obtained after curve fitting.

With trimming, non-linear behaviour of the bandgap reference is minimized. Further, second order curvature can be corrected by multiplying the compensation factor with the ADC output.

3.3 EXPERIMENTAL RESULTS

The circuit was fabricated in 0.35 µm standard CMOS technology. Silicon die picture and layout of the bandgap reference circuit are shown in Fig. 3.8. The circuit has been tested to identify the best trim codes for temperature and magnitude. Bandgap output with respect to temperature for temperature trim codes is shown in Fig. 3.9. To find the best trim code across the temperature, experiments have been conducted by sweeping the trim codes for a particular temperature. Fig

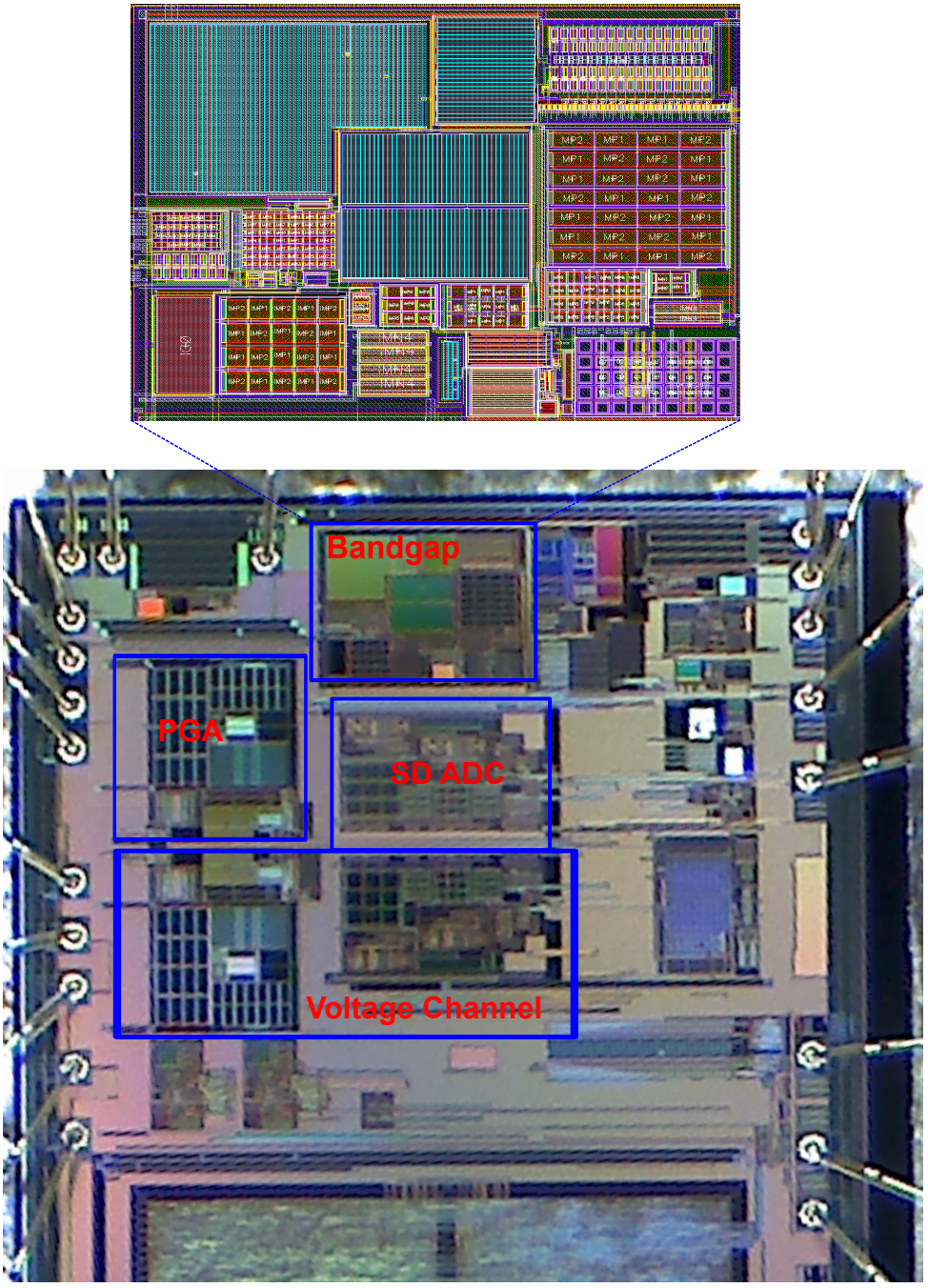

FIGURE 3.8: Layout and die picture of the bandgap reference shown as part of IC

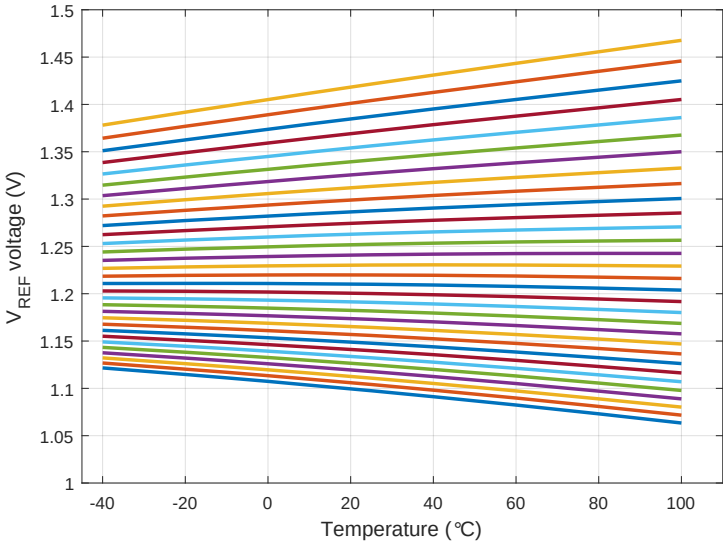

FIGURE 3.9: V_{REF} voltage across temperature for different temperature trim codes

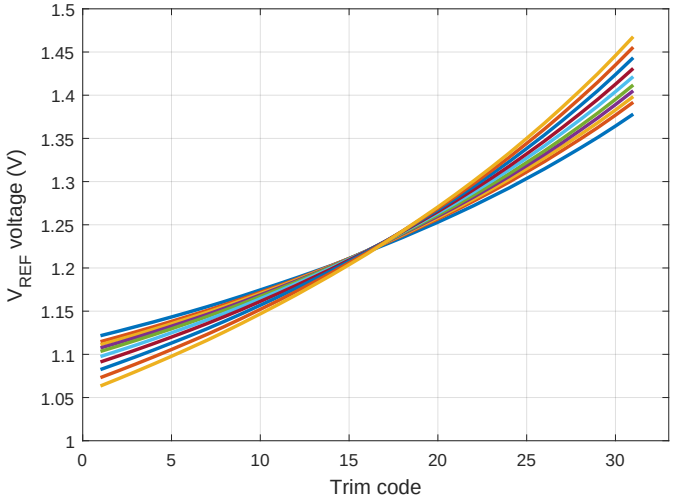

FIGURE 3.10: V_{REF} voltage across different temperature trim codes for complete temperature range

3.10 shows the measured results for a sample across different temperatures and trim codes. It can be seen from the Fig. 3.10 that, codes close to 15 give better results across temperature. Fig. 3.11 shows the result of sweeping temperature from 15 to 18 codes, it is clear that code 17 gives the best performance for this sample. V_{REF} data with respect to all the trim codes is collected at two temperatures -20 °C and 60 °C and from this the best trim code is found. After the temperature trim, magnitude is trimmed to get an absolute value of 1.22V. Fig 3.12 shows the relative error after trimming, from which it is clear that bandgap curvature is present and

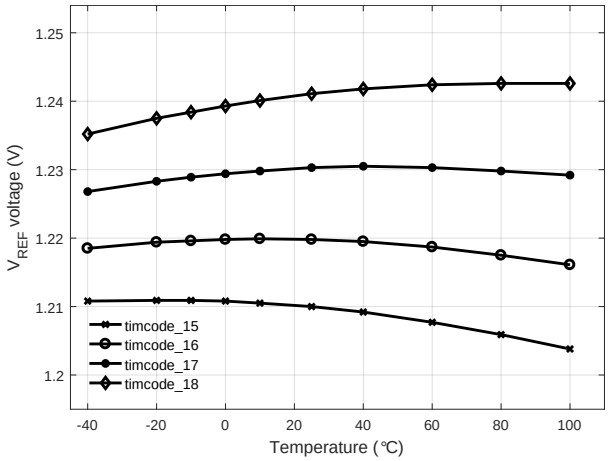

FIGURE 3.11: V_{REF} voltage across temperature for selected temperature trim codes

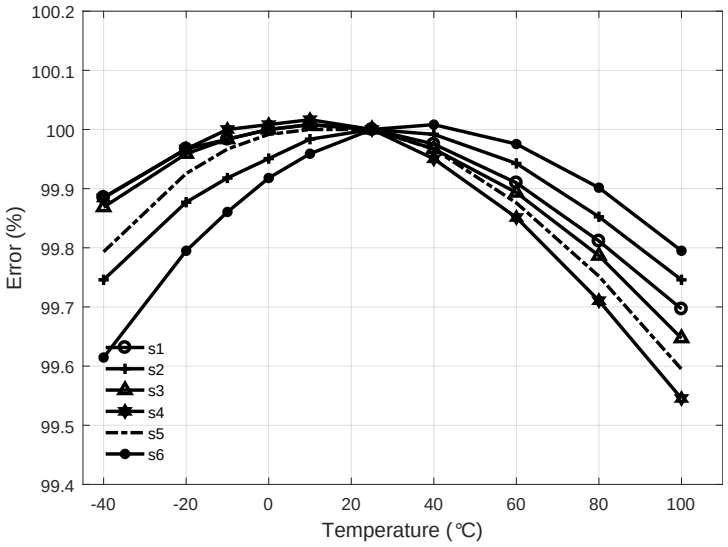

FIGURE 3.12: V_{REF} relative error across temperature after trimming

needs a correction. After the calibration with compensation factor as discussed in the previous section, accuracy of bandgap is shown in Fig 3.13. The overall system error can be seen to be less than ±0.8% which is within the specification of ±1% required for this application.

A comparison of the proposed bandgap with previously published bandgap references is shown and summarized in Table 3.1. Although proposed design uses multiple measurements, it provides a low area solution without buffer to drive the switched capacitor loads. Polynomial correction can be implemented in digital, but for low side current sensing application calculation of the state of charge is a mandate. Coefficients are provided from the test and correction is implemented in

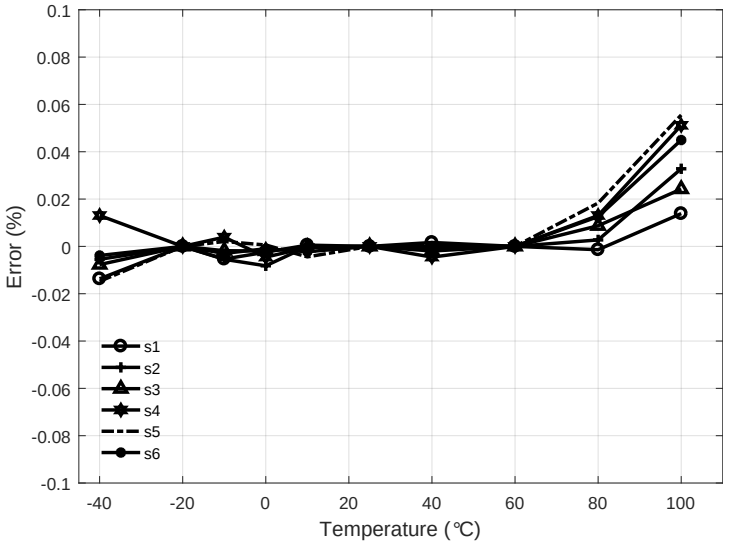

FIGURE 3.13: V_{REF} error after calibration across temperature range

microcontroller.

3.4 Conclusion

In this chapter, bandgap design for low side current sensing application has been presented. Bandgap is trimmed for temperature and magnitude while its residual curvature is corrected by a polynomial compensation factor in microcontroller. The bandgap which can drive switched capacitor loads without any additional buffers has been implemented in 0.35 μm technology. A bandgap reference voltage with a 0.06% of inaccuracy has been achieved for a temperature ranging from -40 °C to 100 °C to meet the accuracy requirement of low side current measurement of 1%.

TABLE 3.1: comparison proposed bandgap reference with published work

Parameter	This work	[34]	[35]	[38]	[39]	[40]
Technology	0.35 μm	0.35 μm	0.13 μm	0.18 μm	0.35 μm	0.6 μm
Supply Voltage	3.3 V	3.3 V	1.8 V	1.8 V	1.4 V	1.8 V-5.5 V
Active Area	0.23 mm^2	0.43 mm^2	0.03 mm^2	1.2 mm^2	-	-
Bandgap voltage	1.22V	1.22V	1.225V	1.0875V	0.858V	1.15V
Inaccuracy	0.06% (box method)	0.04% (3σ)	0.08% (box method)	0.15%[a] (3σ)	0.15%[b] (box method)	0.11%
Noise	0.3 $\frac{\mu V}{\sqrt{Hz}}$ @ 1 KHz	0.15 $\frac{\mu V}{\sqrt{Hz}}$ @ 1 KHz	-	6.3 μV_{RMS} 0.1 to 10 Hz	9.1 μV_{RMS} 0.1 to 10 Hz	53 μV_{RMS} 0.1 to 10 Hz
Temperature range (°C)	-40 to 100	-40 to 100	-40 to 125	-40 to 125	-20 to 100	-20 to 120

[a] Single temperature trim, [b] 1.28mV variation for V_{REF} of 0.858V

Chapter 4

Overview of Cell Monitoring and Balancing

4.1 Introduction

For EVs, HEVs and portable power tools which work on Li-ion based battery packs, Battery Management System (BMS) is essential. A typical BMS records key operational parameters such as individual cell voltage (V), current(I) and the internal temperature(T) of the battery pack which in turn are used to estimate the state of charge (SOC). A BMS should include battery monitoring and protection circuits, to generate alarm and consequently disconnect the battery from load or charger if any of these parameters(V,I and T) exceed the specified value. It should also keep the battery ready to deliver full power when necessary which is possible only when all the cells in a given pack have similar capacities. Hence, cell balancing is required in a BMS along with cell monitoring and measurement.

Typical requirements of cell monitoring and balancing device are [6, 8, 29].

- Safety monitoring
- Cell voltage measurement
- Balancing with option of
    - Active balancing
    - Passive balancing
- Ability to Communicate
- Minimal complexity and being economical

To fulfill the above requirements, several blocks are required as discussed in Chapter 2. This chapter focuses on existing solutions for cell monitoring and balancing and their advantages and limitations. The problems associated with regards to level shifting, balancing and communication with other ICs in a stack are highlighted and at the end, a solution is proposed and discussed. The implementation details of the proposed solution is described in the next chapter. Fig. 4.1 shows cell measurement system discussed in [8, 29] where cell voltages are level shifted and multiplexed and given to ADC to convert to equivalent digital codes. For cell balancing, driver circuits are provided to drive external FETs.

4.2 Cell Monitoring

One of the prime functions of BMS is to protect cells from over charge and deep discharge. To achieve this, cells need to be compared to predefined upper and lower limits. In addition to this, measurement of cell voltages to find the SOC of batteries is important. To achieve both monitoring and measurement, the following blocks are required

- Level shifters to get the cell voltage to ground reference

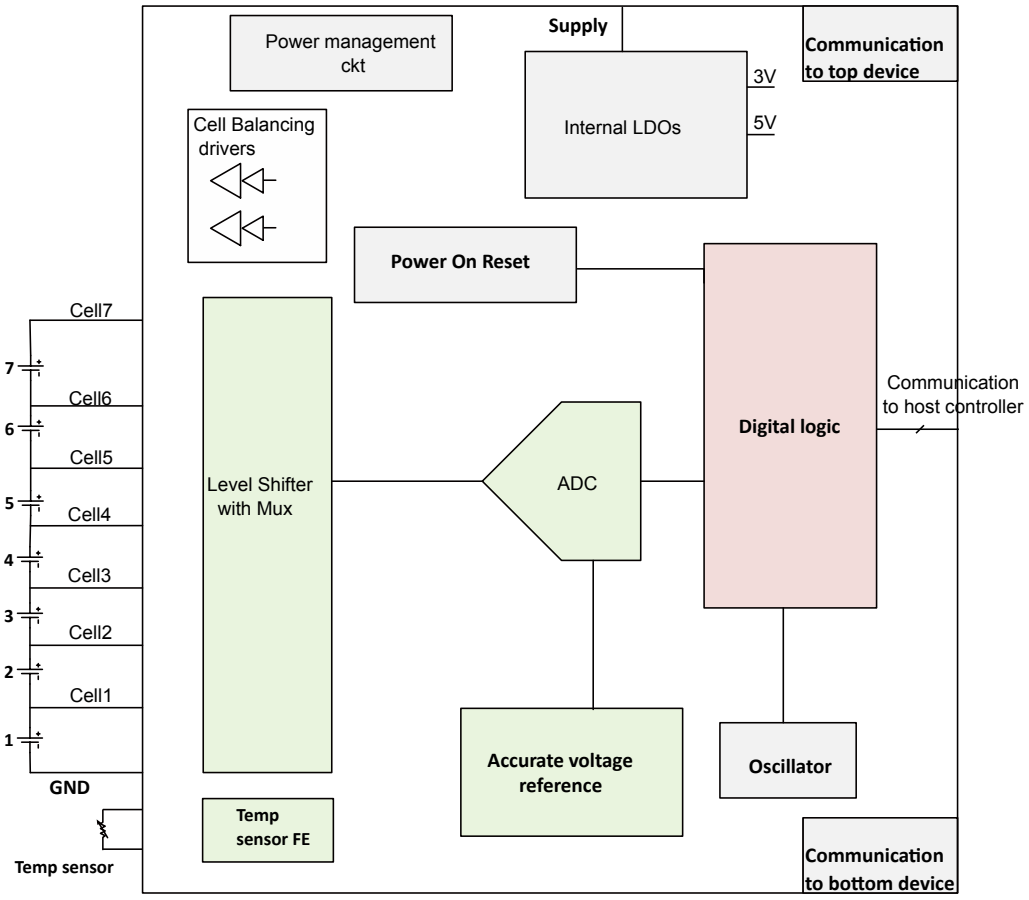

FIGURE 4.1: Typical cell monitoring and balancing device block diagram [6]

- ADC to measure the cell voltages
- Reference generation block to provide reference to ADC and to provide thresholds.

4.2.1 Level shifter

As discussed earlier, a number of Li-ion cells is stacked to get higher voltages and depending on the process technology of the manufacturers, the number of cells monitored by each IC can vary between 6 to 12. The voltages of individual cells can vary from 2 V to 4.5 V based on the Li-ion technology, charging and discharging profiles and this variation for a stack of 6 Li-ion cells lies between 12 V to 27 V. To accommodate such huge variation in the supply is difficult and hence the device is seldom operated in high voltage domain. Also, HV transistors occupy huge area compared to standard CMOS transistors because of the implementation of extended drain and

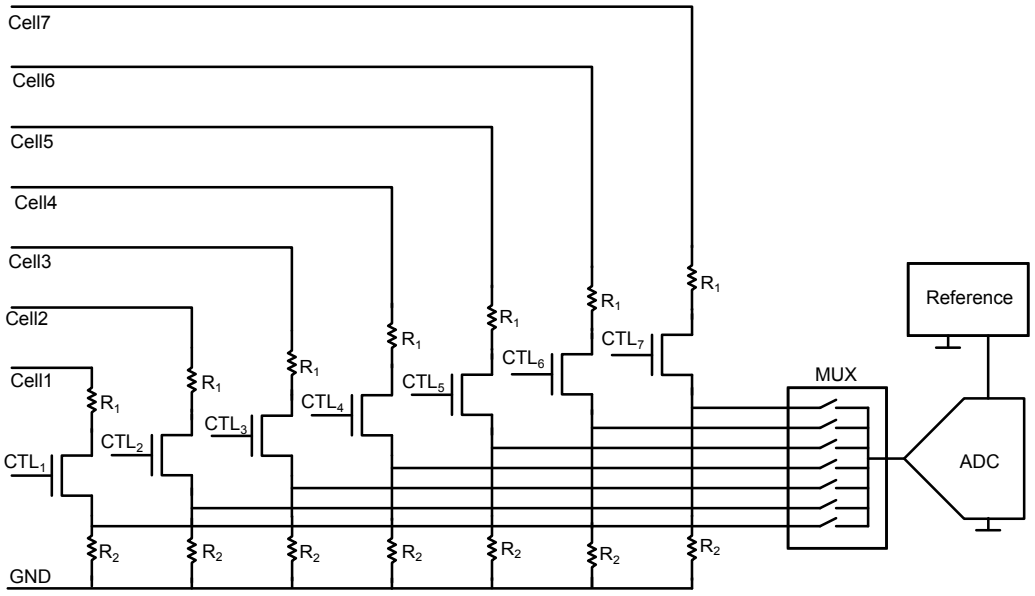

FIGURE 4.2: Resistive divider from end cell monitoring architecture

spacing requirements between wells for each transistor [41]. Hence, it is optimal to operate all the blocks in low voltage domain either at 3 V or 5 V, and level shift the cell voltages to the low voltage domain for further processing. Level shifters can be categorized in to two, namely

- Resistor based level shifters
- Switched capacitor based level shifters

4.2.1.1 Resistive level shifters

Resistor based level shifters are continuous mode architectures, in which current is drawn continuously during the measurement. A simple resistive level shifter architecture is shown in Fig. 4.2. Advantage of resistive level shifter is it is simple and easy to implement. If proper care is taken in matching all the resistors, it gives accuracies close to 0.1%. Without the control switch in the resistive path, there will be continuous power dissipation in the circuit. However, on-resistance of the switch contributes to additional errors as it varies with the process and temperature.

In this approach, two measurements are required to get the voltage of a given cell except for *Cell1*. First the voltage of the given cell is measured and next the voltage of the preceding cell is measured. The difference between these two measurements gives the voltage of a given cell. The level shifting gain ratio of the resistive divider is decided by the input dynamic range of the ADC and this ratio for each cell can be different as it has to accommodate different common modes of cell voltages based on their position in the stack. When voltages of all the cells are maximum, the ADC receives a full-scale input. However, matching gain ratios is difficult because different resistor values are used. To achieve better matching of resistive divider gain, the values of resistors R_1 and R_2 should be the same for all the cells. While using the resistive divider approach implementing same gain ratio for each cell, the ratio is decided by the maximum cell voltage and full-scale voltage of the ADC. In this approach, *Cell1* divider output is the smallest input to the ADC to be resolved. This requirement translates as the resolution of the ADC and accuracy of the reference.

Fig. 4.3 shows the level shifting implementation carried out in [6], in which level shifting is done using a transimpedance amplifier. The cell voltages are level shifted to a common mode voltage of about 2.5 V and the difference voltage is absorbed by resistor R_i. However, current is drawn continuously into the circuit in this design. The common mode voltage to the level shifting circuit can vary in a range where the upper limit is more than twice the lower limit. Hence, maintaining input common mode voltage of transimpedance amplifier at 2.5 V is difficult. As mentioned in [6], fixed resistor values have been used to get the attenuation ratio of 0.48, in which case, transimpedance amplifier should be able to accommodate the common mode change. Transimpedance amplifier biasing should be able to track common mode voltage changes which can vary from 6 V to 30 V for *cell6*. Designing level shifters which accommodate for such large input common mode voltage changes is complex and hence alternative circuit techniques that employ switched capacitors for level shifting need to be discussed.

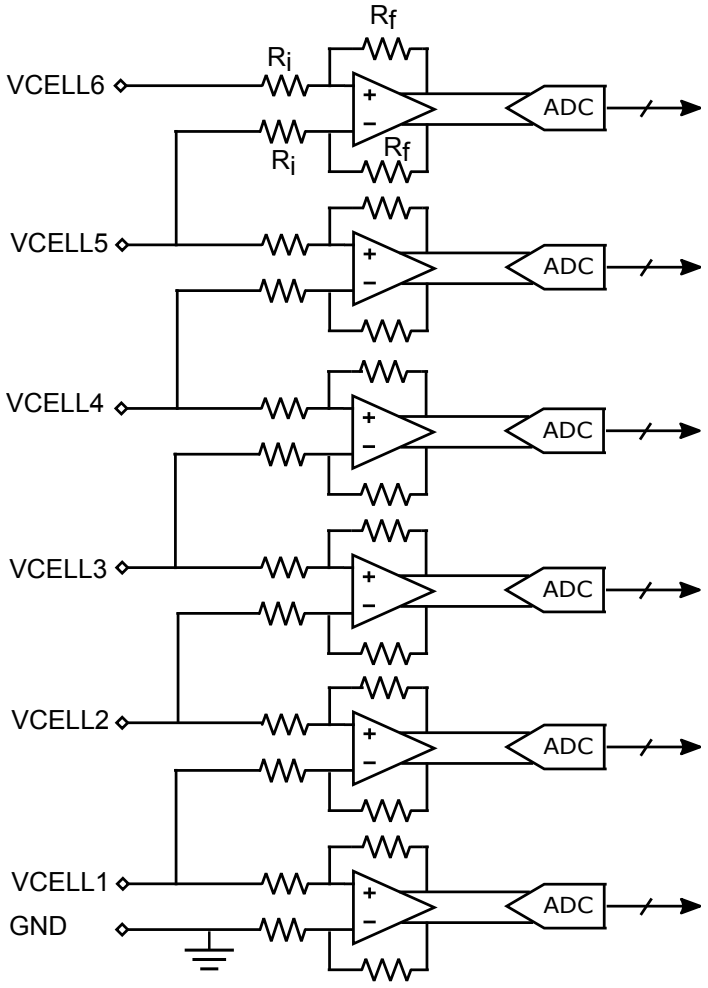

FIGURE 4.3: Level shifting using transimpedance amplifier based architecture [6]

4.2.1.2 Switched capacitor level shifters

Switched capacitor circuits use high voltage capacitors at their inputs which provide isolation to the input of the amplifier from the high common mode voltages. Compared to resistive level shifters, switched capacitor level shifters have no constant current flowing from the cells connected to the stack. The High Voltage (HV) capacitors used in these level shifters should be able to handle difference between the cell voltages and low amplifier input common mode voltages. These HV capacitors are available with foundries that provide process option to deal with high voltages. Based on the process technology, HV capacitors can handle voltages up to 50 V. Metal to metal capacitors are preferred for these kind of applications compared to well-based

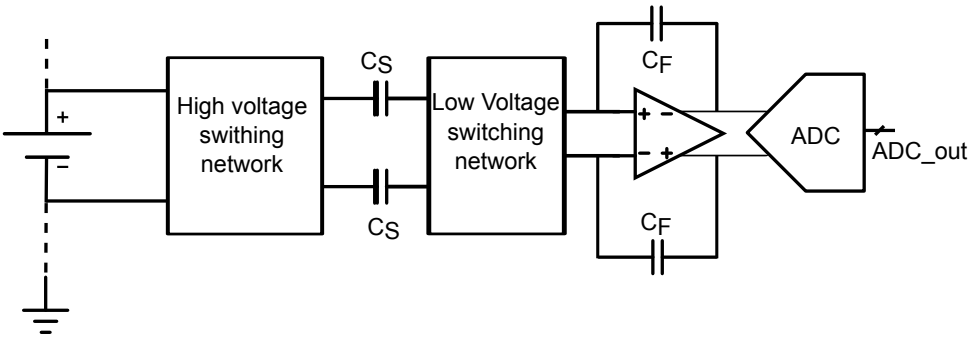

FIGURE 4.4: Capacitive level shifting using time interval technique

capacitors in which the capacitance is based on the voltage across the capacitor.

Conventional architecture of switched capacitor amplifier [42] can be used to level shift the cell voltage to ADC input common mode voltage as shown in Fig. 4.4. Selection of attenuation ratio decides the range of input voltages that the ADC has to handle. Although minimum input voltage for a Li-ion cell is 2 V, it is required in some applications to detect the presence of lower voltages. Hence, rail to rail amplifiers, as discussed in [43], are preferred to accommodate complete input common mode range. Capacitor C_S is a high voltage capacitor to accommodate the difference of cell voltage and common mode voltage. The switches connected to the cell might have to work at high voltages and this poses significant design challenges.

Fig. 4.5 shows the switched capacitor level shifter circuit proposed in [7]. This design is a part of Time Interleaved (TI) ADC and proposes a track and hold circuit to solve the problem of high voltage drop during sampling phase at the input. This design provides accurate cell voltage measurements for a limited input dynamic range of 1.2 V (3 V to 4.2 V). However, in most of the applications cell voltages that are lower than 3 V are to be measured and these voltages can go as low as 2 V. In the circuit described in [7], op-amps require high gain (>115 dB) and high bandwidth (>20 MHz) and hence consume high current.

Apart from cell voltage measurement, comparison is the other operation that is present in BMS which provides basis for cell balancing. It is often preferred to have simultaneous comparison

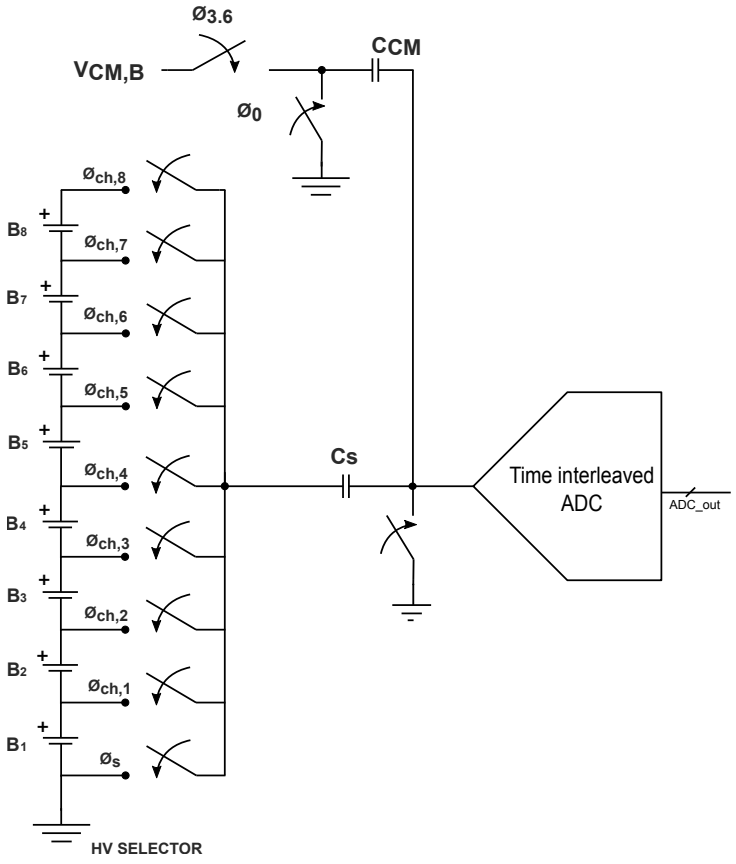

FIGURE 4.5: Switched capacitor level shifter for TI ADC [7]

to take place so that cell balancing decision can be taken based on the current state of the cell voltage. Resistive divider level shifters are simple to implement but their measurement circuits are complex. Also, simultaneous comparison along with measurement is not possible with these level shifters. Although resistive divider level shifter described in [6] supports simultaneous comparison, it requires design of complex transimpedance amplifiers. Switched capacitor based level shifters described in [7] also do not support simultaneous comparison owing to their time-interleaved nature. The conventional switched capacitor level shifter supports simultaneous comparison. However, it requires rail-to-rail amplifiers which increase the design complexity. Hence, a simple switched capacitor based level shifter which supports simultaneous comparison without any need for complex designs is required to address these issues.

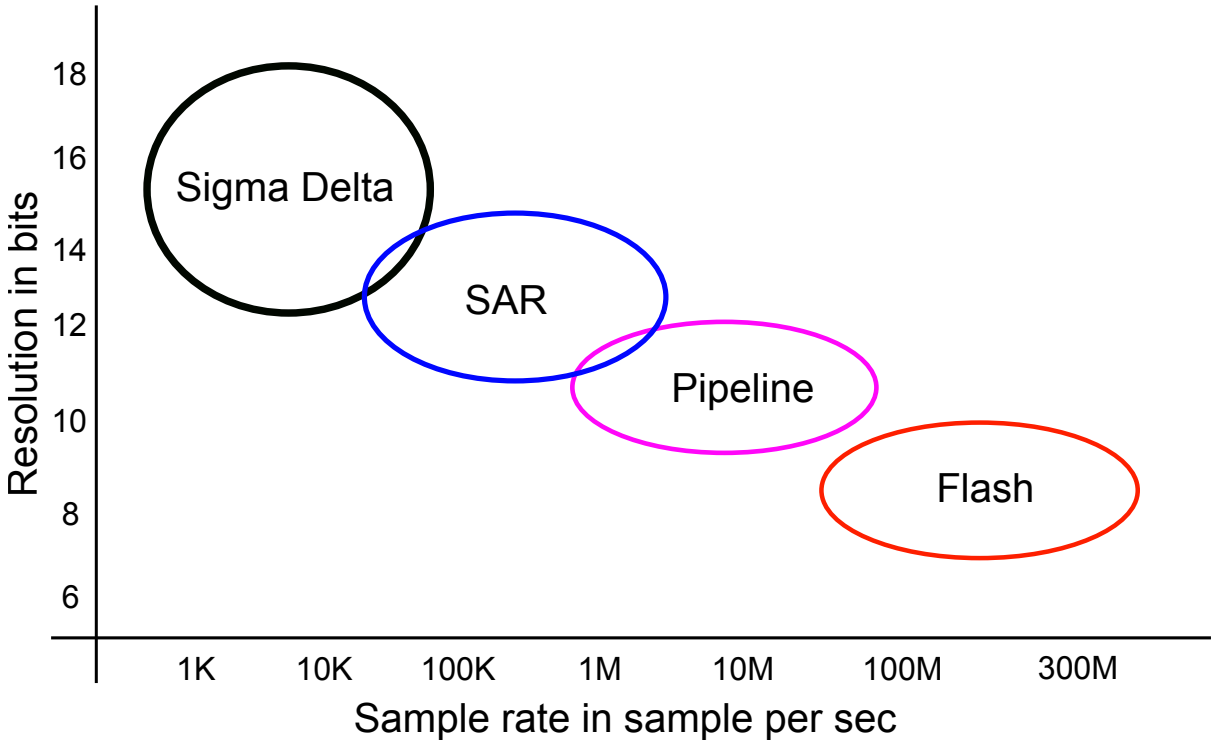

FIGURE 4.6: Comparison of ADC architectures

4.2.2 ADC

Cell voltage measurement with an accuracy of about 0.1% is essential for precise estimation of SOC of each cell. This accuracy requirement demands for an ADC of 12-bit resolution. Since the parameter being measured is a slowly varying battery voltage, the speed of the ADC of the order of few milliseconds is sufficient. Fig. 4.6 shows different ADC architectures comparing their bandwidth (speed of operation) to resolution. It is clear from this figure that the ADCs suiting our requirements are successive approximation register (SAR) and delta-sigma. Of these two ADCs, SAR ADCs have faster sampling rates and offer high-speed voltage conversion along with excellent noise immunity but they tend to occupy larger die-area. They also offer the best combination of data acquisition speed, accuracy, robustness and immunity to the effects of EMI.

Delta-sigma ADCs typically require less die area and are relatively easy to implement. However, they tend to be slower because they use a decimation filter, which reduces the sample rate and data acquisition speed. An alternative solution is to use two or more delta-sigma ADCs in an

interleaved configuration. When dealing with delta-sigma ADCs, their tendency to saturate when subjected to EMI, causes misreporting of cell voltages and has to be considered during design. To avoid these issues, SAR ADC is considered in this design.

4.2.3 Reference

To aid in accurate measurement of cell voltages, ADCs require precision reference voltage generation circuit embedded into the IC. Based on the ADC used, the reference voltage to be generated is fixed. Common practice is to generate accurate 1.2 V and amplify the same to required reference voltage and the same has been followed in [6]. Instead of amplification of 1.2 V, a reference circuit giving 2.5 V output has been presented in [36]. In this work, two BJTs are cascaded to get 2.5 V and this requires additional process steps [44].

To achieve 0.1% accuracy of cell voltage measurement, absolute accuracy of reference should be 0.05% and this poses significant challenges in the design of reference. Also, to achieve this accuracy, trimming and calibration are required.

4.3 Cell Balancing

As discussed in Chapters 1 and 2, cell balancing is an essential requirement in a series stacked battery pack. Most of the devices use external switches for balancing the cells[6],[8]. Number of external components required for the complete balancing system are usually from 24 to 59 and these components include balancing transistors, capacitors, resistors and transformer based isolators. In case of passive balancing, cells with higher voltages are discharged to the level of cell with lowest voltage such that all the cells have same voltage. In a passive balancing application shown in [8], a minimum of 5 components are required as shown in Fig. 4.7.

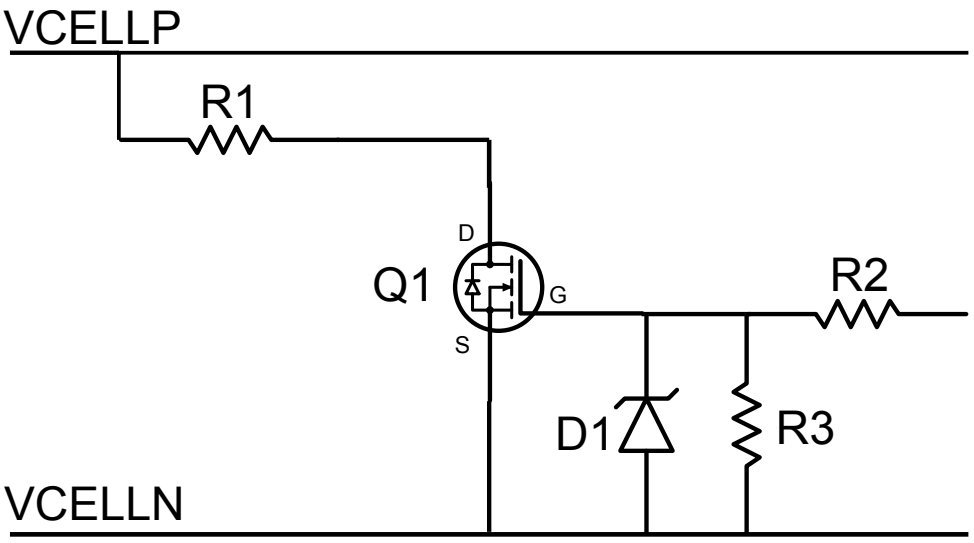

FIGURE 4.7: Cell Monitoring architecture [8]

For active balancing, cells with the lower voltage are charged to reach the level of cells with higher voltage [45].

4.3.1 Balancing current requirement

In automotive applications where charging is required after every discharge, batteries are usually fully charged after every discharge cycle. In these applications, the balancing action can be carried out while the vehicle is not being used. In smart balancing BMS algorithms, balancing is performed during the charging as well, thereby providing more time for balancing.

If high currents are used for balancing, they can stress the cells and increase the temperatures which in turn result in additional imbalance. To compensate increase of temperature, heat sinks are used. Fig. 4.8 shows an application with high current balancing and it is clear that heat sinks occupy significant area, are more complex resulting in driving up the cost of the system. This can however be overcome by switching to lower currents.

Low balancing current levels also prevent wrong balance decisions, which are often caused by unknown temperatures of cell cores. Balancing current can be calculated based on the capacity

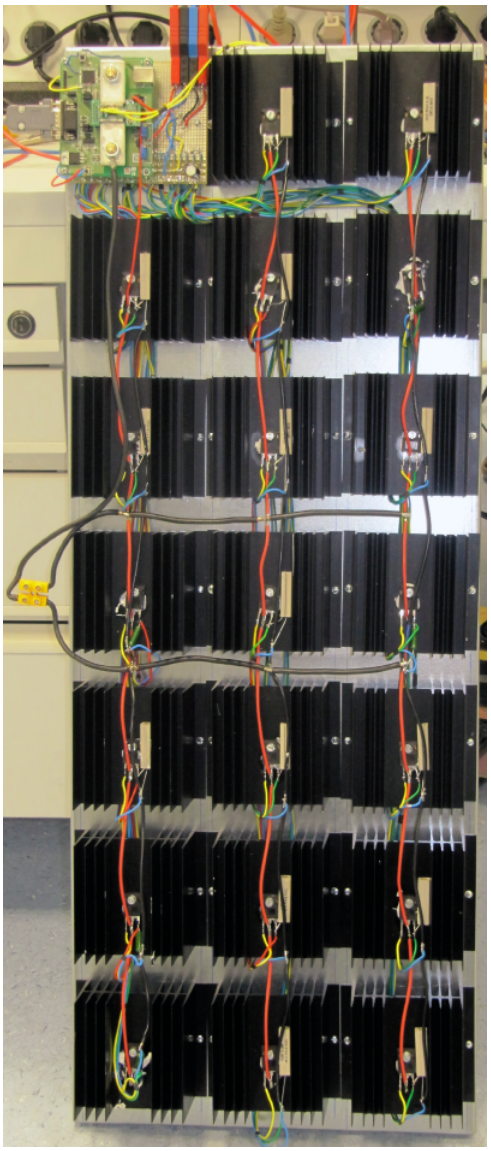

FIGURE 4.8: Balancing with high currents

of the cell and percentage of SOC to be balanced.

As discussed in Chapter 2, cells that are closely matched with respect to their capacities (within 3%) are stacked in series by closely matching their capacities. During the run time, balancing should be performed to maintain cells within this capacity so that gross mis-balance does not happen.

For gross balancing, balancing current is calculated by using the capacity over time, while maintenance balancing current is calculated using the difference in maximum and minimum

leakage currents in the stacked cells [46].

$$Balance\_current[A] = \frac{(Max\_leakage[A] - Min\_leakage[A])}{\frac{Daily\_balancing\_time[hours]}{24[hours]})} \tag{4.1}$$

Typical values of delta leakage current is around 10mA. For a total balancing time of 4 hours, the balancing current requirement is about 60mA. The increase in leakage current, if any, can be compensated by increasing the balancing time. As charging and balancing for EVs is usually preferred overnight, about 100 mA of balancing current is sufficient. It is thus possible to maintain a balanced battery stack, even with a relatively low balancing current, which is a pre-requisite for single chip integration.

4.4 Communication between series connected ICs

As discussed in Chapter 2, communication between ICs is implemented either with isolation or daisy chain. Isolated communication requires external components and result in an increased cost and hence development of daisy chain communication without isolation devices is currently in demand. Fig. 4.9 illustrates the communication between two devices using current mode level shifting without using any external components [6].

In this implementation, level shifting between the ICs has been carried out with current mode translation. During communication from top IC to bottom IC, communication signal V_{IN} is applied to transistor M_1 in top device supply domain. The current I_{TX} of 400 μA is mirrored to bottom device diode connected transistor, which is compared against I_{REF} to generate V_{OUT}. Similar concept is used for communication between bottom IC to top IC, in which transistor M_2 level shifts the signal. In this case, the drain of M_2 sees more than twice the specified supply

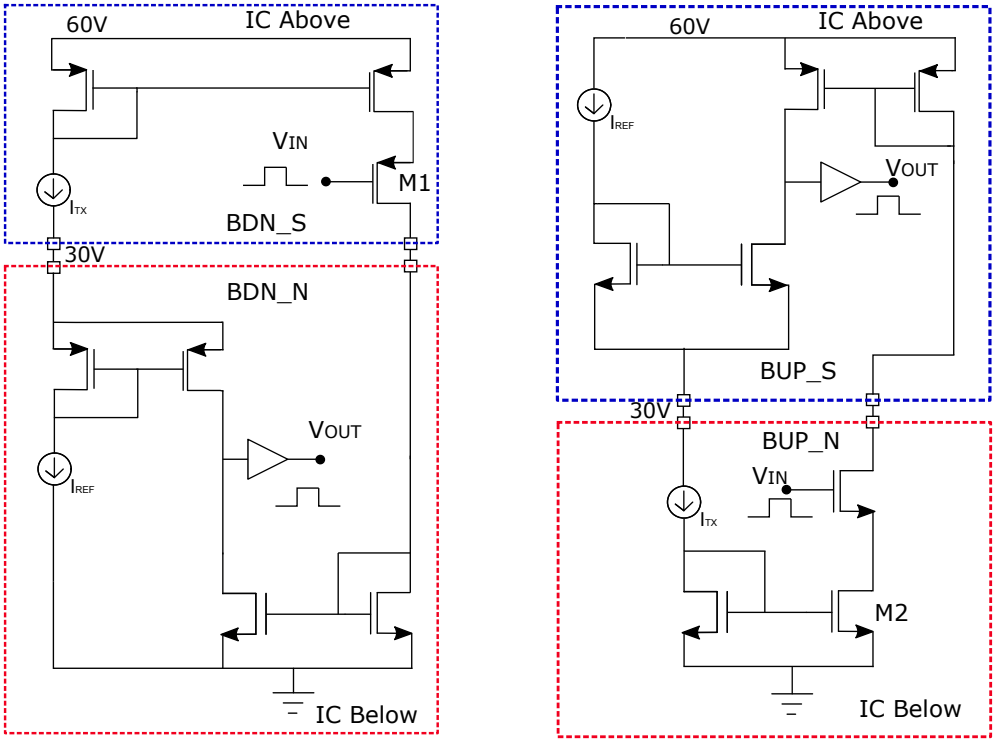

FIGURE 4.9: Device to device communication using current mode level shifting [6]

rating of the IC and might lead the device out of safe operating region. As this is current mode level shifting, communication is preformed asynchronously, which imposes a requirement for special communication protocol. Hence, there is a need for simple and robust level translators to reduce the complexity and cost of BMS systems.

4.5 Proposed cell monitoring and balancing architecture

Increased demand for EVs and battery operated devices creates necessity for Li-ion series connected battery packs. BMS is essential for these battery packs as discussed in the previous chapters and the previous sections of this chapter show that available solutions are complex and expensive. Hence, less complex, robust cell monitoring and balancing system is required. To meet these requirements, it is proposed to integrate balancing switches within the IC to reduce complexity and cost significantly.To reduce the number of external components for balancing

and number of pins in the device, balancing switches are multiplexed to two pins. To reduce the communication speed, simultaneous comparison is introduced in which cell voltage comparison, to identify cells that require balancing, takes place at the same time for all the cells in a given IC. This eliminates the need to measure cell voltages every single balancing cycle, thereby avoiding the requirement for high speed communication between IC and host microcontroller. Measurement is however required to estimate SOC and calculate the reference for balancing. Synchronous communication can be implemented between the stacked devices if the data transfer is done in voltage domain. It is decided to supply a portion of the IC with regulated output from the top device. Because of this, level shifting of the signals from low voltage domain is implemented in current mode and data between stacked devices is transferred in voltage mode. To accommodate both active and passive balancing, an intelligent digital algorithm has also been developed. This algorithm facilitates the use of a single IC which can work standalone without a host microcontroller.

To realize the proposed architecture, a systematic approach has been followed and initially a system model is implemented in VerilogA as a proof of concept. Active and passive balancing approaches have been verified on top level model. Block level model has been carried out to identify required blocks for the system. After analyzing the results and with a few iterations individual block architectures and specifications are drawn. The VerilogA model is detailed in Appendix A.

4.6 Conclusion

In this chapter requirements for cell monitor and balancing methods are discussed. Need for level shifters for cell monitoring is highlighted and available level shifting methods are described focusing on advantages and disadvantages of each method. Requirements of ADC and accuracy

of reference voltage are discussed. Two ADCs, namely Sigma Delta and SAR ADC are found to be equally suitable for this applications, however, SAR ADC is found to be better choice for the reasons discussed. Analysis has been made to find how much balancing current is required for automotive applications, from which its concluded that 100 mA is sufficient, which enables integration of balancing switches. Existing solutions for communication between the stacked devices are also discussed. Issues associated with level shifting, balancing components and communication between the stacked devices are identified and means of addressing them are discussed.

Chapter 5

Implementation of Cell Monitoring and Balancing

5.1 Introduction

For BMS applications, cell monitoring and balancing is essential. In this work we propose, test and validate a flexible and economical cell monitoring and balancing system. As discussed in Chapters 2 and 4, most of the existing solutions require external components for IC to IC communication and external FETs for balancing, which make these systems complex to design and expensive.

5.2 Proposed architecture

In the proposed architecture, balancing switches are implemented internally and no external components are required for communication between the cells. Communication is implemented with simple daisy chain wired communication between the ICs. External components required

for each device can be as minimum as three for a passive balancing application. Communication between the bottom IC and microcontroller is implemented with a Serial Peripheral Interface (SPI) bus protocol. Each device can be connected up to 7 cells, which is optimal for 24 V battery application. By connecting two ICs in series, 48 V can be achieved, suitable for mild HEV [14]. The proposed stacked cell balancing system with two ICs is shown in Fig. 5.1.

As can be seen from the figure, cell voltages are measured using measurement circuit and are communicated to microcontroller connected to the bottom IC. The reference voltage is calculated by microcontroller based on whether the application requires active or passive balancing. This value is then communicated to all the ICs connected in the stack.

When the balancing process is initiated from microcontroller, the IC first compares cell voltages with predefined lower and upper thresholds, to ensure the safety of system. After safety check, comparison of all the cells with respect to the reference voltage is performed simultaneously to find the cells that need to be balanced. Simultaneous comparison of all the cell voltages gives considerable flexibility in balancing. Balancing is usually carried out in quiet conditions i.e, with open circuit voltage (OCV) [4]. With simultaneous comparison, cells to be balanced have same loading conditions as they come across the same load. Theoretically, balancing with low currents and simultaneous comparison should not imbalance the cells even with loading conditions. To compare the cells simultaneously across the devices, a synchronization mechanism is used. Clock from the bottom most device is transmitted to the top devices. During power up, devices work on their individual oscillators. However, after the power up time interval, all the devices synchronize to the clock from the bottom-most device and start working on this clock. This ensures that the maximum delay in comparison from bottom device to the top device is within one clock cycle.

In case of passive balancing, based on the decision of comparators, an external dissipating resistor

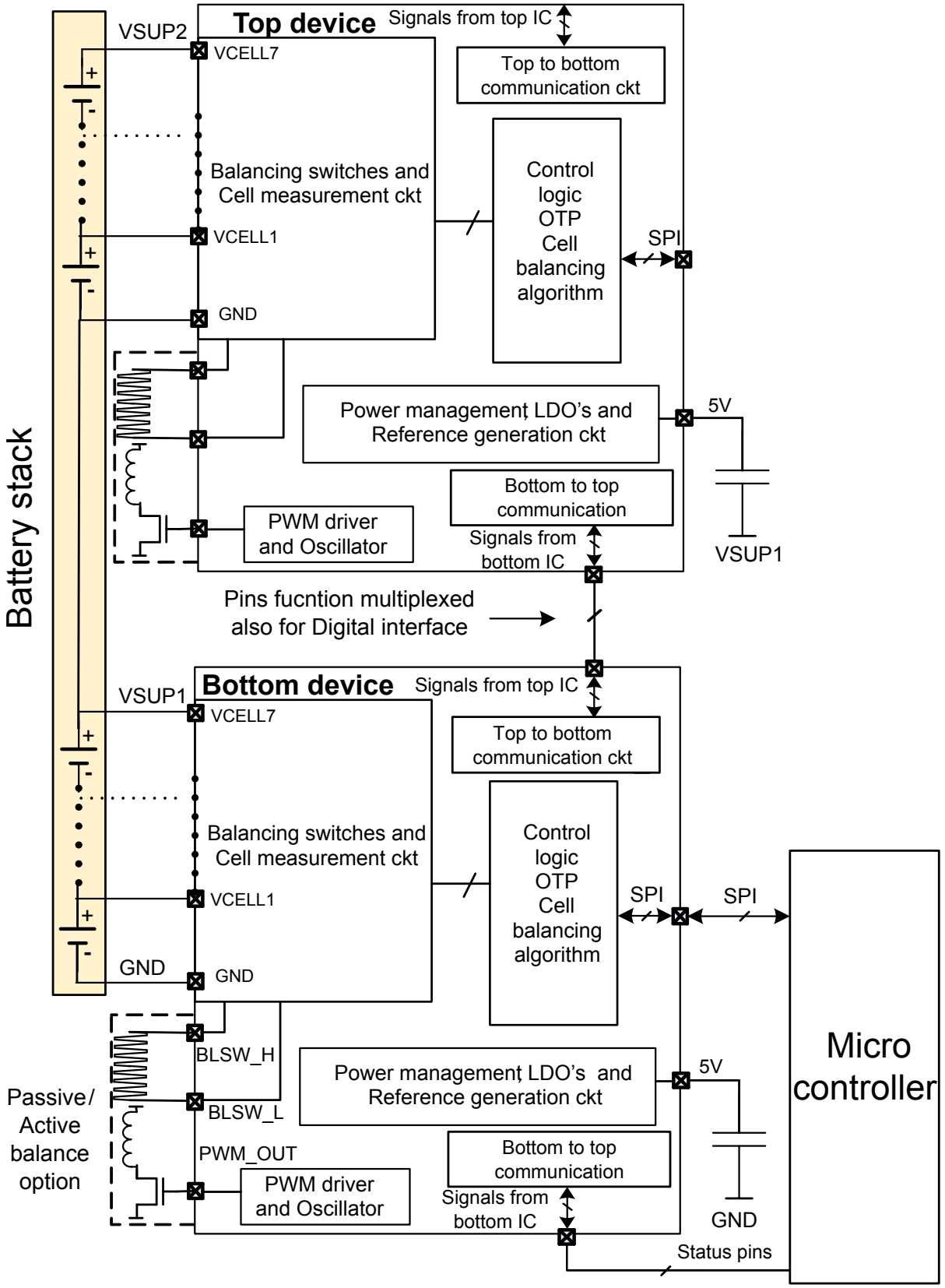

FIGURE 5.1: Stacked cell monitoring and balancing system

is connected across the balancing switches such that cells with higher voltages get discharged. All the cells with higher voltage than the reference voltage are discharged until they reach the reference voltage. In case of active balancing, cells with less voltage than reference voltage need to be charged to reach the reference voltage. This charging is facilitated by a flyback transformer with its secondary coil connected between the switching network and the primary coil connected between pulse width modulated (PWM) driver and either the battery stack or an auxiliary supply voltage. Details of the IC implementation are provided in the section below.

5.3 IC IMPLEMENTATION

The designs are implemented in a high voltage triple well CMOS process with gate extended MOS devices that can handle a maximum voltage of 50 V. Complete Block diagram of the IC is shown in Fig. 5.2. It consists of level shifters, comparators, mux logic, SAR logic to facilitate comparison and cell voltage measurement and monitoring. For each cell, an individual level shifter and a comparator are used to compare with reference and this comparison is carried out simultaneously. Reference voltage for comparison is generated by using a 12-bit resistive DAC, which has a reference generation block that generates accurate reference voltage from a precision bandgap.

To measure cell voltages, a 12-bit SAR ADC is implemented and the measured data is used to calculate the reference voltage by microcontroller which is sent to ICs in the stack as explained in previous section. Once a reference voltage is sent by the microcontroller, the IC takes a decision regarding the cells to be balanced locally. This local decision making ability is made possible by the presence of reference generation circuit and comparators in the IC. Such decision making presence also eliminates the need for the IC to constantly communicate with microcontroller to fetch a decision, thereby significantly reducing the volume of data communicated between the

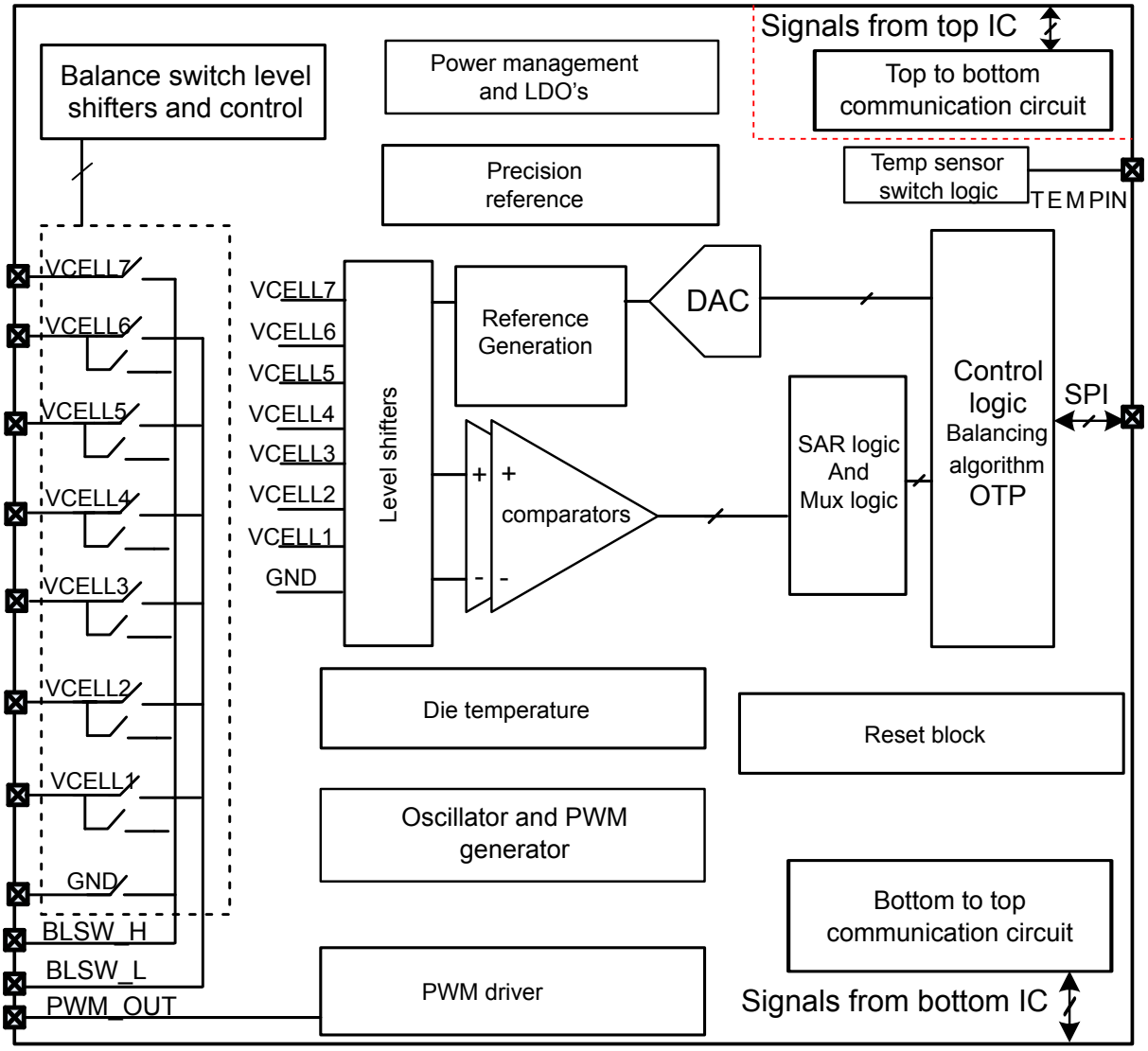

FIGURE 5.2: Block diagram of the design

IC and microcontroller. ADC data is transferred to microcontroller once in a while based on the algorithm to calculate a new reference value.

One of the prime differences of the proposed architecture with the existing solutions is the incorporation of balancing switches within the IC, however, at the cost of significant area consumption. To control these switches, level shifters are required because decision making control signals come from the digital block working on a lower voltage. As discussed, ICs can be stacked to monitor multiple series-connected cells. A custom cyclic redundant bidirectional voltage mode circuit has been implemented to communicate between ICs, while level shifting

within the IC is implemented by current mode design. With this implementation, requirement of high voltage transistor between ICs can be circumvented, leading to a lower level-shifting current [6].

The IC has an oscillator which provides functional clock and PWM generator circuit to drive PWM gate driver in case of active balancing. Digital logic comprises of serial peripheral interface (SPI) and a finite state machine to control the device operation and trim logic. Power management block consists of internal regulator (3 V) and high voltage regulator (5 V). While the measurement circuit works on 5 V domain, digital block works on 3 V. The IC also includes other functional circuits such as power on reset, internal temperature monitor block and bias generation circuit.

The designs are implemented in a high voltage triple well CMOS process with a gate extended MOS devices which can handle maximum voltage of 50 V. Individual functions of the IC are discussed in the following sections.

5.3.1 Balancing switches

For balancing the cells, balancing switches are incorporated within the IC. Fig. 5.3 shows the implementation of these switches. These switches have to be designed such that they have low on-resistance while providing isolation between the cells. On-resistance of the balancing switches plays a major role in selection of external resistor and power dissipation within the device. Balancing switches are multiplexed to reduce the number of pins and external components which poses the requirement of isolation between the cells. As the IC is implemented in triple well isolated HV process, parasitics diodes in this process help in providing the isolation. Fig. 5.4 shows the cross sectional view of HV NMOS transistor [9] and it can be seen that drain is extended from the gate compared to source. This transistor can support drain to source and

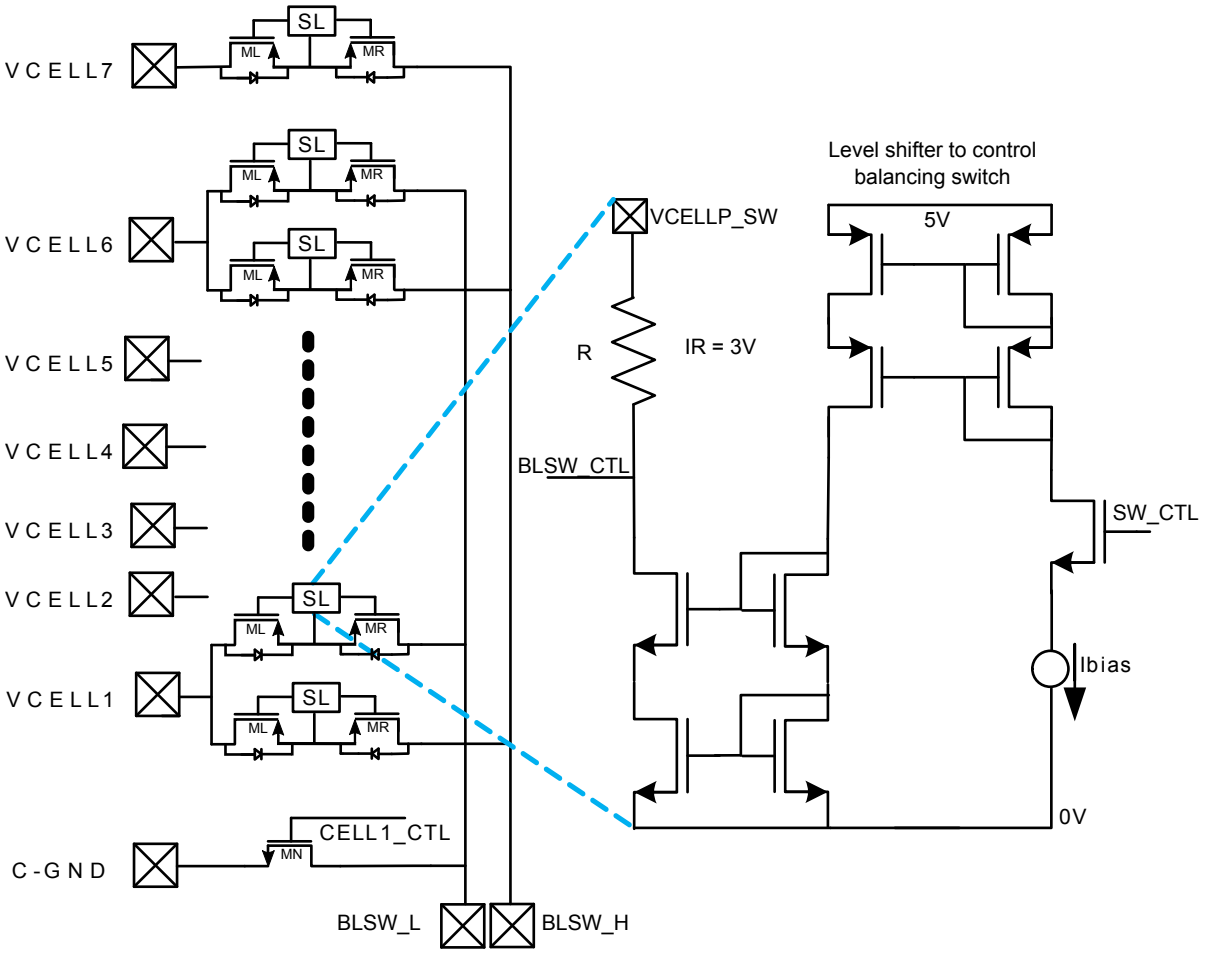

FIGURE 5.3: Schematic of Balancing switches and level shifter

drain to gate voltages up to 50 V, where as gate to source voltage (V_{gs}) is based on the oxide thickness. In this design V_{gs} of 3 V is used. For a HV PMOS transistor, the wells and diffusions are the complements of a HV NMOS transistor.

Each switch is implemented with two high voltage PMOS (50 V) transistors connected back to back to provide isolation between the cells. When balancing device is in ideal state, drain to source parasitic diode of high voltage transistor MR will be reverse biased and provides isolation between the cells. Gate control for these switches is implemented with a level shifter which generates an IR drop across the resistor as shown in Fig. 5.5.

VCELLP_SW node of level shifter is connected between both the source terminals of the balancing switch. Resistor value and current are chosen such that typical value of gate to source voltage is

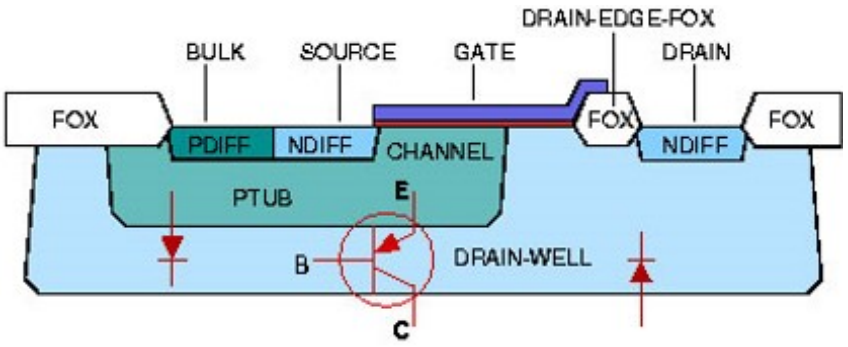

FIGURE 5.4: Cross sectional view of HV NMOSFET [9]

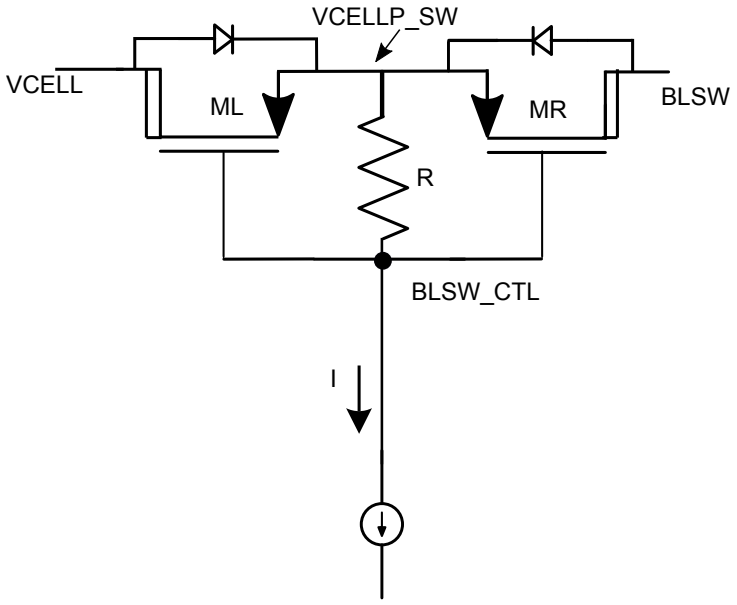

FIGURE 5.5: Schematic of Balancing switches and level shifter

set at 3 V. A trimmed current is given to the level shifter to endure any process variations. The design of switch is optimized for on-resistance and area. Typical on-resistance of each transistor is 4 Ω and for the complete switch it is 8 Ω. In the layout, care has been taken in metal routing to handle 100 mA current. Bottom-most switch to the ground is implemented with an NMOS transistor while the proposed balancing switches are used for passive and active balancing. In case of passive balancing, current is discharged from the selected cell to the external resistor connected between balancing pins. In case of active balancing, particular cell to be charged from the external flyback transformer is connected between balancing pins. Parasitic diodes provide isolation, while charging the cells with lower voltage since cells with higher voltage should not

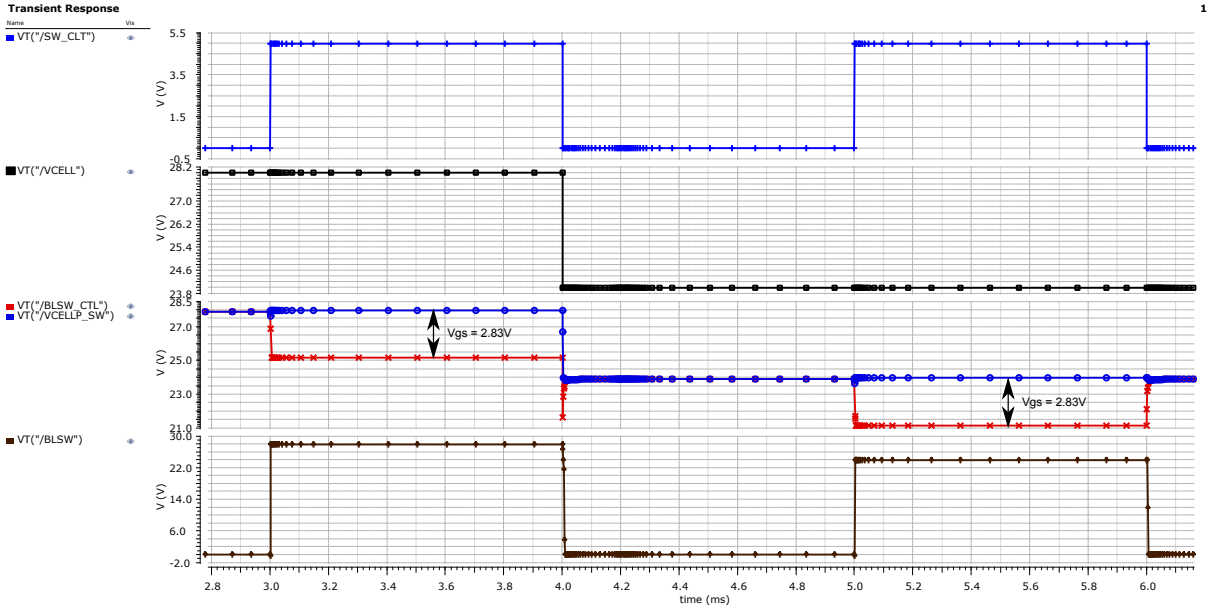

FIGURE 5.6: Simulation result of balancing switch

discharge.

Simulation results of balancing switch described in Fig. 5.3 are illustrated in Fig. 5.6. This figure depicts the output of balancing switch ($BLSW$) successfully tracking the cell voltage ($VCELL$) when the control signal (SW_CTL) is high. The figure also shows the voltage developed across the resistor (the gate to source voltage (V_{GS}) of the balancing transistors ML and MR) to be around 2.8V.

Simulation results of balancing using the proposed balancing switches are illustrated in Fig. 5.7. It is assumed for this simulation that there are seven cells connected in series with each cell having a voltage of 4V and hence a stack voltage of 28V. The control signal $SW\_CTL < N >$ selects N^{th} cell and its voltage has to be acquired by the balancing switch in order to start balancing. From the simulation it is evident that the difference of voltages $BLSW\_H$ and $BLSW\_L$ acquires the voltage of the cell as selected by the control signal $SW_CTL < N >$.

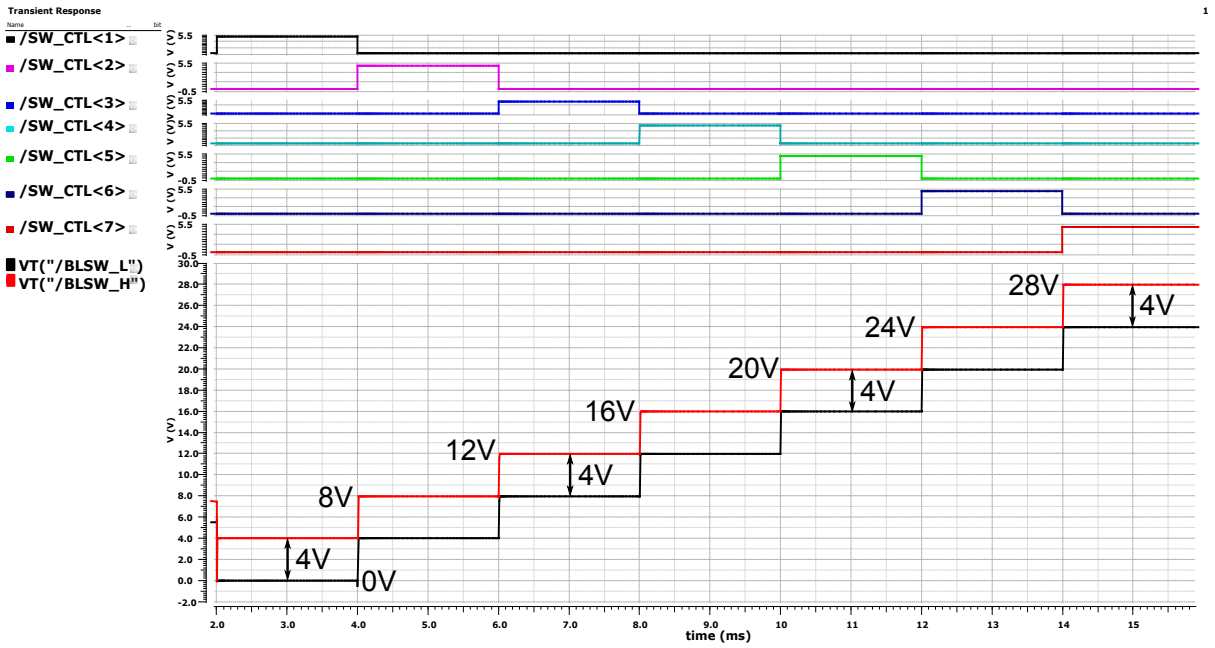

FIGURE 5.7: Simulation results of voltage across balance switches during balancing

5.3.2 Cell voltage level shifter

Since the design can support 7 series connected cells, based on position of the cell in the stack, it can have different common-mode voltages with respect to the ground. To compare these cell voltages with the reference voltage set by 12-bit DAC which works on 5 V domain, level shifters are required. Switched capacitor level shifters are designed to handle the difference between cell voltages and 5 V voltage domain [47]. Fig. 5.8 illustrates the schematic of level shifter circuit. High voltage capacitors which can handle upto 50V are used to support high common mode voltage at the input of cells.

This switched capacitor circuit consists of four sampling capacitors CS1-CS4 and contains several switches to sample cell voltage and reference voltage on to these capacitors. To sample these voltages, system clock is level shifted to the cell voltage domain and non-overlapping clocks are also generated in the same domain. To sample reference voltage, all the clocks are generated in 5 V domain. Circuit operates in two non-overlapping phases where in one phase voltages are sampled while difference generation takes place in another phase as described below:

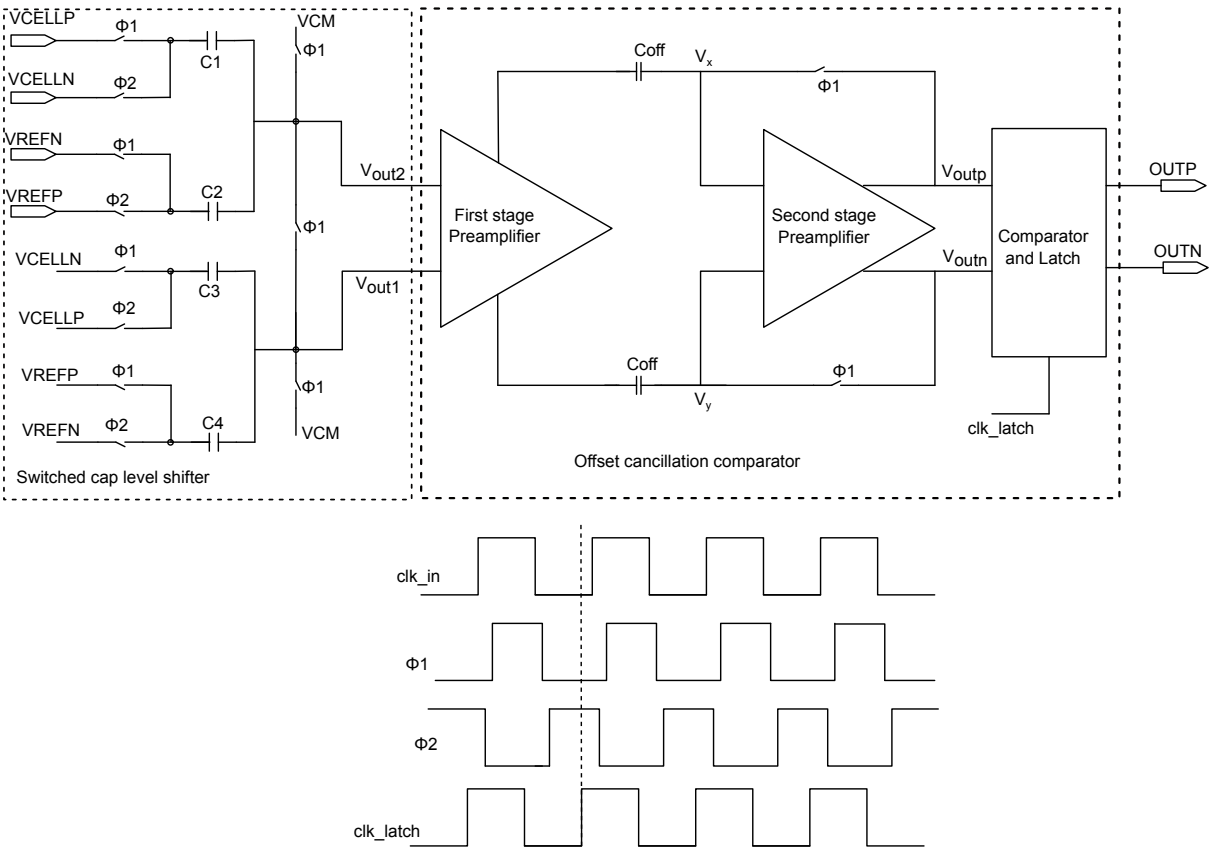

FIGURE 5.8: Schematic of the cell voltage level shifter circuit and non-overlapping clocks

In Phase1 (Φ1) (sampling phase), VCELLP is sampled on to C1, VREFN is sampled on to C2, VCELLN is sampled on to C3 and VREFP is sampled on to C4. Common mode (VCM) voltage of 2.5 V is connected to the other terminal of the capacitors in Phase1. Capacitors absorb the difference between the cell voltage and common mode voltage. In Phase2 (Φ2) where comparator decision is latched, all the sampling capacitors are connected to a different set of voltages with their other sides left floating. With the charge conservation, V_{out1} and V_{out2} can be written as equations (5.1), (5.2) respectively, with an assumption that all the sampling capacitors are of the same value and equal to C_s. C_p is the parasitic capacitor at the input of the comparator.

$$V_{out1} = \frac{-Cs}{2Cs + Cp}\Big((VCELLP - VCELLN) - (VREFP - VREFN)\Big) \tag{5.1}$$

$$V_{out2} = \frac{Cs}{2Cs + Cp}\Big((VCELLP - VCELLN) - (VREFP - VREFN)\Big) \tag{5.2}$$

For the switched capacitor circuit to operate with non-overlapping clocks, clock is level shifted to the cell voltage domain. Difference of cell voltage and reference voltage is level shifted on to a common mode voltage of 2.5 V. Differential output can be written as given below (5.3)

$$V_{out2} - V_{out1} = (VCELLP - VCELLN) - (VREFP - VREFN) \tag{5.3}$$

where V_{out2} and V_{out1} are outputs of switched capacitor level shifter circuit. VCELLP and VCELLN are positive and negative terminal voltages of a cell and VREFP and VREFN are reference voltages. If the difference of the cell voltage (VCELLP - VCELLN) is greater than the reference voltage (VREFP - VREFN) then comparator output becomes high else it is low. Comparator is implemented with a series connected input and output offset cancellation circuit [48].

Consider $Q_{P\phi1}$ and $Q_{N\phi1}$ as the charges associated with capacitor C_{off} for positive and negative inputs respectively of Phase1 ($\phi1$). Similarly $Q_{P\phi2}$ and $Q_{N\phi2}$ are charges associated with C_{off} for positive and negative inputs respectively of Phase2 ($\phi2$). Node V_x is the positive input of the second stage and node V_y is the negative input.

Charges across the capacitor C_{off} in Phase1 ($\phi1$) and Phase2 ($\phi2$) are given below

$$Q_{P\phi1} = C_{off} * \Big((V_{cm} + \frac{A_1 * V_{os1}}{2}) - \frac{V_{os2}}{2}\Big) \tag{5.4}$$

$$Q_{N\phi1} = C_{off} * \Big((V_{cm} - \frac{A_1 * V_{os1}}{2}) + \frac{V_{os2}}{2}\Big) \tag{5.5}$$

$$Q_{P\phi 2} = C_{off} * \left((V_{cm} + A_1 * V_{out2} + \frac{A_1 * V_{os1}}{2}) - V_{os2} \right) \tag{5.6}$$

$$Q_{N\phi 2} = C_{off} * \left(V_{cm} - A_1 * V_{out1} + \frac{A_1 * V_{os1}}{2} \right) \tag{5.7}$$

By applying conservation of charge principle at node V_x, $Q_{P\phi 1} = Q_{P\phi 2}$

$$V_x = A_1 * V_{out1} - \frac{V_{os2}}{2} \tag{5.8}$$

Similarly, by applying conservation of charge principle at node V_y, $Q_{N\phi 1} = Q_{N\phi 2}$

$$V_y = -\frac{V_{os2}}{2} - A_1 * V_{out2} \tag{5.9}$$

Output of the comparator can be written as

$$V_{outp} - V_{outn} = (V_y - V_x) * A_2 \tag{5.10}$$

$$V_{outp} - V_{outn} = (V_{out2} - V_{out1}) * A_1 * A_2 \tag{5.11}$$

By observing the above equations, it is evident that comparator offset is canceled. Pre-amplifiers designed are with diode connected load transistors with a gain below 10. The simulation confirms this by achieving an offset of less than 250 μV.

Fig. 5.9 shows simulation results of the switched capacitor level shifter described in Fig. 5.8. A seventh cell with a voltage of 4V which is operating between 28V and 24V and a reference voltage with $VREFP$ of 4V ($\pm$ 5mV) is assumed for this simulation. When the $VREFP$ is 4.005V, the V_{out2} output of the switched-capacitor level-shifter is lower than the value of V_{out1}.

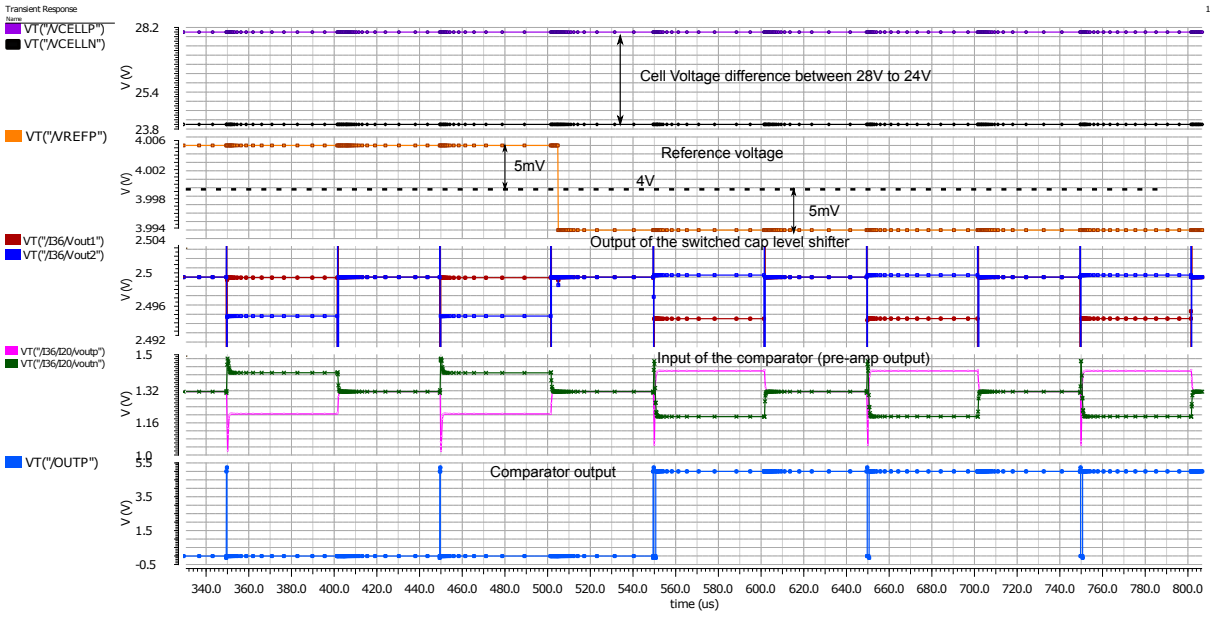

FIGURE 5.9: Simulation results of switched capacitor level shifter

The converse happens when $VREFP$ is 3.995V. Depending on the polarity of the difference of voltages V_{out2} and V_{out1}, the comparator output is either high or low following the equation (5.3).

Sampling switches in the switched capacitor circuit are complementary CMOS switches with dummy switches to avoid charge injunction on the sampling capacitors. These switches are sized to have low on resistance such that sufficient settling time is available for switched capacitor circuit sampling. To sample the cell voltages, clock has to be level shifted to the cell voltage domain and to sample reference voltage, it has to work on 5 V domain. Schematic of the clock level shifter is shown in Fig. 5.10, in which the sampling clock (CLK_IN) and its complement are given as inputs to the differential stage with a diode connected load. Based on the clock polarity, $MP2$ is either switched on or off. When $MP2$ is switched on (when $CLKB$ is low), current is mirrored from $MN2$ to $MN3$ which develops a voltage drop across the resistor R connected between $VCELLP < N >$ and drain of $MN3$, where $VCELLP < N >$ denotes the positive terminal of the N^{th} cell. Voltage across the resistor is connected to an inverter chain operating on voltages $VCELLP < N >$ and $VCELLN < N >$ as V_{DD} and V_{SS} respectively.

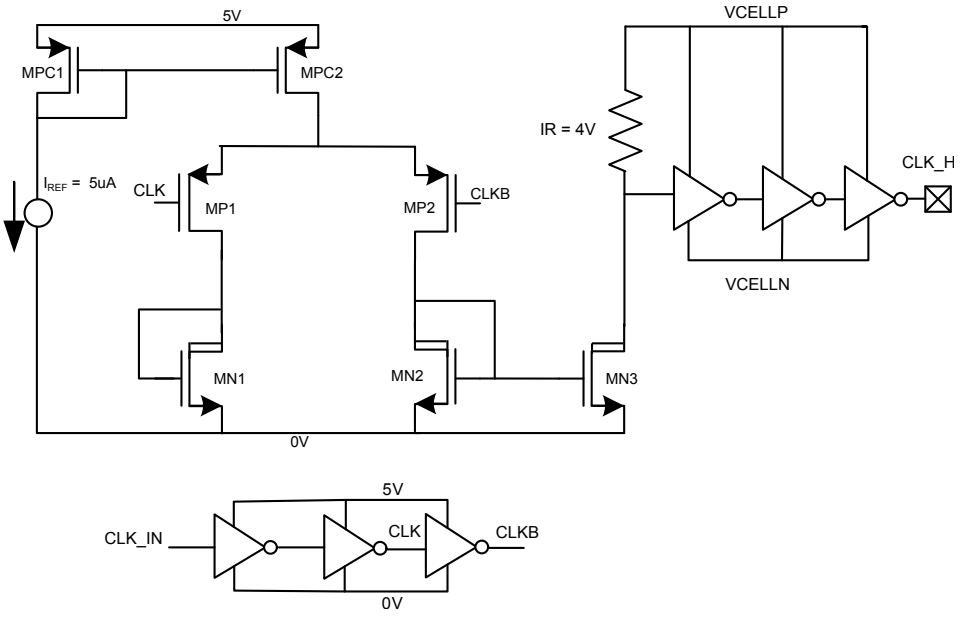

FIGURE 5.10: Schematic of the clock level shifter circuit

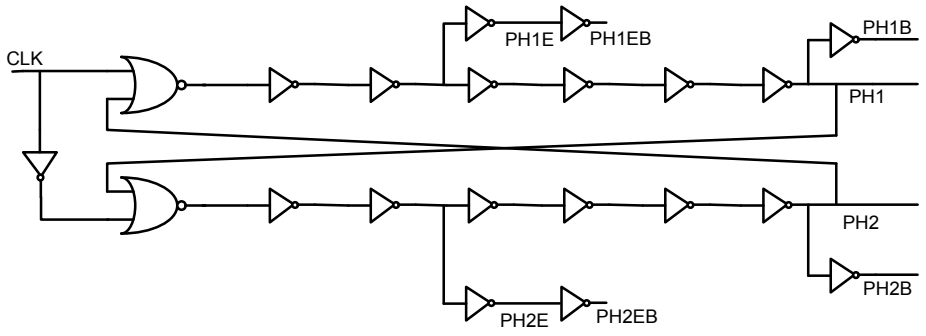

FIGURE 5.11: Schematic of the non-overlapping clock generation circuit

The circuit that generates non-overlapping clocks ($\phi 1$ and $\phi 2$) is shown in Fig. 5.11. Non-overlapping clocks are generated in the level shifted voltage domain to avoid signal dependent offsets. Care is taken during the design to match the delays of the cell voltage non-overlapping clocks and reference voltage sampling non-overlapping clocks.

Simulation result depicting the generation of non-overlapping clocks in reference voltage domain and level-shifted domain is shown in Fig. 5.12. From this figure it is clear that the sampling clock CLK_IN in 5V domain has successfully been level-shifted to voltage domain of cell7 (28V) $CLK1V_{in}$. Non-overlapping counterpart of $CLK1V_{in}$ is also generated in the same voltage

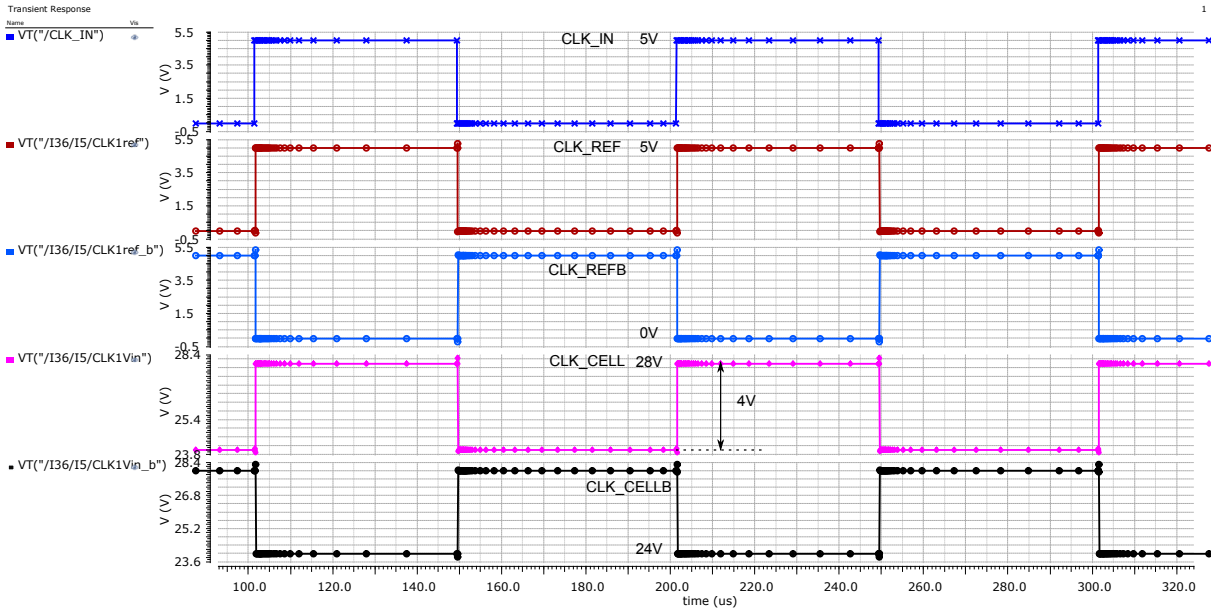

FIGURE 5.12: Simulation results of non-overlap clock generation for switched cap level shifter

domain as $CLK1V_{in}\_b$. Similarly, the clocks to sample the reference voltage ($CLK1ref$ and $CLK1ref\_b$) have been generated from the sampling clock in the 5V domain. For each cell, a separate level shifter is designed for simultaneous comparison.

Fig.5.13 illustrates the schematic implementation of simultaneous comparison.

Reference for the comparators is provided by a 12-bit resistive DAC within the device. Reference voltage to the DAC is generated internally using a precision reference source. Typical accuracy of the precision reference is ±2mV. Comparators compare against the reference and provide the decision based on whether the cell voltage is lower than the reference or higher than the reference.

5.3.3 Analog to Digital converter (ADC)

As explained in the previous sections of this chapter, individual cell voltages need to be measured to be processed by host microcontroller. This is achieved by a 12-bit SAR ADC in this design. Implementation of SAR ADC reuses the level shifter, comparator logic and 12-bit resistive DAC

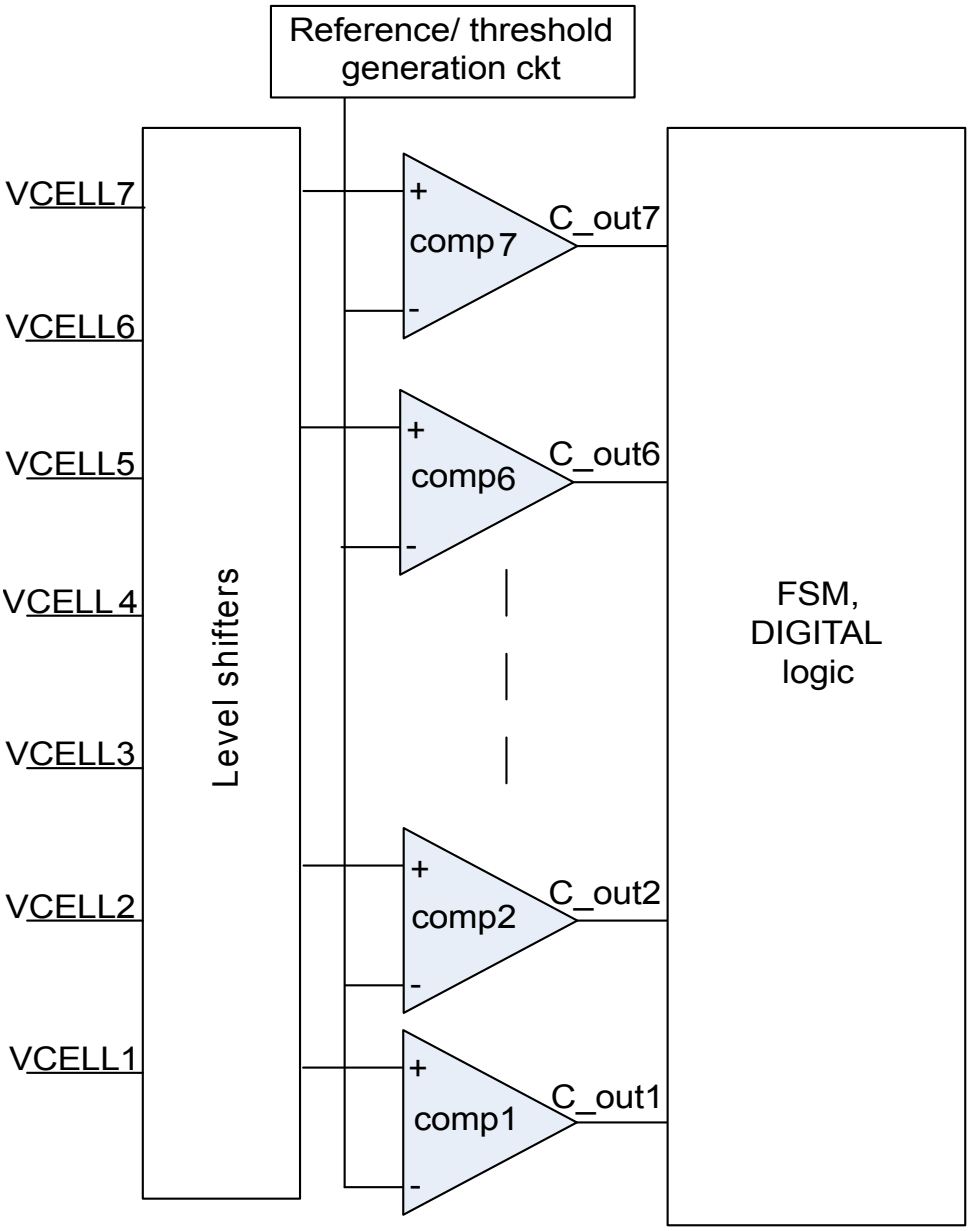

FIGURE 5.13: Schematic of simultaneous comparison

which generates reference voltage for comparators. Because of this reuse, no extra hardware is required in implementing the ADC. Fig. 5.14 shows the implementation of SAR ADC. Comparator outputs are multiplexed for the SAR logic. Cell voltages are measured sequentially from $CELL1$ to $CELL7$. Cell temperature plays a significant role in the SOC of the Li-ion cells and hence two pins are provided to measure the external temperature. These two external temperature sensors are multiplexed and share the same DAC and SAR logic of cell measurement ADC. After the cell voltage measurement, external temperature is measured in a sequential

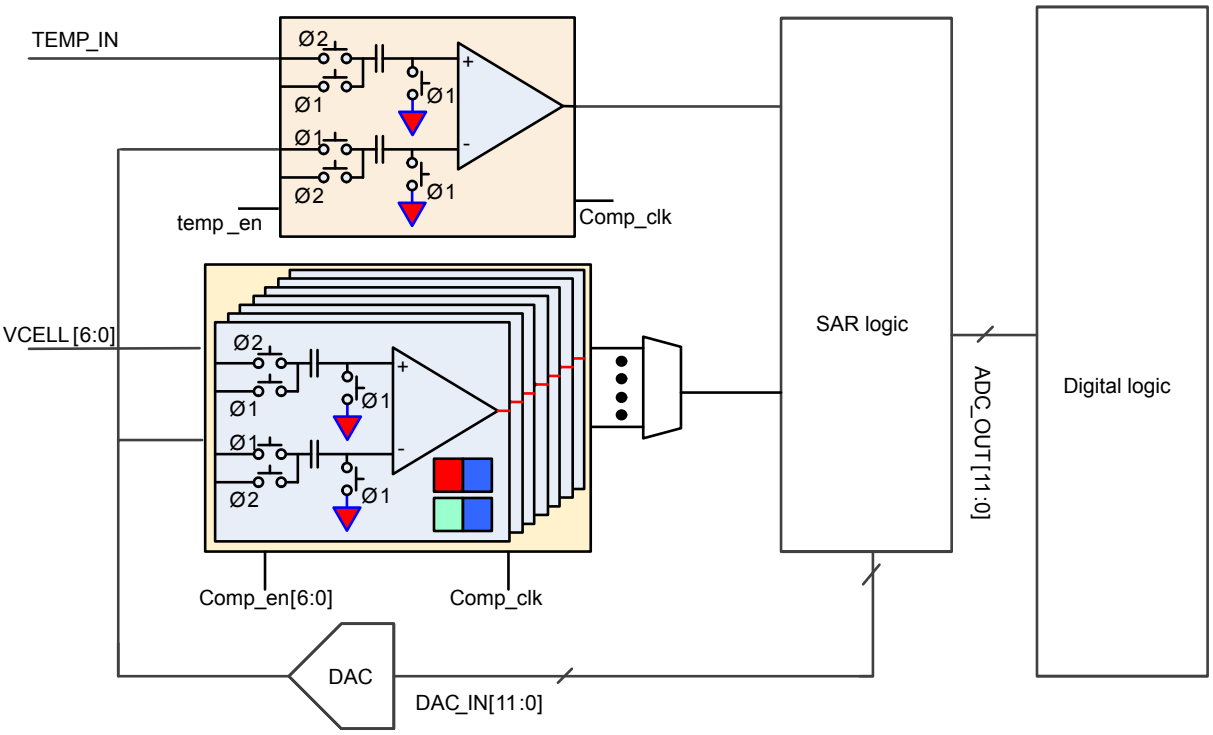

FIGURE 5.14: Block diagram of ADC implementation

manner. A measured accuracy of less than ±4.5 mV is achieved for the ADC.

5.3.4 Device to device communication

To achieve IC to IC communication in the proposed design, a portion of circuit in the bottom IC is supplied with regulated voltage from the top IC. This is implemented with cyclic redundant synchronous bidirectional voltage mode circuit. Level shifting within the device is obtained with current mode level shifting architecture. With this implementation, requirement of high voltage transistor between ICs, as used in [6] can be circumvented and level shifting current requirement also comes down. Because the proposed solution works on synchronous communication between devices, no additional signaling schemes are required. Fig. 5.15 shows the block diagram of the daisy chain communication between two devices. Each device in the stack receives a 5 V supply from top device, except the top most device. In each IC, there is a circuit which works between supply voltage and supply voltage plus 5 V (VSUP1+5 V) as shown in Fig. 5.15 in dotted lines

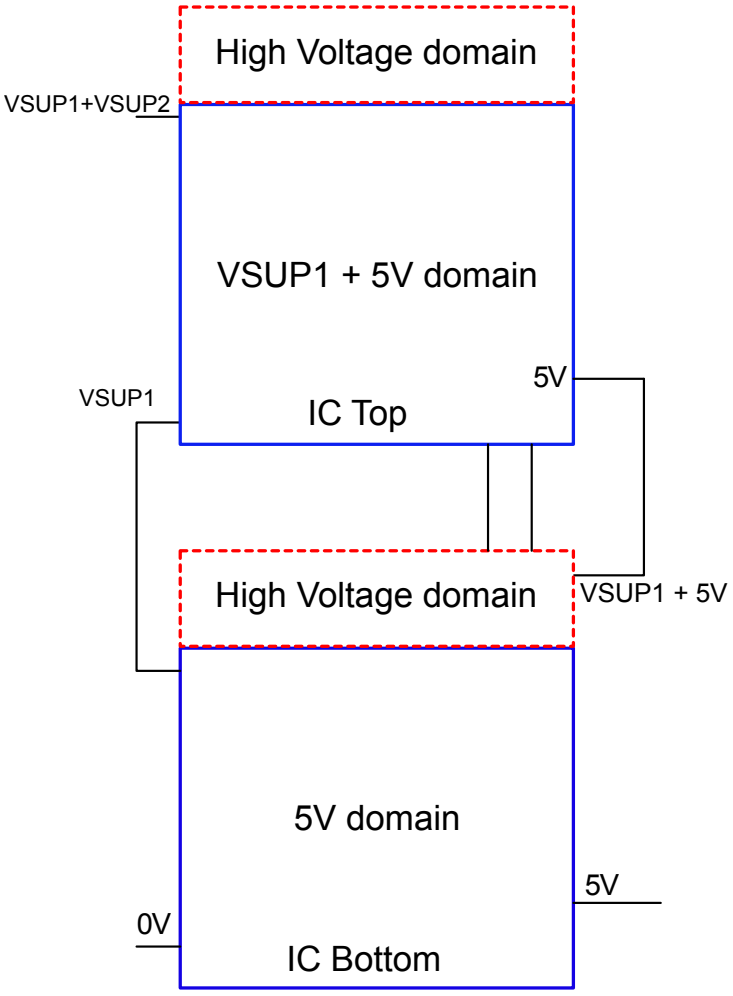

FIGURE 5.15: Block diagram of Device to Device communication circuit

(red colour). Bottom IC supply (VSUP1) acts as ground for this circuit and 5 V from top device acts as supply. This is possible because of using triple well HV CMOS process.

Communication from bottom device to top device is explained in Fig. 5.16 . Signal INL is from the bottom device to be level shifted to OUTH to the top device which is level shifted by current mode within the device. Based on the input INL, current through the mirrors develops Iref·RH voltage drop for the inverter, which works between the bottom device supply (VSUP1) and 5 V supply ($5V\_IN$) from the top device. If INL is low, then there is no current into resistor RH and is pulled to $5V\_IN$ and inverter gives low output (OUTH). The converse happens when INL is high. The values of Iref and RH are selected such that there is enough margin for the inverter to toggle across the corners. Although the current mirrors operate in the low voltage domain, a

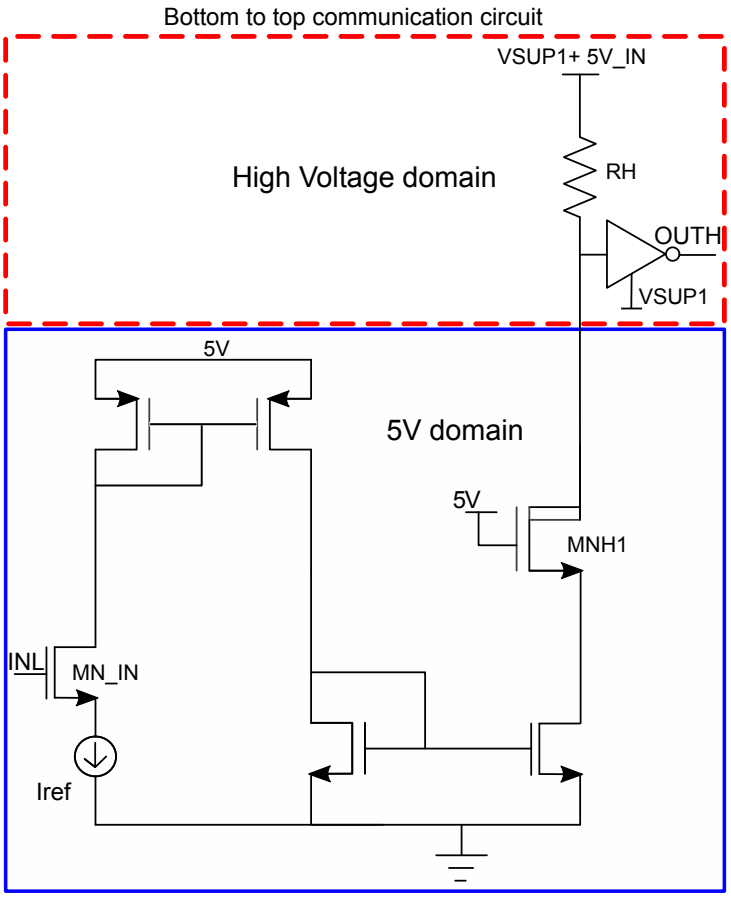

FIGURE 5.16: Schematic of bottom to top communication circuit

high voltage transistor between the high voltage domain and low voltage domain protects the low voltage transistors. For the bottom to top communication, NMOS high voltage protection transistor (MNH1) is placed between the current mirrors. Gate of the NMOS transistor is connected to local 5 V supply.

Similar approach is used to level shift signals from top device to bottom device which is shown in Fig.5.17. Signal from the top device is given to the circuit which works between supply voltage and supply plus 5 V (VSUP1+5 V). Signal INH will be level shifted to OUTL, and a HV PMOS transistor (MPH1) is used to protect the low voltage transistors connected in the bottom section of the IC. Gate of the transistor MPH1 is connected to VSUP1 and level shifted output OUTL will be in 5 V domain. With this design no transistors work between absolute ground of the system and VSUP2, and they all operate in their safe operating range.

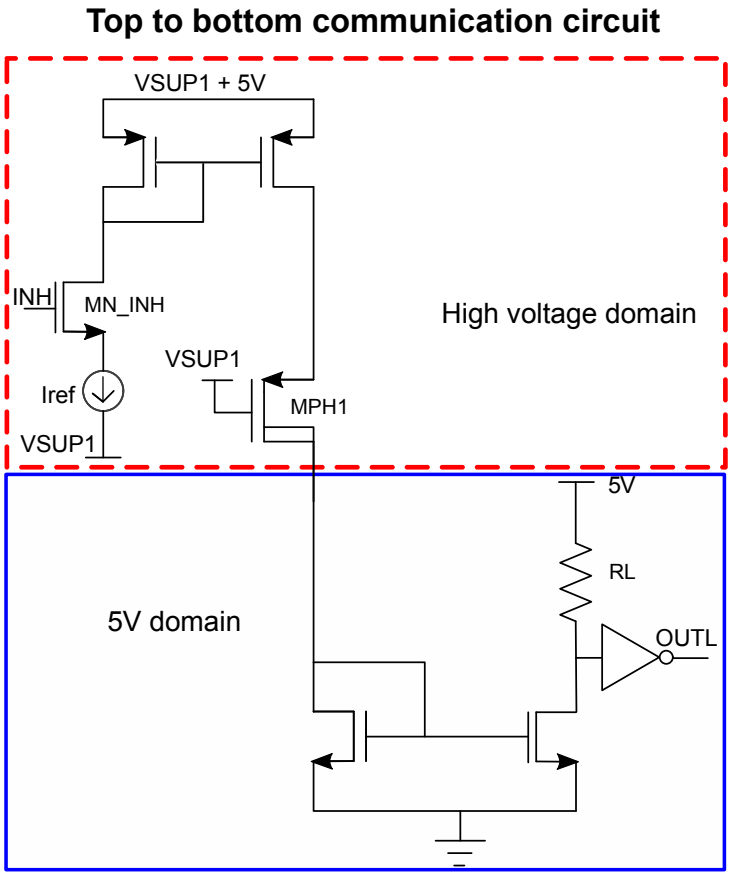

FIGURE 5.17: Schematic of top to bottom communication circuit

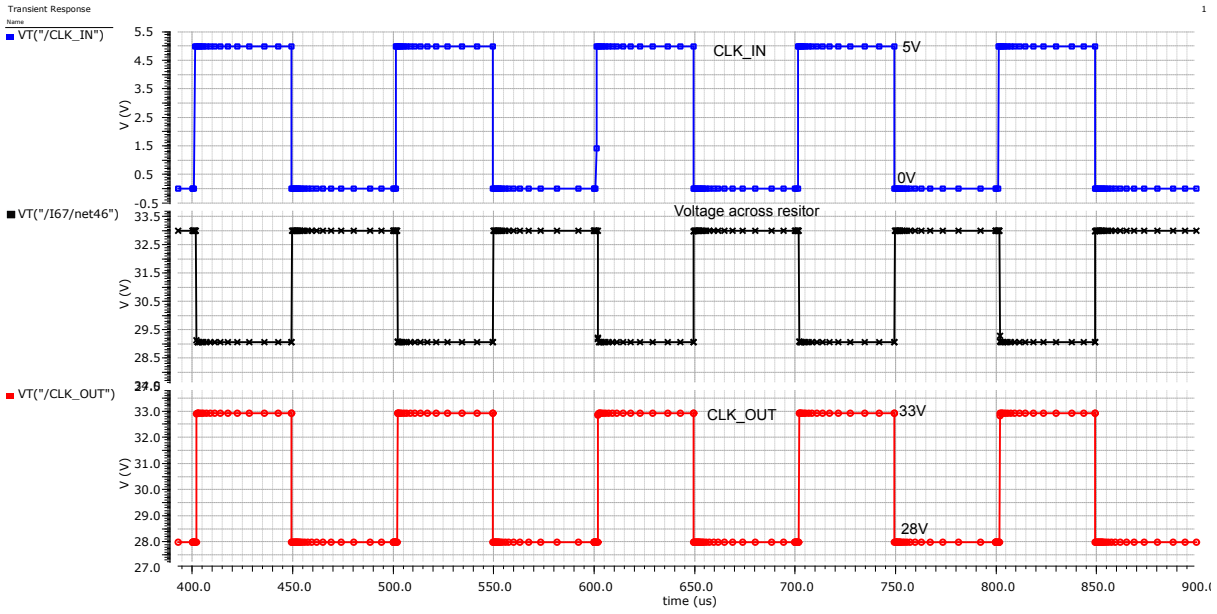

FIGURE 5.18: Simulation results of bottom to top communication

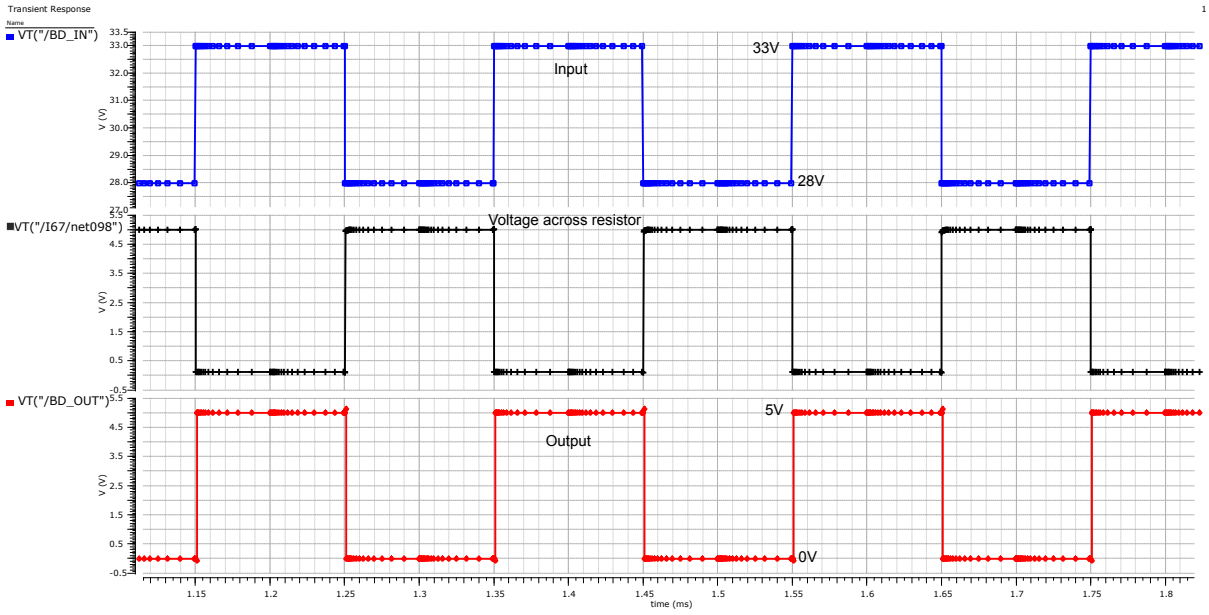

FIGURE 5.19: Simulation results of top to bottom communication

Level shifting simulation results of CLK_IN signal from bottom IC to top IC are illustrated in Fig. 5.18. When 7 cells of each 4V are connected in series in the stack, the voltage $VSUP$ of bottom device becomes 28V. It is clear from the simulation result that the CLK_IN from 0 to 5V domain has successfully been level shifted to CLK_OUT in 28V to 33V domain.

Simulation result of BD_IN from top IC to BD_OUT of bottom IC are illustrated in Fig. 5.19. Results shows that BD_IN from 28V to 33V domain has successfully been level shifted to BD_OUT in 0 to 5 V domain.

When multiple devices are stacked, each device needs to be identified by its own address. In the stack, a device that is connected to host microcontoller and connected to the true ground acts as the master device and the rest of the devices in the stack become its slaves. Instructions from the microcontroller are provided to the master device, which initiates communication to all other devices. With the address allocation process, individual ICs are configured with a unique identification address. Host microcontroller can access device status and data by this unique address. As described in the proposed architecture section, clock from the master device is synchronized to all the slave devices in the system. Top device is identified by a specific

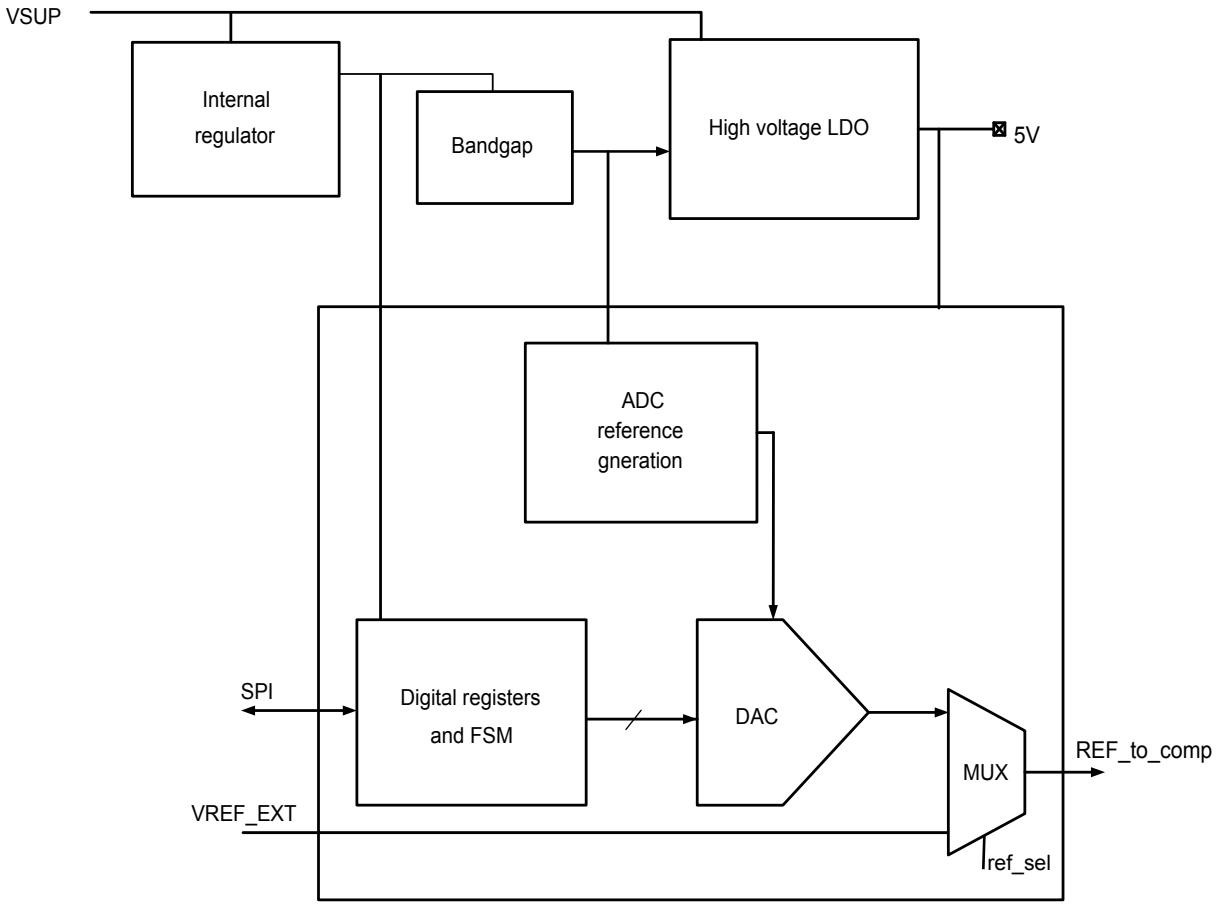

FIGURE 5.20: Block diagram of Power management

pin configuration on board, in addition to additional input configurations connected to slave devices. Communication can be performed between host microcontroller and a specific device or by broadcasting the information to all the devices in the stack.

5.3.5 Power management and Reference generation circuit

Power management block consists of power on reset block, bandgap reference and LDOs. Supply voltage range for the device is from 6 V to 31.5 V. This range is because of the minimum and maximum permissible cell voltages which are 2V and 4.5V respectively and the IC can support a minimum number of 3 cells and a maximum number of 7 cells.

5.3.5.1 Internal regulator

Schematic of internal voltage regulator is shown in Fig. 5.21. This circuit works on IC supply voltage(6 V to 35V) and provides 3V output [10]. High voltage circuit is implemented with 50 V transistors. In this design PJFET is used to generate constant current for the circuit. Transistors MP2, MP3, Q1 and Q2 and resistors R1 and R2 form the bandgap circuit based on Brokaw principle. Transistors MP1-MP4 and MN1-MN2 form current mirror based OTA to drive the high voltage common source stage MHN1 and MHP1. Output of the V3V_REG can be set by the ratio of R3 and R4 if base currents of Q1 and Q2 are neglected. Transistors MHN_BG and MHNPASS are sized to support the loads on these transistors. Precision bandgap circuit is implemented on 3V3_UREG output. High voltage LDO (HVLDO) works on supply voltage and provides 5 V output which can drive upto 50 mA. Reference to the HVLDO is given by prevision bandgap and is externally compensated. Except the digital and precision bandgap circuit all other circuits including the reference generator circuit for the comparators work on 5 V supply. In a stacked system, output of 5 V regulator is given to the bottom device. Communication between the devices works with this supply domain, as discussed in the device to device communication section.

Fig. 5.22 illustrates the simulation results of internal regulator circuit. For this simulation, a VSUP of 6V is considered as this is the minimum supply with a slow ramp rate of 1 sec. Results show V_{BG} settling in about 0.6 sec and $3V3\_REG$ also settling around the same time.

5.3.5.2 Precision bandgap reference

In this IC, precision bandgap reference is implemented by using piecewise linear curvature correction method[49]. Main reason for using this type of bandgap compared to the bandgap presented in chapter 3 is, comparison of cell voltages to the reference voltage should happen

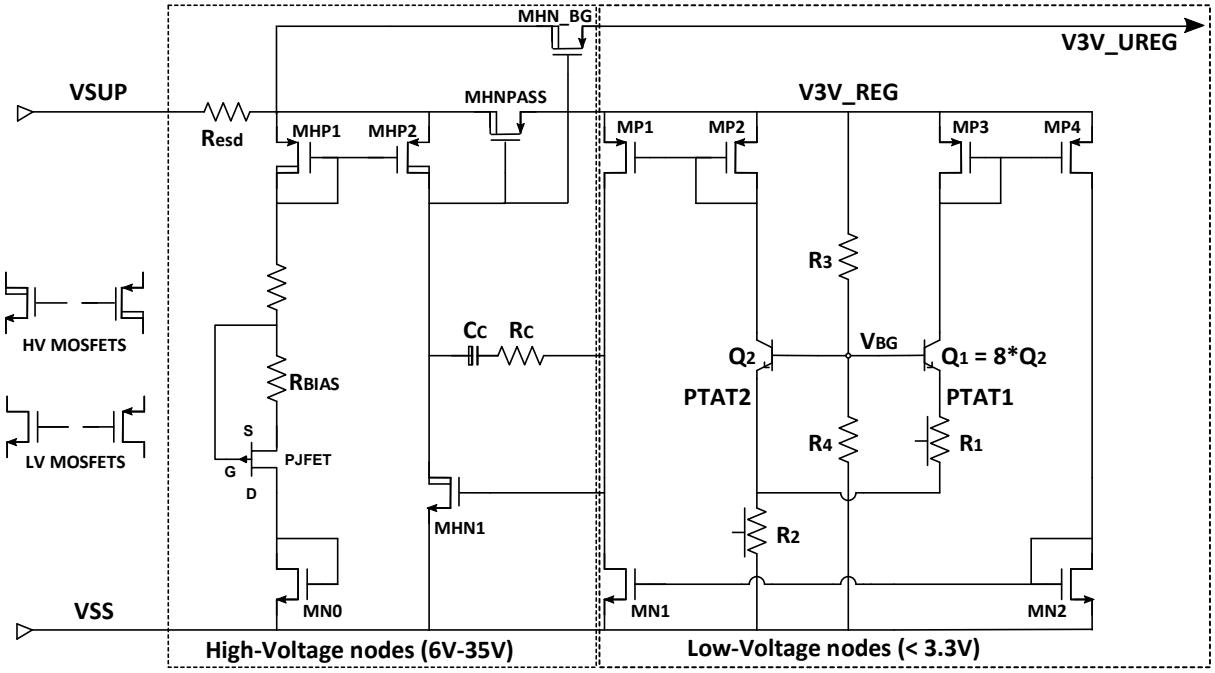

FIGURE 5.21: Schematic of internal regulator circuit [10]

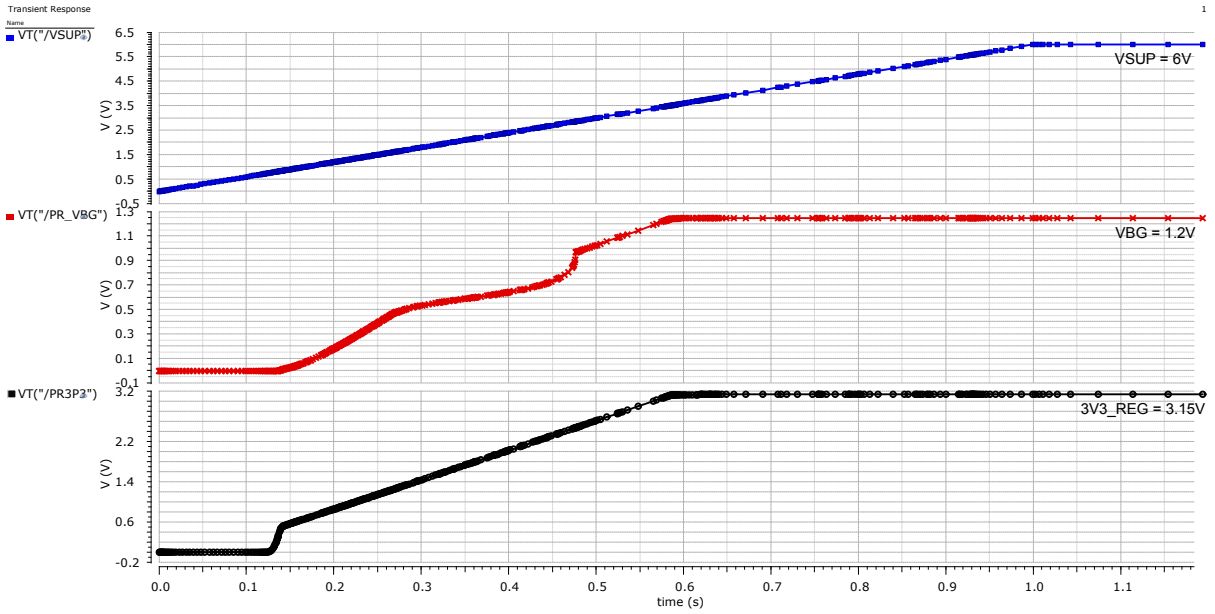

FIGURE 5.22: Schematic of internal regulator circuit

within the IC to facilitate local decision making. It is not possible to calibrate using the host microcontroller. Compared to the bandgap design presented in chapter 3, this design is 4 times larger in size due to piecewise linear curvature correction circuit.

Schematic of the bandgap is shown in the Fig. 5.23. Coarse trim is implemented by using R_{C_trim} and fine trim is implemented by R_{F_trim}. Output of the bandgap core (V_{ref_core}) has a curvature error. Nonlinear current I_{NL_Cur} from the curvature corrected circuit is passed through the resistor R_{corr}. Fig.5.24 illustrates graphical representation of non-linear curvature current. V_{ref_out} is a curvature corrected output of the bandgap. Output of the bandgap is given by

$$V_{ref\_out} = V_{BE2} + (V_{BE1} - V_{BE2}) * (1 + \frac{R2}{R3}) + R_{corr} * I_{NL\_Cur} \tag{5.12}$$

$$V_{ref\_out} = V_{BE2} + Vt * (ln(n)) * (1 + \frac{R2}{R3}) + R_{corr} * I_{NL\_Cur} \tag{5.13}$$

Fig.5.25 shows simulation results of output of the non-linear current generation circuit. It can be seen that 7 current sources are used to generate a non-linear current which has the opposite curvature of bandgap reference. Fig. 5.26 illustrates the simulation results of curvature corrected and un-corrected bandgap reference output.

5.3.5.3 Reference generation

Reference voltage for the comparators is generated in two possible ways. One by an external source and the other by an internal resistive DAC. In case of stacked system, a 12-bit DAC is used to generate the reference, based on the code received from the microcontroller. A 4.5 V trimmed voltage for DAC is generated by amplifying precision bandgap reference of 1.2 V.

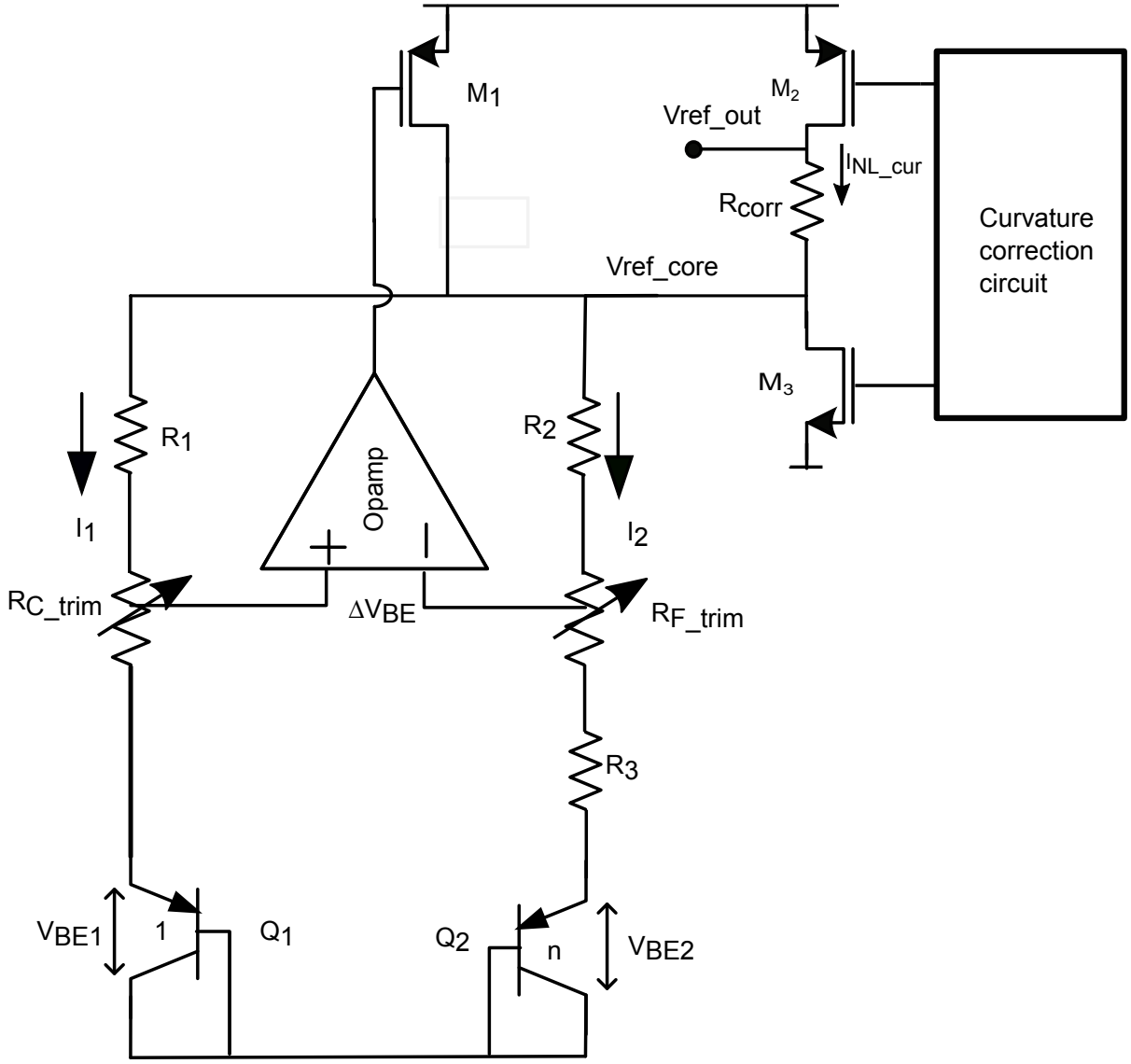

FIGURE 5.23: Curvature corrected bandgap

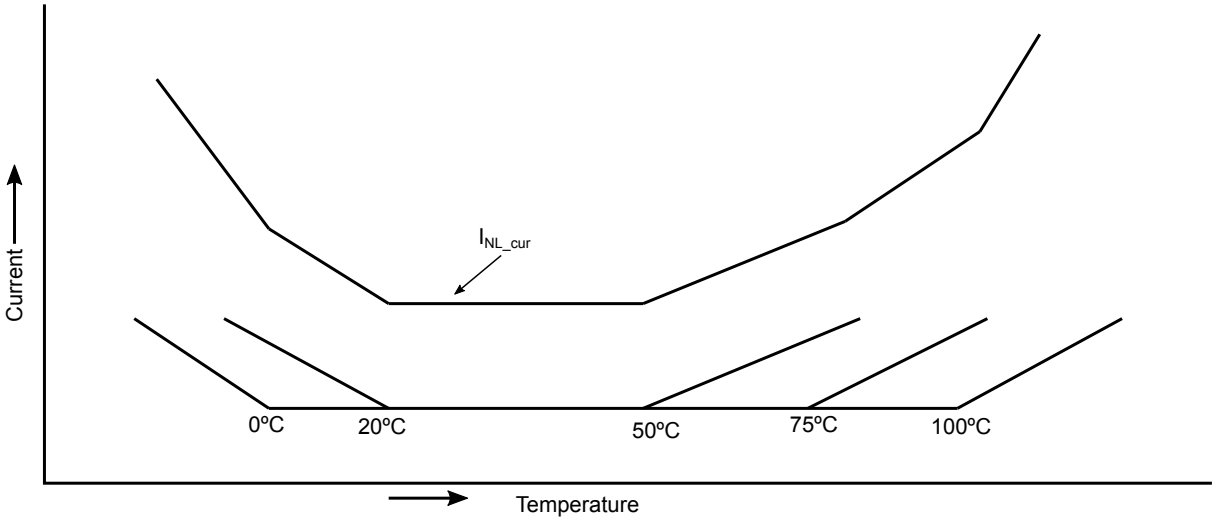

FIGURE 5.24: Graphical representation of curvature correction

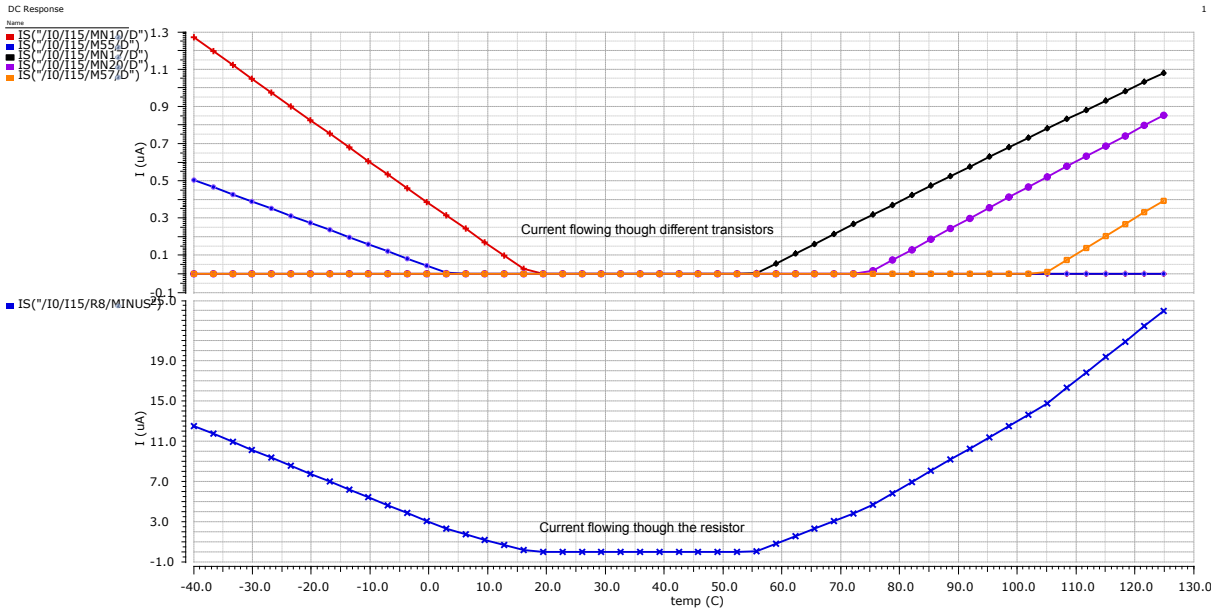

FIGURE 5.25: Simulation results of the non-linear current generation block

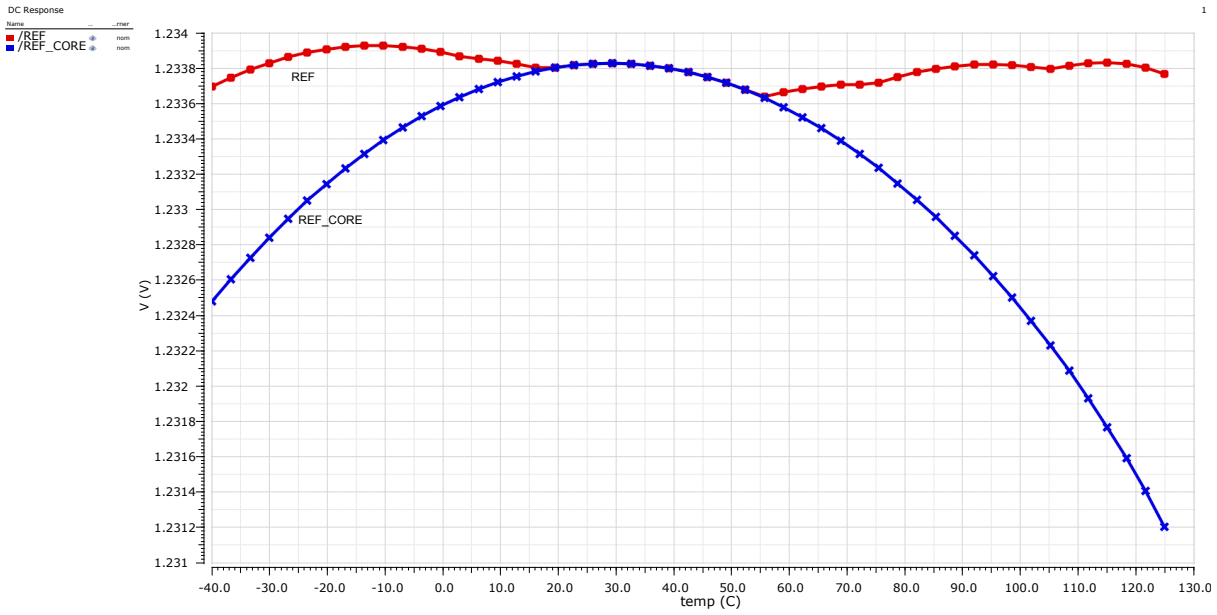

FIGURE 5.26: Simulation results of reference voltage with and without curvature correction

For a single device, reference voltage can be provided by an external resistive divider. Such external reference providers are helpful when the IC needs to work standalone without a host microcontroller. Reference in this case is always the average value of the cell voltage stack. Whenever balancing is initiated, comparators compare with predefined thresholds to ensure safety. These thresholds are selected by using either the fixed threshold defined within the device or by using the value generated by DAC. Since the device has flexibility to support a minimum

of 3 cells and a maximum of 7 cells, cell detection should also be performed during the power up of the device. A minimum threshold of 500 mV is compared with the cell voltages to detect the presence of a cell. Fig. 5.27 shows the schematic of reference multiplexer. This multiplexer circuit selects one of the four reference values depending on the select line. These four reference values are (i) Upper threshold (THU) (ii) Lower threshold (THL) (iii) Reference voltage to which the cell has to be balanced (VIN) and (iv) Cell detect value (500mV).

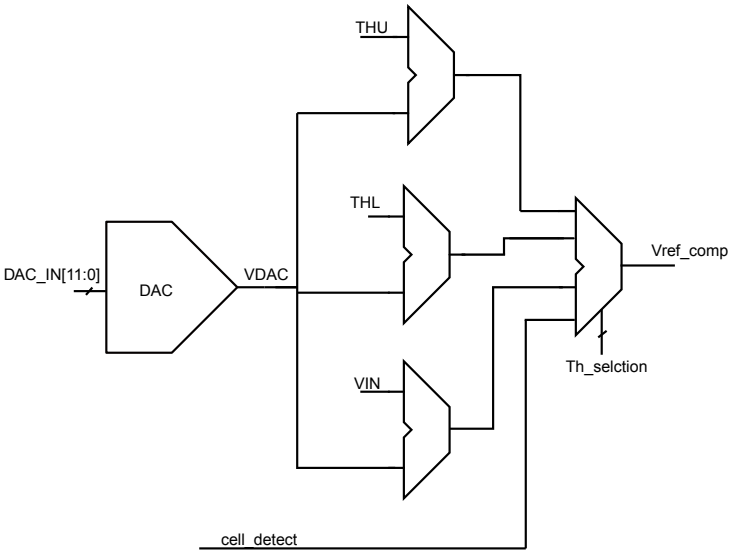

FIGURE 5.27: Schematic of reference multiplexer

5.3.6 Pulse Width Modulated Oscillator

For the active balancing application, secondary of the flyback transformer can be connected between the balancing switches BLSW_H and BLSW_L pins shown in Fig. 5.2. Primary of the transformer is driven by an external transistor. Gate of the external transistor is controlled with a PWM driver generated internally. PWM oscillator is designed such that its frequency and duty cycle can be programmed. Circuit diagram of PWM oscillator is shown in Fig 5.28. The oscillator generates a PWM frequency by comparing the capacitor voltage with high precision band gap reference voltage Ref [50]. The capacitor C is charged with a constant current I_{const} and the comparator toggles once the charging voltage of capacitor reaches the reference voltage.

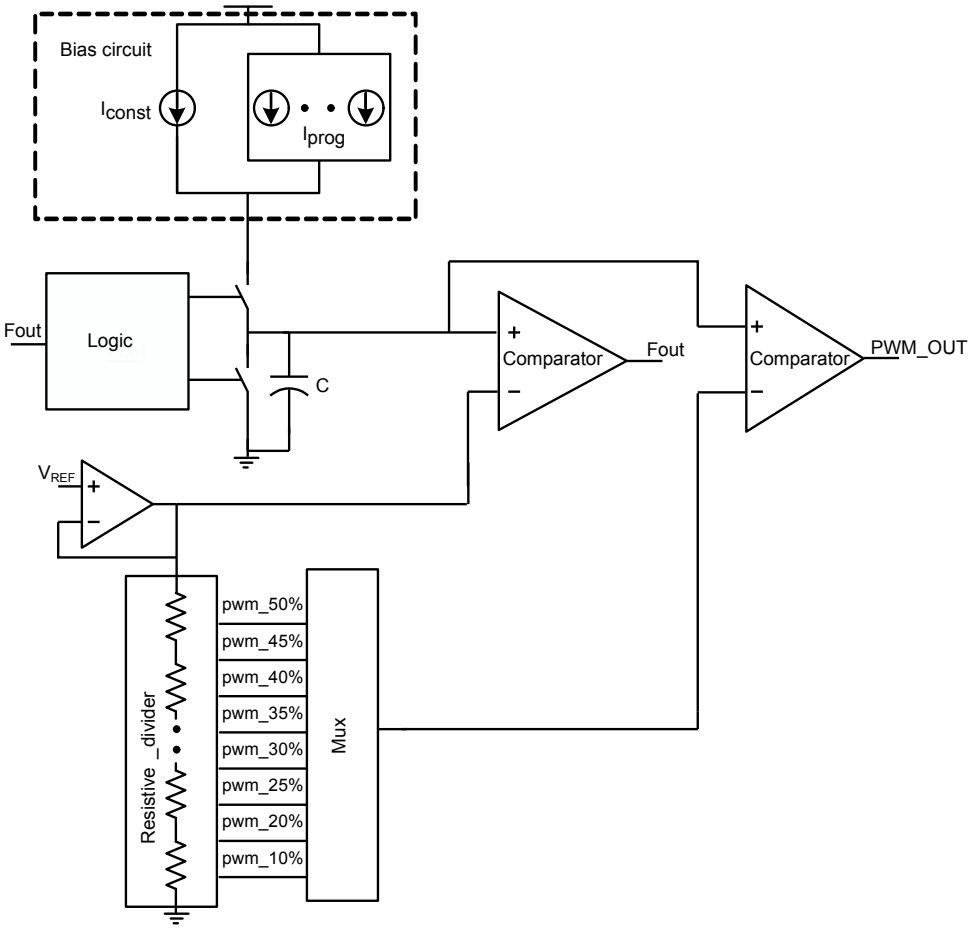

FIGURE 5.28: PWM generation circuit

Logic circuit controls the charging and discharging of capacitor based on comparator decision. Frequency of the oscillator is based on the charging current, capacitor and the reference voltage. Frequency is given by following equation

$$F_{pwm} = \frac{I_{const} \pm I_{prog}}{2 \cdot V_{REF} \cdot C} \tag{5.14}$$

Programmable frequencies of 25 KHz, 50KHz, 100 KHz and 200KHz are implemented. Duty cycle from 10% to 50% can be programmed. Based on the application, frequency and duty cycle are adjusted.

Fig. 5.29 depicts the simulation results of the PWM oscillator. In the figure, PWM output and its corresponding reference voltages are captured for all possible combinations and care is taken

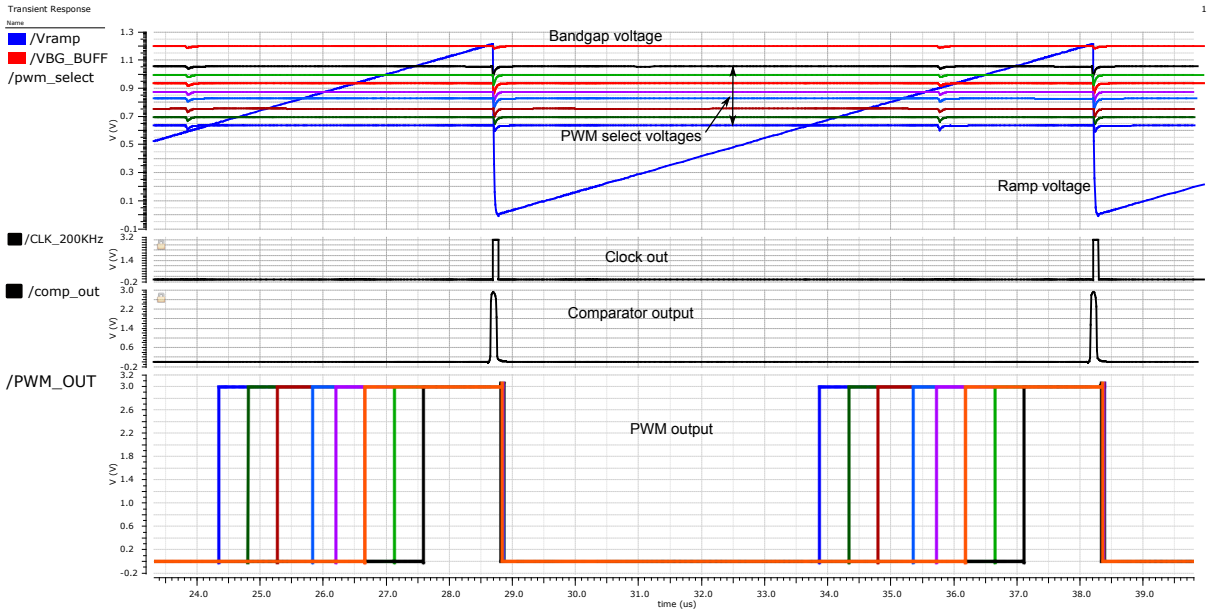

FIGURE 5.29: Simulation results of PWM circuit

to match the colors of PWM output and its corresponding reference voltages.

5.4 Conclusions

In this Chapter detailed description of proposed architecture is discussed with a focus on stacked cell monitoring and balancing system. Design and implementation detail of individual blocks are described. Schematic and design details of balancing switches are explained with an emphasis on on-resistance and area of the balancing switches. A switched capacitor level shifter has been proposed, to shift the levels of different cell voltages to a common mode of 2.5 V. To improve the resolution of measurement to less than 1 mV, an offset cancellation comparator has been implemented. By reusing the comparators and DAC used for reference comparison, a 12-bit SAR ADC has been implemented. IC to IC communication is implemented with cyclic redundant synchronous bidirectional voltage mode circuit. The power management system implemented consists of a high-voltage (5 V) regulator to power most of the analog blocks in IC and a low-voltage internal regulator (3 V) to power the digital core. Housekeeping analog circuitry

for proper operation of the IC includes power-on-reset, voltage and current bias generators, a 80.0KHz master oscillator and a programmable PWM generation circuit.

Chapter 6

Evaluation setup and Experimental Results

This chapter is organized into two sections. First section focuses on the lab evaluation setup to evaluate the fabricated IC and demo board to demonstrate the balancing concept. Experimental results are discussed in the second section.

6.1 Evaluation setup

Evaluation setup consists of Device Under Test (DUT) board and an FPGA board. Evaluation software is developed in LabView, from which commands to control the DUT are sent to FPGA. FPGA communicates to DUT using SPI to access the specified registers in the DUT. FPGA board acts an interface between the computer and the DUT. Individual functions of the device are evaluated with this setup, which is shown in Fig 6.1.

Demo board setup is demonstrated in Fig 6.2, in which two battery packs of three Li-ion cells stacked in each pack are used. It consists of two cell monitoring and balancing ICs, one for

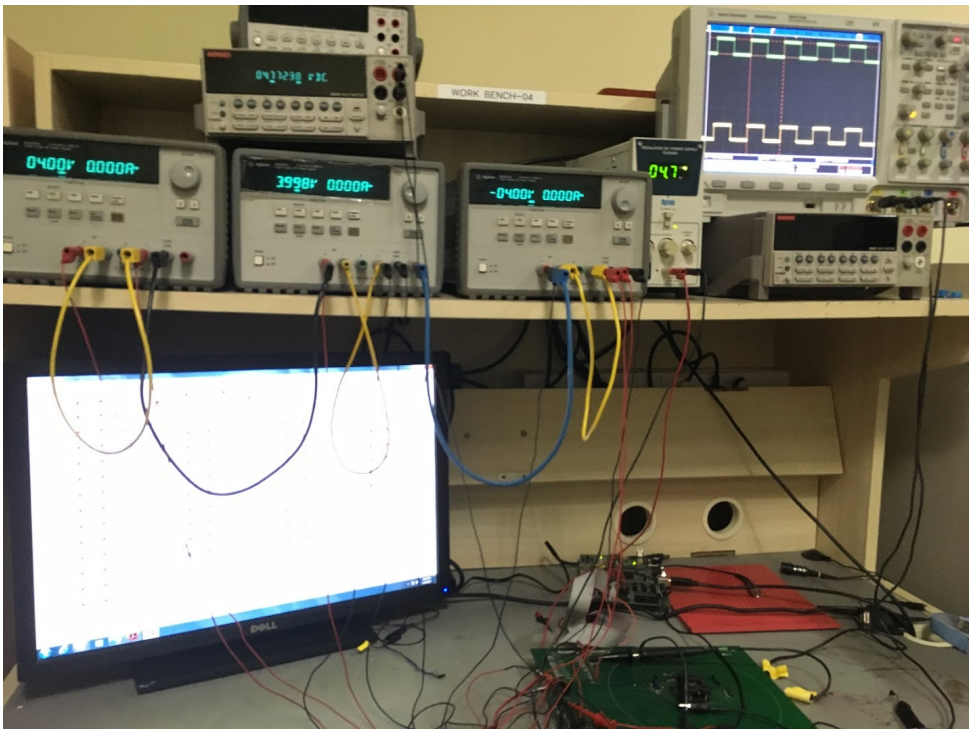

FIGURE 6.1: Lab evaluation setup

each pack, flyback transformer for active balancing and a separate IC for current measurement. Board is also connected to a TFT display to assist in displaying the status of critical parameters. External switches are used to provide control inputs to the demo board.

6.2 Experimental results

As mentioned earlier, the complete design has been fabricated in 0.35μm High voltage CMOS process. Chip micro graph is shown in Fig. 6.3. It uses very few external components for the measurement and balancing. In case of passive balancing, only one external resistor is sufficient for the measurement and balancing. For passive balancing, external resistor value is chosen such that current through the balancing switches is not more than 100 mA (maximum). To reduce the power dissipation within the device it is important to keep the resistance of balancing switches as low as possible, while also taking device area into consideration. Measured results of typical on-resistance of balancing switches is shown in Fig. 6.4. At room temperature, it is around 8 Ω

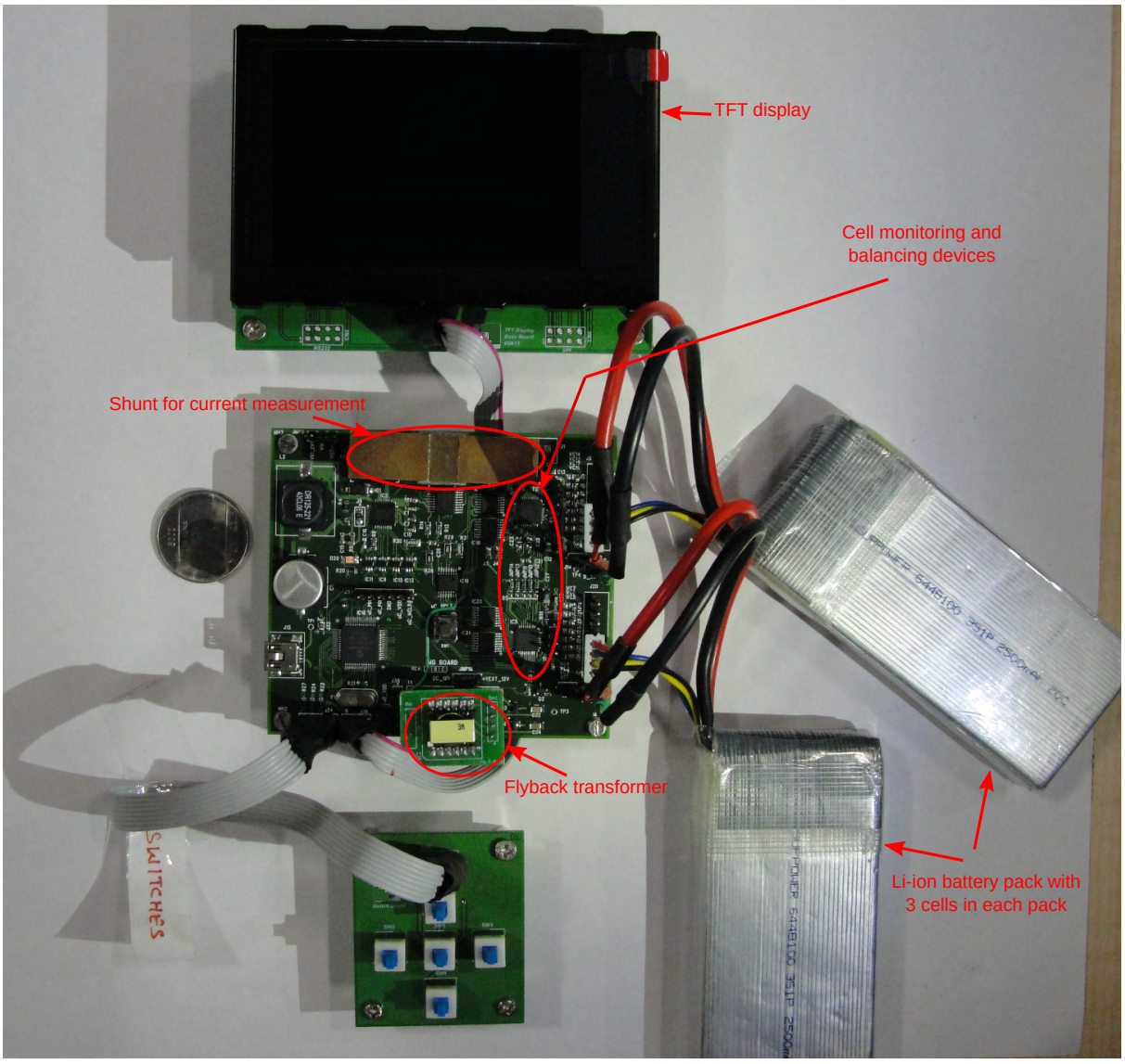

FIGURE 6.2: Demo board setup with 3 cells in each pack

for both top and bottom switches. Balancing can be initiated from the microcontroller by setting the reference. If balancing is done after a charging cycle, then the reference can be a fixed voltage. It must be mentioned that all the cells will be discharged to the reference voltage. To meet the required balancing accuracy, reference voltage of the series connected cells need to be within the limits of accuracy. Fig. 6.5 shows that at room temperature, reference voltage is trimmed to 4.5 V (typical) with a ± 2 mV accuracy. Measurement of cell voltages is carried out in a sequential mode. Fig. 6.6 and Fig. 6.7 show the measured error in cell voltages at cell voltages of 1.8 V and 3.6 V respectively. Measurement is carried out on 10 samples at room temperature. Results

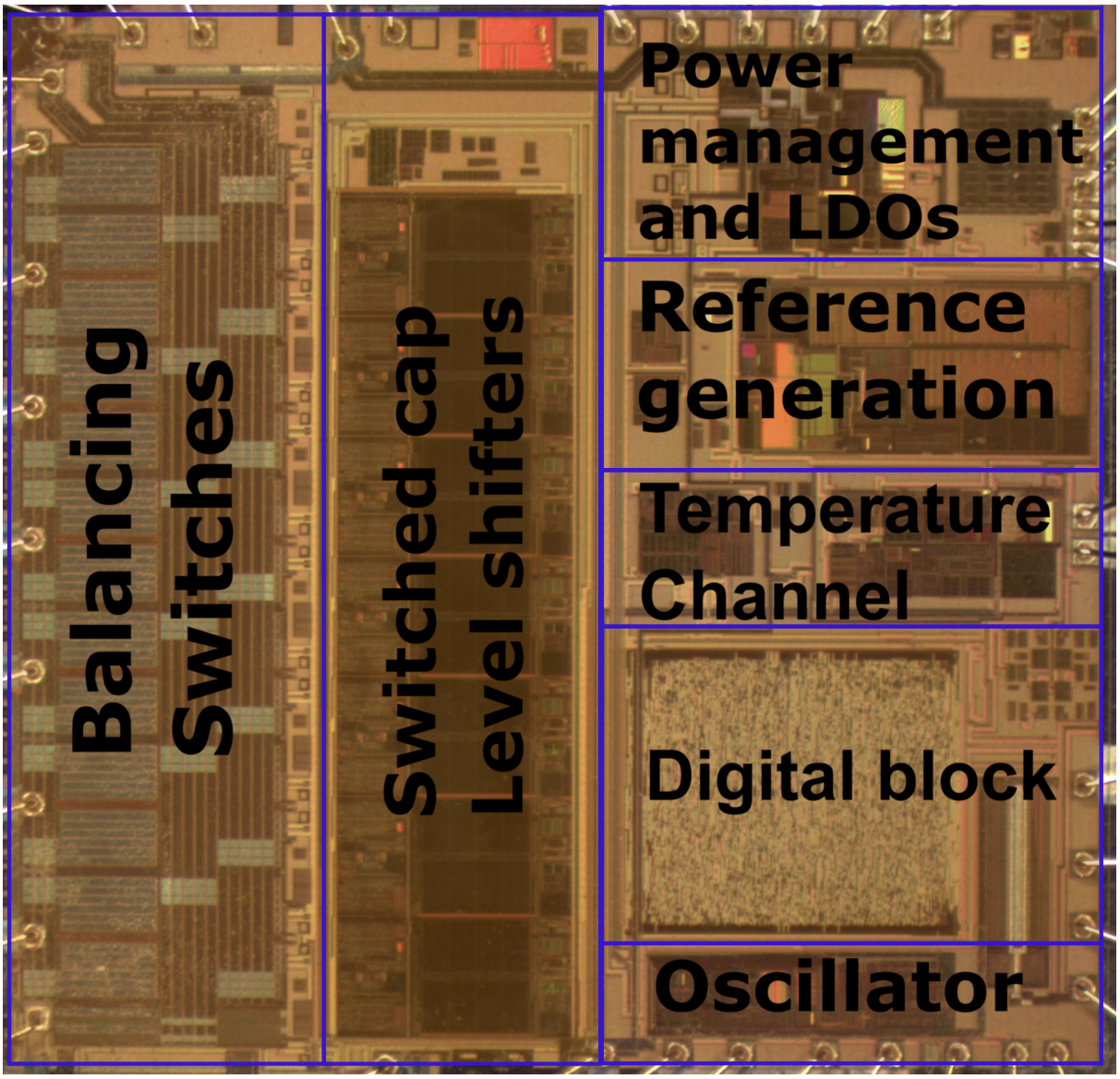

FIGURE 6.3: Image of chip

show that error is less than ± 4.5 mV. For synchronization of measurement, clock from master device is transmitted to top slave device as shown in Fig.6.8. In this measurement, each cell voltage is set to 4 V thus the ground for the clock of slave device is 28 V.

Measurement results of balancing using the proposed balancing switches are illustrated in Fig. 6.9. In this measurement setup, there are seven cells connected in series with each cell having a voltage of 4V and hence a stack voltage of 28V. From the plot, it is evident that the voltage across the balancing pins is the voltage of the cell as selected by the control signal.

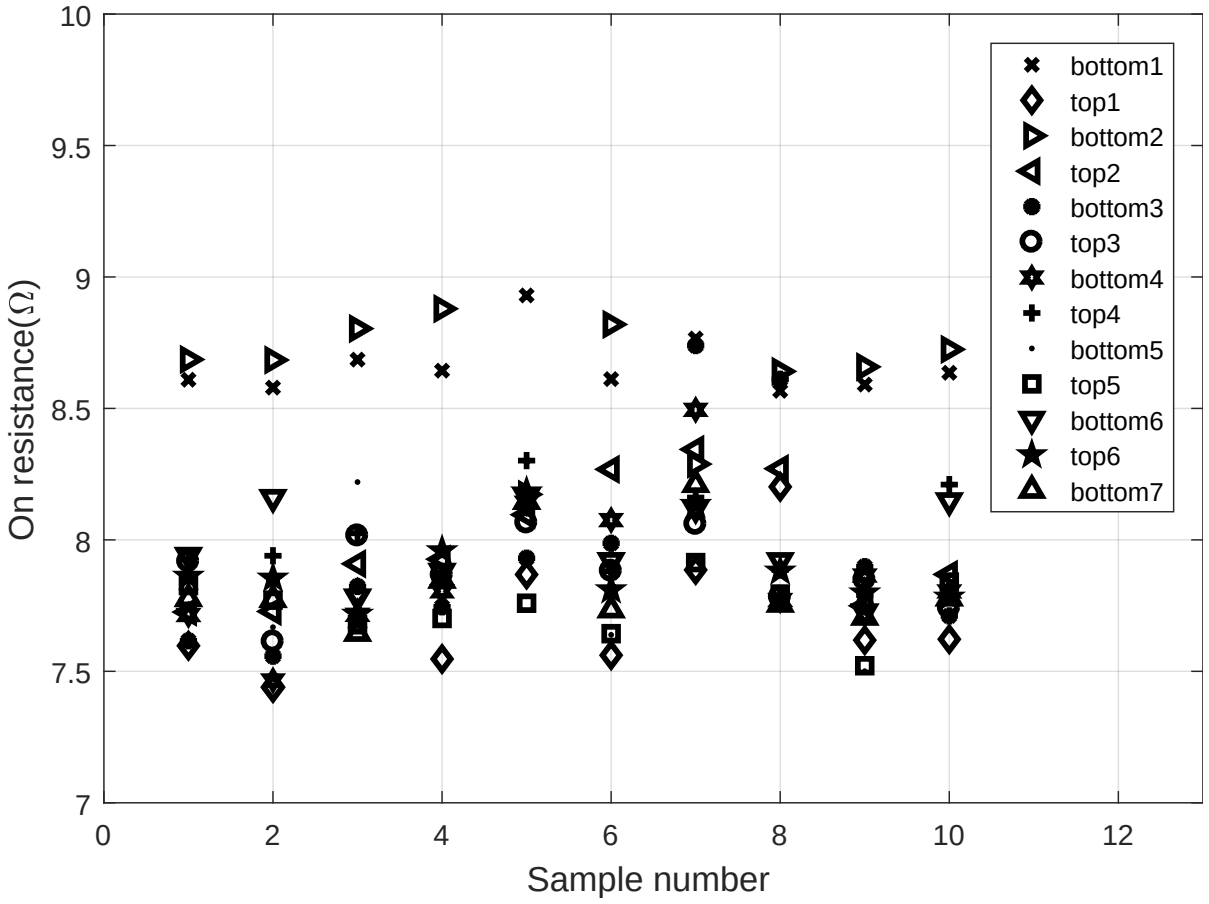

FIGURE 6.4: Measurement results of Balancing switches ON resistance for both top and bottom switches of 6 cells and bottom switch of 7th cell

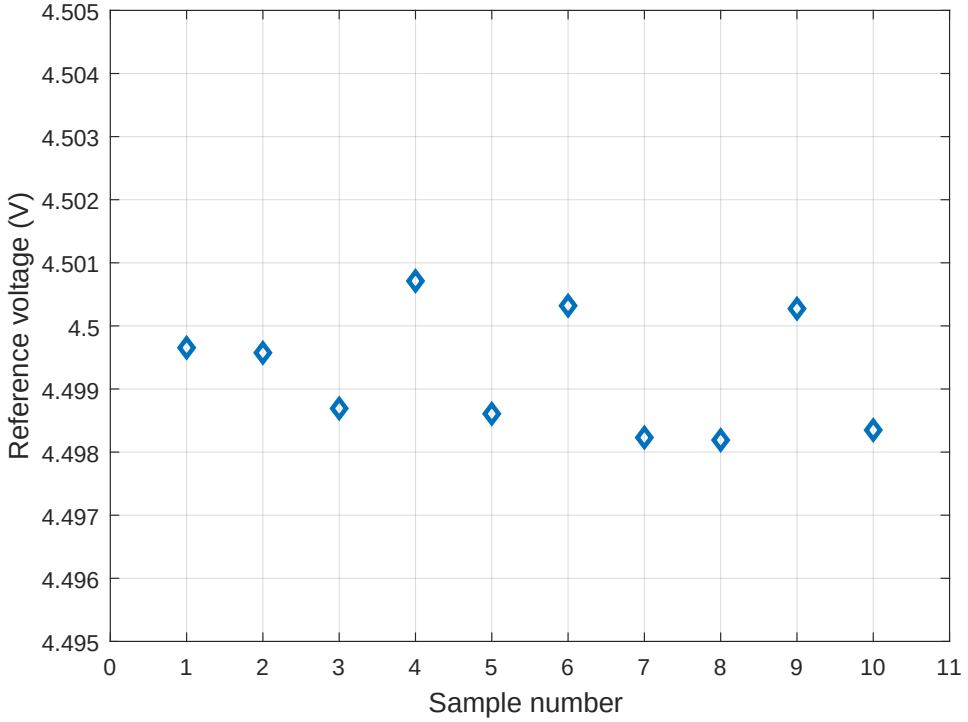

FIGURE 6.5: Measurement results of reference voltage

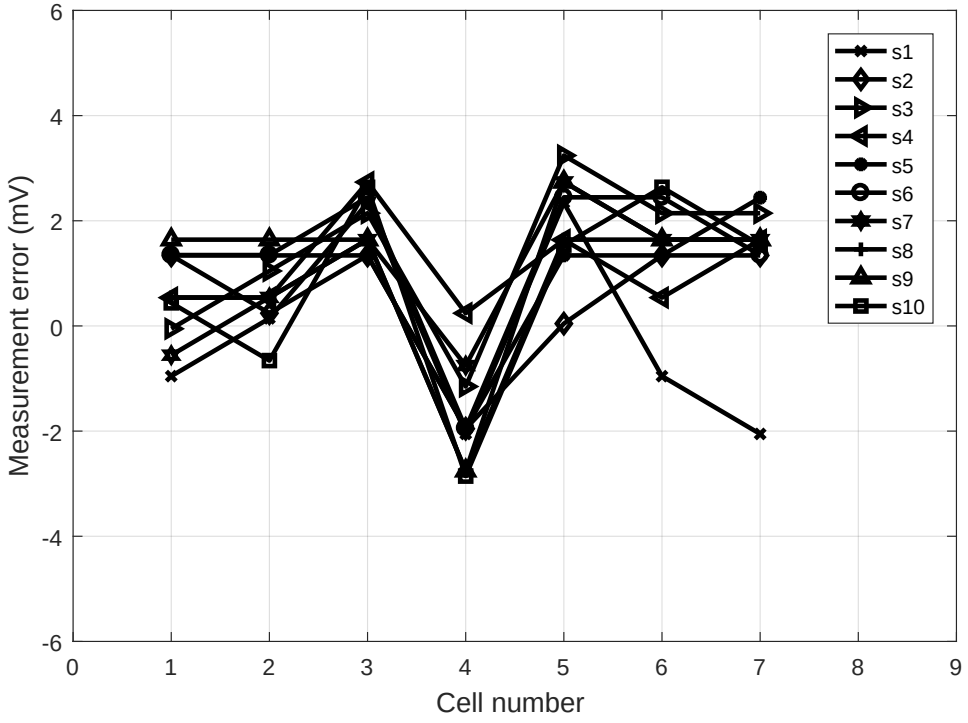

FIGURE 6.6: ADC measurement error at 1.8V cell voltage

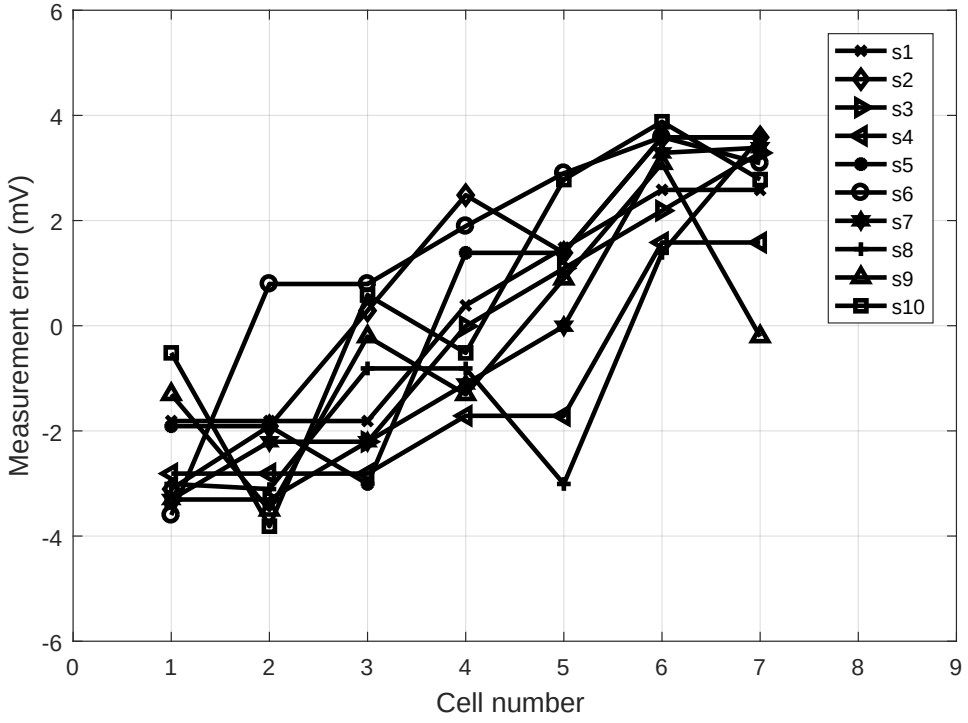

FIGURE 6.7: ADC measurement error at 3.6V cell voltage

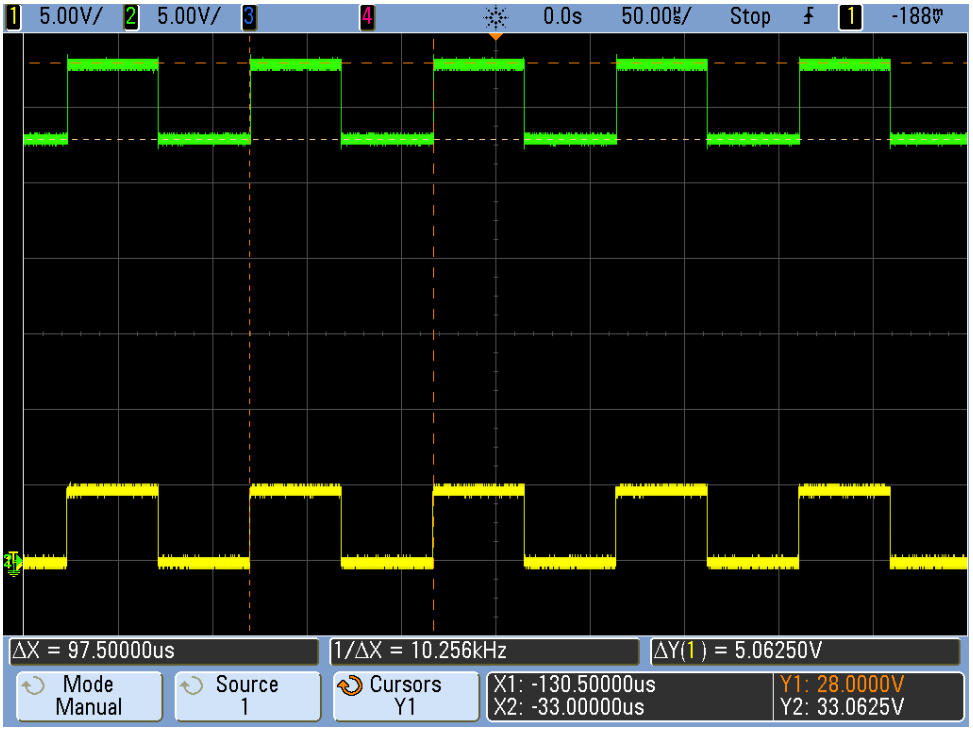

FIGURE 6.8: Clock from the bottom device transmitted to clock of top device

FIGURE 6.9: Measured results voltage across balance switches during balancing

Experiments are carried out on the stacked system with 3 cells connected to Master device and another 3 cells connected to the slave device. Active balancing results with external source are shown in Fig. 6.10. An 8 cell battery system is placed in the application where motor and inverter are placed. Experiments are performed for the stack communication by measuring the cell voltages through the daisy chain communication with motor and inverter turned ON. Communication worked without fail even under these conditions. Fig. 6.13 shows the system that is implemented.

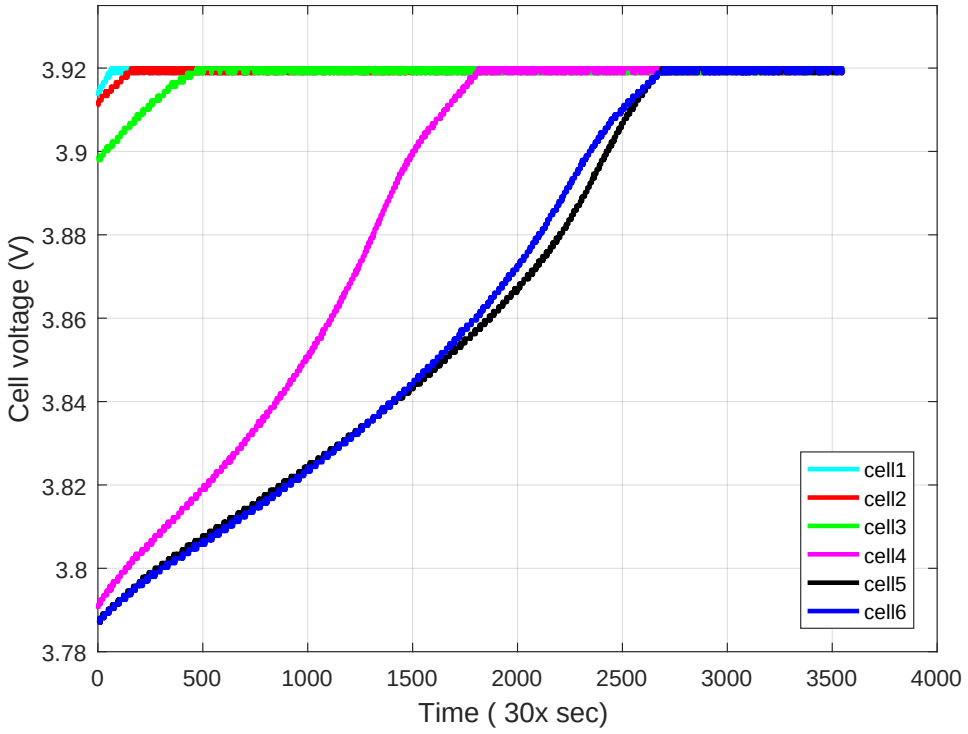

FIGURE 6.10: Active balancing with external source

Fig. 6.11 shows the demo-board used to validate balancing in a single device working standalone without host microcontroller. Fig. 6.12 shows the 7-cells in the standalone device discharged initially to different values indicating imbalance. From the figure it is clear that after 2000sec all the imbalanced cells have been balanced to a reference voltage of 3.2V.

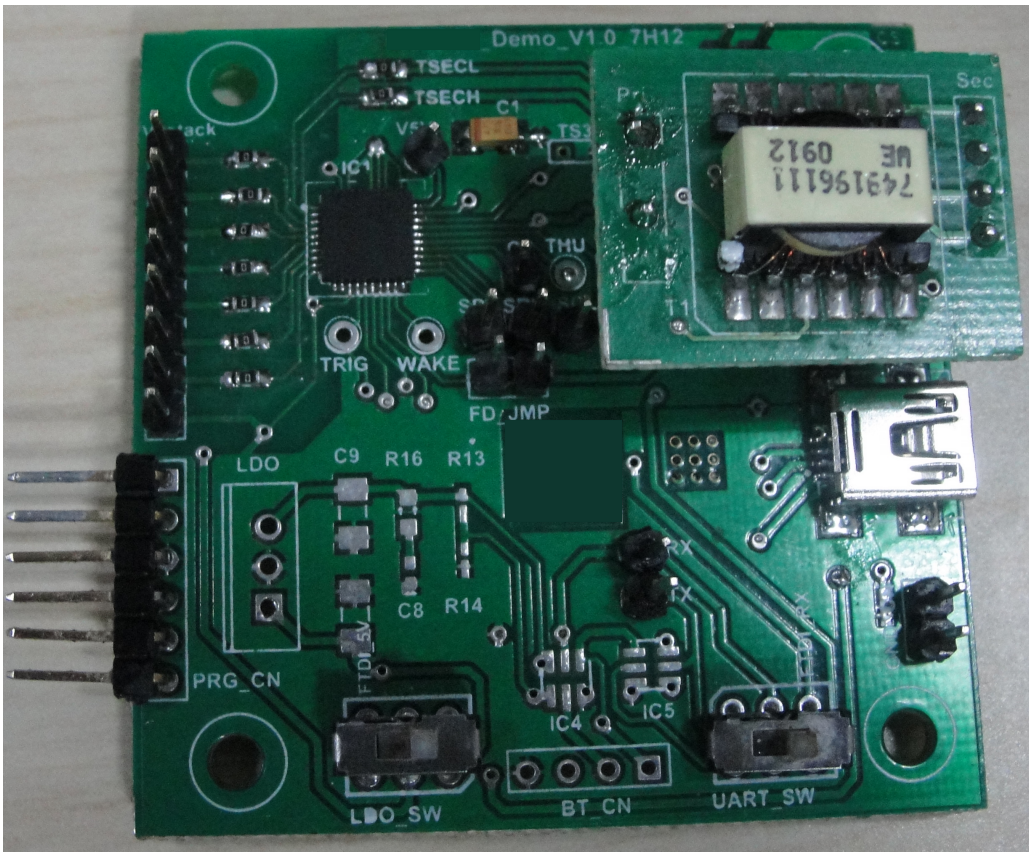

FIGURE 6.11: Cell balancing Application

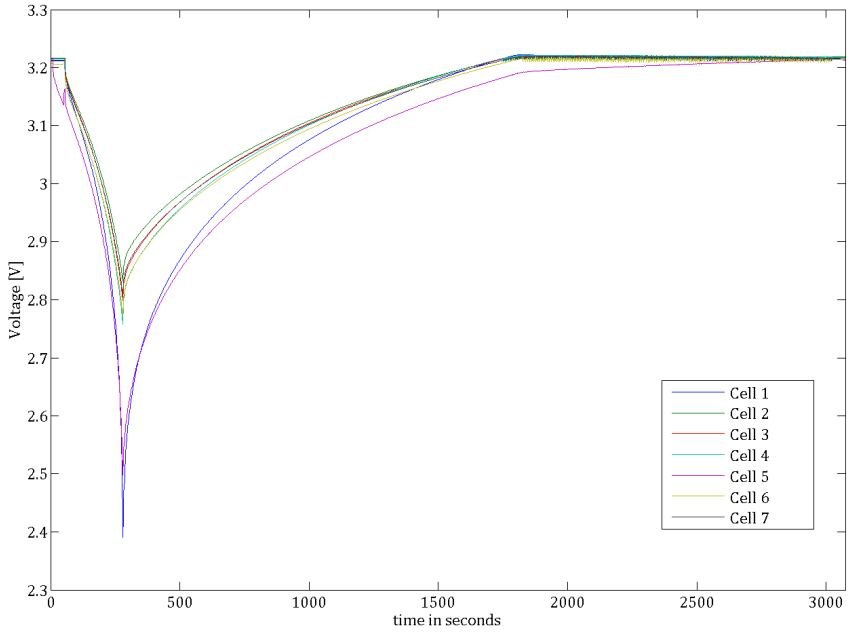

FIGURE 6.12: Active balancing in a standalone device with an external source

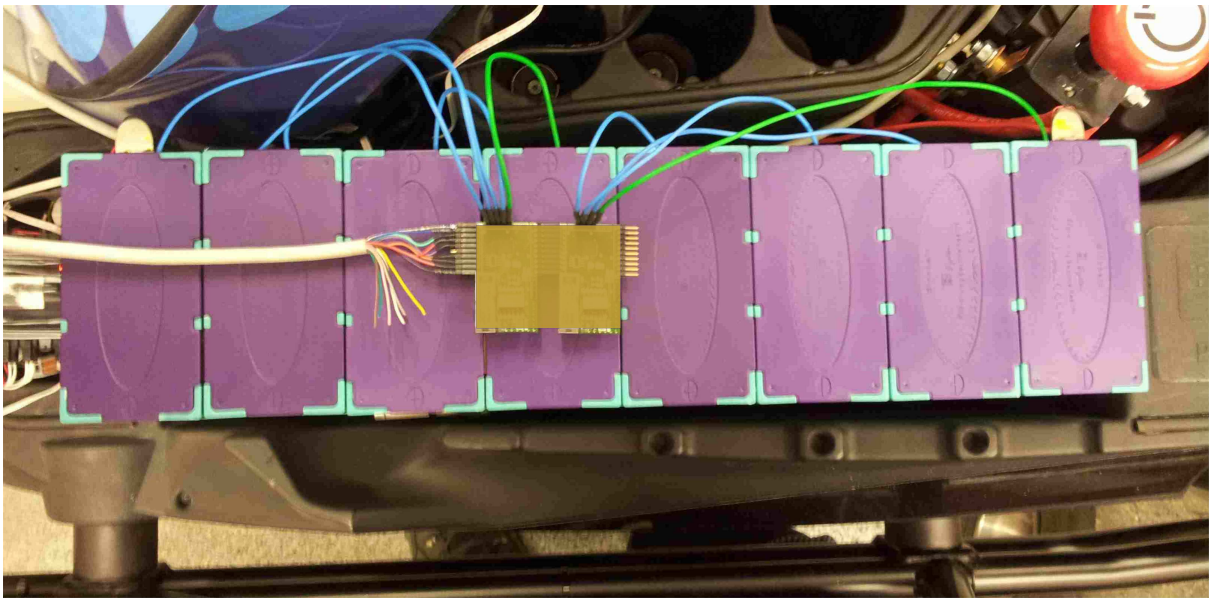

FIGURE 6.13: Cell balancing Application

A comparison of this work with previous published work is shown in Table6.1. Compared to existing designs, the proposed design requires significantly less number of additional components and thus reduces the overall complexity of the system. While the measurement error in comparison with the system reported in [6] is more, it may be noted that it is less than 1% of the cell voltage as desirable.

TABLE 6.1: A comparison of performance with existing designs

Property	This work	[6]	[29]	[8]	[17]
Balancing switches	Internal	External	External	External	External
Simultaneous comparison	Yes	No	No	No	No
Communication	No external components	No external components	External diodes	External capacitors	Opto isolators
Cell balancing	Active or Passive	Active or Passive	Passive only	Passive only	Passive only
Quiescent Current	17uA	15uA	13uA	75uA	NA
ADC Accuracy	4.5mV	1.5mV	4.5mV	None	No ADC
No.of ADC's	1	13	1	1	NA

Chapter 7

Conclusions

In this work, a complete battery monitoring circuit for electric vehicles and hybrid electric vehicles has been demonstrated. The design, which has been realized as an IC, can monitor and balance seven Li-ion cells. Multiple ICs can be daisy chained to measure cell voltages of a stack of series-connected cells. To enable simultaneous comparison, level shifters and comparators have been implemented separately for each cell. A 12-bit resistive DAC has been implemented that provides the voltage level to cells in a given stack that are to be charged/discharged. Required cell voltages and temperatures are measured in a sequential fashion by a 12-bit SAR ADC. This information can be transmitted to an external host for further processing using a cyclic redundant synchronous voltage mode bi-directional communication interface. This interface allows communication between the ICs without the use of external components. To address cell-to-cell variation, balancing switches have been incorporated in the IC as opposed to the external balancing switches present in the existing designs. In order to facilitate active balancing, PWM driver has been implemented in the circuit. A digitally calibrated bandgap has also been proposed which helps in accurate current measurement.

The designed IC consumes a quiescent current of 17 μA. The measured accuracy of the 12-bit SAR ADC is less than 4.5 mV which corresponds to 0.1% of the maximum cell voltage of 4.5 V. In order to meet the accuracy requirements of the ADC which is a part of the design, a piecewise-linear curvature corrected bandgap circuit has been designed and implemented. Using the reference provided by this bandgap, a 4.5 V reference is generated with an absolute accuracy of 0.05%. Power requirement for the internal blocks is provided by the On-chip 3 V and 5 V LDOs.

In order to comply with functional safety standards of ISO26262, current and pack voltage measurement IC has been implemented separately . To facilitate accurate current measurement, a bandgap is designed and implemented, which is trimmed for temperature and magnitude and calibrated digitally. Experimental results show a maximum of 0.06 % variation in the bandgap output for a temperature range of -40 °C to 100 °C at a power supply voltage of 3.3 V.

7.0.1 Future Work

Owing to the 50V HV CMOS process, the 48V battery stack is monitored in this work using two stacked ICs. In future, we plan to work with a higher voltage (60V) process as and when available and would like to design a single IC solution to monitor and balance the 48V battery stack suited for mild HEVs. We also plan to improve the measurement accuracy of the ADC and reference voltage generation blocks used in the current design to improve the efficiency of the balancing process thereby improving the battery capacity.

Appendix A

VerilogA model for cell balancing

Cell monitoring and balancing concepts have been verified in VerilogA model before going for actual implementation. Over all cell balancing system has been implemented to verify the concept. Fig. A.1 illustrates the schematic of the simulation setup with verilogA model for a passive balancing system. It can be seen that only one external resistor is used in the setup.

In this simulation setup each cell voltage is considered as close to 3V. To verify the concept, three cells $VCELL1$, $VCELL3$ and $VCELL7$ have been considered to be more than the reference voltage. The value of $VCELL7 > VCELL3 > VCELL1$. Fig. A.2 shows the simulation results of the balancing system in which it is evident that $VCELL1$ is discharged first followed by $VCELL3$ and $VCELL7$. As soon as all the cells reach reference voltage (in this simulation 3V), the balance done BD_OUT signal goes high. Fig.A.3 shows voltage across the balancing pins $BLSW\_H$ and $BLSW\_L$, and it is clear that balancing of $VCELL1$ stops first compared to the other two cells.

System partitioning between analog front end and digital circuit has been performed based on the system requirements. Different analog blocks have been identified and implemented with ideal circuits or as verilogA modules to check the complete functionality of the system. Individual

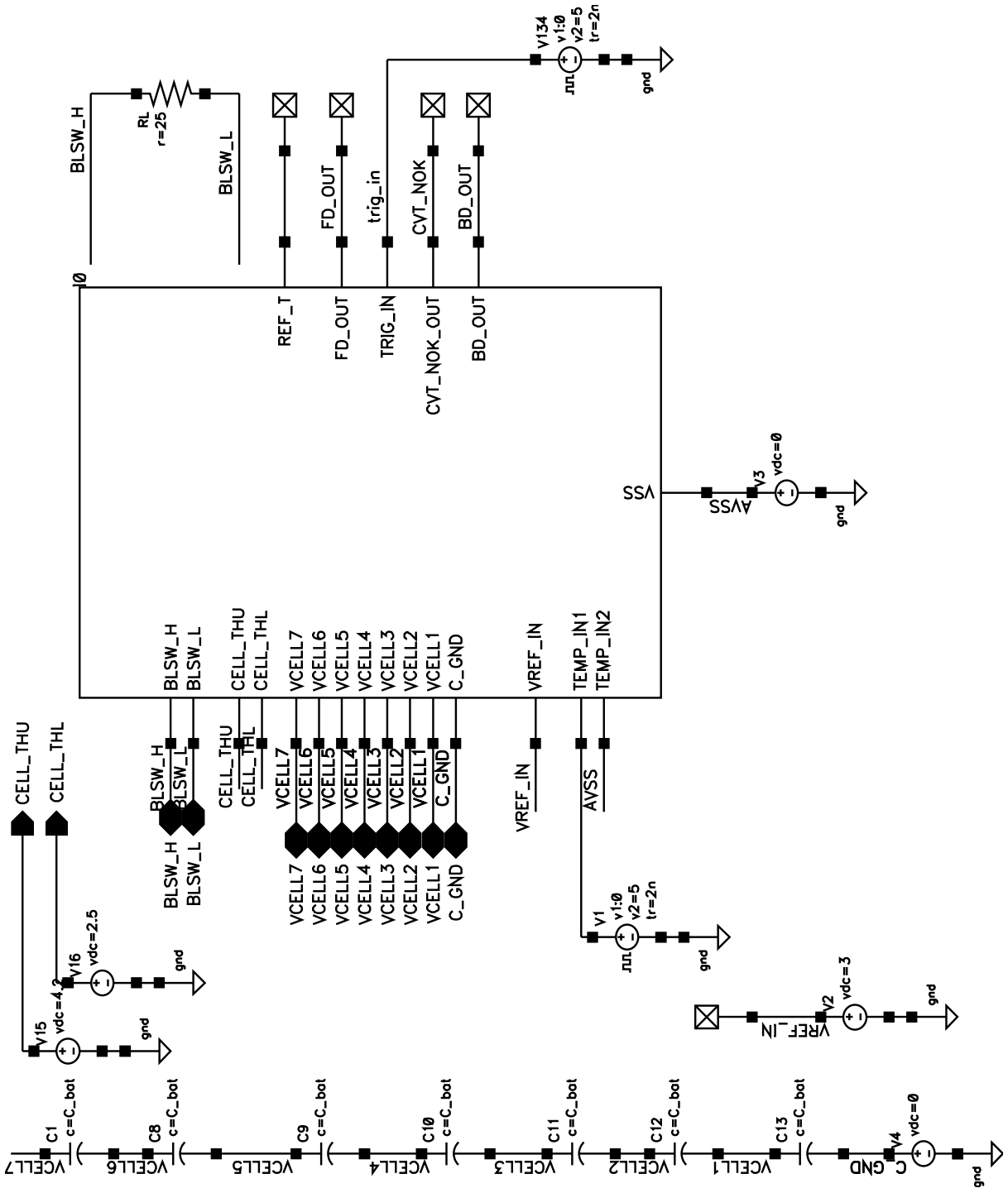

FIGURE A.1: System model for passive balancing

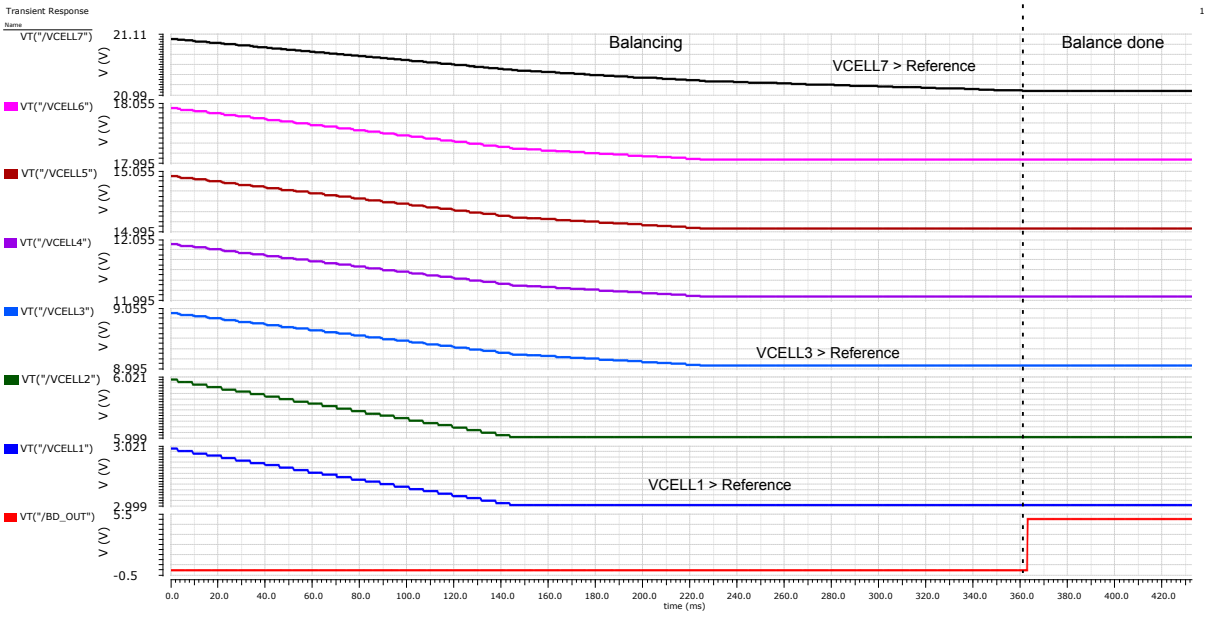

FIGURE A.2: Simulation results of passive balancing

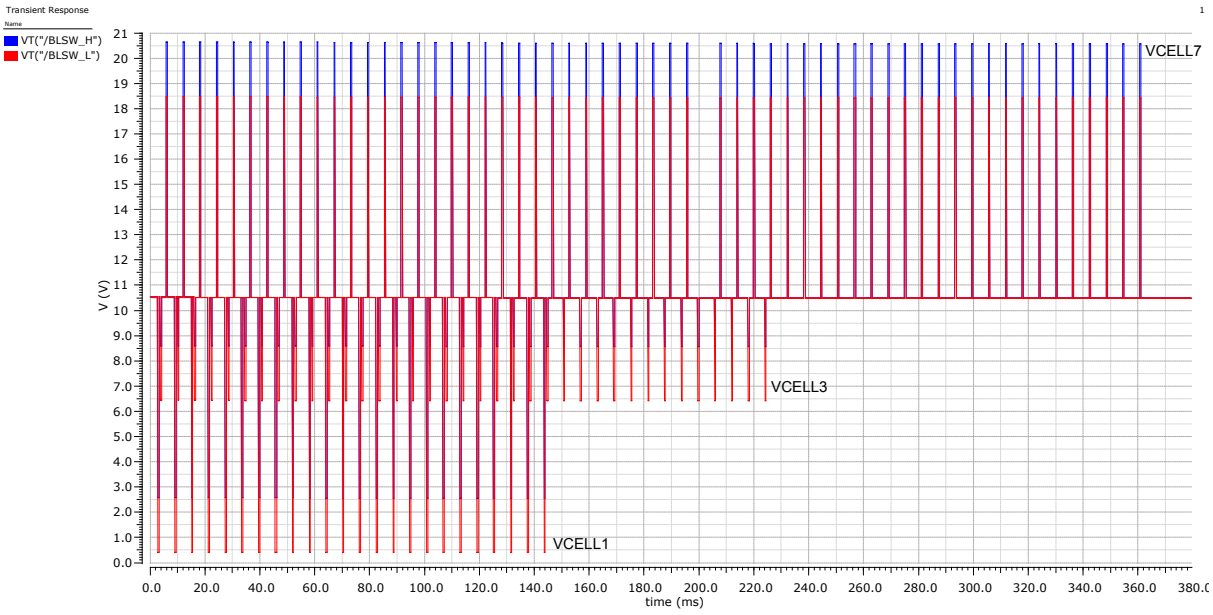

FIGURE A.3: Voltage across the balancing pins during passive balancing

block specifications are then derived from the system model. Fig A.4 shows the simulation setup of a active balancing system with analog and digital partitioning circuit.

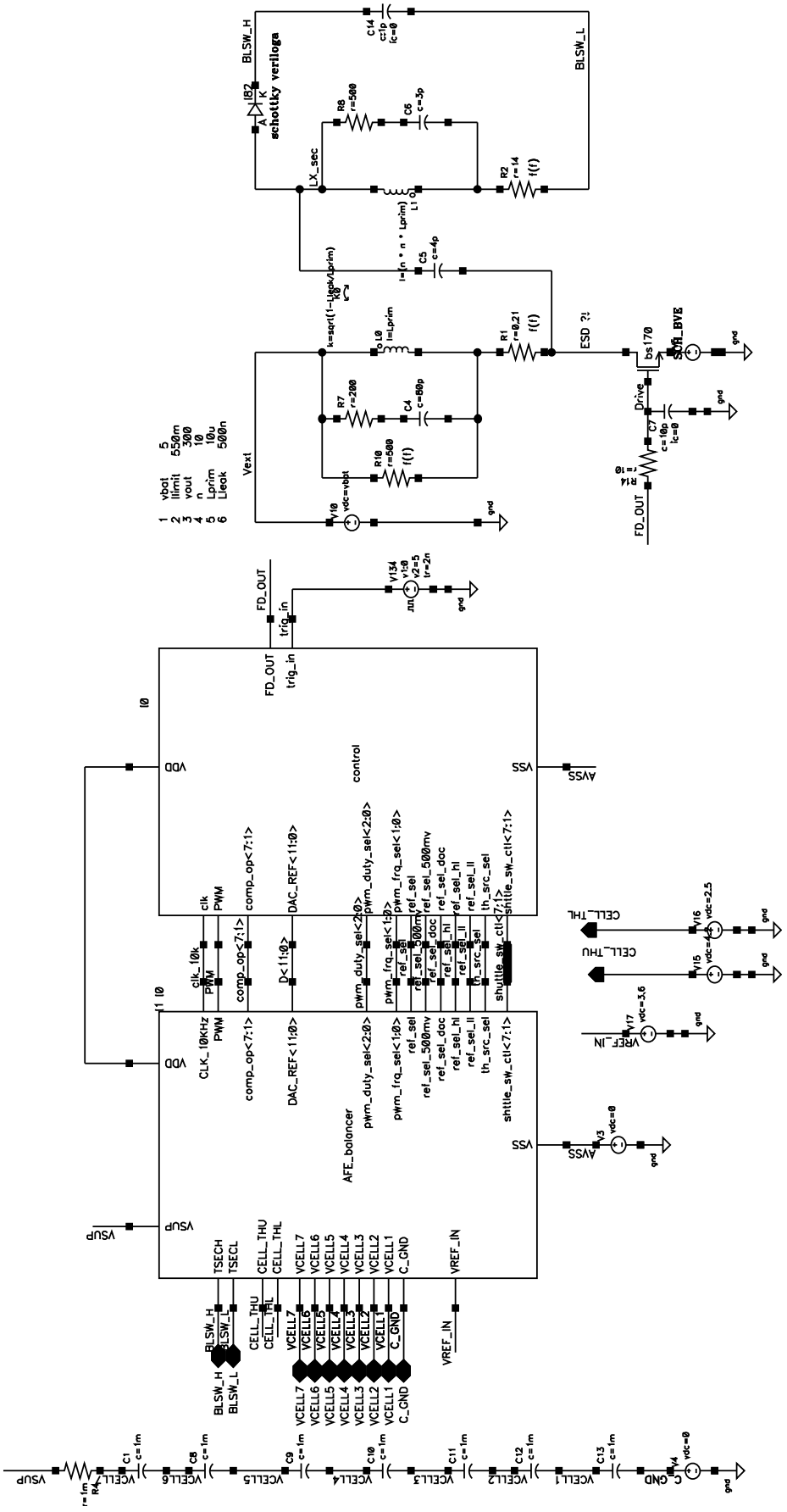

FIGURE A.4: System model for active balancing

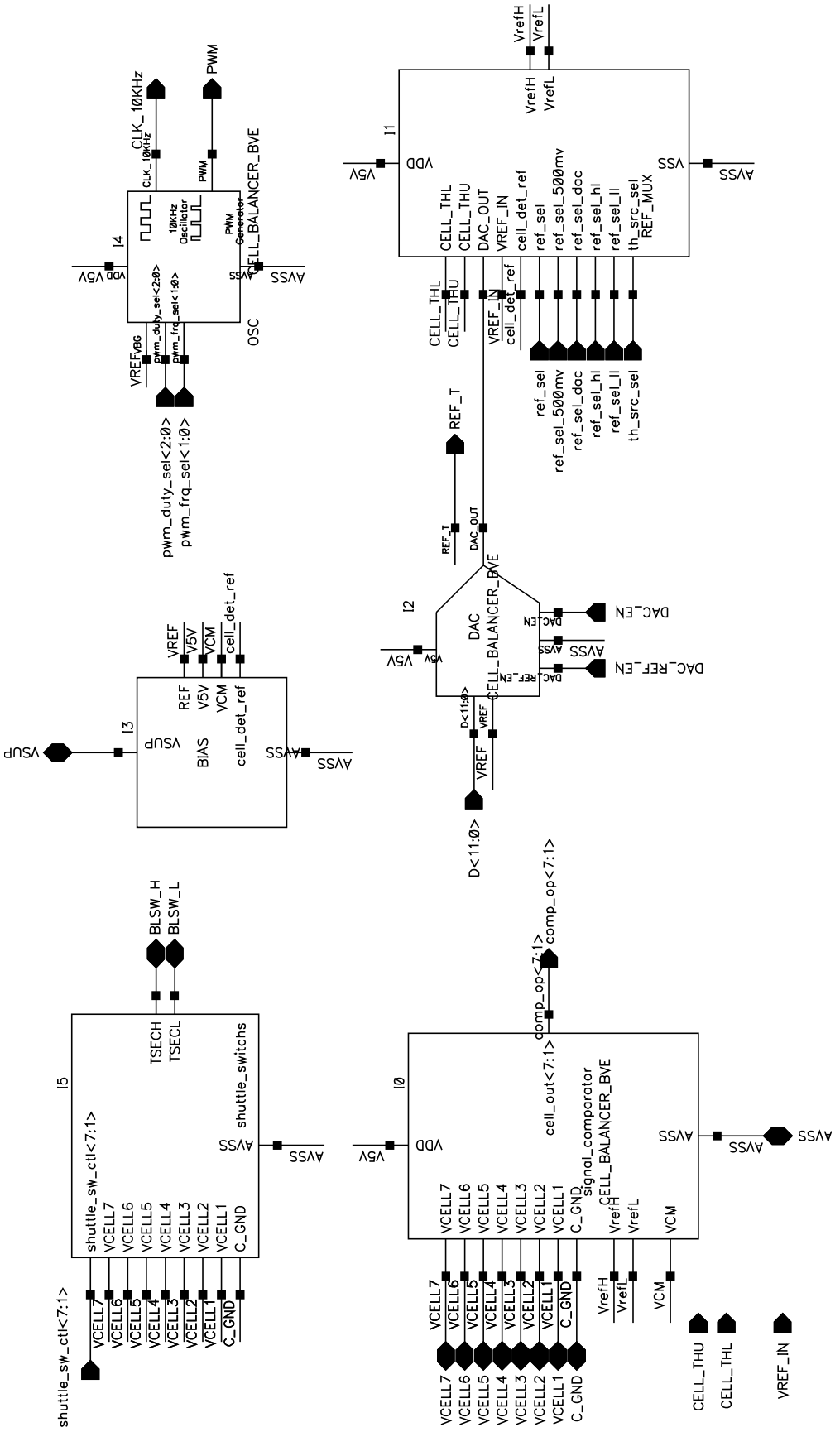

FIGURE A.5: Schematic of analog front partitioning with verilogA and ideal components

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Publications Related to this Thesis

[1] Gopinath, Anjali, Ravi Kumar Adusumalli, Veeresh Babu Vulligaddala, and M. B. Srinivas, "A Switched-Capacitor Amplifier with True Rail-to-Rail Input Range without Using a Rail-to-Rail Op-Amp," *In VLSI Design and 2017 16th International Conference on Embedded Systems (VLSID),2017 30th International Conference on* , Jan 7 2017 pp. 1329–334.

[2] V. B. Vulligaddala, R. K. Adusumalli, S. Singamala, and M. B. Srinivas, "A Digitally Calibrated Bandgap Reference with 0.06% Error for Low Side Current Sensing Application," *Submitted to IEEE Journal of Solid State Circuits, Received reviewer comments and currently working on them.*

[3] V. B. Vulligaddala, S. Singamala, S. Vernekar, R. K. Adusumalli, V. Ele, M. Brandl, and M. B. Srinivas, "A 7-Cell, Stackable, Li-ion Battery Monitoring and Active/Passive Balancing IC with In-Built Cell Balancing Switches for Electric and Hybrid Vehicles," *Submitted to IEEE Journal of Solid State Circuits.*

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