Study on Electronic Behaviour of Nanocrystalline Silicon Thin Film Transistors

THESIS

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by

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CERTIFICATE

This is to certify that the thesis entitled **"Study on Electronic Behaviour of Nanocrystalline Silicon Thin Film Transistors"** and submitted by **Ms. Prachi Sharma** ID No. **2011PHXF408P** for award of Ph.D. of the Institute embodies original work done by her under my supervision.

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To My Parents

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ABSTRACT

Thin film transistor (TFT) works as a switching element and plays an important role for the fabrication of highly functional active matrix (AM) backplanes for large area display applications such as active matrix liquid crystal displays (AMLCDs) and organic light emitting diodes (OLEDs). Nanocrystalline silicon (nc-Si:H) has recently achieved lot of interest over existing hydrogenated amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si) due to its superior properties which makes it suitable channel material for the fabrication of TFTs. The nc-Si:H material provides high mobility, better stability and high doping efficiency over a-Si:H. In addition, it provides high uniformity and low fabrication cost over poly-Si.

The staggered top-gate n-channel nc-Si:H TFTs structure show higher mobility, better electrical stability and high on-off current ratio. However, the top-gate nc-Si:H TFTs have several issues related to device performance and device stability, on which the thesis focuses. The main goal of the present work is to study the electronic behaviour of nc-Si:H TFT. This goal is achieved by developing device models, performing simulations and experimental work, which will be further useful for the device fabrication.

The nc-Si:H film is deposited on Corning glass 1737 substrate using e-beam PVD process to study the structural morphology of nc-Si:H film. The nc-Si:H film having different thicknesses (100nm, 150nm and 200nm) are deposited in the vacuum of 8×10^{-6} Torr with controlled beam current of 90mA and deposition rate of 1.2 Å/s. The results show that the optimized nc-Si:H film exhibits high conductivity of the order of 100 S/cm and small grain sizes in the range of 2-15nm. Therefore, this deposited nc-Si:H film is useful as the channel layer for the fabrication of top-gate nc-Si:H TFT and can provide high mobility and hence high on current. The outcome of this study is incorporated in device modeling of nc-Si:H TFT.

The performance of top-gate nc-Si:H TFT device depends on the material to be used for gate dielectric. Three approaches i.e. Ashby's approach, VIKOR and TOPSIS are used to choose best suitable material for the gate dielectric. Various dielectric materials such as

Si_3N_4, Al_2O_3, ZrO_2, Ta_2O_5 and HfO_2 are analyzed. Two performance indices based on four material indices are considered for this analysis. The investigation shows that Si_3N_4 is the best suitable material and can provide high drain current and less leakage current when used for gate dielectric in top-gate nc-Si:H TFT. In this thesis, Si_3N_4 is used as the gate dielectric for the device modeling of top-gate nc-Si:H TFT.

An analytical model for threshold voltage based on physical parameters such as gate insulator thickness, trap density, doping density and temperature, is proposed for top-gate nc-Si:H TFT. The results illustrated that the decrease in gate insulator thickness and the rise in temperature causes the decrease in threshold voltage. The results also show that the threshold voltage increases with increase in trap density and doping concentration. In addition, an analytical model for effective mobility is also proposed by incorporating the effect of grain boundaries. The results show that mobility due to parallel grain boundaries is higher as compared to mobility due to perpendicular grain boundaries. This proposed model is further used for calculating drain current. These proposed models provide the accurate estimation of drain current and thereby can be used for improving the device characteristics.

In order to improve the stability of top-gate nc-Si:H TFT, the effects of various physical parameters on threshold voltage shift are also analyzed in this thesis. The model proposed for threshold voltage shift shows that higher trap density, greater doping concentration and larger gate insulator thickness provides stability to top-gate nc-Si:H TFT device. The results also show that for smaller grain sizes ($D_G < 20$nm), threshold voltage shift decreases with decrease in grain size. However, for larger grain sizes ($D_G > 20$nm), no considerable threshold voltage shift is observed.

To further get the physical insights about the performance of nc-Si:H TFT, the effects of density of states (DOS) and channel length is analyzed using ATLAS 2D device simulator. The results show that the higher value of characteristic decay energy of channel material causes the degradation in transconductance and drain current. In addition, it is observed that transconductance degradation also occurs with the increase in channel length from 50 to 100μm which degrades the device performance.

The physical insight into the device characteristics and device non idealities reported in this thesis provides important step towards TFT backplane and for the production of high performance large area display devices.

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LIST OF SYMBOLS

μ_{eff}	Effective mobility
I_{DS}	Drain current
C_i	Gate insulator capacitance
W	Channel Width
L	Channel Length
V_{GS}	Gate voltage
V_T	Threshold voltage
V_{DS}	Drain voltage
R	Parasitic resistance
g_m	Transconductance
B	Full width half maxima
λ	Wavelength of X-rays
K	Scherrer constant
ρ_f	nc-Si:H film Resistivity
Rs	Sheet resistance of nc-Si:H film
t_{si}	nc-Si:H film thickness
σ_{eff}	Conductivity of nc-Si:H film
F	Functional requirements
G	Geometric parameters
M	Material indices
P	Performance of material
x_{ij}	Performance alternative of ith alternative with respect to the jth criteria
X	Decision Matrix
G_i	Maximum group utility
R_i	Minimum regret of the opponent
w_j	Weights of criteria
Q_i	i^{th} alternative of VIKOR
v	weight of maximum group utility
A^i	Alternative considered
S^*	Euclidean distance from the ideal solution
A^*	Ideal solution
S^-	Euclidean distance from negative ideal solution
A^-	Negative ideal solution
N_m	Normalized decision matrix
n_{ij}	Element obtained by the Euclidean normalization
v_{ij}	Product of n_{ij} and w_j
V	Weighted normalized matrix obtained from v_{ij}
Z_i	Relative closeness to the ideal solution

I_{PFO}	Generation current at zero electric field
I_{PF}	Leakage current due to Poole-Frenkel emission
β_{PF}	PF coefficient
V_{FB}	Flat band voltage
ε_i	Dielectric constant of gate insulator
t_i	Thickness of gate insulator
$\varepsilon_{nc\text{-}si}$	Permittivity of nc-Si:H channel layer
k	Boltzmann constant
T	Temperature
ε_o	Permittivity of free space
E_g	Energy band gap
$\varepsilon_{i,high\text{-}k}$	Dielectric constant of high-k material
ΔE_c	Conduction band offset
Q_{it}	Interface trapped charge
D_{it}	Interface charge density
C_{LF}	Capacitance measured at the onset of strong inversion at low frequencies
C_{HF}	Capacitance measured at the onset of strong inversion at high frequencies
φ	Electrostatic potential
ρ	Charge density
D_G	Average grain size
N_t	Density of trapping states
E	Electric field
q	Charge
E_s	Surface electric field
φ_s	Surface potential
N_a	Doping density
n_i	intrinsic carrier density
h	Planck’s constant
m_n^*	Effective electrons masses in nc-Si:H
m_p^*	Effective hole masses in nc-Si:H
E_i	Gate insulator electric field
D_{GB}	Size of grain boundary
D_d	Width of depletion region
ψ_B	Potential barrier across grain boundaries
R_G	Resistance of single grain
R_{GB}	Resistance of grain boundary
n_g	Number of grains
μ_G	Mobility of grain

μ_{GB}	Mobility of grain boundary
σ_G	Conductivity of the grain
σ_{GB}	Conductivity of the grain boundary
A	Cross sectional area of channel
R_T	Total resistance consist of grain and grain boundary resistances
N_d	Electron concentration in the bulk of the grain
n	Electron concentration in grain boundaries
μ_{perp}	Effective mobility in presence of perpendicular grain boundaries
N	Total carrier concentration in the strong inversion channel
n_t	Density of charged states at the grain boundaries
μ_0	Carrier mobility at the equilibrium condition
t_G	Thickness of single grain
t_{GB}	Thickness of grain boundary
A_G	Cross sectional area of grain
A_{GB}	Cross sectional area of grain boundary
$\sigma_{eff,perp}$	Equivalent conductivity of the channel due to perpendicular grain boundaries
$\mu_{parallel}$	Effective mobility in presence of parallel grain boundaries
$\sigma_{eff,parallel}$	Equivalent conductivity of the channel due to parallel grain boundaries
M	Mobility degradation factor
τ	Characteristic trapping time
β	Stretched-exponential exponent
E_C	Conduction band edge energy
E_V	Valence band edge energy
NTA	Conduction band edge intercept tail states density
NTD	Valence band edge intercept tail states density
NGA	Conduction band edge intercept deep states density
NGD	Valence band edge intercept deep states density
EGA	Peak energy of deep states as $E=E_C$
EGD	Peak energy of deep states as $E=E_V$
WTA	Characteristic decay energy of tail states as $E=E_C$
WTD	Characteristic decay energy of tail states as $E=E_V$
WGA	Characteristic decay energy of deep states as $E=E_C$
WGD	Characteristic decay energy of deep states as $E=E_V$

LIST OF ABBREVIATIONS

TFT	Thin Film Transistor
LCDs	Liquid Crystal Displays
OLEDs	Organic Light Emitting Diodes
a-Si:H	Hydrogenated Amorphous Silicon
poly-Si	Polycrystalline Silicon
PECVD	Plasma Enhanced Chemical Vapour Deposition
CMOS	Complementary Metal Oxide Semiconductor
nc-Si:H	Nanocrystalline Silicon
HWCVD	Hot Wire Chemical Vapour Deposition
DOS	Density Of States
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
ICP-CVD	Inductively Coupled Plasma Chemical Vapour Deposition
EBPVD	Electron-Beam Assisted Physical Vapor Deposition
FESEM	Field Emission Scanning Electron Microscopy
AFM	Atomic Force Microscope
XRD	X-Ray Diffraction
EDS	Electron Diffraction Spectroscopy
RCA	Radio Corporation of America
MCDM	Multi-Criteria Decision Making
MODM	Multi-Objective Decision Making
MADM	Multi- Attribute Decision Making
VIKOR	VlseKriterijumska Optimizacija I Kompromisno Resenje in Serbian
TOPSIS	Technique for Order Preference by Similarity to Ideal Solution

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Thin film transistor (TFT) is commonly used as a pixel addressing element and is the heart of large area electronic devices over the past few decades [1-3]. Large-area electronics involves various display applications such as liquid crystal displays (LCDs) and organic light emitting diodes (OLEDs). The aim of these applications is to spread electronic components over large area substrate at low fabrication cost.

For the production of new generation large displays, an active matrix addressing scheme is required for display panels where pixels are located at row and column interactions in order to minimize capacitive losses in column and row lines. This addressing scheme basically consists of two TFTs per pixel, of which one is operated under continuous gate bias and hence requires a high electrical stability.

For fabricating TFTs, various materials can be used as an active channel layer. The commonly used materials are hydrogenated amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si).

The main advantage of a-Si:H is the possibility of direct deposition over large area at relatively low temperature [4]. Plasma Enhanced Chemical Vapour Deposition (PECVD) is commonly used technique for the a-Si:H deposition over large area at low temperatures. The a-Si:H is an amorphous silicon alloy with incorporated hydrogen atoms. However the disadvantages of a-Si:H are low electron mobility and instability due

to low temperature PECVD process which causes the formation of defect states. The a-Si:H has electron mobility as low as 0.1-1 cm^2/Vs [5] and hole mobility is so low that the p-type devices are not used in any application.

Another material commonly used for the fabrication of TFT is poly-Si. It is having low hydrogen atoms in large grained silicon films and thus poly-Si is not called as "hydrogenated". The main advantages of poly-Si are high electron mobility and better stability. Since poly-Si is a network of randomly oriented crystalline grains interconnected by thin grain boundaries, the defects in poly-Si are concentrated in the grain boundaries whereas in a-Si:H materials they are uniformly distributed in the bulk. In case of poly-Si, large grains are preferred, as the larger grain size results in lesser grain boundaries across the channel. This results in lower density of defect states [6] in poly-Si, leading to lesser trapping of carriers at grain boundaries and hence higher mobility (~100 cm^2/Vs) [7] than a-Si:H materials. Poly-Si TFTs provide sufficient electron and hole mobility in n-type and p-type devices for CMOS (complementary metal oxide semiconductor) operation. The main problem with poly-Si is that the crystallization process requires a much higher temperature (usually higher than 300˚C) than the a-Si:H deposition temperature. In addition to this problem, poly-Si also suffers from poor spatial uniformity as random positioning of grain boundaries causes irregularity across the channel. This results in mobility degradation and threshold voltage non-uniformity over large area substrate [7, 8].

Nanocrystalline silicon (nc-Si:H) has been proven as the best alternative material over a-Si:H and poly-Si. The advantages of nc-Si:H over a-Si:H are better stability under bias and light stress and high field effect mobility due to the presence of higher silicon crystallites [9]. For top gated devices, field effect mobility (μ_{FET}) is in range of 40 cm^2/Vs [10] to 150 cm^2/Vs [11] and for bottom gate, it is in the range of 0.5-3 cm^2/Vs [12,13]. Due to the presence of lower hydrogen concentration, nc-Si:H have improved stability under bias and illumination stress [9] than a-Si:H. The benefits of nc-Si:H over poly-Si are low processing temperatures, low manufacturing cost and better uniformity [14]. Hot wire chemical vapour deposition (HWCVD) provide possibility of direct deposition of nc-Si:H at very low temperature over large area and at high deposition rates [14]. The

resulting nc-Si:H film consists of small silicon crystallites than poly-Si, with an average grain size of a few nanometers, embedded into a-Si:H. However, the main problem with nc-Si:H TFT is that it is affected from high drain leakage currents, i.e. off-current.

Table 1.1 illustrates the comparison between a-Si:H, poly-Si and nc-Si:H materials used for TFT fabrication.

1.2 TFT STRUCTURE

The TFTs consist of three electrodes (i.e. source, drain and gate), gate insulator, and thin semiconductor layer.

Based on the level of the gate electrode, the TFTs are divided into two types, top gate TFT and bottom gate TFT. In top gate TFT, the gate electrode is located above the semiconductor layer whereas in bottom gate TFT, the gate electrode is located below the semiconductor layer. These two types are further subdivided into coplanar and staggered devices, giving a total of four basic types of TFT structures. The architectural view of these structures is illustrated in Fig. 1.1. The term coplanar/staggered describes the location of source and drain electrodes with respect to the gate electrode. In coplanar case, the source and drain electrodes are located at the same side as the gate electrode while in staggered case, the source and drain electrodes are located at the opposite side to the gate electrode separated with the semiconductor layer. Further, TFTs can be characterized based on various device characteristics.

Table 1.1: Comparison between different materials used for the TFT fabrication [15, 16]

Parameters	a-Si:H	nc-Si:H	Poly-Si
Mobility	Low	Much higher than a-Si:H	High
Circuit type	NMOS	NMOS/PMOS	NMOS/PMOS
Stability	Less stable	More stable than a-Si:H	Stable
Uniformity	High	Potentially high	Poor
Cost	Low	Low	High

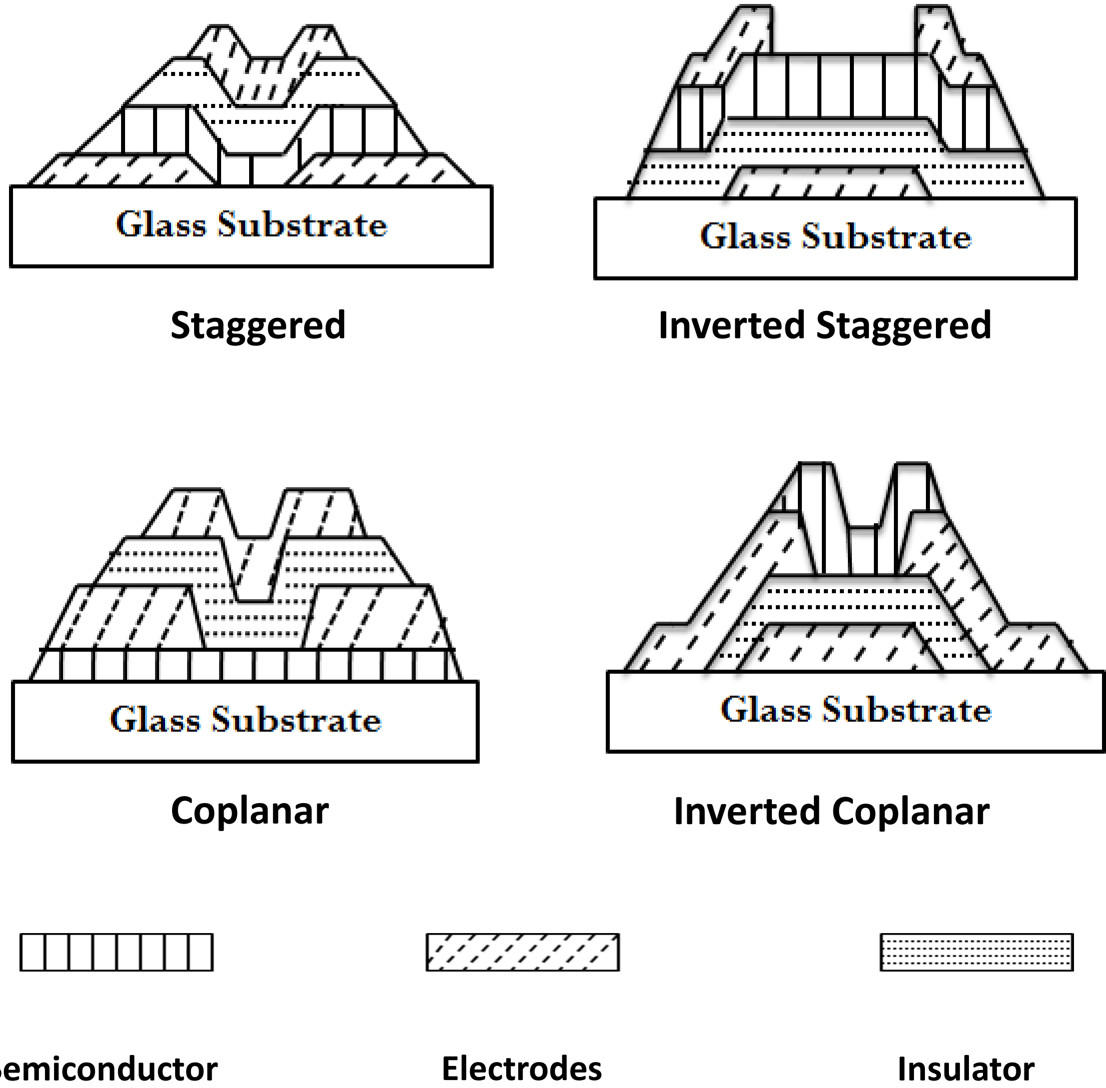


Fig. 1.1. Illustration of four basic types of TFT structures [17]

1.3 DEVICE CHARACTERISTICS

The performance of nc-Si:H TFT can be analyzed on the basis of various device characteristic parameters. These characteristic parameters plays important role in the evaluation of the performance of nc-Si:H TFT. These characteristic parameters are mentioned below:-

1.3.1 Density of States (DOS):

The low temperature process used for nc-Si:H deposition as well as the amorphous nature of non-crystalline substrate (like glass) lead to the formation of material having missing atoms. Deep defect states in the forbidden energy gap of the nc-Si:H are associated with these missing atoms, i.e. dangling bonds. Deep defect states are also associated with the deviation in bond length and angle which results in states below the conduction band, known as band tail states. The density of states (DOS) in nc-Si:H (as depicted in Fig. 1.2) is composed of two Gaussian distributed deep defect states (acceptor-like and donor-like deep states) and two exponentially distributed band tail states (acceptor-like and donor-like tail states). The DOS has a strong relevance on performance of nc-Si:H TFT. In this thesis, the effect of DOS is analyzed in chapter 6.

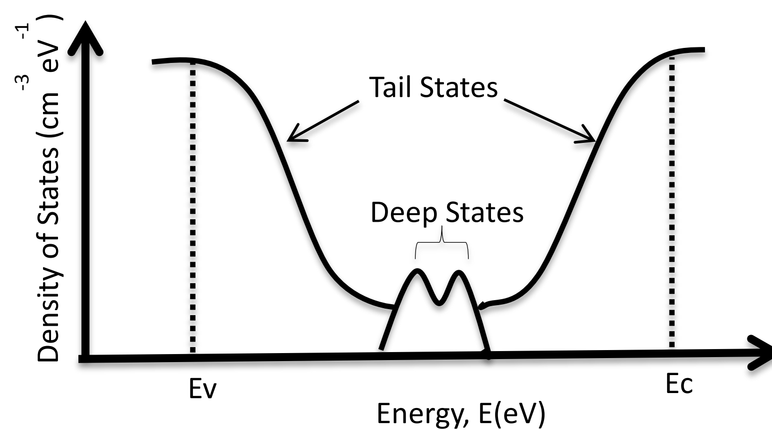


Fig. 1.2. Density of states within the band gap of nc-Si:H [18]

1.3.2 Threshold Voltage (V_T):

In nc-Si:H TFTs, there is a difference between threshold voltage and the ON voltage. Basically, the threshold voltage is defined as the gate voltage at which the inversion channel begin to appear within the grain and the ON voltage is defined as the knee of the characteristics. Accurate estimation of threshold voltage plays a crucial role for the TFT design as it decides the onset of conduction channel. In this thesis, the model for threshold voltage including the effects of various physical parameters is presented.

1.3.3 Effective Mobility (μ_{eff}):

Carrier mobility in a TFT channel is an important parameter that determines the performance of the device. Carrier mobility measures how fast the charge carriers respond to an external electric field. In TFT, various scattering mechanism affect the carrier mobility, such as surface roughness scattering, lattice scattering and imperfection scattering [5]. So, in this thesis for device modeling, effective mobility term is used to incorporate these effects. Using Mathiessen's rule, the effective mobility in the TFT channel layer can be written as

$$\frac{1}{\mu_{eff}} = \sum_{i=1}^{k} \frac{1}{\mu_i} \qquad \text{where } i = 1,2,3\ldots ,k \tag{1.1}$$

1.3.4 Drain Current (I_{DS}):

TFT uses intrinsic layer as a channel layer which causes high DOS in the band gap, therefore in order to operate TFT under inversion region, high gate voltage is required as compared to Metal-oxide-semiconductor field-effect-transistor (MOSFET), for the adequate generation of drain current. In two different regions of operation, the drain current is given by:

$$I_{DS}(linear) = \mu_{eff} C_i \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^{\;2}}{2}\right] \tag{1.2}$$

$$I_{DS}(saturation) = \mu_{eff} C_i \frac{W}{2L}(V_{GS} - V_T)^2 \tag{1.3}$$

where μ_{eff} is the field effect mobility, C_i is the gate capacitance, W and L are the width and length of the TFT, V_{DS} is drain voltage, V_{GS} and V_T are gate and threshold voltage respectively.

1.3.5 Parasitic Resistance (R):

In top gated staggered nc-Si:H TFT, series resistance of active layer, series resistance of contact layers and contact resistance between metal electrode and source/drain contacts form the parasitic resistance [19] which also affects the performance of the nc-Si:H TFT [20]. These resistances are shown in Fig. 1.3. As these resistances are in series, parasitic resistance is given as:

$$R = R_{ch} + R_i + R_s + R_c \tag{1.4}$$

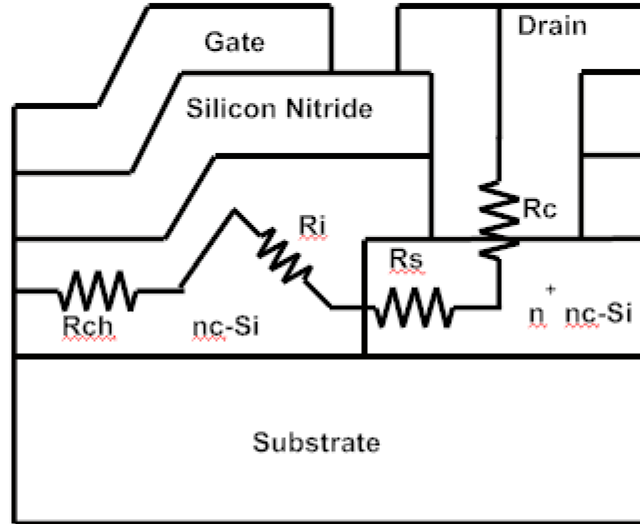


Fig. 1.3. Parasitic resistance in top-gated staggered nc-Si:H TFT

1.3.6 Transconductance (g_m):

The transconductance can be obtained from the differentiation of device transfer characteristics and is defined as

$$g_m = \frac{dI_{DS}}{dV_{GS}} \tag{1.5}$$

In this thesis, analyses of transconductance at different channel lengths are investigated using SILVACO device simulator. This analysis is presented by considering the saturation region (V_{DS}=10V) because at high drain bias, the effect of parasitic resistance is more prominent as compared to linear region (low V_{DS}) which in turn degrades the transconductance and causes instability in the device performance.

1.3.7 Threshold Voltage Shift (ΔV_T):

The TFTs suffers from threshold voltage shift under bias stress due to two possible instability mechanisms [21], first one is charge trapping in the gate dielectric and/or in the interface between the gate dielectric and channel and second one is defect state creation in the active layer which causes the increase in total density of defect states and therefore decreases the drain current of TFT device.

1.4 DEVICE SIMULATION

In this thesis, analysis of nc-Si:H TFT is done using ATLAS from SILVACO Corporation. ATLAS simulator predicts the characteristics of the particular device under bias conditions on the basis of their physical structure. This is accomplished by approximating the device operation onto a grid of two or three dimensions. This grid comprises of various grid points known as nodes. The transport of the carriers through the device structure can be simulated by applying Maxwell differential equations onto this grid. This implies that the performance of the device can now be demonstrated in DC, AC or transient operation modes. The fundamental point of preference of physical-based device simulator is that it is much faster and less expensive than carrying out the experiment practically. It additionally gives data related to device characteristics that is hard to quantify. In ATLAS device simulator, the problem which needs to be simulated is stating by defining physical structure of the device, physical models to be used for simulation and the bias conditions under which electrical characteristics need to be simulated.

In this thesis, DOS model, which is available in TFT module in ATLAS tool package, is used to extract the density of defects present in the band gap of nc-Si:H. Further, the two

dimensional nc-Si:H TFT structure is virtually fabricated and electrical characteristics are extracted using ATLAS device simulator.

1.5 RESEARCH MOTIVATION AND OBJECTIVES

The nc-Si:H TFTs have bought evolution in the market of large area electronics and leading growth in the utility of new generation displays like LCDs, OLEDS over past few decades. To maintain the development and growth of large area electronics, the production of high performance nc-Si:H TFT is essential.

In past, various techniques have been used for the deposition of nc-Si:H film however each of these techniques has some limitations related to temperature, RF power and hydrogen dilution. Therefore alternative technique for the deposition of nc-Si:H film suitable for top-gated nc-Si:H TFT device needs to be analyzed.

The rapid performance improvement in flat panel displays has been achieved by scaling down the size of TFT. However the reduction in size of TFT and thus of gate dielectric causes two major problems that are leakage current and reliability [10]. The SiO_2 material has been used as a gate dielectric for decades due to its remarkable properties. However prevention of leakage current requires a suitable gate dielectric that must have high dielectric constant must be greater than SiO_2 (~3.9). Various high-k dielectric materials are being investigated for the gate insulator of nc-Si:H TFT. As each of the high-k material possess some practical challenges, therefore selection of best high-k material is necessary in order to improve nc-Si:H TFT device performance.

Many theories and models have been presented for explaining the electrical properties of TFTs based on different conduction mechanism of carriers through nanocrystalline film. But each of these models has their own conditions of validity and also has limited range of applicability. As technology evolves, further model improvement is needed to describe the effect of various physical parameters like temperature, doping density, trapping-state density and grain size on the threshold voltage and therefore on characteristic of the device.

New generation active matrix displays such as OLEDs requires TFT with high stability and therefore the drain current degradation are not acceptable. Although various

researchers claimed that nc-Si:H TFTs have better stability than a-Si:H TFT yet electrical instability mechanisms for top-gate nc-Si:H TFT have not been deeply analyzed.

Thus the work presented in this thesis belongs to the nc-Si:H based TFT. This work aims to understand the electronic behavior of nc-Si:H TFTs. Thus in order to fulfill the goal of the research, the **objectives** of the work was divided into following points:

- To deposit and analyze the structural morphology of nc-Si:H film.
- To select best high-k material as a gate insulator for nc-Si:H TFT.
- To develop a physically-based analytical model for threshold voltage, effective mobility and drain current for nc-Si:H TFT.
- To analyze various physical effects on the carrier transport over wide range of channel length, temperature, doping density, trapping-state density and grain size using device modeling and simulation.
- Analysis of the threshold voltage shift and the density of states behavior under prolonged gate bias stress.

1.6 ORGANISATION OF THESIS

This thesis is divided into **seven** chapters. The organization of this thesis is as follows:

Chapter 1 starts with an introduction and overview of TFT with the focus on materials commonly used for its channel layer. The next section provides the brief description of various structures and the characteristics of TFT. It is followed by the motivation and objectives of this research. Last section of this chapter explains the structure of the thesis.

Chapter 2 describes the detailed literature review of nc-Si:H based TFT. This chapter also includes the various models presented in past to explain the conduction mechanism of nc-Si:H TFT. It is followed by the review of the mechanisms which causes the electrical instability in TFT.

Chapter 3 emphasize on the study of nc-Si:H channel material. In this chapter, the e-beam evaporation technique used for the deposition of nc-Si:H film is explained. It is followed by various characterization results which validates the formation of high quality nc-Si:H film.

Chapter 4 describes the material selection methodology for gate dielectric in nc-Si:H TFT. Various possible materials for the gate dielectric of top-gate nc-Si:H TFT and their material properties like dielectric constant, bandgap, conduction band offset and interface trap density are taken into consideration and by using Ashby's, VIKOR and TOPSIS approaches, the most appropriate material is selected.

Chapter 5 focuses on the analytical modeling of top-gated nc-Si:H TFT. The model for threshold voltage incorporating various physical parameters like temperature, doping density, trapping-state density and grain size is presented in this chapter. This is followed by the proposed model for effective mobility and drain current.

Chapter 6 deals with the non-idealities in nc-Si:H TFT. An analytical model for threshold voltage shift is described in next section. It is followed by the transconductance degradation analysis performed using ATLAS two-dimensional device simulator. The analysis is presented in the next section that realizes the effect of channel length and channel material quality on transconductance and thereby on device performance.

Chapter 7 finally concludes the results and contributions of this research and provides suggestions for future work related to the nc-Si:H TFTs.

CHAPTER-2

THIN FILM TRANSISTOR: LITERATURE REVIEW

2.1. INTRODUCTION

The performance of TFT depends upon the various process parameters used during the fabrication of TFT and also on the conduction and instability mechanisms that occurs under electrical stress. So it is important to look into all these aspects.

When the nc-Si:H film is deposited over the amorphous substrate like glass then its crystallinity is not very high in the initial growth phases because the nc-Si:H is usually grown up in the form of cone-shape that is from bottom to top. The grain size and therefore the crystallinity increases with the increase in nc-Si:H film thickness [22]. This structural difference in top and bottom layers of nc-Si:H film plays crucial role in nc-Si:H TFT designing. In case of bottom-gate structure, the device performance depends on the bottom layer of nc-Si:H film where the channel is formed as compared to top-gate TFT, where the channel is located in highly crystalline part at the top of nc-Si:H film [23]. Owing to this, the top-gate nc-Si:H TFT provides high mobility and also the better performance as compared to bottom-gate TFT.

For this reason, top-gate structure of nc-Si:H TFT is considered in this work. The first section of this chapter explains the important outcomes and the research carried till date in the area of nc-Si:H top-gate TFT. In the second section, models for conduction in nc-Si:H TFT, given by various researchers are reviewed. In third section, the mechanisms which cause the electrical instability in TFT are explained in detail.

2.2. FABRICATION OF nc-Si:H BASED TFTs

The key findings of published research in the area of top-gate nc-Si:H TFT are as follows:

R.B.Min et.al. [24] discussed that the nc-Si:H film in ideal condition grow quickly, provide highest mobility in minimum thickness and provide lowest conductivity under electrical stress. The lowest conductivity at room temperature in nc-Si:H film is achieved as low as conductivity of crystalline silicon which is around 10^{-7}S/cm. They proposed that as the film thickness increases from 50 to 350nm, the magnitude of film conductivity increased by the order of five. This is due to the increase in magnitude of electron field effect mobility by order of two and also increase in carrier density. The increase of electron mobility with the increase in film thickness is the key point behind the use of top-gate structure of nc-Si:H TFT to avail benefit of carrier mobility which is premier at the top level of the nc- Si film. However authors didn't present any information regarding hole mobility. Authors also discussed that in case of TFT, the leakage current is basically the conduction current which is related to channel layer under flat band situation. Therefore it is necessary to reduce the electron carrier density present in channel in neutral condition. In TFT, the leakage current must be lowest for its possible application as switch, to provide voltage stability or in CMOS circuits to provide minimal power consumption. They have used PECVD technique for the fabrication of top-gate coplanar TFT and proposed that the compensation doping, gettering of water and oxygen content from mixture of base gases, or addition of chlorine content during film deposition can help in reducing the electron carrier density.

I.C. Cheng et. al. [25] presented top-gate staggered nc-Si:H TFT deposited using PECVD at low temperature of about 150ºC. They proposed that the quality of the nc-Si:H material can be measured by the mobility of carriers present in the nc-Si:H channel in saturation condition as it directly reveals the capability of nc-Si:H material because saturation current is not influenced by the trapping and detrapping of charge carriers in gate dielectric. In addition to this, there is insufficient activity of doped layer under saturation condition and therefore saturation mobility reflects the lower limit of nc-Si:H channel capability.

In later research [26] they proposed that the structural formation of nc-Si:H film is based on various parameters like hydrogen dilution, temperature during deposition, nc-Si:H film thickness and type of the substrate. They used both glass and plastic (Kapton E polymide) substrates for their study and fabricated both p-type and n-type staggered top-gate TFT devices on a single substrate using PECVD. They have achieved sufficient mobilities for realizing CMOS circuit on plastic but fail to achieve low off current and less threshold voltage shift due to poor quality of dielectric and the interface between gate dielectric and channel. They reported that for the better performance of the device, the substrate must have low thermal expansion coefficient, high thermal stability, low surface roughness, high chemical stability and transition temperature of glass, low permeability by oxygen and water and low shrinkage capability to avoid misalignment during photolithography.

C.H.Lee et. al. [27] proposed ambipolar transistor which worked alternatively as p-type and n type transistor by the application of negative and positive gate voltages respectively. The fabrication of ambipolar transistor is not reported earlier as it is difficult to realize high quality contact between metal and semiconductor and also to deposit high quality nc-Si:H film. They have used nc-Si:H/Cr stack as source-drain contacts in place of n+ nc-Si:H for the fabrication of top-gate TFT. They proposed that hydrogen atoms cleans the surface of Cr electrodes, during the initial phase of nc-Si:H film formation and this leads to highly crystalline nc-Si:H film and therefore Cr silicidation provides lower electron as well as hole injection barrier. They reported that at higher gate voltages, leakage current increases exponentially for both p- and n-type TFTs, which validates ambipolar operation. This behavior is due to accumulation of holes and electrons in n-channel and p-channel under reverse gate voltages through injection from Cr drain, this discriminates TFT with Cr silicide contacts from TFT with n^+ nc-Si:H contacts.

C.H.Lee et. al. [11] presented the low temperature (i.e. 260ºC) fabrication of top-gate nc-Si:H TFT through 13.56 MHz PECVD by the use of silane diluted with hydrogen. They propose that the hydrogen dilution of silane controls the crystallinity of nc-Si:H layer [28] however, this increase the level of oxygen impurity in nc-Si:H film and at the grain boundaries. The high concentration of hydrogen atoms in the silane plasma is the main

requirement for the deposition of low temperature highly crystalline nc-Si:H film. They reported that low dark conductivity can be achieved by providing hydrogen chemical cleaning during the deposition of nc-Si:H film.

In later research C.H. Lee et. al. [29] proposed that the field effect mobility (μ_{FE}) is the ratio of free charge carriers in extended energy states, n_{band}, to the total number of induced charge carriers (which comprises of trapped carriers, n_{trap} and free carriers) times the band mobility μ_{band}, and is expressed as:-

$$\mu_{FE} = \left[\frac{n_{band}}{n_{band} + n_{trap}} \right] \mu_{band} \tag{2.1}$$

The grains of nc-Si:H are enclosed by amorphous grain boundaries. Low temperature process provides low oxygen content in nc-Si:H film and thereby reduces probability of defect state creation at grain boundaries. This avoids band bending and thereby offers high mobility. This validates that low temperature is necessary for the deposition of highly crystalline nc-Si:H film.

J. H. Park et. al. [22] presented the fabrication of top-gate nc-Si:H TFT using inductively coupled plasma (ICP) CVD with different channel thicknesses at the temperature of 180 ºC. They proposed that ICP-CVD reduces the surface damage usually caused by ion bombardment by generating the remote plasma without causing the bombardment of ions. This reduction in surface damage provides highly crystalline growth of nc-Si:H film and avoids amorphization in Si deposition surface. They proposed that grain size increases with increase in film thickness because of the growth of nc-Si:H layer in form of cone shape i.e. from bottom to top. In addition to this, the surface roughness also increases with increase in nc-Si:H thickness. The formation of isolated grains of nc-Si:H occurs during the initial phase but these grains competed with the nearby grains which results into the formation of grain boundaries due to collisions between the grains. These grain boundaries cause the increase in surface roughness. They reported that the new in-situ process that is used for nc-Si:H TFT fabrication provides reduction in off-current without sacrificing on-current. This is due to the suppression in conduction of off-current through trap-states.

C.H.Lee et. al. [30] proposed that the top-gate nc-Si:H TFT provides better stability and high on/off ratio as compared to bottom-gate nc-Si:H TFT. The high stability of top-gate nc-Si:H TFT makes it highly suitable device for display application like pixel driver in OLED to maintain low line voltages. They have used silicon nitride as the gate dielectric for the fabrication of both top-gate and bottom-gate n-channel nc-Si:H TFT because silicon nitride provides high reliability, high breakdown field and also allow processing at low temperature.

D.W.Kang et al. [31] also presented the effect of film thickness on the nc-Si:H TFT performance. They proposed that as thickness of nc-Si:H film increases, the field effect mobility also increases due to increase in grain size. However this causes the increase in leakage current. According to them, this increase in leakage current is due to the reduction in total resistance present in TFT.

The increase in grain size causes the reduction in resistivity which in turn reduces the channel resistance and also the total resistance of nc-Si:H TFT. They proposed that sheet resistance and contact resistance of drain/source can be reduced by the activation of dopants using excimer laser annealing.

H.J.Lee et al. [32] reported the mechanisms that are responsible for gate leakage current. They proposed that at high gate and low drain bias, thermal emission of charge carriers that are trapped in grain boundary regions is responsible for leakage current whereas Poole-Frenkel emission mechanism in drain depletion state is responsible at high gate bias and high drain bias. Under low gate bias, ohmic conduction via bulk channel layer is responsible mechanism for leakage current. They presented that high leakage current causes loss of signal in pixels and also increases the power consumption of the driving circuitry. They proposed that reduction in leakage current can be attained either by using offset-gated configuration or by employing lightly doped drain regions.

I.C.Cheng et. al. [33] reported the effect of contact resistance on the performance of staggered top-gate nc-Si:H TFT and for this study they have fabricated both n+ and p+ nc-Si:H TFT at various channel lengths. The total resistance of nc-Si:H TFT comprises of channel resistance R_{CH} and the contact resistance R_o. They reported that $R_o \times W$ decreases with increase in gate overdrive voltages. They also proposed that if the channel

length of n-type TFT is below 10µm and of p-type TFT is below 25µm, then the drain current at V_{DS}=10V is restricted by the contact resistance.

Y.Djeridane et.a al. [34] proposed that during the growth of nc-Si:H film over the amorphous like substrate, a residual amorphous phase called as incubation layer is formed at the interface between substrate and the film. This incubation layer can be avoided by controlling the deposition plasma parameters. They also reported that silicon nitride provides better stability when used as gate dielectric for the fabrication of n-type nc-Si:H TFT. However, for fabrication of p-type TFT they have used SiO_2 as a gate dielectric due to its wide bandgap, large conduction and valence band off-set.

A. Subramaniam et. al. [35] reported that ambipolar operation can be achieved by reducing the oxygen concentration in the nc-Si:H channel. The ambipolar transistor allows the production of complementary inverter using single type device. They fabricated both n-type and p-type top gate staggered nc-Si:H TFT at submicron dimensions with no short channel effects.

Table 2.1 summarized nc-Si:H top-gate TFT device dimensions and performance parameters of the published experimental works. So based on the literature review, it is clear that n-channel nc-Si:H TFT provides higher mobility compared to p-channel TFT and staggered top-gate structure of TFT provides better stability and high on-off current ratio. So in this thesis, staggered top-gate n-channel nc-Si:H TFT is considered and investigated for its electrical behavior.

Table 2.1: Experimental published data for top-gate nc-Si:H TFT

Reference	**Esmaeili et. al. [23]**	**Cheng et. al. [25]**	**Min et. al. [24]**	**Lee et. al. [27]**
Gate contact	Al 300nm	Al 200nm	Al 200nm	Al 300nm
Source/ Drain Contact layer	-	Cr 50nm	Cr 50nm	Cr 50nm
Doped layer	n+ nc-Si 80nm	n+ nc-Si 60nm	n+ nc-Si:H 60nm	n+ a-Si :H 50nm
Process nc-Si	PECVD 50nm	VHF PECVD 50nm	VHFPECVD 300nm	PECVD 100nm
Dielectric	SiO_2 270nm	SiO_2 300nm	SiO_2 370 nm	a- SiO_x
Temperature	350 ºC	150 ºC	150 ºC	260 ºC
Width to Length ratio (W/L)	180µm /45µm	200µm /30µm	240µm /40µm	W= 200µm L= 20, 50, 100, 200 µm
Structure Type	Top-gate Coplanar	Top-gate Staggered	Top-gate Staggered	Top-gate Staggered
Substrate	Glass	Glass, Kapton	Glass	Glass
Mobility	11 cm^2/Vs (at $V_{ds} = 10V$)	Glass $30cm^2/Vs$ Kapton $23cm^2/Vs$	$40cm^2/Vs$	100-$150cm^2/Vs$
Leakage current	$1 \times 10^{-12}A$	-	-	-
Sub-threshold Slope	2.5V/dec	-	-	0.22-0.25V/dec
On/off Ratio	10^8 at V_{DS} =10V	-	-	10^6
Threhold voltage	2.5V (at $V_{DS} = 0.1$ V)	-	-	1.5-2V
Threshold voltage shift	-	-	-	-
Year	2002	2002	2002	2005

Reference	**Fonrodona et. al. [36]**	**Cheng et. al. [26]**	**Kamei et. al. [28]**	**Fonrodona et. al. [37]**
Gate contact	Al Thermally evaporated	Al 300nm	Sputtered Al 300nm	Al Thermally evaporated
Source/Drain contact layer	-	-	-	-
Doped layer	n+ or p+ a-Si :H 150nm	Cr 100nm	Cr 100nm	n+ nc-Si 150nm
Process nc-Si	HWCVD 200nm	PECVD 100nm	RF PECVD 300nm	HWCVD 200nm
Dielectric	SiO_2 100nm	a- SiO_x 300nm	SiO_2 300nm	SiO_2 100nm
Temperature	200 ºC	260 ºC	150ºC	200ºC
Width to Length ratio (W/L)	20µm /60µm	200µm /50µm	200µm /50µm	100µm /20µm
Structure	Top-gate Coplanar	Top-gate Staggered	Top-gate staggered	Top-gate coplanar
Substrate	Glass covered with 200nm APCVD deposited SiO_2	Glass	Glass	Glass covered with APCVD deposited SiO_2
Mobility	$22cm^2/Vs$	$150cm^2/Vs$	$450cm^2/Vs$	$11.5\ cm^2/Vs$
Leakage current	-	-	-	-
Sub-threshold Slope	0.5 V/dec	0.3 V/dec	0.6 V/dec	0.34 V/dec
On/off Ratio	$>10^6$	10^7	10^6	-
Threshold voltage	6.3 V	2V	2V	5.70V
Threshold voltage shift	-	-	-	0.5V at V_{GS} = -10V
Year	2005	2005	2006	2006

<table>
<tr><th>Reference</th><th colspan="3">Lee et. al.
[30]</th><th>Lee et. al.
[29]</th><th>Kang et. al.
[31]</th><th>Subramaniam et. al. [35]</th></tr>
<tr><td>Gate contact</td><td colspan="3">Al</td><td>Al
300nm</td><td>Al
300nm</td><td>Al
Liftoff</td></tr>
<tr><td>Source /Drain contact layer</td><td colspan="3">Cr</td><td>n+ nc-Si</td><td>n+ nc-Si</td><td>Cr or Ti</td></tr>
<tr><td>Doped layer</td><td colspan="3">n+ nc-Si:H
60nm</td><td>-</td><td>-</td><td>n^+ nc-Si
100nm</td></tr>
<tr><td>Process nc-Si</td><td colspan="3">PECVD
80nm</td><td>ICP-CVD
60, 90, 130nm</td><td>ICP-CVD
60, 90, 130nm</td><td>PECVD
250nm</td></tr>
<tr><td>Dielectric</td><td colspan="3">a-SiN_x:H
300nm</td><td>SiO_2
150nm</td><td>SiO_2
150nm</td><td>SiO_2</td></tr>
<tr><td>Temperature</td><td colspan="3">240 ºC</td><td>180ºC</td><td>-</td><td>250˚C</td></tr>
<tr><td>Width to Length ratio (W/L)</td><td colspan="3">200µm/50µm</td><td>20µm/10µm</td><td>20µm/10µm</td><td>20µm/10µm</td></tr>
<tr><td>Structure type</td><td colspan="3">Top-gate</td><td>Top-gate</td><td>Top-gate
Staggered</td><td>Top-gate
Stagggered</td></tr>
<tr><td>Substrate</td><td colspan="3">Glass</td><td>Glass</td><td>Glass</td><td>p-type silicon</td></tr>
<tr><td>Mobility Resistivity</td><td colspan="3">0.5 cm^2/Vs
at V_{DS}=1V
0.6 cm^2/Vs at V_{DS}=10V</td><td>69 cm^2/Vs
with 60nm film
99 cm^2/Vs
with 90nm film</td><td>26cm^2/Vs
with 60nm film
77cm^2/Vs
with 90nm film
119cm^2/Vs
with 130nm film</td><td>-</td></tr>
<tr><td>Leakage current</td><td colspan="3">$6.75x10^{-14}$A
at V_{DS} =0.1V
$2x10^{-11}$A
at V_{DS} =10V</td><td>At V_{GS}= -4.4 V
$8.4x10^{-11}$ A
with 60nm film
$3.6x10^{-10}$A
with 90nm film</td><td>7.2 x 10^{-10} to
1.9 x 10^{-8}A
at V_{GS}=-4.4V</td><td>-</td></tr>
<tr><td>Sub-threshold Slope</td><td colspan="3">0.82V/dec
at V_{DS} =1V
0.93V/dec
at V_{DS} =10V</td><td>217mv/dec
with 60nm film
230 mv/dec
with 90nm film</td><td>-</td><td>-</td></tr>
<tr><td>On/off Ratio</td><td colspan="3">10^6
at V_{DS}=1V
$2x10^5$
at V_{DS} =10V</td><td>10^7
at V_{DS} = 0.1 V</td><td>10^4
at V_{DS}=0.1V</td><td>-</td></tr>
<tr><td>Threshold Voltage</td><td colspan="3">2.4 V
at V_{DS}=1V
2.7 V
at V_{DS} =10V</td><td>2.2 V
with 60nm film
2.3 V
with 90nm film</td><td>-</td><td>-</td></tr>
<tr><td rowspan="2">Threshold voltage shift</td><td>V_{DS}=1V</td><td>V_{DS}=10V</td><td>V_{GS}</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td></tr>
<tr><td>0.35
0.77
1.52</td><td>0.34
0.57
1.23</td><td>20V
30V
40V</td></tr>
<tr><td>Year</td><td colspan="3">2007</td><td>2007</td><td>2008</td><td>2012</td></tr>
</table>

2.3. CONDUCTION MODELS:

Various device models have been presented in past for explaining the electrical behavior of nc-Si:H TFTs. This section presents the key assumptions, their conditions of validity and range of applicability of important analytical models of nc-Si:H TFTs.

Dosev et. al. [38] reported the physical phenomenon accountable for different operation regimes and presented an analytical model for nc-Si:H TFTs associated to this phenomenon. This model is based on existing models for a-Si:H TFTs, which have been extended to account for observed physical phenomena in nc-Si:H TFT. They proposed that, the density of the defect states (i.e. DOS) is lesser in nc-Si:H than in a-Si:H due to higher internal order of atoms in nc-Si:H.

$$I_{Dsat} = \mu_{fet} C_i \frac{W}{L} V_{DSe} (1 + \lambda V_{DS}) V_{GTe} \quad \text{(for above threshold regime)} \qquad (2.2)$$

where μ_{fet} is the field effect carrier mobility, C_i is the capacitance of gate insulator, V_{DS} is drain to source voltage, λ is parameter relating to the effect of gate-length modulation, V_{DSe} is effective voltage from drain to source and V_{GTe} is the effective gate overdrive voltage.

Dosev et al. [39] presented the numerical simulation results of nc-Si:H TFTs, using ATLAS device simulator. They examined that acceptor-like defect states in nc-Si:H TFTs are filled at lower gate voltages as compared to a-Si:H having similar threshold voltages. The transconductance shape of nc-Si:H TFTs is same as of a-Si:H TFTs before the acceptor-like states are occupied. When acceptor-like states are filled by electrons then transconductance shape of nc-Si:H TFTs become typical as of poly-Si TFTs. Due to this behavior of acceptor-like states, the nc-Si:H TFTs properties typically lies between a-Si:H and the poly-Si transistors. However, authors considered a gap of 1.91 eV which is not a usual value for a-Si:H as well as for nc-Si:H TFT devices. For nc-Si TFT devices with an optical gap of 1.72 eV, M. Estrada et. al. [40] demonstrated that the anomalous effect of transconductance is due to trapped charge concentration and if some conditions are fulfilled related to the trapped charges concentration in defect states and concentration of free charges in the material then this effect can also observed for a-Si:H devices with

acceptor tail states activation energy similar to normal values of 0.035eV. Therefore the behavior of nc-Si:H is not necessarily suggested between a-Si:H and poly-Si.

The mobility and drain current models for nc-Si:H TFT devices, is presented by Cerdeira et. al. [41] including a second region examined in above-threshold regime, which are not exist in a-Si:H TFTs.

Hatzopoulos et. al. [42] proposed the model for drain current in regime of above threshold, on the basis of exponential distribution of tail states energy. Under linear region, this proposed model explained the observed super linear rise of drain current with gate voltage by the value of characteristic thermal energy of band tails being higher than 1.5 times the lattice thermal energy. When the characteristic temperature distribution of tails states is equal to 1.5 times the lattice temperature, then the derived current analytical model leads to the general quadratic metal-oxide-semiconductor (MOS) expression which is reported by I. Pappas et. al. [43].

$$I_D = \frac{W}{L}\mu B\left[\left(V_G - V_T\right)^{2AkT_t} - \left(V_G - V_T - V_D\right)^{2AkT_t}\right] \quad \text{(for above-threshold regime)} \qquad (2.3)$$

$$I_{Dsat} = \frac{W}{L}\mu B\left(V_G - V_T\right)^{2AkT_t} \quad \text{(for saturation regime)} \qquad (2.4)$$

where

$$B = \frac{n_i}{qA^2\sqrt{2kT_tN_t/\varepsilon_s}}\left(\frac{C_{ox}{}^2}{4\varepsilon_s kT_tN_t}\right)^{AkT_t} \qquad (2.5)$$

and

$$A = \frac{1}{kT} - \frac{1}{2kT_t} \qquad (2.6)$$

$$\mu_{FE} = \frac{\mu B}{C_{in}} 2AkT_t(2AkT_t - 1)\left(V_G - V_T - V_D\right)^{2(AKT_t - 1)} \qquad (2.7)$$

where I_D is drain current, μ_{FE} is field effect mobility, k is Boltzmann constant, μ is low electric field mobility of electron, T_t is characteristic temperature of tail state distribution, N_t is tail states volume density at intrinsic level, n_i is intrinsic carrier concentration, C_{ox} is gate dielectric capacitance, ε_s is silicon permittivity, kT is thermal energy at room

temperature, V_G, V_D and V_T are gate, drain and threshold voltage respectively, W is channel width and L is channel length.

When μ_{FE} is constant and is independent of gate voltage then from equation (2.6), $AkT_t =$ 1and $T_t > 3T/2$ .Under this condition, equation (2.3), (2.4) and (2.7) becomes,

$$I_D = \frac{W}{L} C_{in} \mu_{FE} \left[(V_G - V_T) V_D - \frac{V_D{}^2}{2} \right] \qquad \text{(for } V_D < V_G - V_T\text{)} \qquad (2.8)$$

$$I_{Dsat} = \frac{W}{2L} C_{in} \mu_{FE}' \left[(V_G - V_T)^2 \right] \qquad \text{(for } V_D \geq V_G - V_T\text{)} \qquad (2.9)$$

$$\mu_{FE}' = \frac{3\mu kTn_i}{2q\sqrt{3\varepsilon_s kTN_t}} \frac{C_{in}}{N_t} \qquad (2.10)$$

The off current in nc-Si:H TFT is examined by Mohammad R. Esmaeili-Rad et al. [44] and analyzed that the presence of fixed charges at the nc-Si:H/passivation nitride interface serves to increase the band bending, leading to an increase in off current by about two orders of magnitude. The reduction in leakage current can be achieved by using a-Si:H/nc-Si:H bilayer as the channel of nc-Si:H TFT device. When the nc-Si:H channel layer is capped with a-Si:H, the reduction in leakage current can be determined by the bulk conductivity of nc-Si:H because a-Si:H layer typically makes less defective interface with the nitride layer which is used for the passivation.

Ahnood et. al. [45] presented a general analytical technique capable of removing contact resistance effects, both ohmic and non-ohmic based solely on I-V measurements, enabling the extraction of an accurate and physically meaningful mobility. They proposed that the omission of contact resistance effects can results in an incorrect extraction of the maximum μ_{FET} by a factor of 2.

Mao [46] demonstrated the impact of the grain size of nc-Si:H on the surface potential of doped nc-Si:H TFTs. During the calculation of the surface potential of nc-Si:H, authors examined that the change in the dielectric constant of nc-Si:H should be considered when its diameter is smaller than 10 nm and the change in the bandgap of nc-Si:H should be

considered when its diameter is larger than 6 nm. They proposed a simplified surface potential equation for nc-Si:H TFTs under strong inversion conditions.

$$E(\varphi_s)=\sqrt{\frac{2q}{\left(1+\frac{10.4}{1+\left(\frac{1.38}{d\times10^9}\right)^{1.37}}\right)\varepsilon_0}\left[\frac{N_{ST}}{d}\varphi_s+\frac{1}{N_{Aa}^-}\frac{4kT(2\pi kT)^3(m_e m_h)^{\frac{3}{2}}}{h^6}\exp\left(-\frac{E_g(\infty)+q\left(\frac{3.4382}{d\times10^9}+\frac{1.1483}{\left(d\times10^9\right)^2}\right)}{kT}\right)kT\exp\left(\frac{q\varphi_s}{kT}\right)\right]} \tag{2.11}$$

where N_{Aa}^- is active dopant concentration, d is average grain size, q is electronic charge, N_{ST} is grain boundary surface state density, $E_g(\infty)$ is bulk band gap, k is Boltzmann constant, T is temperature, φ_s is surface potential, ε_o is dielectric constant of free space, m_e and m_h are effective electron and hole masses respectively and h is Planck's constant.

Anutgan et. al. [47] performed the capacitance analyses of nc-Si:H TFT. They found that the conducting thin layer in nc-Si:H film enlarges the effective area of capacitor beyond the electrode in nc-Si:H TFT structure. This increase of the effective area can be related with bulk capacitance-resistance branches and also with channel resistance where the earlier is governing at higher frequencies and the latter is accountable for the further increase in effective area at lower frequencies. Thus, they proposed that the hole conductivity along the nc-Si:H TFT interface is less as compared to electron conductivity.

Steinke et. al. [48] presented a model for determining the threshold voltage of nc-Si:H TFTs by examining the multiple boundaries between neighboring crystalline grains limit the charge-carrier transport. They consider that electrons in the channel may either occupy trap states at the grain boundaries or conduction band states in the grains. They have calculated the macroscopic densities of free and trapped carriers and then relate these densities with the site and bond occupation probabilities of a two dimensional percolation problem in which sites correspond to grains and bonds to grain boundaries. In the site-bond percolation problem, they determined the threshold by using Monte-Carlo simulations. They proposed that a lattice spanning cluster appears at the percolation threshold which allowing for a conduction path from source to drain and the particular

gate bias required to reach the threshold define the threshold voltage of the TFT. However, the model only describes transistor behavior near-threshold and could not explain the linear behavior soon after the transistor is turned on at low drain bias.

2.4. ELECTRICAL INSTABILITY IN TFTs

In general, the silicon (Si) based TFT suffers from electrical instability due to two possible instability mechanisms: (a) Charge trapping in gate insulator and/or in the interface between the gate insulator and channel (b) Defect state creation in active layer

(A) Charge Trapping

Under electrical stress, the electrons trapping take place in the gate insulator and/or in the interface between the gate insulator and channel material. Various mechanisms of electron trapping have been reported to illustrate the electrical instability in TFT. In TFT, the gate/insulator/channel trilayer is basically acts as a Metal-Insulator-Semiconductor (MIS) capacitor. Fig.2.1 shows the energy band diagram of MIS structure biased at positive voltage.

After the formation of channel via electron accumulation near the insulator interface, various electron trapping mechanisms can take place. Fig. 2.1 illustrates these mechanisms; that are (1) Direct tunneling from valence band [49, 50], (2) Fowler-Nordheim injection [51, 52], (3) trap assisted injection [53], (4) constant energy tunneling from silicon conduction band [54], (5) tunneling from conduction band to E_f (phonon assisted or via surface states) [55] and (6) hopping at the Fermi level [56] may occur . It is difficult to determine the dominant mechanism responsible for the charge trapping and is dependent on applied electric field and density of trap states in insulator.

(B) Defect State Creation

When the electrical stress is applied on the Si based TFTs then the density of electrons which take part in conduction increases in the a-Si:H active layer. These electrons interact with the weak Si-Si bond and cause the breaking of bonds which in turn leads to the formation of new dangling bonds in the a-Si:H material due to which electrons gets frequently trapped into and released from defect states.

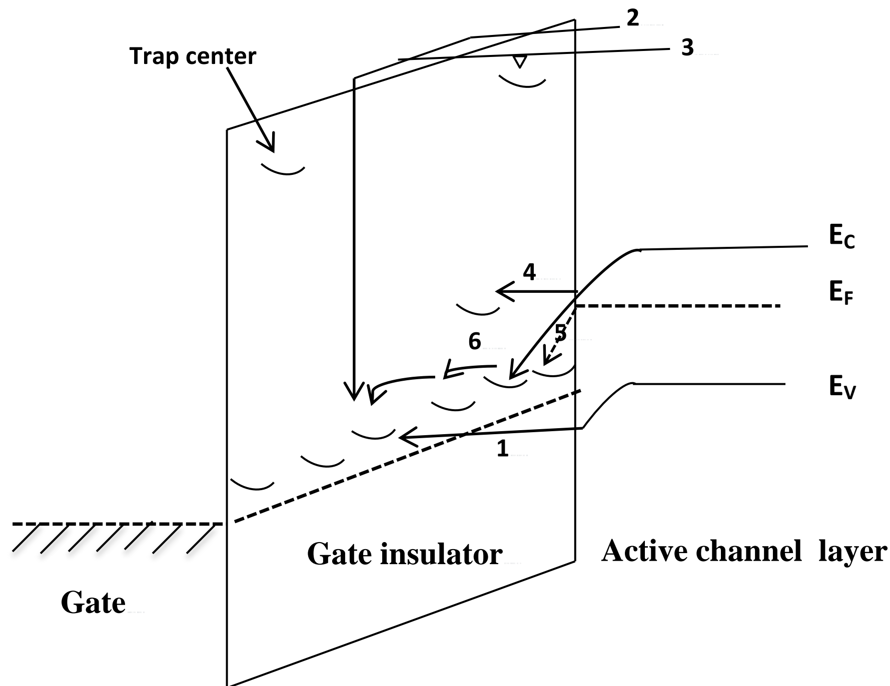


Fig 2.1. Charge Trapping Mechanisms: (1) Direct tunneling from valence band (2) Fowler-Nordheim injection, (3) trap assisted injection, (4) constant energy tunneling from silicon conduction band, (5) tunneling from conduction band to E_f (phonon assisted or via surface states), (6) hopping at the fermi level. Chain line represents quasi -Fermi level at t=0. Arrow represents the direction of electron [56]

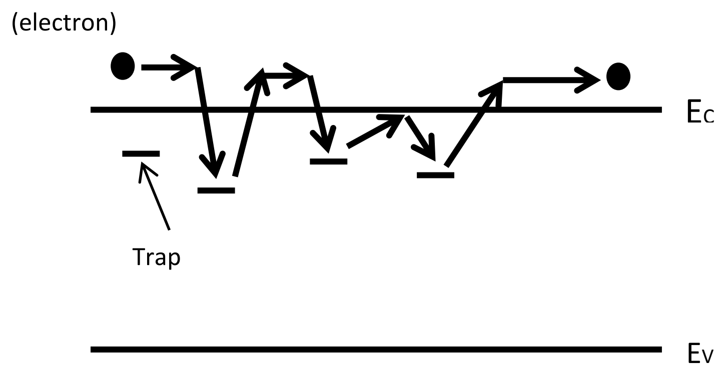


Fig 2.2. Trap and release model of electrons from band tail states [57]

This effectively increases the total density of states and decreases the drain current and increase the threshold voltage.

2.4.1. Models for Threshold Voltage Shift in TFTs

These instability mechanisms cause the shift in threshold voltage and thereby change the drain current of TFT. In the following section, we discuss about the attributes of these instability mechanisms which are presented by the various researchers.

(A) Powell's Model

Powell [56] analyzed that the electrical instability mechanism in amorphous silicon-silicon nitride TFTs, operate with low electric fields (~3 x 10^5 V cm^{-1}) in the dielectric, is basically the charge trapping that occur in silicon nitride layer that causes the threshold voltage shift and thus causes drain current degradation for a given biasing condition. Since silicon nitride as a gate dielectric have a high density of trap states thus causes charge trapping instabilities in TFT. Author proposed that the rate limiting process involved in the charge transfer at low electric field is basically the conduction in the nitride by variable range hopping at Fermi level and not the supply function from the semiconductor. Since the space charge in the nitride and the variable hopping conduction both depends on density of states in silicon nitride thus the threshold voltage shift is determined by the density of states at the Fermi level.

However author [58] further proposed that the nitride dependency of the hopping rates was due to variation in wave function rather than the trap density. The magnitude of threshold voltage shift is strongly temperature dependent with activation energy of 0.3eV. This activation energy is determined by the mean hop energy required for charge injection deep into the silicon nitride at the low applied electric fields. The strong temperature dependency of charge trapping is due to charge redistribution in the silicon nitride by thermally activated variable hopping from occupied states.

The logarithmic time dependence of threshold voltage shift is given as-

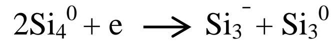
$$\Delta V_T = r_d \log\left(1+\frac{t}{t_o}\right) \tag{2.12}$$

where r_d is constant and contains the density of traps and tunneling constant.

Later, Powell and his research group [59] analyzed that in addition to the existing process of charge trapping near the interface, following mechanisms are also possible: (1) tunneling into the dielectric, (2) trapping into states at semiconductor-dielectric boundary, (3) localization in deep states within the amorphous silicon layer.

They proposed that the new mechanism responsible for instability of a-Si:H TFTs is the creation of metastable dangling bond states within the a-Si:H layer near to dielectric interface as a result of the field-effect-induced changes in electron density.

If phosphorus doping is used in order to move the Fermi level into the conduction band tail, then this makes the unstable configuration of silicon atom with five electrons. This silicon atom located just below the fermi level and thus causes the breaking of weak Si-Si bond and hence the formation of dangling bond defects. This process is shown by following equation:



$$2Si_4^0 + e \longrightarrow Si_3^- + Si_3^0$$

The main difference [60] between the two instability mechanisms is that, in case of charge trapping mechanism [56], the charge carriers are slowly trapped into electron states (also known as slow states) which are in poor communication with the a-Si:H conduction band. This trapping process produces a fixed shift in the transfer characteristic of a-Si:H TFTs. However in case of defect state creation mechanism [59], there is a slow increase of extra states (also known as fast states) which are in good communication with the a-Si:H conduction band.

Berkel et. al. [60] analyzed the bias dependence of threshold voltage shift in amorphous silicon-silicon nitride ambipolar TFTs and reported the co-existence of both instability mechanisms. They proposed that the state creation is dominated at low positive bias whereas charge trapping is dominated at higher positive as well as negative bias. An ambipolar TFT possess electron as well as hole accumulation layers under positive and negative gate biases, respectively. In this case, the number of created dangling bonds is given as [60]

$$\Delta N_{dh} = C\frac{V_e - V_h}{2}(cm^{-2}) \tag{2.13}$$

where C is the capacitance, V_e and V_h are the shift of threshold voltage for electron conduction and hole conduction respectively, while the density of slow states is given by

$$\Delta n_t = C\frac{V_e + V_h}{2}(cm^{-2}) \tag{2.14}$$

Author conclude that the extra states are created due to the absence of bonding electrons and these reactions will separately proceed whenever conduction band states or valence band states are populated and thus for bond breaking, recombination events are not required which is considered essential by Stutzmann et. al. [61]. Berkel et. al. [60] provide clear evidence for the charge trapping in the nitride and thus for the presence of slow states at the a-Si:H/a-SiN:H interface. Charge exchange with the nitride layer causes the net positive charge after negative bias stress and also net negative charge after positive bias stress. Under positive bias, the charge trapping mechanism is strongly field dependent.

Powell and his group [62] provide further refinement in bias dependency of the threshold voltage shift by including the effect of nitride composition. They reported that state creation is independent of the nitride composition and dominant at lower biases whereas the charge trapping is dependent on the nitride composition and dominant at higher biases. This indicates that the state creation process occur in the a-Si:H layer whereas the charge trapping occur in a-SiN:H layer. The defect states can be directly created by populating the conduction band tail states in the undoped material which moves the Fermi level up to the energy similar to these states. They also proposed that the charge trapping process is strongly field dependent which is associated with the field enhanced hopping at the Fermi level.

They also measured the time and temperature dependence of two instability mechanisms [63] and found that at the bias above which the charge trapping in the nitride dominates, the threshold voltage shift shows the logarithmic time dependence whereas at the bias below which state creation in the a-Si:H dominates, the threshold voltage shift shows the power law dependence, $\Delta V_T = \alpha\left(t / t_o\right)^{\beta}$ where β is about 0.5. They also found that the state creation is thermally activated but the charge trapping is weakly temperature

dependent. The charge trapping shows logarithmic time dependence and the small temperature dependence because the rate limiting step is basically the charge injection from the a-Si:H to the silicon nitride with charge trapping close to the semiconductor interface and no charge redistribution occur due to the conduction in the nitride. The threshold voltage shift due to the state creation is small and is given as

$$\Delta V_T = (V_G - V_T)\left(t / t_o\right)^{\beta} \tag{2.15}$$

Thus the rate of state creation is proportional to the band tail electrons and t_o is independent of density of band tail electrons. The magnitude of E_a ~ 0.9eV (i.e. activation energy of t_o) and temperature dependent β (~0.45 to 0.65) are uniform with dispersive hydrogen diffusion. Thus, they proposed that, the state creation process is similar to that of dangling bond creation process which occurs due to the breaking of weak Si-Si bonds sustained by dispersive diffusion of hydrogen [64, 65].

Powell et. al. [66] also reported that the charge trapping mechanism causes a shift of the electron and hole threshold voltages in the same direction whereas the state creation mechanism causes a shift in opposite direction. The electron threshold voltage is shifted in positive direction while hole threshold voltage is shifted in negative direction. For the transistor which uses silicon nitride as a gate dielectric, state creation in the lower part of the band gap is the dominant process at the low positive bias whereas the removal of states from the lower part of the gap dominates at the low negative bias. However, for the transistor that uses oxide as the gate dielectric, state creation is the dominant process for both positive and negative bias. For positive bias, states creation occurred in the lower portion of the band gap whereas for negative bias, it occurred in the upper portion of the band gap. In addition to this, for oxide transistor the positive and negative bias annealing causes overall increase in the density of states whereas for nitride transistor negative bias annealing causes a decrease in the density of states due to the annealing of defect states presents below the midgap. This difference between nitride and oxide transistor is because of the different zero-bias Fermi energy position at the interface due to the existence of an electron accumulation layer in the nitride transistor.

For nitride transistor, the dominant mechanism for threshold voltage shift under the higher biases stress is the charge trapping which occurs for both high positive as well as high negative bias. The magnitude of the threshold voltage shift for state reduction is smaller than for the state creation. Authors also found that threshold voltage shows the power law time dependence for both the polarities and in addition to this the activation energy is same (~0.9eV) for both positive and negative bias. This concludes that the state creation process for positive bias is similar to that of state removal process for negative bias.

Powell and his group [67] further proposed that the parameter β is not appropriate for measuring the TFT instability and thus a new concept known as thermalization energy concept have been proposed. According to them, defect creation during bias-stress exhibits a thermal barrier for defect removal with the maximum energy around 1.1-1.4 eV based on the time and temperature at which defects were created. This barrier is not important under thermal equilibrium, because the defect creation and removal is balanced by the formation energy of defects however under non-equilibrium condition, this energy barrier is important in order to identify the specific intermediate step.

They reported the expression for thermalization energy as [67].

$$E = \left(k_B T\right) ln(\nu t) \tag{2.16}$$

It means that after time t, all defect-creation sites with activation energy $E_a \leq E$ would have converted into defects. Deane S. C. et. al. [67] plotted threshold voltage shift as a function of stress time at various temperatures and then applied the thermalization concept to the bias stress data by plotting threshold voltage shift as a function of thermalization energy and found a unique curve at a single fitting parameter i.e. attempt-to-escape frequency υ_o (=10^{10} Hz). They also plotted stretched exponential as a function of thermalization energy and found that the stretched exponential curve matched well with the experimental data for the E<0.95eV but curves shows mismatched for E>0.95eV and thus they proposed that to obtain a stretched exponential, the defect state creation has to be proportional to the number of excess band tail carriers $(\Delta N_{BT})^{\alpha}$ with α between 1.5 to 1.7. For α=1.5, threshold voltage shift is given as equation

$$\Delta V_t \propto \left[\left(\frac{t}{t_0} \right)^{\beta} + 1 \right]^{-2} \quad (2.17)$$

They provide the following comparison between defect state creation and defect removal-

1) Defect state creation possess E_a=0.975 eV with υ_o=10^{10}Hz whereas defect removal shows E_a between 1.1 to 1.5 eV with υ_o of 10^{13}Hz.
2) Defect creation mechanism occurs due to the breaking of weak Si-Si bond which results into the thermalization of SiHD (i.e. SiH defect) in the H-DOS (hydrogen density of states) whereas the defect removal occurs due to the release of hydrogen from the SiHD defect.

(B) Libsch's Model

Libsch et. al. [68] proposed that the charge injection from the a-Si:H channel into the traps presented in the a-Si:H/a-SiN_X:H interface and in the nitride layer close to the interface causes the threshold voltage shift (ΔV_T) in the transfer characteristic of TFT. They proposed the stretched-exponential equation given as-

$$|\Delta V_T| = |\Delta V_0| \left\{ 1 - \exp\left[-\left(\frac{t}{\tau} \right)^{\beta} \right] \right\} \quad (2.18)$$

where ΔV_0 is the effective voltage drop across the insulator, $\tau = \tau_0 \exp(E_T / kT)$ is the characteristic trapping time of the carriers with τ_o being the thermal prefactor for emission over the energy barrier, $E_a = E_T \beta$ represent the thermal activation energy with β as the stretched-exponential exponent and E_T being the average effective energy barrier for the carriers enter into the insulator from the a-Si:H channel. When the shorter stress times, lower stress electric fields or lower stress temperatures is applied on the nitride gate dielectric a-Si:H TFT then the carriers inject directly into the bottom energy states of a-Si:H/a-SiN_X:H interface and in the a-SiN_X:H transitional layer near the a-Si:H/a-SiN_X:H interface. However when longer stress times, higher stress electric fields or higher stress temperatures is applied then large concentration of states in the insulator near the a-

Si:H/a-SiN$_X$:H interface will get filled and as a result probability of emission from these states increases.

Staebler et. al. [69] reported that β and τ are independent of gate bias while ΔV_0 is dependent on gate bias and is given as $\Delta V_0 \approx V_g\text{-}V_{ti}$ with no power dependence (i.e. α=1.0). β is given as $\beta = \left(T_{ST} / T_0^*\right) - \beta_0$ with equilibrium temperature, $T_0^* \approx 229$K and $\beta_0 \approx 1.04$ for stress temperature, $T_{ST} \leq 80$˚C while for $T_{ST} \geq 80$˚C, β become temperature independent with $\beta \approx 0.5$. A non-zero value of β_0 shows that ΔV_T is independent of gate dielectric which differs from the conclusion given by Jackson et. al.s [70].

(C) Nathan's Model

Nathan and his group [71] proposed that when a bias is applied on the gate terminal with the drain and source grounded then the threshold voltage shift shows the power law dependence on gate bias stress and can be given by defect pool model [72]. According to defect pool model, the rate of defect state creation is dependent on barrier to defect state formation, number of band tail electrons and density of week Si-Si bonds. Thus, the threshold voltage shift is given as

$$\Delta V_T = A(V_{ST} - V_{Ti})\left(t\right)^{\beta} \tag{2.19}$$

where V_{ST} is the gate bias stress voltage, V_{Ti} is the threshold voltage of TFT before gate bias is applied, A and β (~0.3) are temperature dependent parameters and t is the gate bias stress time. However, when both gate and drain terminals of the nitrogen rich gate dielectric TFTs are subjected to bias voltage then for small gate stress biases (≤15V), where the defect state creation is the dominant instability mechanism, TFT shows less threshold voltage shift as compared to the presence of only gate bias stress. Authors reported that the increase in drain bias stress results in the increase of lateral electric field which in turn decreases the channel carrier concentration (n_{BT}) close to drain. However in the saturation mode ($V_{DS}=V_{GS}\text{-}V_T$), the channel carrier concentration remains constant and thus causes negligible threshold voltage shift. Similarly, TFTs subjected into deeper saturation ($V_{DS}>V_{GS}\text{-}V_T$) shows less threshold voltage shift. Thus the charge stored on the gate when TFT is subjected to both gate and drain bias stresses is given as [71]:

$$Q_G = \frac{2}{3} C_G W L \frac{\left(V_{GS} - V_T\right)^3 - \left(V_{GD} - V_T\right)^3}{\left(V_{GS} - V_T\right)^2 - \left(V_{GD} - V_T\right)^2} \tag{2.20}$$

In linear region, $V_{GD} = V_{GS}$ $$Q_{G0} = C_G.W.L\left(V_{GS} - V_T\right) \tag{2.21}$$

In saturation region, $V_{GD} \rightarrow V_T$ $$Q_G = \frac{2}{3} C_G.W.L\left(V_{GS} - V_T\right) \tag{2.22}$$

Now threshold voltage shift is given as,

$$\Delta V_T = \left(\frac{Q_G}{Q_{G0}}\right) A(V_{GS} - V_{Ti})\left(t\right)^{\beta} \tag{2.23}$$

where Q_G is given by eq. (2.20) and Q_{G0} is given by eq. (2.21).

In constant current stressing, the drain and gate terminals of the TFTs are shorted in the diode connected configuration with the source terminal grounded. The constant drain current is maintained by the progressive adjustment of the gate bias for the compensation of threshold voltage shift. Such compensation thus maintained the constant band tail carrier density (n_{BT}) and hence threshold voltage shift shows no trend of saturation.

Nathan and his group [73] further modified the power law dependency of ΔV_T which is given as

$$\Delta V_T\left(t\right) = \left[V_{GS}(t) - V_T(t)\right]^{\gamma} \left(\frac{t}{t_0}\right)^{\beta} \tag{2.24}$$

where $$t_0 = \left(\frac{\beta w N_{BT}}{A N_{WB} D_{00} w^{\beta}}\right)^{\frac{1}{\beta}} \tag{2.25}$$

Here A is proportionality constant, N_{BT} is the band tail states density, w is the attempt-to-escape frequency of hydrogen, D_{00} is the microscopic diffusion coefficient, β is power-law index and γ is a power parameter having values between 1.5 to 1.9. The power law parameters, β, γ and t_0 are dependent on temperature and stress history of the TFT.

2.5. CONCLUSION

In this chapter, a literature review of the research carried in the area of nc-Si:H TFT is presented. Based on the literature review, it is found that n-channel nc-Si:H TFT provides higher mobility as compared to p-channel TFT and top-gate staggered TFT structure provides better electrical stability and high on-off current ratio. Therefore in this thesis, staggered top-gate n-channel nc-Si:H TFT is considered and investigated for its electrical behavior. The mechanisms which cause the shift in threshold voltage and thereby the electrical instability in TFT are also discussed in this chapter. It is found that defect state creation in channel layer and charge trapping in gate insulator or in gate insulator-channel interface are the two main mechanisms that causes electrical instability in TFT.

CHAPTER 3

DEPOSITION AND CHARACTERIZATION OF nc-Si:H FILM

3.1. INTRODUCTION

It is required to deposit the good quality nc-Si:H film in order to achieve high effective mobility and high on current and thereby improved TFT performance. Various deposition methods like PECVD [74], electron cyclotron resonance CVD [75], microwave CVD [76], very high frequency PECVD [77] and hot wire CVD [78] have been used to obtain nc-Si:H films. Table 3.1 summarized the results of published techniques used for nc-Si:H film deposition. Among these techniques, PECVD is the most commonly used method. However, in order to provide greater hydrogen carrier density and higher thermal energy for the nano-crystallization of silicon layer, nc-Si:H film formation using PECVD method usually requires high RF power and high temperature as compared to that of a-Si:H film. This high RF power causes high energy ion bombardment which results into amorphization of crystalline growth [79].

The hydrogen dilution is another critical parameter that is required for nanocrystallization of silicon. The hydrogen atoms that are generated during most of the gaseous CVD techniques tie up with the part of dangling bonds and help to reduce the density of defect states in the energy gap. However, it is found and reported that the dilution of hydrogen is not the necessary condition for formation of nc-Si:H film [80]. The physical vapor deposition of nc-Si:H film is another method that has not been addressed so far in the literature.

Table 3.1: Experimental published data for nc-Si:H film

Process nc-Si:H	RF Power	Deposition Pressure(Pd)/Base Pressure(Pb)	Gases	Temperature	nc-Si:H Film Thickness	Crystalline volume fraction	Ref
HWCVD	-	Pd =$1x10^{-2}$ mbar	SiH_4:H_2=4:76	125 ºC	250nm	-	**[81]**
Cat-CVD	-	Pb=<10^{-8} mbar	SiH_4:H_2 =4:76	-	200nm	90%	**[82]**
HWCVD	-	Pd =3.5 X 10^{-2} mbar	SiH_4:H_2=4:76	150ºC	250nm	-	**[83]**
VHF PECVD 80MHz	86-93 mW/cm^2	Pd =500 mTorr	R=[H_2]/[SiH_4+$SiCl_2H_2$] =20-30	150 ºC	300nm	-	**[25]**
PECVD 13.56MHz	110$mWcm^{-2}$	Pd =900 mTorr	H_2:SiH_4:SiF_4 =50:2:35	-	50nm	-	**[24]**
Microwave plasma ECR-CVD	-	Pd =12 mTorr Pb=10^{-6} Torr	~15% H_2 dilution 2% SiH_4 in H_2	400ºC	90-100nm	-	**[84]**
PECVD 13.56 MHz	90W	Pd =0.9 Torr Pb=1.5 x 10^{-6} Torr	H_2/SiH_4 ~100	260 ˚C	100nm	80%	**[28]**
PECVD 13.6 MHz	-	-	H_2:SiH_4=100:1	260̊C	100nm	80±2%	**[27]**

Process nc-Si:H	**RF Power**	**Deposition Pressure(Pd)/Base Pressure(Pb)**	**Gases**	**Temperature**	**nc-Si:H Film Thickness**	**Crystalline volume fraction**	**Ref**
Capacitively coupled RF reactor (13.56MHz)	-	-	SiF_4 and Ar diluted in H_2	230℃	150nm	-	**[85]**
PECVD 80MHz	86mW/ cm^2	-	$[H_2]/[SiH_4+SiCl_2H_2]$ =20 to 30	150˚C	300nm	-	**[33]**
HWCVD	-	Pd =$2x10^{-2}$ Torr	SiH_4 diluted in H_2 =3%	250℃	300nm	59.05% on glass 73% on a-Si:H 84.32% on nc-Si:H	**[86]**
PECVD	15W	Pd =1.9 Torr	$SiF_4/H_2/Ar$ =1/3/40	200℃	120nm	Small grain=80% Large grain=16% Voids=4%	**[34]**
ICP-CVD	700W	Pd =50 mTorr Pb =≤ 1 mTorr	$He:SiH_4$ =40:3	350℃	200nm	-	**[87]**
ICP-CVD 13.56MHz	$36mWcm^{-3}$	Pd =0.67 Pa	$[H_2]/[SiH_4+H_2]$=0.6	300 ˚C	10nm and 40nm	73.6% at 10nm 75.1% at 40nm	**[88]**
HWP-PECVD	-	Pd =300 Torr Pb=3 x 10^{-5} Torr	He, H_2, SiH_4 SiH_4 conc.= 0.05% H_2/SiH_4 ratio = 70	250˚C	500nm	57% at scan speed= 50mm/s	**[89]**
LTPECVD	20 to 100W	Pd =0.2 Torr	H_2 free He diluted SiH_4 =100sccm	250˚C	200nm	12.5% to 32%	**[80]**

In present work, electron-beam (e-beam) assisted physical vapor deposition (EBPVD) of nc-Si:H thin film has been presented with supportive characterization results. The EBPVD of nc-Si:H provides an alternative way to PECVD process with substantial advantages in TFT by deposition of device quality nc-Si:H film with no hydrogen dilution. It provides no deterioration of the nc-Si:H film that normally occurs in PECVD due to existence of impurity chemical traces.

High deposition rate, large substrate area are the two basic requirement for the fabrication of nc-Si:H TFT. This EBPVD process fulfill both the requirements by facilitating large area fabrication and also rapid deposition of nc-Si:H film which leads to the reduction in cost for large area application [90]. In addition to this, EBPVD method provides low temperature processing which is necessary in order to achieve nc-Si:H film with less defect states and high crystallinity [29]. The highly crystalline layer basically provides less series resistance which results into the increase in effective mobility and therefore the on-current [28] of TFT device.

The e-beam evaporator system has been used to deposit nc-Si:H film on Corning glass 1737 substrate. A 100nm thick nc-Si:H film is deposited to study the surface morphology, conductivity and grain size. In addition to this, the nc-Si:H films having thicknesses 150nm and 200nm are also deposited to analyze the effect of thickness on the grain size.

The deposited film having thickness 100nm has been characterized using Field Emission Scanning Electron Microscopy (FESEM), AFM (Atomic Force Microscope), Raman Spectroscopy, X-Ray Diffraction (XRD) and Electron Diffraction Spectroscopy (EDS) techniques. The FESEM and AFM results are provided for deposited films having thickness 150nm and 200nm. This result shows the effect of thickness on film morphology. To validate the feasibility of deposited nc-Si:H film for TFT application, conductivity measurement is carried for 100nm thick film.

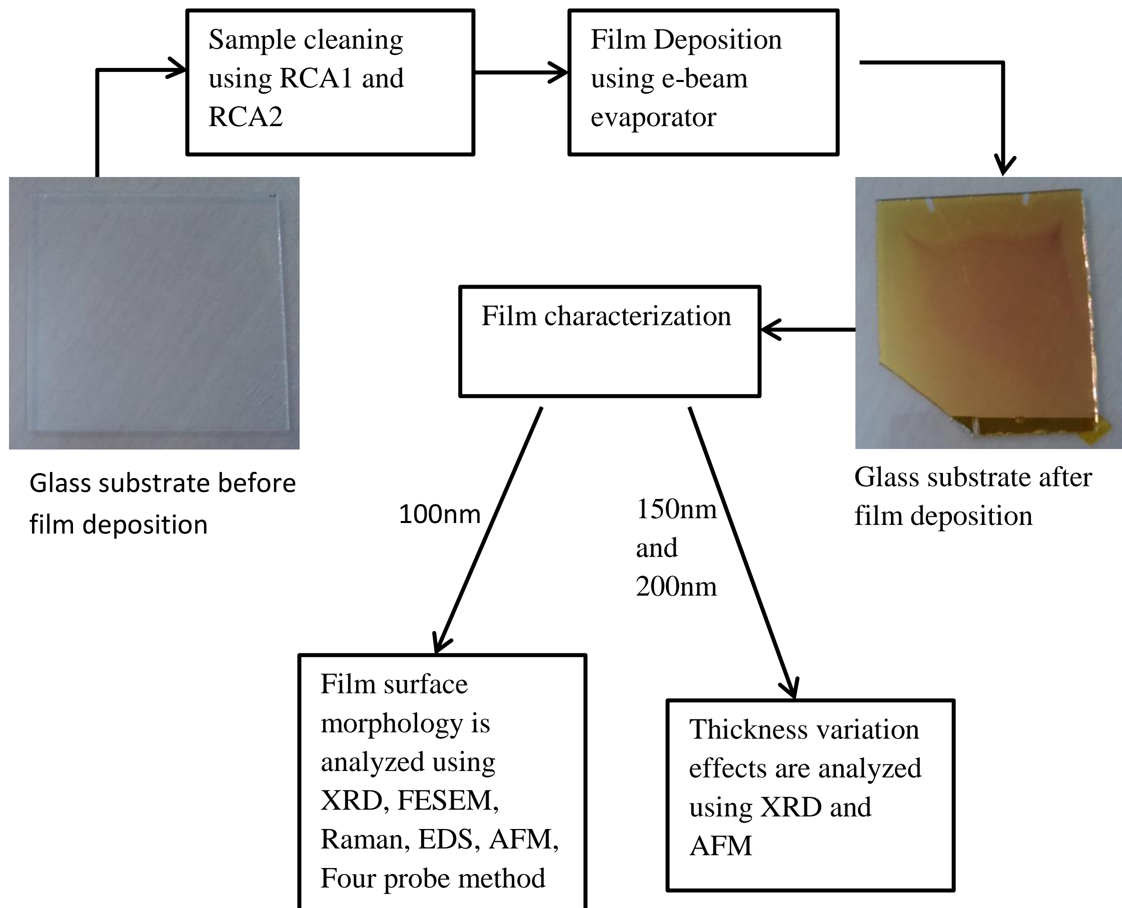


Fig. 3.1. Process flow for deposition and characterization of nc-Si:H film

3.2. SAMPLE PREPARATION

Fig. 3.1 illustrates process flow used in present study to analyze the nc-Si:H film deposited on substrate.

The Corning glass 1737 sample of size 1x1 inch was considered for the deposition of nc-Si:H film. Corning glass substrate was used over other substrate like silicon because it fulfilled the requirements needed for the fabrication of TFT by providing transparency, low density and comparable low coefficient of thermal expansion.

To avoid the contamination, the sample was given to chemical cleaning treatment before deposition. This cleaning technique was proposed by Werner Kern [91] in 1965 while

working for Radio Corporation of America (RCA). This is the most standard method for sample cleaning which comprise of RCA1 and RCA2.

(A) RCA 1

This solution contains a mixture of distilled water, hydrogen peroxide (H_2O_2), ammonium hydroxide (NH_4OH) in the ratio of 5:1:1. It is also known as ammonium-peroxide mixture (APM). Wafers were immersed in this solution for 10 minutes, followed by a thorough rinse in distilled water. This procedure removes organic dirt (resist).

(B) RCA 2

This solution contains distilled water, H_2O_2, hydrochloric acid (HCL) in the ratio 6:1:1. Wafers are immersed in this solution for 10 minutes. This procedure removes metal ions. The second RCA cleaning process is essential to keep the deposition furnaces free from metal contamination.

Both cleaning processes leave a thin oxide on the wafers. For stripping the oxide layer from the wafers a dip in dilute (hydro fluidic acid) HF (distilled water: HF: 50:1) for a few seconds was carried out. Since HF reacts with the glass, this solution is carried in Teflon beakers.

3.3. ELECTRON-BEAM EVAPORATION SYSTEM

Fig. 3.2 shows a schematic view of e-beam evaporator system. A very hot and small filament is located in the electron gun which boils off the electrons. These electrons are accelerated by the high voltage, forming an electron beam. Electron beam is directed magnetically towards the crucible where the material in the form of ingot awaits. Upon striking the ingot, electrons loosed their energy and produces heat. This thermal energy melts the ingot and thereby results into the vapors which can be used to coat the substrate surface. The heat generated during the evaporation process increases the temperature of the surface. Therefore, the substrate must be placed at the adequate distance from the filament. The 4-target e-beam evaporator system (shown in Fig. 3.3) was used for the deposition of nc-Si:H thin film. This system was equipped with four e-guns.

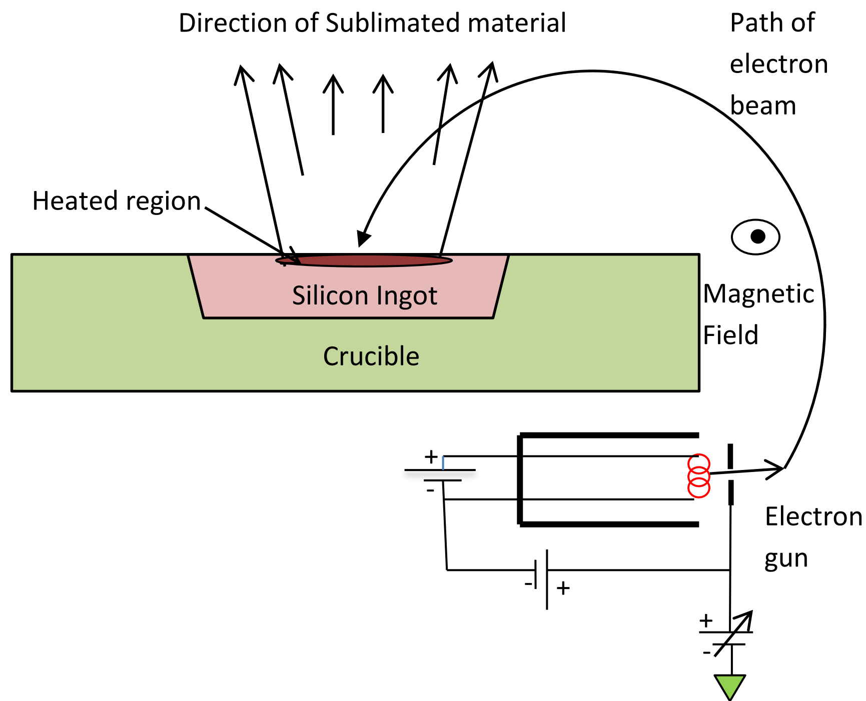


Fig. 3.2. Schematic of e-beam evaporator

Fig. 3.3. 4-target e-beam evaporation setup at IIT Bombay (CEN)

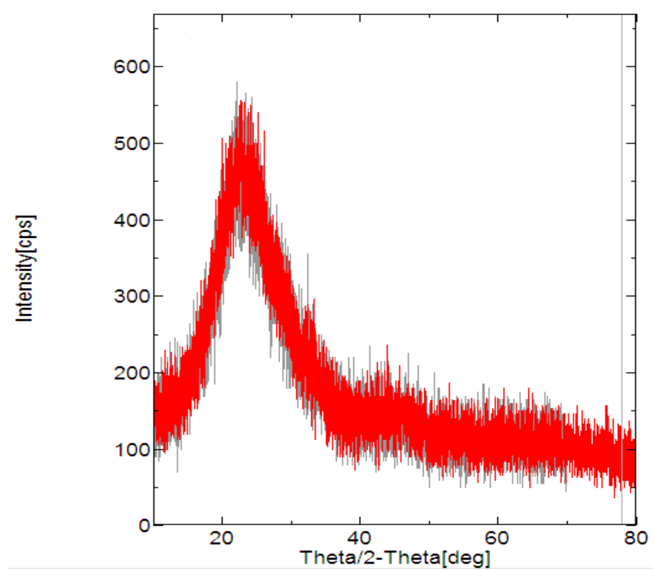
A control unit provides the power supplies for the e-gun and allows for a variation of the beam intensity and hence the deposition rate of the evaporated Si. The sample was loaded in the vacuum chamber by venting the chamber with N_2. The chamber was closed after loading of glass samples. The silicon ingot in cuboid form with the purity of 99.999% was placed in a boat over the hearth or crucible of e-gun. Before deposition, the turbo pump was opened till the process pressure of 8 $x10^{-6}$ Torr was achieved. After the vacuum was reached to desired level, the required thickness value was set and e-beam supply was turned on. After some time when the metal begins to evaporate, the shutter was opened in order to start the deposition process. The substrate temperature is as low as 90ºC. The rate of deposition was maintained at 1.2 Å/s using the beam current. A beam current of 90mA and voltage of 4 kV was used to evaporate the silicon in order to achieve a thickness of 100nm. The shutter was closed after 21 minutes i.e. after the deposition of film of required thickness.

After the deposition process, the deposited film was subjected to annealing process for 30 minutes. Under annealing process, slow heating is provided to the sample at the rate of 150˚C/hr and slow cooling is done at the rate of 200℃/hr. This improves the crystallinity of the film and provides nc-Si:H film with few nanometer sizes of grains. The annealing process is carried in the presence of argon gas with a flow rate of 100sccm to avoid the oxidation of deposited film.

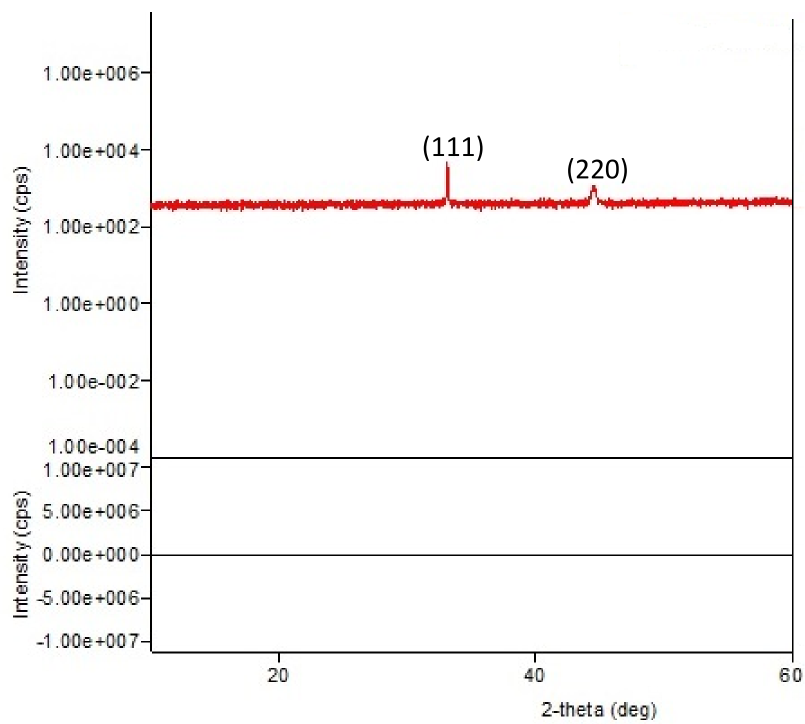
3.4. CHARACTERIZATION OF nc-Si:H FILM

3.4.1 Surface Morphology

A film having thickness 100nm is deposited on the Corning glass 1737 substrate. The XRD analysis was done using Rigaku model in order to confirm the crystalline nature of deposited film before and after the annealing process. From the results (shown in Fig. 3.4.), it is clear that annealing process results into the nanocrystallization of silicon film. The slow heating during annealing process causes the transformation of amorphous like film (shown in Fig. 3.4(a)) into nc-Si:H film (shown in Fig. 3.4(b)).



(a)



(b)

Fig 3.4. XRD Results (a) Before annealing (b) After annealing at room temperature

The occurrence of peaks (111) and (220) in XRD pattern in Fig. 3.4(b) verifies the nanocrystalline nature of the deposited film. The grain size, *d*, of the deposited film was calculated from XRD data (Fig. 3.4 (b)) by using Scherrer formula given as

$$B = \frac{K\lambda}{d\cos(\theta)} \tag{3.1}$$

In equation (3.1), B is full width half maxima (FWHM) of XRD graph, λ is wavelength of the X-ray, K is the Scherrer constant which is taken as 0.94 [92]. For present study, B=0.080, λ= 1.5Å and 2θ=33.068 based on XRD data. By putting these values in equation 3.1, d comes out to be 2nm.

To further validate the nanocrystalline nature of deposited film after annealing, various characterizations were done. The FESEM and EDS analysis was done by using model ZEISS. The film morphology image from FESEM is shown in Fig. 3.5. This micrograph illustrates the grain size of deposited film in the range of 5-6 nm. The elemental details given by EDS are shown in Fig. 3.6(a). Existence of Ca, O, Al, Mg and C in addition with Si are due to the Corning glass as the substrate.

The grain size estimated by using FESEM data is higher as compared to XRD morphology due to the physical error in deducing the grains edges in FESEM graph.

The RAMAN (LabRAM HR 800, JY) analysis was done and is shown in Fig. 3.7. The crystallinity was evaluated by using RAMAN intensity ratio,

$$X_C = \frac{I_{520}}{I_{520} + \eta I_{480}} \tag{3.2}$$

where I_{480} and I_{520} are deconvoluted intensities deduced from RAMAN spectra in a-Si:H transverse optical (TO) (~480 cm^{-1}) and crystalline silicon TO (~520 cm^{-1}) peaks, respectively and η is back scattering cross sections ratio which was taken as 0.8 [93]. The occurrence of sharp peak at 520cm^{-1} (as shown in Fig. 3.7) verifies the high crystalline nature of the deposited film.

The surface morphology of the films has been measured by AFM (model NT-MDT SOLVER Next), as illustrated in Fig. 3.8. This AFM graph validates the presence of fine grains in 100nm thick film.

To further analyze the effect of thickness on the grain size, the nc-Si:H films of different thicknesses (150nm and 200nm) are deposited. The FESEM and AFM results of 150nm and 200nm thick nc-Si:H film are shown in Fig 3.9 and Fig. 3.10 respectively.

The FESEM micrograph (shown in Fig 3.5, 3.9(a) and 3.10(a)) shows that grain size increase from 5 to 12 nm as thickness increases from 100 to 200nm. The AFM results shows broader grain in thicker film with thickness of 200nm (Fig 3.10(b)) as compared to thin film with thickness of 100nm (Fig. 3.8). These results of FESEM and AFM are matched well with the published results [22] which reported that the nc-Si:H film is usually grown in the form of cone shape i.e. from bottom to top which provides the increase in grain size with the increase in thickness.

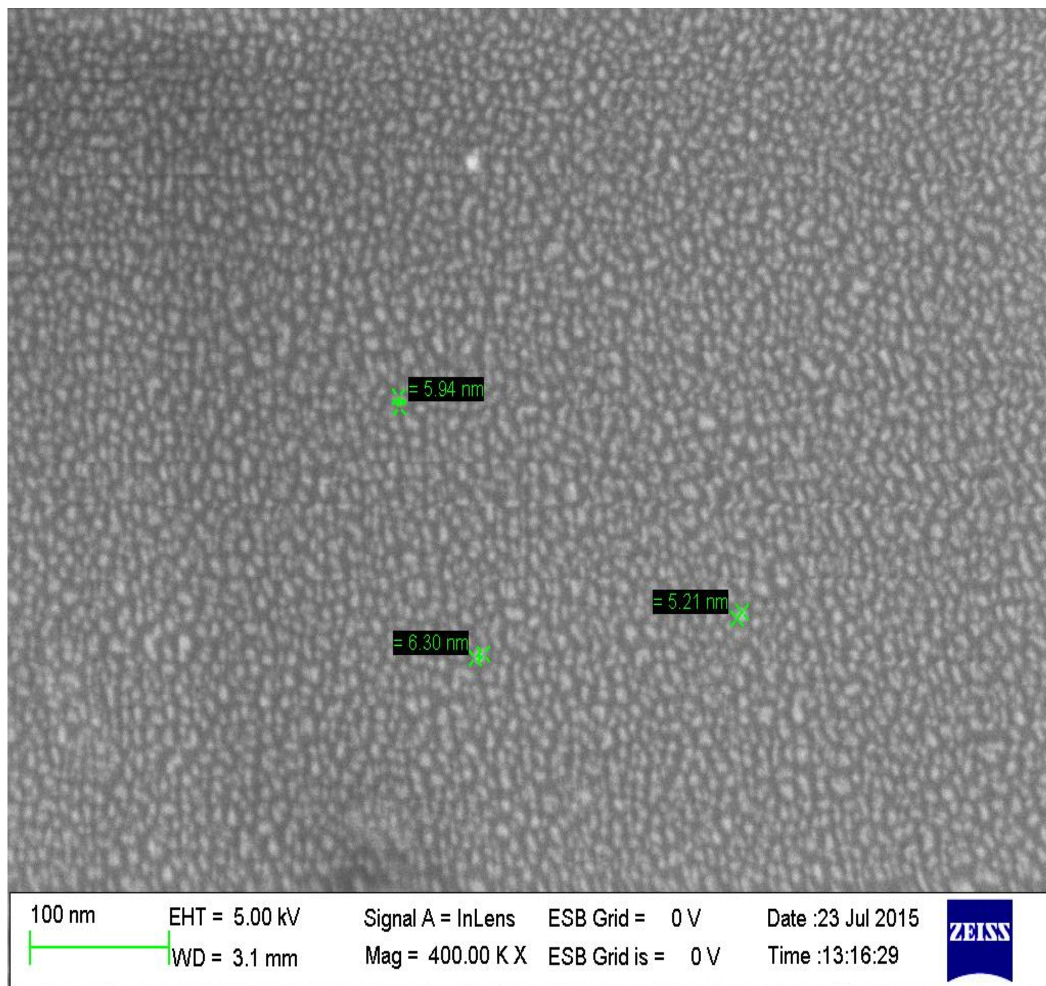
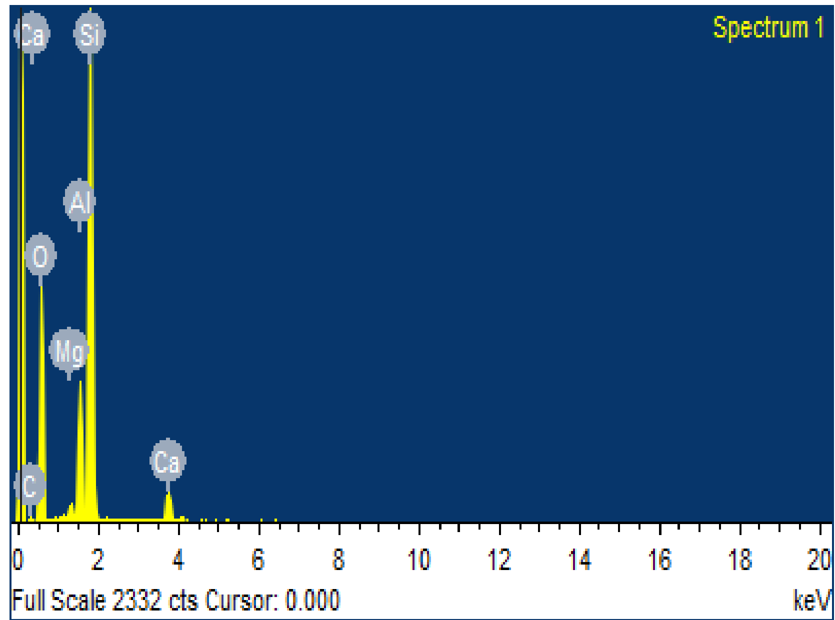


Fig. 3.5. FESEM Micrograph of 100nm thick nc-Si:H film



(a)

Element	**Weight%**	**Atomic%**
C K	4.20	6.79
O K	52.51	63.69
Mg K	0.77	0.62
Al K	7.48	5.38
Si K	31.69	21.90
Ca K	3.34	1.62

(b)

Fig. 3.6. EDS results (a) Analysis graph
(b) Elemental data of 100nm thick nc-Si:H film

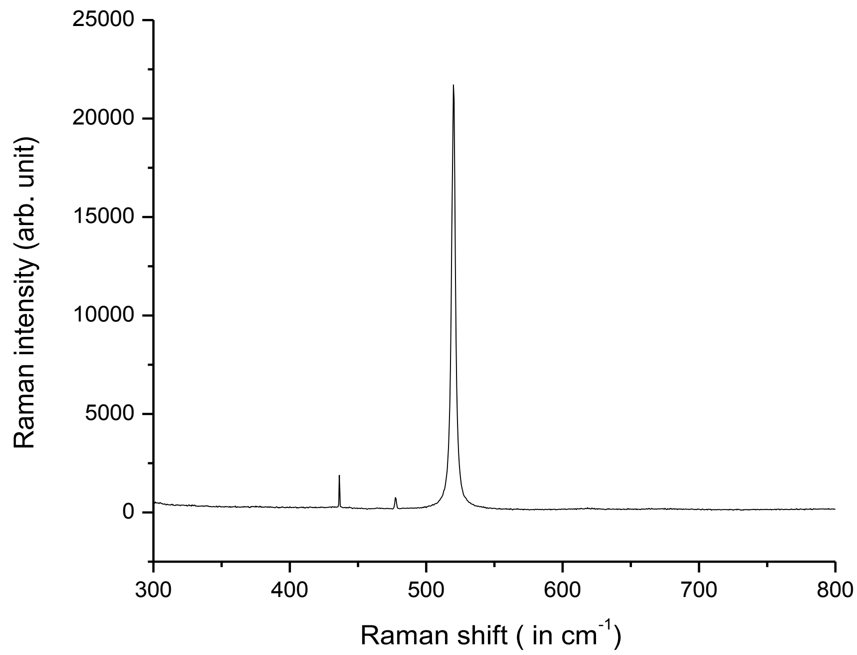


Fig. 3.7. RAMAN Spectra of 100nm thick nc-Si:H film

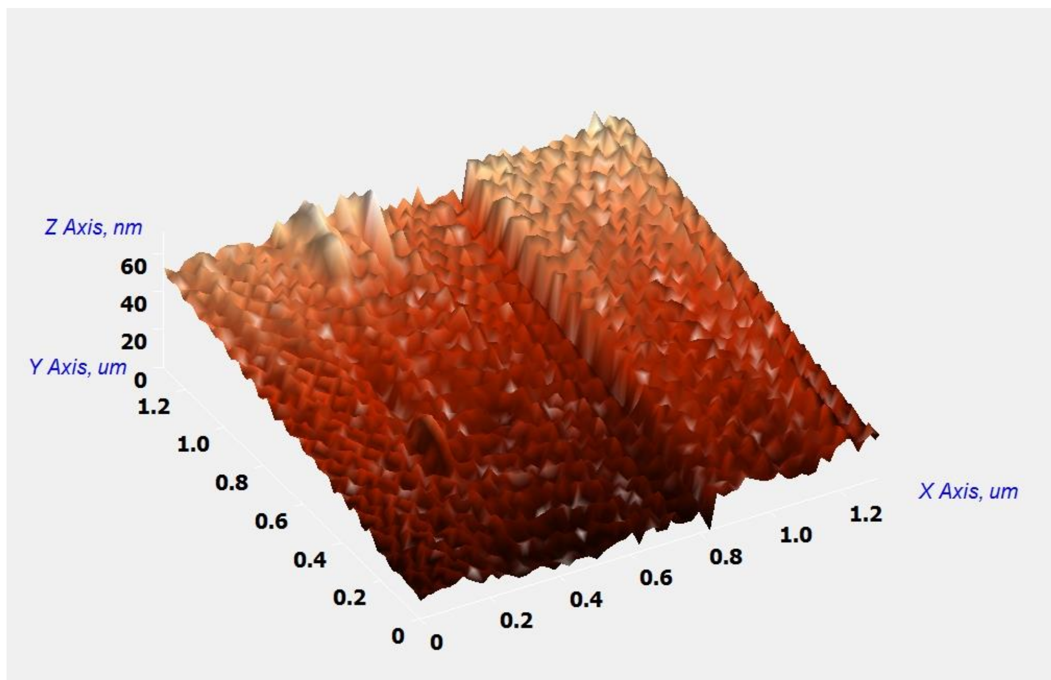
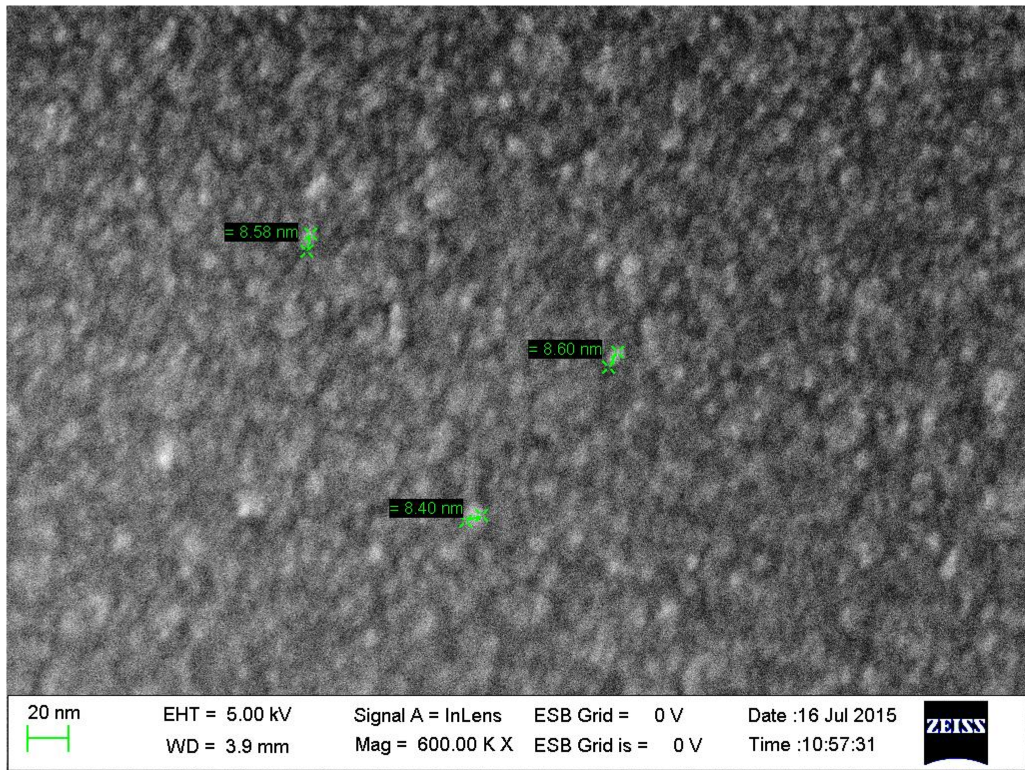
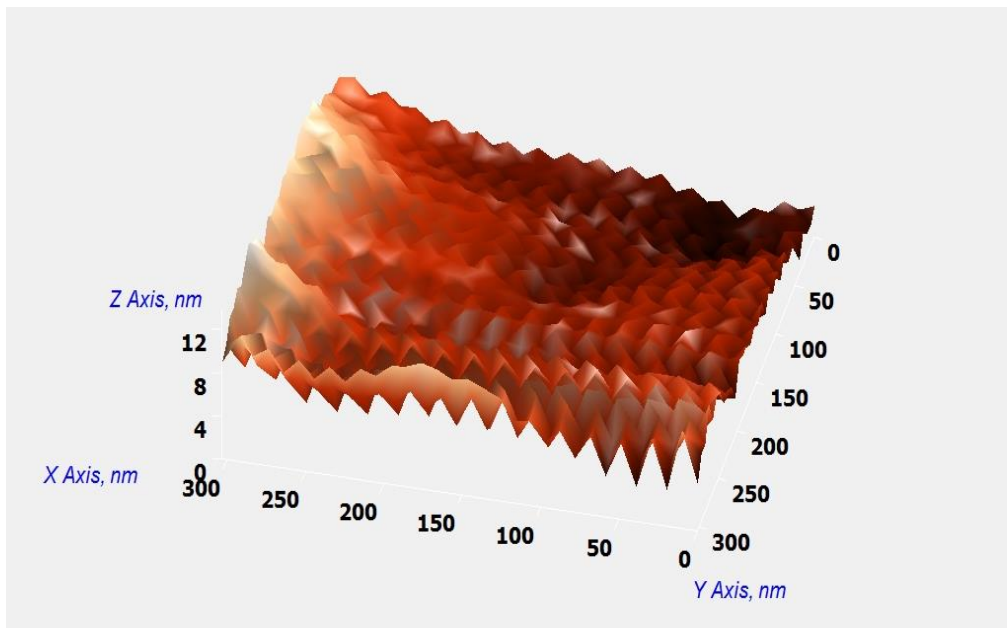


Fig. 3.8. AFM micrograph of 100nm thick nc-Si:H film

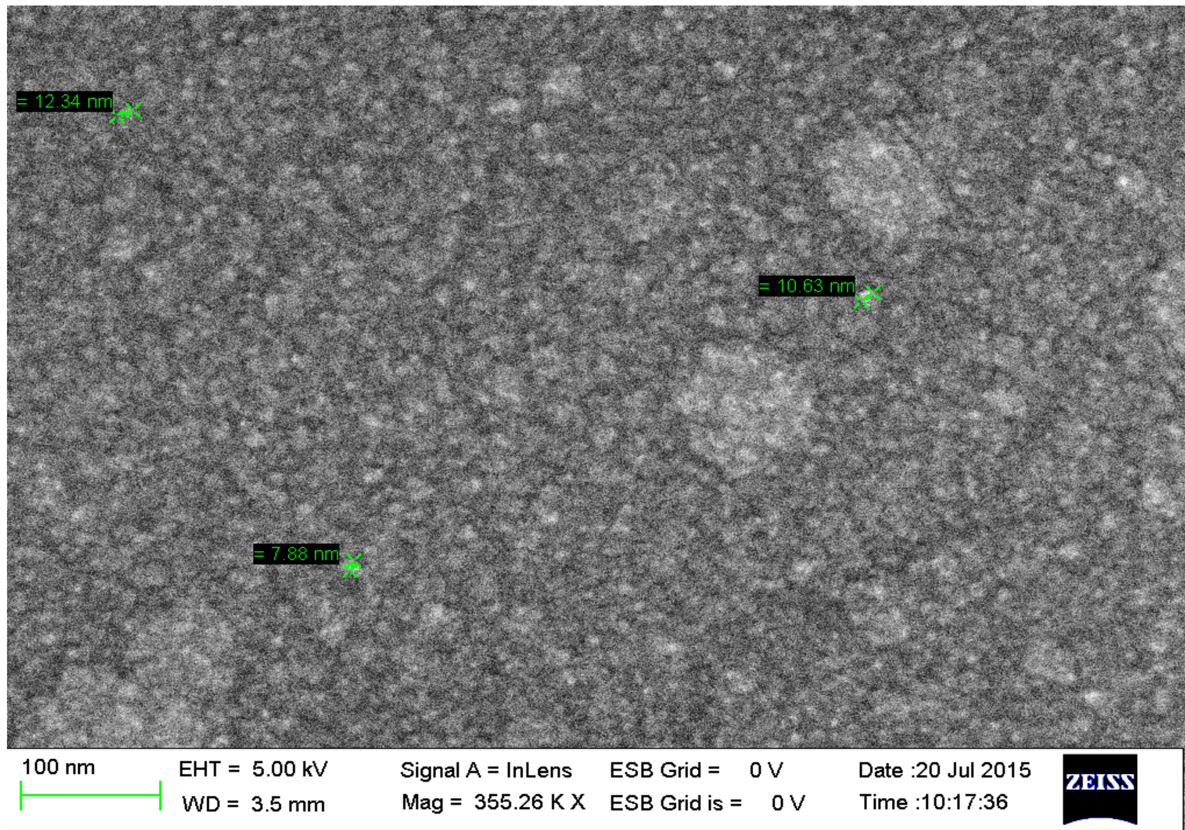


(a)

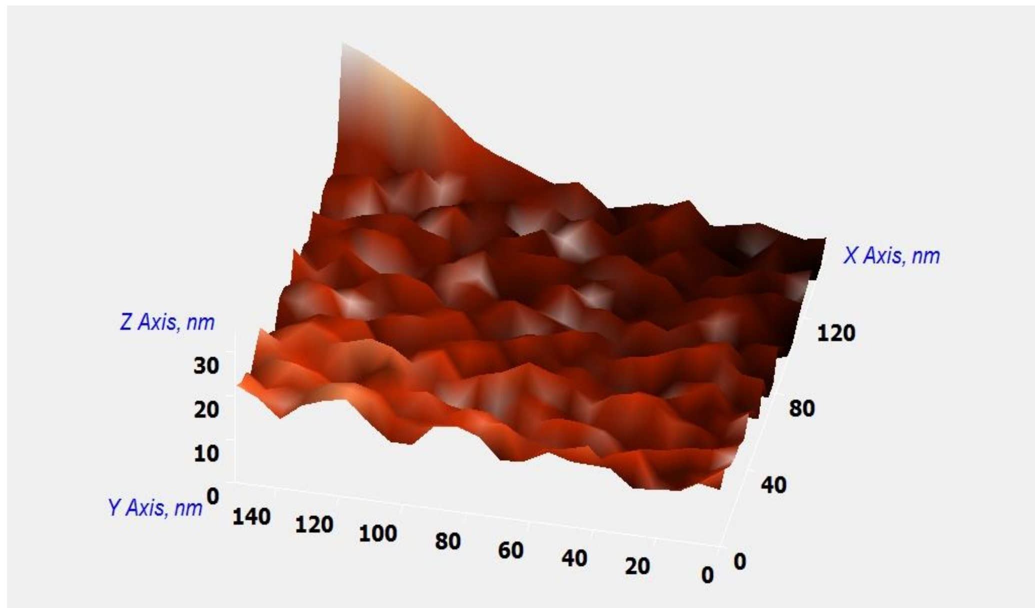


(b)

Fig. 3.9. Results of 150nm thick nc-Si:H film (a) SEM Micrograph (b) AFM Graph



(a)



(b)

Fig. 3.10. Results of 200nm thick nc-Si:H film (a) SEM Micrograph (b) AFM Graph

3.4.2 Conductivity Measurement

To demonstrate the feasibility of nc-Si:H film for TFT application, the average conductivity of 100nm thick deposited film was measured using 4-probe method and calculated from measured I-V data as shown in Fig. 3.11.

The calculations are as follows-

Resistivity of film, $\rho_f = R_s$ (Sheet resistance) x t_{si} (nc-Si:H film thickness)

$\rho_f = 1/0.00138 \text{ x } 100\text{nm} = 0.01\Omega\text{cm}$

Conductivity of nc-Si:H film, $\sigma_{eff} = 1/\rho_f = 100$ S/cm

The high conductivity equals to 100S/cm is achieved. This result validates that the deposited film is highly suitable as channel layer for the fabrication of TFT because it is highly conductivity in nature which attributed to high effective mobility [24].

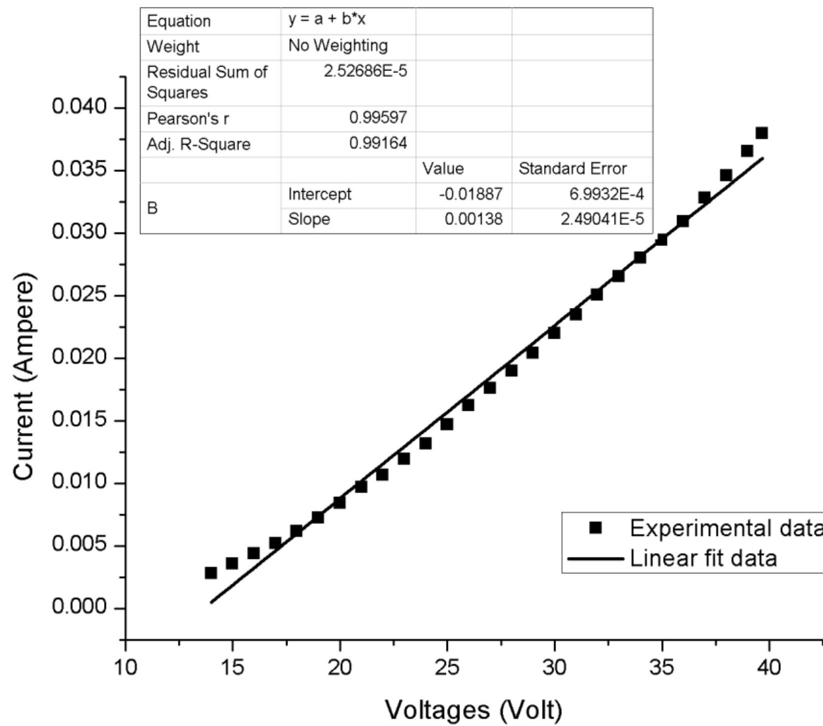


Fig. 3.11. I-V curve for 100nm thick nc-Si:H film. Square dotted line represents the experimental I-V data extracted using 4-probe method. Solid line shows the fitted data which gives the slope of 0.00138

3.5. CONCLUSION

The EBPVD process is used for nc-Si:H film deposition over conventional PECVD process because in PECVD, high RF-power and hydrogen dilution are needed to facilitate silicon nano-crystallization which leads to deteriorated quality of nc-Si:H film. In this work, the nc-Si:H films having thickness 100nm was deposited on Corning glass 1737 substrate using EBPVD method in the vacuum of 8 x 10^{-6} Torr with controlled beam current and deposition rate at moderately low temperature. The deposited nc-Si:H film was further characterized using XRD, FESEM, EDS, Raman Spectroscopy and AFM. The characterization results confirm the nanocrystalline nature of the deposited film. The nc-Si:H films with different thicknesses (i.e. 100nm, 150nm and 200nm) are also deposited to analyze the effect of film thickness. The FESEM and AFM results shows that the grain size increases as film thickness increases which validates the cone shape type growth of nc-Si:H film. The results indicate that EBPVD is the cost effective alternative of PECVD. The controlled grain size and required thickness of nc-Si:H film can be easily achieved by EBPVD for the fabrication of TFTs.

To validate the feasibility of deposited nc-Si:H film for TFT application, conductivity measurement of deposited film was done using four-probe method and the conductivity of approx. 100 S/cm was achieved. This highly conductive film with nanometer size grains is highly suitable as channel layer for the fabrication of TFT because it can provides high effective mobility and high on-current.

From the surface morphology of nc-Si:H film it is clear that nc-Si:H possess grain separated by grain boundaries, however the size of grain is very less (~5 to 12nm) as compared to poly-Si which provide difference in the behavior of TFT fabricated using nc-Si:H film. All the outcomes of the study are used in developing the conduction model for nc-Si:H TFTs.

CHAPTER - 4

MATERIAL SELECTION FOR GATE DIELECTRIC

4.1. INTRODUCTION

The rapid performance improvement in flat panel displays has been achieved by scaling down the size of TFT. However the reduction in size of TFT and thus of gate dielectric causes two major problems that are leakage current and reliability [94]. The SiO_2 material has been used as a gate dielectric for decades due to its remarkable properties like large bandgap, large conduction band offset, low Si/SiO_2 interface trap density, high resistivity but scaling down of SiO_2 after tunneling limit may lead to the high leakage current. The high leakage current is due to direct tunneling of electrons from the conduction band of channel layer to the gate without going through thin gate oxide tunneling barrier. Thus prevention of leakage current requires a suitable gate dielectric that must have high dielectric constant greater than SiO_2 (~3.9).

The high-k dielectric material basically provides very high capacitance densities at relatively higher physical thickness of gate insulator with wider tunneling barrier and thus avoids the adverse effect of thin gate insulator. Various high-k dielectric materials like Si_3N_4, Al_2O_3, ZrO_2, Ta_2O_5 and HfO_2 are being investigated for the gate insulator of nc-Si:H TFT [30, 80, 95] however each of these high-k materials imposes some practical challenges. Therefore selection of best high-k material is necessary in order to improve nc-Si:H TFT performance. The most common technique used for selecting the best alternative from the set of possible alternatives with respect to

predefined attributes is the Multi-Criteria Decision Making (MCDM) technique [96]. MCDM techniques are classified as Multi-objective decision making (MODM) and Multi- attribute decision making (MADM). The role of MCDM techniques has been justified by many researchers in numerous applications and case studies [97-101]. In MODM approach, optimization of alternative is carried out based on the prioritized objectives however in MADM approach, ranking and thus the selection of best alternative or alternatives is performed on the basis of prioritized attributes.

In present work, most popular MODM technique known as Ashby's approach [97, 98] and well established MADM techniques known as VIKOR (VlseKriterijumska Optimizacija I Kompromisno Resenje in Serbian) [99, 100] and TOPSIS (Technique for order preference by similarity to ideal solution) [101] are defined and investigated. Ashby's technique is widely used by the design experts for selecting the best alternative however it basically unable to generate ranking score when the numerous performance indices are present. In comparison to this, VIKOR and TOPSIS are well stable approaches and are commonly used for wide range of material selection problem. The major differences between VIKOR and TOPSIS approaches are as follows [102]:

1) VIKOR method uses linear normalization whereas TOPSIS method uses vector normalization in order to convert different scales of various criteria into standard measureable units.

2) VIKOR method provides the compromise solution by determining maximum group utility of the majority and minimum individual regret of the opponent whereas TOPSIS method provides the solution by determining the shortest distance from the ideal solution and greatest distance from the negative ideal solution.

4.2. MATERIAL SELECTION APPROACHES

Material selection approaches provide an easy way to recognize the trade-offs between conflicting materials properties and also to select the optimal material for better device performance. In addition to this, these approaches also help us to provide ranking to the alternatives from best to worst. Therefore, these approaches provide a platform to select and prioritize the possible materials and also provide support to perform rigorous evaluation of the possible alternatives.

The flowchart used for material selection analysis is shown in Fig. 4.1.

4.2.1. Ashby's Approach

M. F. Ashby's [97, 98] provides effective material selection approach to select the best material based on their material and performance indices for better device performance.

Material indices are group of material properties which enhance the device performance for a given requirement. These material indices are derived based on the device requirement through the investigation of objectives and constraint. Performance index is a combination of material indices which governs some characteristics of device performance.

This approach involved four basic steps. In first step, the design requirements are translated into the objectives that are necessary to optimize the device performance and the constraints that material must meet. In second step, the wide choices of possible materials are confined, first by applying the constraints which screen out the materials that do not fulfill the design requirement and then by considering the material indices. In third step, ranking is provided to the material based on their ability to fulfill the objective and to provide the better performance. In next step, the supporting information for the shortlist material termed as prime candidate is explored and final result of best suitable material is compared with the supporting experimental data.

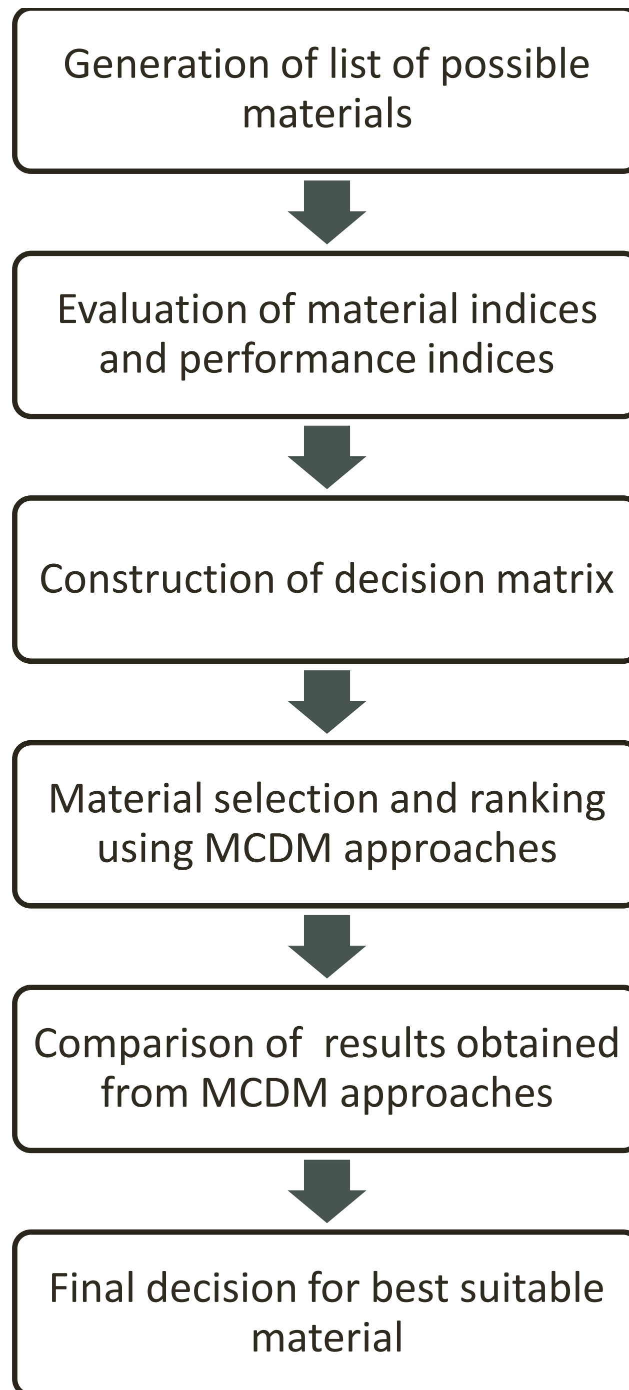


Fig. 4.1. Flowchart for material selection

In Ashby's approach, the design of a material is described by three attributes as

$P = f$ [(Functional requirements, F), (Geometric parameters, G), (Material indices, M)]

$$\text{or } P = f[F,G,M] \tag{4.1}$$

where f defines as a function which describes few aspects of the performance (P) of the material.

The variables in equation (4.1) are said to be separable when this can be expressed as

$$P = f_1(F)\, f_2(G)\, f_3(M) \tag{4.2}$$

where f_1, f_2, f_3 are separated functions.

4.2.2. VIKOR Approach

This approach was first proposed by Opricovic in 1998 [100] which provides the ranking list of various alternatives based on the agreement established by mutual concessions and also determines the feasible solution close to the ideal solution for a problem with conflicting criteria. This compromise solution can help the design expert to make the final decision.

Step 1- Determine the best x_j^* and the worst x_j^- values of all criterion functions, where $j=1, 2,..,n$. If the jth criterion represents a benefit criterion then $x_j^* = max\ x_{ij}$, $x_j^- = min\ x_{ij}$ and if j^{th} criterion represents a cost criterion then $x_j^* = min\ x_{ij}$, $x_j^- = max\ x_{ij}$ for $i=1, 2,\ldots,m$. For this, we have to form a decision matrix, X based on the respective values of defined attributes for possible alternatives.

Step 2- Construct the maximum group utility G_i and minimum regret of the opponent R_i values for i=1,2,…,m by the following relation:

$$G_i = \sum_{j=1}^{n} w_j \frac{\left(x_j^* - x_{ij}\right)}{(x_j^* - x_j^-)} \tag{4.3}$$

$$R_i = \max_j \left[w_j \frac{\left(x_j^* - x_{ij}\right)}{(x_j^* - x_j^-)} \right] \tag{4.4}$$

where w_j are the weights of criteria, expressing their relative importance and given as,

$$\sum_{j=1}^{n} w_j = 1 \quad \text{for j=1,2,3,….,n}$$

The labels for the weighting are as follows:

w = {*Essential; Very High; Fairly High; High; Moderate; Low; Fairly Low; Very Low; Unnecessary*}

Step 3- Calculate the value of Q_i, i=1,2…,m, by the following equation

$$Q_i = v\frac{G_i - G^*}{G^- - G^*} + (1-v)\frac{R_i - R^*}{R^- - R^*} \tag{4.5}$$

where G^* = min G_i, G^- = max G_i , R^* = min R_i, R^- = max R_i and v is usually taken as 0.5 and is consider as weight for strategy of G_i and (v-1) is the weight of R_i.

Step 4- Compute the ranking order (A^1, A^2, ..., A^m) of the alternatives by sorting the values of G, R and Q in the increasing order.

Step 5- Propose the compromise solution, alternative A^1, which is best ranked by having minimum value of measure Q, if the following conditions are satisfied:

Condition 1: “Acceptable advantage”- $Q(A^2)$- $Q(A^1) \geq DQ$, where $DQ=1/(m-1)$.

Condition 2: “Acceptable stability in decision making” – Alternative A^1 must have minimum value of measure G or/and R. If this condition is satisfied then it means the proposed compromise solution is stable within a decision making process whether it is: “voting by majority rule” (v>0.5), “by consensus” (v=0.5), or “with vote” (v<0.5).

If one of the above conditions are not satisfied then a set of compromise alternatives, consists of alternative A^1 and A^2 if condition (2) is not satisfied and alternatives A^1, A^2, ..., A^m if condition (1) is not satisfied, is proposed. The value of A^m is computed by relation $Q(A^m) - Q(A^1) < DQ$ for maximum value of m and the position of these alternatives A^1, A^2, ..., A^m are very close to each other.

4.2.3. TOPSIS Approach

TOPSIS approach was proposed by K. Yoon and H. C. Lai in 1981 [101]. This decision making approach is basically used to determine the best alternative which

should have shortest Euclidean distance (S^*) from the ideal solution (A^*) and largest Euclidean distance (S^-) from negative ideal solution (A^-)

The various steps involved in TOPSIS decision making approach are as follows:

Step 1- To prepare normalized decision matrix

Normalized decision matrix N_m, consists of $n_{ij,}$ elements with i^{th} number of alternatives under j^{th} number of criterion.

$$n_{\mathrm{ij}} = \frac{x_{\mathrm{ij}}}{\sqrt{\sum_{i=1}^{m}\left(x_{ij}\right)^2}} \tag{4.6}$$

where i, set of alternatives$=1,2,3,\ldots\ldots.m$ and $j,$ set of criteria$=1,2,3,\ldots.,n$

Step 2- To construct weighted normalized matrix

Weighted normalized matrix, V consists of elements v_{ij} and is basically the product of normalized decision matrix, N_m and the weights of criteria $W= \{w_j\}$ and thus given as

$$v_{ij} = n_{ij} \times w_j \qquad \text{for } i = 1,2,3,\ldots\ldots.m\ , \quad j = 1,2,3,\ldots.,n \tag{4.7}$$

where $\sum_{j=1}^{n} w_j = 1$ for $j=1,2,3,\ldots.,n$

Step 3- To generate ideal and negative ideal solutions

The ideal solution ($A*$) and negative ideal solution (A^-) for the weighted normalized matrix are given as

$$A^* = \{(\max v_{ij} |\ j \in J_1), (\min v_{ij} |\ j \in J_2)\} \quad = \{v_1^*, v_2^*, \ldots\ldots, v_n^*\} \tag{4.8}$$

$$A^- = \{(\min v_{ij} |\ j \in J_1), (\max v_{ij} |\ j \in J_2)\} \quad = \{v_1^-, v_2^-, \ldots\ldots, v_n^-\} \tag{4.9}$$

where $J_1 = \{j=1,2,3\ldots.,n\}$ and j is associated with beneficial criteria

$J_2 = \{j=1,2,3\ldots.,n\}$ and j is associated with cost criteria.

Step 4- To calculate the separation measure

The separation measures for ideal and negative ideal solution can be calculated by using Euclidean distance method and is given by

$$S_i^* = \sqrt{\sum_{j=1}^{n}\left(v_{ij} - v_j^*\right)^2} \text{, from ideal solution} \qquad \textit{for } i = 1,2,3,\ldots.,m \tag{4.10}$$

$$S_i^- = \sqrt{\sum_{j=1}^{n}\left(v_{ij} - v_j^-\right)^2} \text{, from negative ideal solution} \qquad \textit{for } i = 1,2,3,\ldots.,m \tag{4.11}$$

Step 5- To measure the relative closeness to the ideal solution

$$Z_i = \frac{S_i^-}{S_i^* + S_i^-} \qquad 0 < Z_i < 1, \text{ for } i = 1,2,3,....,m \tag{4.12}$$

Step 6- To ranked the alternatives

Provide the ranking to the alternatives based on the Z_i value. The larger value of Z_i corresponds to the better performance of the alternative.

4.3. PERFORMANCE AND MATERIAL INDICES

Two major problems caused due to the reduction in the size of nc-Si:H TFT and the gate dielectric, are leakage current and reliability. Hence leakage current and drain current are considered as two main performance indices in this analysis. These performance indices have to be defined in the form of material properties in order to determine the material indices for nc-Si:H TFT.

In nc-Si:H TFT, the responsible mechanism for leakage current under high gate-source voltage (V_{GS}) and high drain-source voltage (V_{DS}) is basically the Poole-Frenkel (PF) emission in the drain depletion region and is given as [103]

$$I_{PF} = I_{PF0} \exp(\beta_{PF} \sqrt{E_{pk}}) \tag{4.13}$$

where I_{PFO} is the generation current at zero electric field and E_{pk} is the peak electric field given as:

$$E_{pk} = |V_{GS} - V_{DS} - V_{FB}| \varepsilon_i / t_i \varepsilon_{si} \tag{4.14}$$

where V_{FB} is the flat band voltage, ε_i is dielectric constant of gate insulator, t_i is thickness of gate insulator and $\varepsilon_{nc\text{-}Si}$ is the permittivity of nc-Si:H channel layer

β_{PF} in eq. (4.13) is the PF coefficient [104]

$$\beta_{PF} = q^{\frac{3}{2}} / \sqrt{\pi \varepsilon_{nc-si}} kT \tag{4.15}$$

where k is the Boltzmann constant and T is the temperature

The drain current (I_{DS}) of nc-Si:H TFT under the linear region can be extracted by using conventional MOSFET theory,

$$I_{DS} = \mu_{eff} \frac{W}{L} C_i \left[V_{DS}(V_{GS} - V_T) - \frac{V_{DS}^{\ 2}}{2} \right] \tag{4.16}$$

As the reduction in size require scaling of gate insulator thickness in order to achieve high capacitance densities and thus high drain current. The capacitance density C_i (F/cm^2) is given as [94]:

$$C_i = \frac{\varepsilon_o \varepsilon_i}{t_i} \tag{4.17}$$

where ε_o is the permittivity of free space.

TFT requires low leakage current and high drain current for the better device performance and it is clear from equation (4.13) and (4.14) that ε_i should be low in order to get low leakage current. However, ε_i should be high in order to get high capacitance density (given by equation (4.17)) and thus high drain current. Therefore, the first material index (MI_1) related to leakage current and drain current is ε_i and is expressed as,

$$MI_1 = \varepsilon_i \tag{4.18}$$

The high band gap corresponds to high energy barrier height for the electrons tunneling process and therefore less leakage current. The energy band gap (E_g) of high-k material is given as [105]

$$E_g \approx 20 \left(\frac{3}{2 + \varepsilon_{i,high-k}} \right)^2 (eV) \tag{4.19}$$

where $\varepsilon_{i,high-k}$ is the dielectric constant of high-k material. So, the second material index (MI_2) related to leakage current is energy band gap E_g and is given by,

$$MI_2 = E_g \tag{4.20}$$

Conduction band offset (ΔE_C) defines the barrier height between gate dielectric layer and silicon substrate when the electrons travel from substrate to gate. High-k material which have large conduction band offset is required to prevent the unwanted leakage

current through the gate dielectric. Generally, it is difficult to reduce leakage current because the energy band gap and dielectric constant shows inverse correlation. Therefore, the third material index (MI_3) related to leakage current is conduction band offset ΔE_C and is described by,

$$MI_3 = \Delta E_C \tag{4.21}$$

The various impurities and crystal defects exists in semiconductor and gate insulator layers even if these are deposited under clean and controlled processes. These defects causes the generation of excess ions and electrons that presents at the interface between semiconductor and gate insulator and are responsible for interface trapped charge (Q_{it}) (illustrated in Fig. 4.2). The interface trapped charges causes the energy states of the device to be different than that of semiconductor alone. When the bias is applied to the device, the interface charge density (D_{it}) ramps from deep depletion region to accumulation or vice versa and along with this the Fermi level at the surface will go through each interface-impurity-allowed energy state and the charge state of trap must be change at each energy level. As Q_{it} can vary with allowed energy state, D_{it} can be given by charge number per electron volt per area ($cm^{-2}eV^{-1}$).

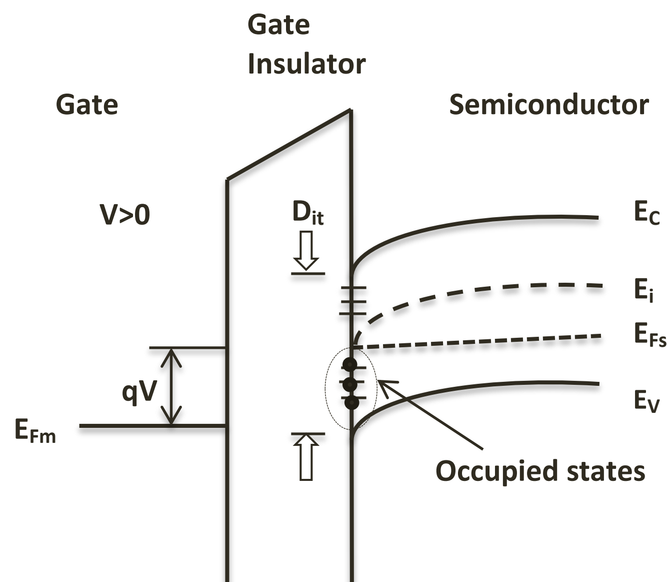


Fig. 4.2. Location of interface trap charges [106]

The interface trap density D_{it} (~ $cm^{-2}eV^{-1}$) is given as [107]:

$$D_{it} = \frac{C_i}{q}\left(\frac{C_{LF}}{C_i - C_{LF}} - \frac{C_{HF}}{C_i - C_{HF}}\right) \tag{4.22}$$

where C_i is the gate insulator capacitance, C_{LF} and C_{HF} are the capacitance measured at the onset of strong inversion at low and high frequencies respectively. The interface trap density is the key parameter and it should be less in order to improve the device performance. Therefore, the fourth material index (MI_4) related to leakage current is interface trap density D_{it} and is given by,

$$MI_4 = D_{it} \tag{4.23}$$

Therefore, the two performance indices that are considered in present material selection analysis are defined as,

$$PI_1 = f(\varepsilon_i) \tag{4.24}$$

$$PI_2 = f(\varepsilon_i, E_g, \Delta E_C, D_{it}) \tag{4.25}$$

4.4. RESULTS AND ANALYSIS

Three material selection methodologies; Ashby's, VIKOR and TOPSIS are applied to select the most suitable gate dielectric material for nc-Si:H TFT. The material properties of the possible high-k gate dielectric materials are given in Table 4.1.

4.4.1. Ashby's Approach

Fig.4.3-4.5 shows the variation of band gap, dielectric constant and conduction band offset vs. interface trap density respectively, for possible high-k materials for nc-Si:H TFT.

It can be observed from the Fig. 4.3 that all the possible high-k materials i.e. Al_2O_3, Si_3N_4, ZrO_2 and HfO_2 shows sufficient dielectric constant greater than SiO_2 (~3.9) and thus satisfy the dielectric constant constraint. However, from the Fig. 4.4 and Fig. 4.5, it is found that Ta_2O_5 have lowest bandgap and lowest conduction band offset as compared to other high-k dielectric materials and thus Ta_2O_5 may causes device performance degradation by generating high leakage current and hence eliminated from the choice of gate dielectric material.

Similarly, from Fig. 4.4 and Fig 4.5, it is clear that Al_2O_3 shows higher band gap and higher conduction band offset compared to other high-k materials but it shows very high interface trap density, as shown in Fig. 4.3, which causes increase in threshold voltage. Therefore Al_2O_3 material is also eliminated from the list of choices of gate dielectric material.

Fig.4.4 also shows that although Si_3N_4 have lower bandgap but it shows larger conduction band offset and lower interface trap density compared to ZrO_2 and HfO_2 materials as shown in Fig. 4.5.

So, the Ashby's approach result shows that the Si_3N_4 is the most suitable candidate for the gate dielectric of nc-Si:H TFT.

Table 4.1: Properties of possible high-k gate dielectric material [108-110]

Gate Dielectric Materials	Dielectric constant ($\varepsilon_{i,high\text{-}k}$)	Band gap (eV)	Conduction band offset (eV)	Interface trap density ($\times 10^{10} cm^{-2} eV^{-1}$)
Si_3N_4	7	5.3	2.4	120
Al_2O_3	9	8.8	2.8	300
ZrO_2	25	5.8	1.5	200
HfO_2	25	5.8	1.4	200
Ta_2O_5	22	4.4	0.35	160

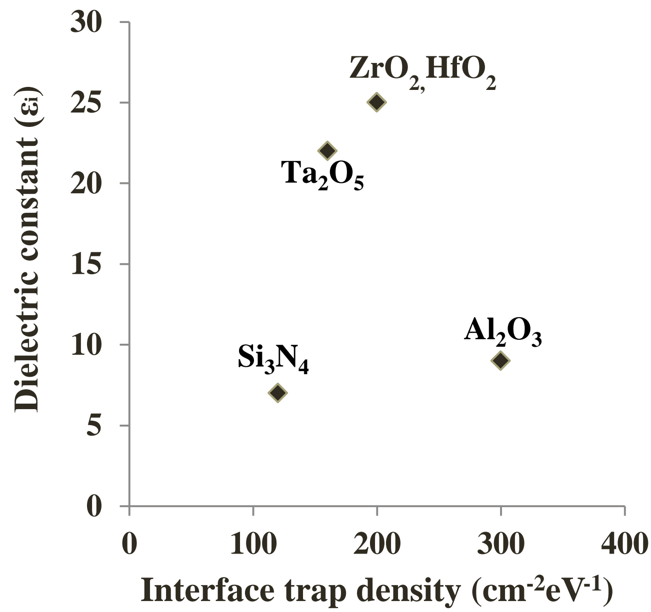


Fig. 4.3. Variation of dielectric constant vs. interface trap density for different possible high-k gate dielectric material

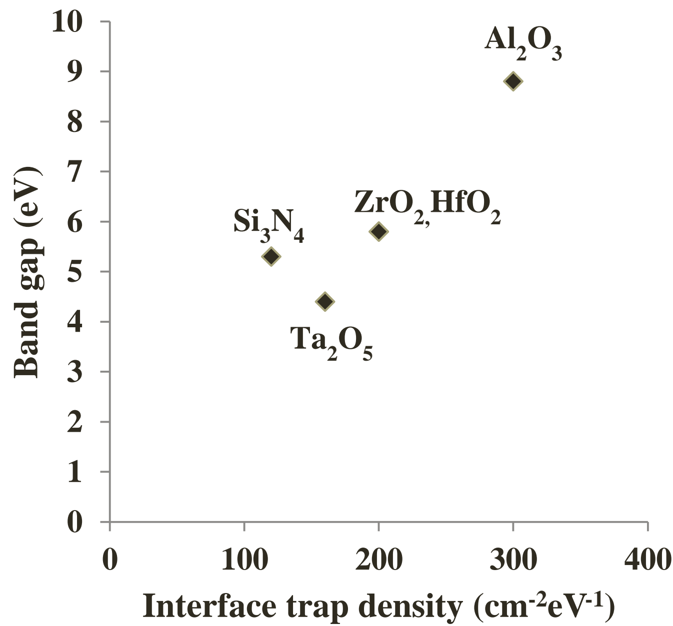


Fig. 4.4. Variation of band gap vs. interface trap density for different possible high-k gate dielectric material

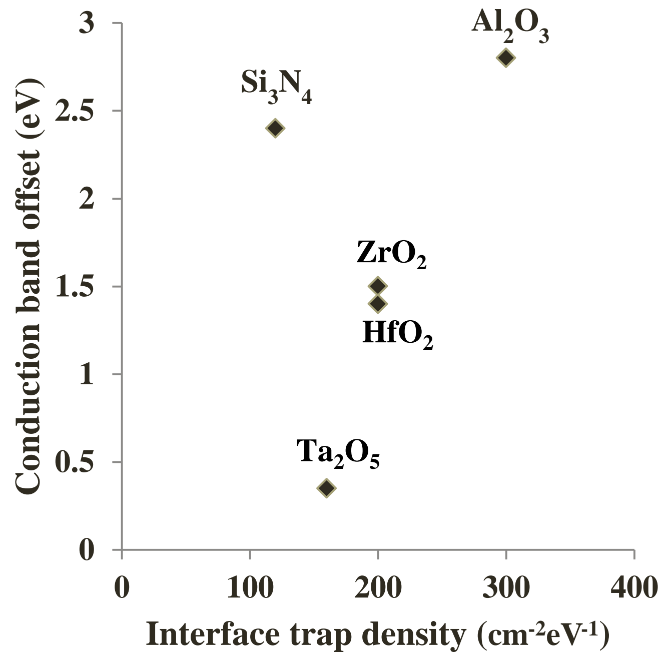


Fig. 4.5. Variation of conduction band offset vs. interface trap density for different possible high-k gate dielectric material

4.4.2. VIKOR Approach

The decision matrix on the basis of the respective values of defined attributes for possible alternatives (as mentioned in Table 4.1) is given as:

$$\text{Decision matrix, } X = \begin{bmatrix} 7 & 5.3 & 2.4 & 40 \\ 9 & 8.8 & 2.8 & 300 \\ 25 & 5.8 & 1.5 & 200 \\ 25 & 5.8 & 1.4 & 200 \\ 22 & 4.4 & 0.35 & 160 \end{bmatrix}$$

For the determination of weights we have considered essential, very high, fairly high and high weight for interface trap density, conduction band offset, band gap and dielectric constant respectively. The interface trap density is the most crucial and essential indices as compared to other material indices because the high value of interface trap density causes Fermi level pinning which prevents control over channel

charge carrier and thereby severely affects the drive current of nc-Si:H TFT. In addition to this, the dielectric constant is weighted less as compared to other parameter because nc-Si:H TFT is usually used for large area applications and therefore sufficient value of dielectric constant is enough for the fabrication of nc-Si:H TFT.

Weight of criteria, $w_j = \begin{bmatrix} 0.1 & 0.2 & 0.3 & 0.4 \end{bmatrix}$

By using equations (4.3) to (4.5), we can calculate maximum group utility (G), minimum regret of opponent (R) and Q values as shown in Table 4.2 to compute the ranking of possible alternatives. The computed values of G^*, G^-, R^* and R^- are 0.2079, 0.6056, 0.1590 and 0.4 respectively.

The results of VIKOR approach proposed Si_3N_4 as the best alternative. This solution is acceptable because it satisfy condition 1 by having minimum *G* and *R* value and also satisfy condition 2 by having $Q(A^2)-Q(A^1)=0.373-0=0.373$ greater than $DQ=1/(5-1)=0.25$.

Table 4.2: Ranking of alternatives by VIKOR approach

Gate Dielectric Materials	**Maximum group utility, *G***	**Ranking based on *G* values**	**Minimum regret of opponent, *R***	**Ranking based on *R* values**	***Q* (v=0.5)**	**VIKOR Ranking**
Si_3N_4	0.2079	1	0.1590	1	0	A1
Al_2O_3	0.4880	4	0.4	4	0.8521	A5
ZrO_2	0.4734	2	0.1778	2	0.3730	A2
HfO_2	0.4856	3	0.1778	2	0.3880	A3
Ta_2O_5	0.6056	5	0.3	3	0.7925	A4

4.4.3. TOPSIS Approach

Normalized decision matrix:

$$N = \begin{bmatrix} 0.1621 & 0.3823 & 0.5667 & 0.2618 \\ 0.2084 & 0.6348 & 0.6612 & 0.6546 \\ 0.5790 & 0.4184 & 0.3542 & 0.4360 \\ 0.5790 & 0.4184 & 0.3306 & 0.4360 \\ 0.5096 & 0.3174 & 0.0826 & 0.3491 \end{bmatrix}$$

Weighted matrix:

$$W = \begin{bmatrix} 0.1 & 0.2 & 0.3 & 0.4 \end{bmatrix}$$

Weighted normalized matrix:

$$V = \begin{bmatrix} 0.0162 & 0.0764 & 0.1700 & 0.1047 \\ 0.0208 & 0.1269 & 0.1984 & 0.2618 \\ 0.0579 & 0.0836 & 0.1063 & 0.1744 \\ 0.0579 & 0.0836 & 0.0992 & 0.1744 \\ 0.0509 & 0.0634 & 0.0248 & 0.1396 \end{bmatrix}$$

By using TOPSIS method, we can compute the values of S^*, S^- and Z using equations (4.10)-(4.12). These values are listed in Table 4.3 to further determine the ranking of possible alternatives. The results obtained by TOPSIS approach also shows higher ranking for Si_3N_4.Hence, all the three material selection methodologies shows that Si_3N_4 is the best high-k gate dielectric for nc-Si:H TFT. Lee [30] reported high stability and better performance of nc-Si:H TFTs using Si_3N_4 as the gate dielectric. This confirms the validity of the proposed analysis.

Table 4.3: Ranking of alternatives by TOPSIS approach

Gate Dielectric Materials	S^*	S^-	Z	**TOPSIS Ranking**
Si_3N_4	0.0714	0.2143	0.7501	1
Al_2O_3	0.1615	0.1848	0.5336	2
ZrO_2	0.1229	0.1280	0.5101	3
HfO_2	0.1287	0.1236	0.4898	4
Ta_2O_5	0.1881	0.1270	0.4030	5

4.5. CONCLUSION

In this chapter, material selection for the gate insulator layer of nc-Si:H TFTs using three methodologies i.e. Ashby's approach, VIKOR and TOPSIS methods is presented. Ashby's approach can provide best material however it cannot give the ranks of the alternatives therefore to further validate the results and for getting the ranks of the materials MADM like TOPSIS and VIKOR approaches are used. Si_3N_4, Al_2O_3, ZrO_2, Ta_2O_5 and HfO_2 materials are being investigated for the gate insulator of nc-Si:H TFT. Four material indices (band gap, dielectric constant, conduction band offset and interface trap density) and two performance indices (drain current and leakage current) are considered for material selection analysis. The analysis shows that for better performance and less leakage current in nc-Si:H TFT, Si_3N_4 material is the best possible gate dielectric for nc-Si:H TFT. The result shows very good agreement between Ashby's, VIKOR and TOPSIS approaches and also with the experimental findings. In this thesis, Si_3N_4 material is used as the gate dielectric for the modeling and performance analysis of nc-Si:H TFT.

CHAPTER 5

ELECTRICAL CHARACTERISTICS

5.1. INTRODUCTION

An accurate analytical model for a new device is prerequisite for utilizing the devices in circuit designs. A number of researchers have analyzed the problem both numerically and analytically [38, 39, 42, 46, 48] and some insights have begun to emerge. Dosev et. al. [38] presented an analytical model related to physical phenomenon responsible for the different operation regimes of the nc-Si:H TFT. They proposed that, in nc-Si:H the density of the defect states (i.e. DOS) is lower than in a-Si:H because of the higher internal atomic order. A. Cerdeira et. al. [39] presented drain current model covering a second region observed in the above-threshold regime for nc-Si:H TFT devices, which are not present in a-Si:H TFTs. A. T. Hatzopoulos et. al. [42] presented the drain current model above threshold voltage, based on an exponential energy distribution of band tail states. However, these models [38, 39, 42] could not explain the influence of doping density, trapping state density, gate insulator thickness and temperature on the threshold voltage of the nc-Si:H TFT. Ling-Feng Mao [46] demonstrated the impact of the temperature and doping density on the threshold voltage however not discussed the trapping state density and gate insulator thickness dependence on threshold voltage. In addition, the effect of grain boundaries available in nc-Si:H film on the performance of nc-Si:H TFT was not discussed by the researchers [38, 39, 42, 46]. Steinke and Ruden [48] presented a model for determining the threshold voltage in nc-Si:H TFTs by examining the multiple boundaries between neighboring crystalline grains, which limits the charge-

carrier transport, using Monte-Carlo simulations. However, this model only describes transistor behavior near-threshold and could not explain the linear behavior soon after the transistor is turned on at low drain bias.

It is worth studying, how the threshold voltage in nc-Si:H TFTs is affected by gate insulator thickness and grain boundary trapping states at different doping density and temperature. Moreover, it is required to analyze the effect of grain boundaries that are present in nc-Si:H film (as discussed in chapter 3) on the performance of nc-Si:H TFT. In this chapter, an analytical model for calculating the threshold voltage and effective mobility in n-channel nc-Si:H TFT is developed which is further used to drive drain current and the respective device transfer characteristic.

This chapter is organized as follows: First section, presents an analytical model for calculating the threshold voltage using one-dimensional Poisson's equation. In this study, it is assumed that the gate insulator-silicon interface traps are uniformly distributed across the interface region and the channel of the device contains large number of grain boundaries. Based on this assumption, this section presents a simple and unique model for extracting the value of threshold voltage.

Second section describes the effect of grain boundaries in nc-Si:H TFT and presents the influence of all the effects on mobility and hence on the drain current. It is clear from the deposition of nc-Si:H film that the channel layer contains grains separated by grain boundaries. Therefore, in this study, it is assumed that the nc-Si:H film which is used as the channel material in TFT consists of grain boundaries perpendicular as well as parallel to the carrier flow. In this section, analytical model for mobility due to perpendicular grain boundaries and mobility due to parallel grain boundaries are developed separately and then the overall effective mobility is calculated incorporating both types of grain boundaries.

5.2. ANALYTICAL DEVICE MODELING

The schematic view of top-gate nc-Si:H TFT shown in Fig 5.1 consists of a glass substrate, above which a nc-Si:H layer is used to form the channel followed by silicon nitride (Si_3N_4) layer which acts as a gate dielectric. Fig. 5.2 shows energy band diagram of top-gate nc-Si:H TFT under strong inversion or ON-state condition.

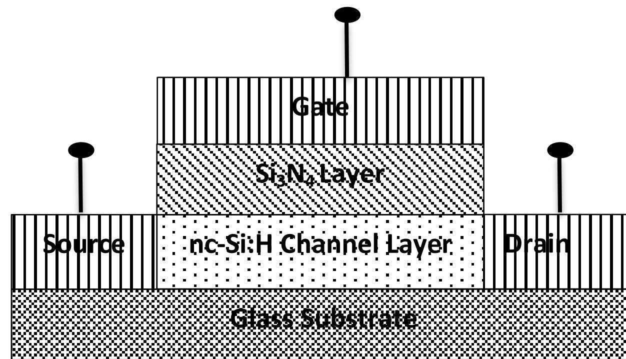


Fig. 5.1. Schematic view of top-gate nc-Si:H TFTs

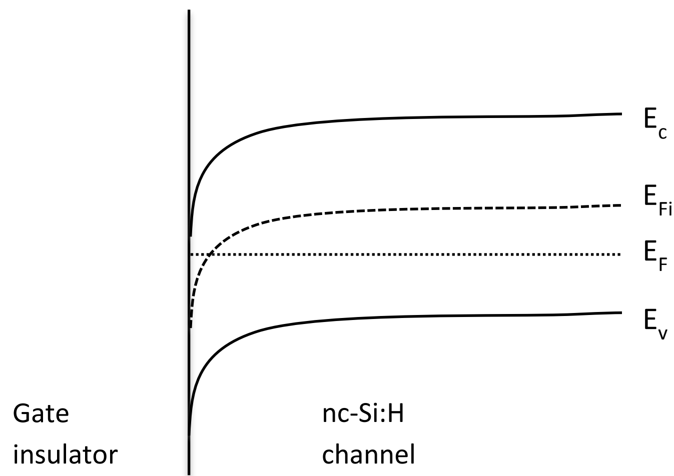


Fig. 5.2. Energy band diagram of top-gate nc-Si:H TFT under strong inversion condition

5.2.1. Threshold Voltage

Threshold voltage plays an important role in device modeling for switching applications. So it is required to satisfy its behavior due to various effects in operating temperature. In present analysis, the Poisson's equation in one dimensional form is used for determining the band bending at the gate insulator/nc-Si:H layer interface of the TFT, which is given as:

$$\frac{\partial^2 \varphi}{\partial x^2} = -\frac{\rho}{\varepsilon_{nc-Si}} \tag{5.1}$$

where φ is the electrostatic potential, ρ is the charge density and ε_{nc-Si} is the screening dielectric constant of nc-Si:H layer which can be calculated theoretically by using the formula [111] given as:

$$\varepsilon_{nc-Si}(D_G) = 1 + \frac{10.4}{1 + \left(\frac{1.38}{D_G \times 10^7}\right)^{1.37}} \tag{5.2}$$

where D_G is the average grain size (in cm).

The charge density ρ is related to the density of trapping states N_t ($cm^{-3}eV^{-1}$) in nc-Si:H film, by the following equation

$$\rho = -q^2 N_t \varphi \tag{5.3}$$

Equation (5.1) can also be written in the form of electric field E as

$$E\frac{\partial E}{\partial \varphi} = q^2 N_t \frac{\varphi}{\varepsilon_{nc-Si}} \tag{5.4}$$

In order to get surface electric field, integrating equation (5.4) from the bulk towards the surface as

$$\int_{Bulk}^{Surface} E\partial E = \frac{q^2 N_t}{\varepsilon_{nc-Si}} \int_{Bulk}^{Surface} \varphi \partial \varphi \tag{5.5}$$

which gives surface electric field as

$$E_s = q\varphi_s \sqrt{\frac{N_t}{\varepsilon_{nc-Si}}} \tag{5.6}$$

where φ_s is the surface potential and under strong inversion can be given as

$$\varphi_{s(inv)} \approx 2\varphi_F \approx 2\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) \tag{5.7}$$

where φ_F is the Fermi potential, N_a is the doping density (cm^{-3}), k is Boltzmann's constant, T is the temperature and n_i is the intrinsic carrier density which can be calculated by using the equation [106]

$$n_i = 2\left(\frac{2\pi kT}{h^2}\right)^{\frac{3}{2}}\left(m_n^* m_p^*\right)^{\frac{3}{4}} e^{-\frac{E_g}{2kT}} \tag{5.8}$$

where h is the Planck's constant, E_g is the bandgap energy (= 1.12eV) and m_n^* and m_p^* are the effective electrons and holes masses in nc-Si:H given as $m_n^*=0.34m_o$ and $m_p^*=0.55m_o$ [111].

Now the gate insulator electric field can be determined by using the following equation

$$E_i = \frac{\varepsilon_{nc-Si}}{\varepsilon_i} E_S \tag{5.9}$$

where ε_i is the dielectric constant of insulating layer. In this study, we have assumed the insulating layer as silicon nitride (Si_3N_4).

From equations (5.2), (5.6) and (5.9), we get the gate insulator electric field at threshold as

$$E_{Si-N_X}(inv) = \frac{q\varphi_s}{\varepsilon_i}\sqrt{N_t \times \left[1 + \frac{10.4}{1+\left(\frac{1.38}{D_G \times 10^7}\right)^{1.37}}\right]} \tag{5.10}$$

The threshold voltage is given as

$$V_T = \varphi_s + V_i(inv) \tag{5.11}$$

where $V_i(inv)$ is the voltage across the silicon nitride insulator and thus equal to $t_i E_i(inv)$ here t_i is the insulator thickness. Therefore the threshold voltage becomes

$$V_T = \varphi_s \left[1 + \frac{q t_i \sqrt{N_t}}{\varepsilon_i} \sqrt{1 + \frac{10.4}{1 + \left(\frac{1.38}{D_G \times 10^7} \right)^{1.37}}} \right] \tag{5.12}$$

The value of threshold voltage (V_T) is extracted for D_G=25nm, N_a=10^{16}cm^{-3} and N_t= 2×10^{16}cm^{-3} from equation (5.12) by using MATLAB and it comes out to be 2.86V which matched well with the experimental value [30]. The excellent match shows the validity of our model.

Fig. 5.3 shows the variation of threshold voltage with gate insulator thickness for different trap density values. It is observed that the threshold voltage increases with increases in trap density for a given value of gate insulator thickness. This is attributed to the fact that number of free carriers available for the conduction decreases with increase in trap density. Fig. 5.3 also depicts that as thickness of gate insulator increases, threshold voltage also increases for all values of trap density. This is due to the fact that as gate insulator thickness increases, the gate voltage which is required to achieve strong inversion state in the nc-Si:H channel layer also increases.

Fig. 5.4 shows the threshold voltage variation with the doping density at different value of gate insulator thickness. It is observed that the threshold voltage increases with increase of doping concentration at a given value of gate insulator thickness. It is also observed that difference in threshold voltage is higher for large values of doping density as compared to that of small value of doping density. This is attributed to the fact that the trap density becomes high for larger doping density and these trap states increases the potential barrier across the nc-Si:H layer and thus degrade the performance of the device.

Fig. 5.5 depicts the threshold voltage variation with trap density at various values of gate insulator thickness. It is observed that the decrease in gate insulator thickness causes decrease in trap states that exist in gate insulator and thus decreasing the threshold voltage. Fig. 5.6 shows that how threshold voltage varies with trap density at different temperatures. It is seen that as the temperature increases, the carriers available for conduction increases and thus channel formation occur at small gate voltage. This results in the reduction of threshold voltage.

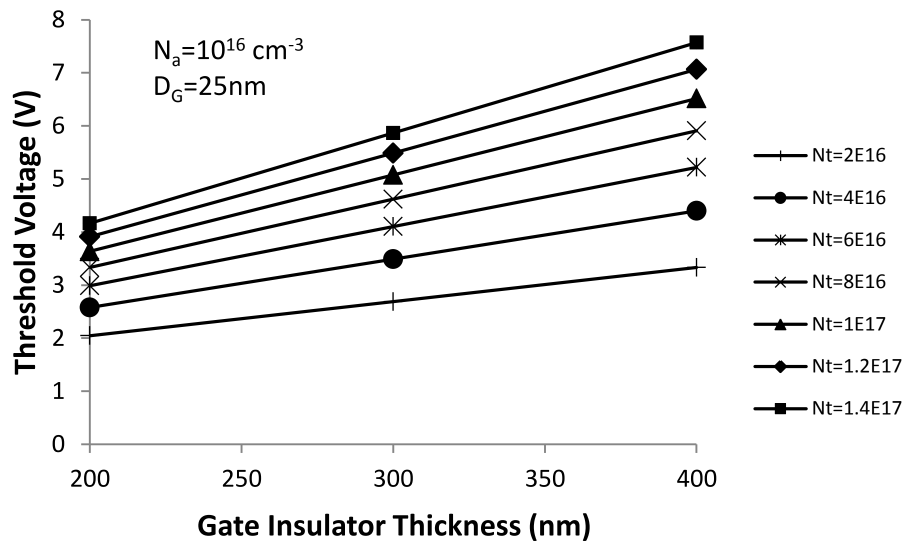


Fig. 5.3. Variation of threshold voltage as a function of gate insulator thickness for different values of trap density

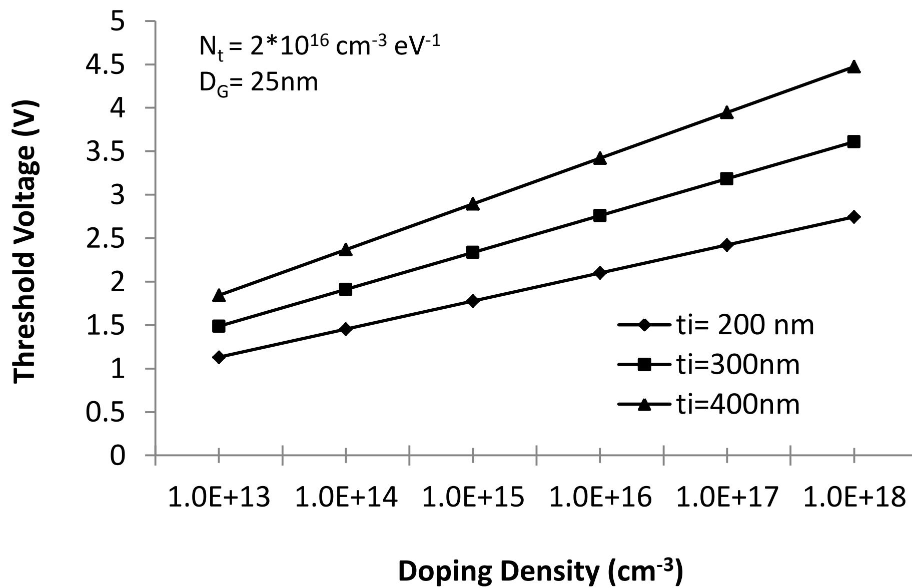


Fig. 5.4. Variation of threshold voltage as a function of doping density for different values of gate insulator thickness

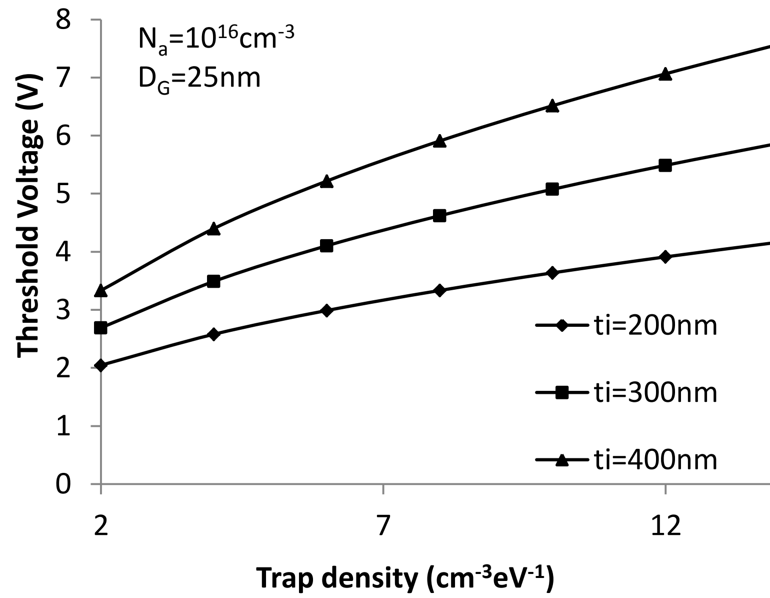


Fig. 5.5. Variation of threshold voltage as a function of trap density for different values of gate insulator thickness

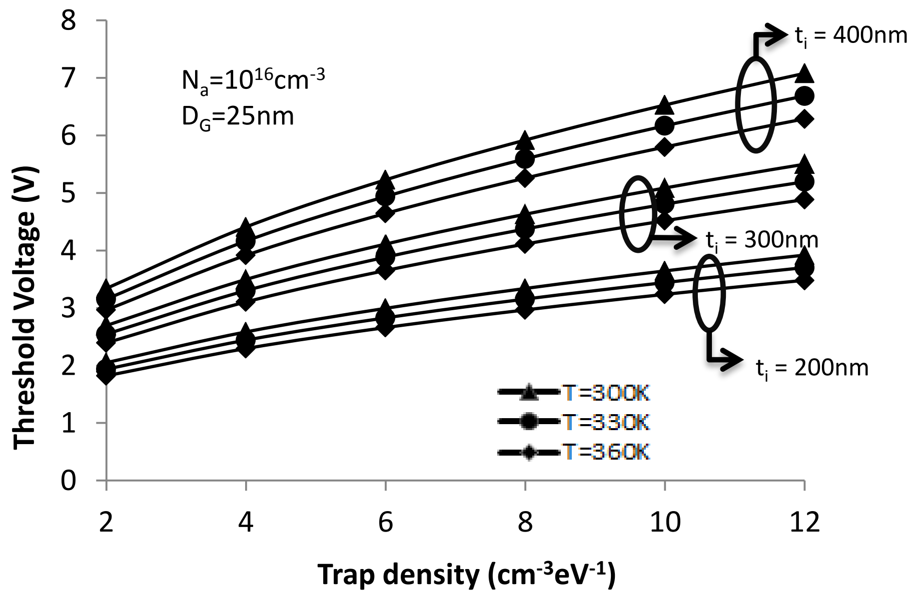


Fig. 5.6. Variation of threshold voltage as a function of trap density for different values of gate insulator thickness at different temperatures

5.2.2. Effective Mobility and Drain Current

Fig. 5.7 shows the perpendicular grain boundaries as well as the energy band diagram along the length of the channel of nc-Si:H TFT device. In the figure, D_G is the grain size, D_{GB} is the grain boundary width, D_d is the width of the depletion region ($D_{GB} << D_G$). The grain boundaries contain trap states which trap electrons, thereby leading to a reduction in effective hole concentration in the grain boundaries. Difference in hole concentration between the bulk and the grain boundaries leads to band bending at the grain boundaries. Ψ_B represents the potential barrier across the grain boundaries and is the amount of band bending at the grain boundary.

For perpendicular (transverse) grain boundaries in the channel, let $R_{G, perp}$ represent the resistance of a single grain, $R_{GB, perp}$ represent the resistance of a grain boundary, $n_{g,perp}$ represent the number of grains, μ_G and μ_{GB} represent the mobility of the grain and grain boundaries respectively, σ_G and σ_{GB} represent the conductivity of the grain and grain boundary respectively, L represent the total length of the channel, A be the cross sectional area of the channel, $\sigma_{eff, perp}$ and μ_{perp} be the equivalent conductivity and mobility of the channel due to perpendicular grain boundaries respectively.

Assuming that the grains and grain boundaries together form a series combination of resistances along the channel from source to drain, the total channel resistance $R_{T, perp}$ is given by

$$R_{T,\,perp} = n_{g,\,perp} R_{G,\,perp} + (n_{g,\,perp} - 1)\, R_{GB,\,perp} \tag{5.13}$$

where $n_{g,\,perp} = L / D_G$ approximately, considering that $D_{GB} << D_G$.

$$R_{T,\,perp} = \frac{L}{A\sigma_{eff,perp}}, \quad R_{G,\,perp} = \frac{D_G}{A\sigma_G}, \quad R_{GB,\,perp} = \frac{D_{GB}}{A\sigma_{GB}}$$

Substituting these values in equation (5.13),

$$\frac{L}{A\sigma_{eff,perp}} = \frac{n_{g.perp} D_G}{A\sigma_G} + \frac{(n_{g.perp.} - 1) D_{GB}}{A\sigma_{GB}} \tag{5.14}$$

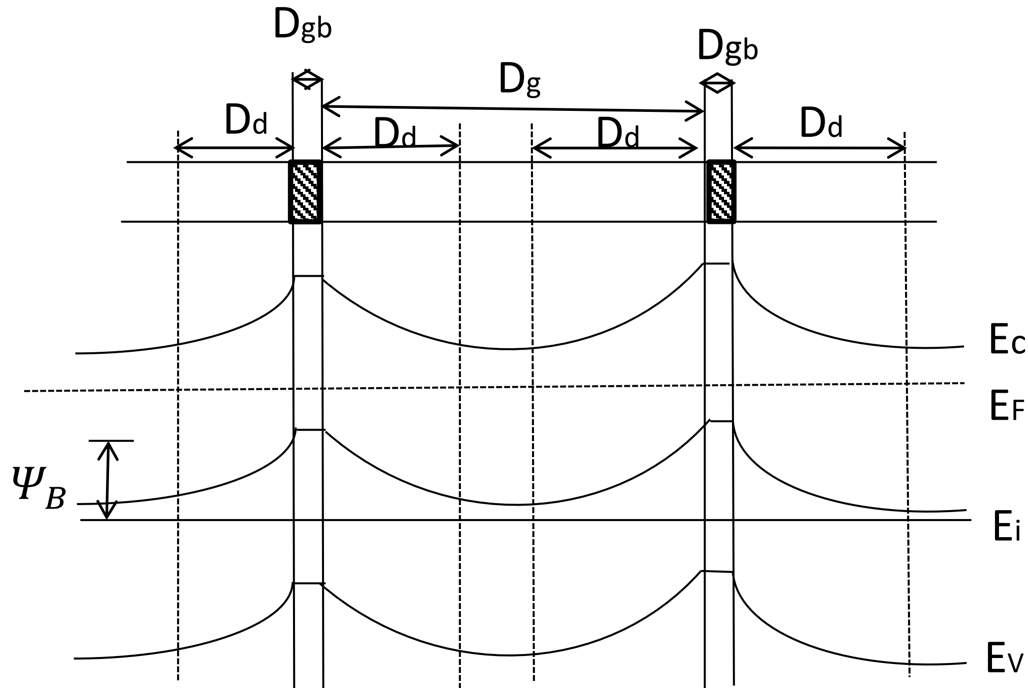


Fig. 5.7. (top) Cross-section in presence of perpendicular (transverse) grain boundaries. The shaded regions represent the grain boundaries.

(below) Energy band diagram along the length of the nc-Si:H film

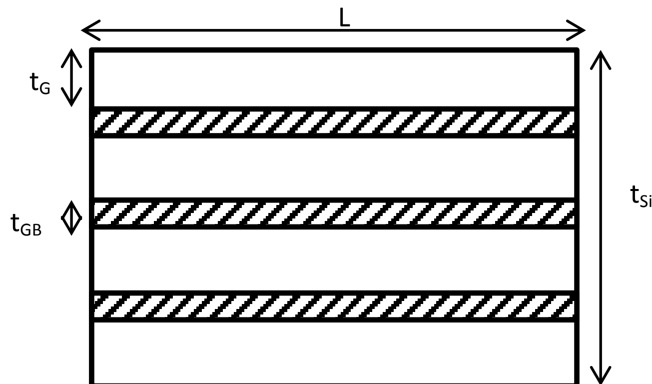


Fig. 5.8. Channel in presence of parallel (longitudinal) grain boundaries. The shaded regions represent the grain boundaries

Let N_d be the electron concentration in the bulk of the grain.

$\sigma_{eff,perp} = qN_d\mu_{perp}$ and $\sigma_G = qN_d\mu_G$

$\sigma_{GB} = (q\mu_{GB})n$, where '$n$' is the electron concentration in the grain boundaries

$$\sigma_{GB} = (q\mu_{GB})n_{\mathrm{i}}\exp\left((E_F - E_i)_{\mathrm{GB}} / kT\right)$$

$$= (q\mu_{GB})n_{\mathrm{i}}\exp\left(\left((E_F - E_i)_{\mathrm{bulk}} - q\Psi_B\right) / kT\right)$$

$$= (q\mu_{GB})n_{\mathrm{i}}\exp\left((E_F - E_i)_{\mathrm{bulk}} / kT\right)\exp(-q\Psi_B / kT)$$

$$= (q\mu_{GB})N_d\exp(-q\Psi_B / kT) \tag{5.15}$$

[Taking $n_{\mathrm{i}}\exp\left((E_F - E_i)_{\mathrm{bulk}}\right) / kT) = N_d$, the electron concentration in the bulk of the grain where n_{i} is the intrinsic carrier concentration].

Now equation (5.14) becomes,

$$\frac{n_{g,perp}D_G}{AqN_d\mu_{perp}} = \frac{n_{g,perp}D_G}{AqN_d\mu_G} + \frac{(n_{g,perp} - 1)D_{GB}}{AqN_d\mu_{GB}\exp\left(-\frac{q\Psi_B}{kT}\right)} \tag{5.16}$$

Solving equation (5.16) for μ_{perp} we get

$$\mu_{perp} = \frac{\mu_G}{1 + \left[\frac{(n_{g,perp} - 1)\mu_G D_{GB}}{n_{g,perp}\mu_{GB}D_G}\right]\exp\left(\frac{q\Psi_B}{kT}\right)} \tag{5.17}$$

where the potential barrier height within the grains is given as [112]:

$$\psi_B = \frac{qn_t^2}{8N\varepsilon_{nc-si}} \tag{5.18}$$

where N is the total carrier concentration in the strong inversion channel and it is approximately equal to gate induced electron concentration and is given as [113]:

$$N = \frac{C_i(V_{GS} - V_T)}{qt_{si}} \tag{5.19}$$

where V_{GS} is the gate voltage, t_{si} is the nc-Si:H inversion layer thickness and C_i is the gate insulator capacitance per unit area.

The n_t (cm^{-2}) in equation (5.18) is the density of charged states at the grain boundaries and can be extracted from a linear fit to $\ln\left(\frac{I_{DS}}{V_{GS}}\right)$ vs. $\frac{1}{V_{GS}}$ by using the following equation [83]:

$$\frac{I_{DS}}{V_{GS}} = \frac{W}{L}\mu_0 V_{DS} C_i \exp\left(-\frac{q^3 n_t^2 t_{si}}{8\varepsilon_i kTC_i}\frac{1}{V_{GS}}\right) \tag{5.20}$$

where *W/L* is the channel width to channel length ratio, V_{DS} is the drain-source voltage, μ_0 is the carrier mobility at the equilibrium condition.

Now assuming that channel also consists of parallel (longitudinal) grain boundaries which are shown in Fig. 5.8. Assuming that t_G is the thickness of a single grain and t_{GB} is the thickness of a grain boundary. As in the case of perpendicular grain boundaries, the trapping of electrons at grain boundaries leads to reduction of electron concentration in the grain boundaries, resulting in band bending at the grain boundaries. It is assumed that the extent of band bending at the grain boundaries (Ψ_B) is the same as in the perpendicular case.

Let there be $\mathrm{n_{g,parallel}}$ parallel grains in the channel and consequently $\left(\mathrm{n_{g,parallel}} - 1\right)$ grain boundaries. Thus, the thickness of channel layer is given by,

$$\mathrm{t_{si}} = \mathrm{n_{g,parallel}}\mathrm{t_G} + \left(\mathrm{n_{g,parallel}} - 1\right)\mathrm{t_{GB}} \tag{5.21}$$

The resistance of a single grain (of thickness $\mathrm{t_G}$) = $\mathrm{R_{G,\ parallel}} = \frac{L}{\sigma_G A_G}$, where A_G is the cross sectional area of the grain , ie, $\mathrm{A_G} = \mathrm{Wt_G}$ and $\sigma_\mathrm{G} = \mathrm{N}_d \mathrm{q}\,\mu_\mathrm{G}$.

$$\text{Thus } \mathrm{R_{G,\ parallel}} = \frac{L}{N_d q \mu_G t_G W} \tag{5.22}$$

Resistance of a single grain boundary = $\mathrm{R_{GB,\ parallel}} = \dfrac{L}{\sigma_{GB} A_{GB}}$ where A_{GB} is the cross sectional area of the grain boundary, ie, $\mathrm{A_{GB}} = \mathrm{Wt_{GB}}$ and

$\sigma_{\mathrm{GB}} = \left(\mathrm{q}\,\mu_{\mathrm{GB}}\right)\mathrm{N}_d \exp(-\mathrm{q}\Psi_{\mathrm{B}}/\mathrm{kT})$ from equation (5.15).

Thus $$\mathrm{R_{GB,parallel}} = \frac{L}{q\mu_{GB} N_d \exp\left(-\dfrac{q\psi_B}{kT}\right) t_{GB} W} \tag{5.23}$$

It is clear from Fig. 5.8, that the grains and grain boundaries form a parallel combination of resistances. Hence the equivalent resistance of the entire film can be written as

$$\frac{1}{R_{T,parallel}} = \frac{n_{g,parallel}}{R_{G,parallel}} + \frac{\left(n_{g,parallel} - 1\right)}{R_{GB,parallel}} \tag{5.24}$$

Let $\sigma_{\mathrm{eff,parallel}}$ be the equivalent conductivity of the channel due to parallel grain boundaries. Let μ_{parallel} be the effective mobility in presence of parallel grain boundaries only.

$$\sigma_{\mathrm{eff,parallel}} = \mathrm{qN}_d \mu_{\mathrm{parallel}} \tag{5.25}$$

$\mathrm{R_{T,parallel}} = \dfrac{L}{\sigma_{\mathrm{eff,parallel}} A}$, [where A=cross sectional area of the entire film]

$$= \frac{L}{\left(qN_d \mu_{parallel}\right)\left[\left(n_{g,parallel} - 1\right) t_{GB} + n_{g,parallel} t_G\right] W} \tag{5.26}$$

using the fact that $\mathrm{A} = \left[\left(n_{g,parallel} - 1\right) t_{GB} + n_{g,parallel} t_G\right] W$

Substitution of $\mathrm{R_{G,\ parallel}}$, $\mathrm{R_{GB,parallel}}$ and $\mathrm{R_{T,parallel}}$, and from equations (5.22), (5.23) and (5.26) in equation (5.24), gives

$$\mu_{parallel} = \frac{\mu_G t_G}{t_G + \left(1 - \frac{1}{n_{g,parallel}}\right) t_{GB}} + \frac{\mu_{GB} t_{GB} \exp\left(-\frac{q\Psi_B}{kT}\right)}{t_{GB} + \frac{t_G}{\left(1 - \frac{1}{n_{g,parallel}}\right)}} \tag{5.27}$$

The effective mobility (μ_{eff}) can be obtained from the following relation

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{perp}} + \frac{1}{\mu_{parallel}} \tag{5.28}$$

Fig. 5.9 and 5.10 shows the variation of mobility for parallel and perpendicular grain boundaries respectively, at room temperature. It is observed that parallel mobility increases nominally however perpendicular mobility increases rapidly with the increase in gate voltage. Also as N_d increases, barrier potential will decrease. This means that available carriers for transport will increase hence it decreases the trap states at the channel- gate insulator interface of nc-Si:H TFT. This effect results in an increase in the channel mobility. It can also be clearly verified by comparing Fig. 5.9 and 5.10 that the parallel mobility is much greater that perpendicular mobility for all values of gate voltage. This is attributed due to the fact that the grain boundary is a region that presents an energy barrier containing trap states and therefore reduced number of grain boundaries obviously leads to increased mobility in the parallel mobility model.

Therefore, $\mu_{\text{parallel}} \gg \mu_{\text{perp}}$ for all values of gate voltage

that is, $\frac{1}{\mu_{parallel}} \ll \frac{1}{\mu_{perp}}$

Therefore from equation (5.28),

$$\mu_{eff} \approx \mu_{\text{perp}} \tag{5.29}$$

So the expression for μ_{eff} given in equation (5.28) can be modified as

$$\mu_{eff} = \frac{\mu_G}{1 + M\left[\frac{\mu_G D_{GB}}{\mu_{GB} D_G}\right] \exp\left(\frac{q\psi_B}{kT}\right)} \tag{5.30}$$

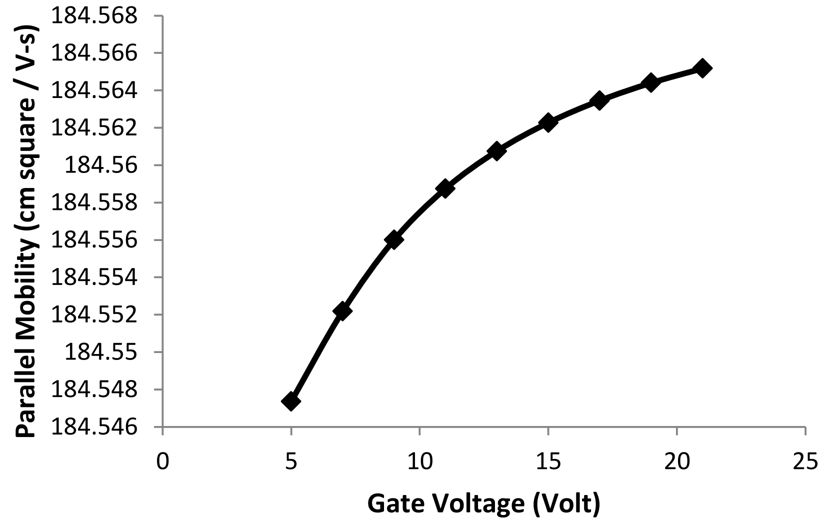


Fig. 5.9. Computed variation of parallel mobility with gate voltage at room temperature

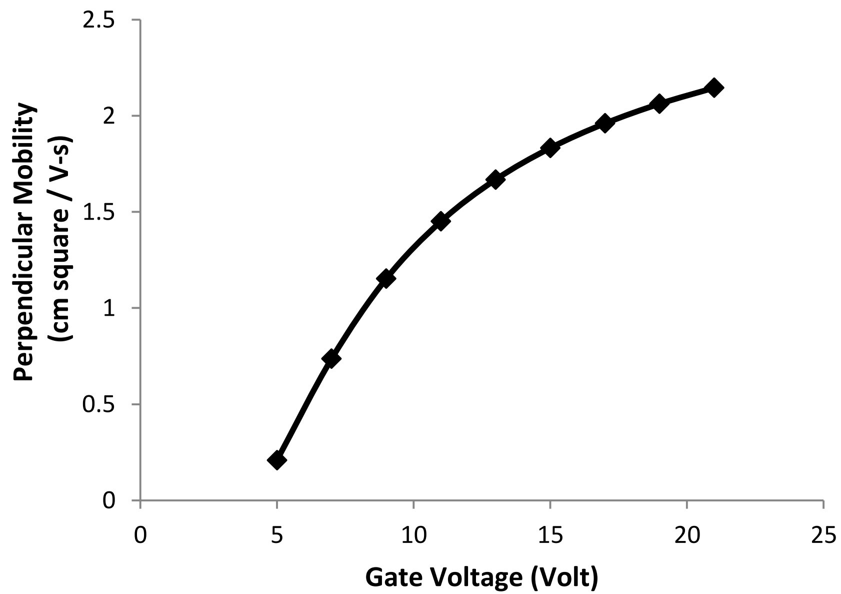


Fig. 5.10. Computed variation of perpendicular mobility with gate voltage at room temperature

where M is the mobility degradation factor given as M=exp(γ). This mobility degradation factor is required in order to include the effect of carrier scattering due to surface roughness which exponentially decreases the effective carrier mobility with the gate voltages.

The drain current (I_{DS}) of nc-Si:H TFT under the linear region can be given as [113]:

$$I_{DS} = \mu_{eff} \frac{W}{L} C_i \left[V_{DS} \left(V_{GS} - V_T \right) - \frac{V_{DS}^2}{2} \right] \qquad (5.31)$$

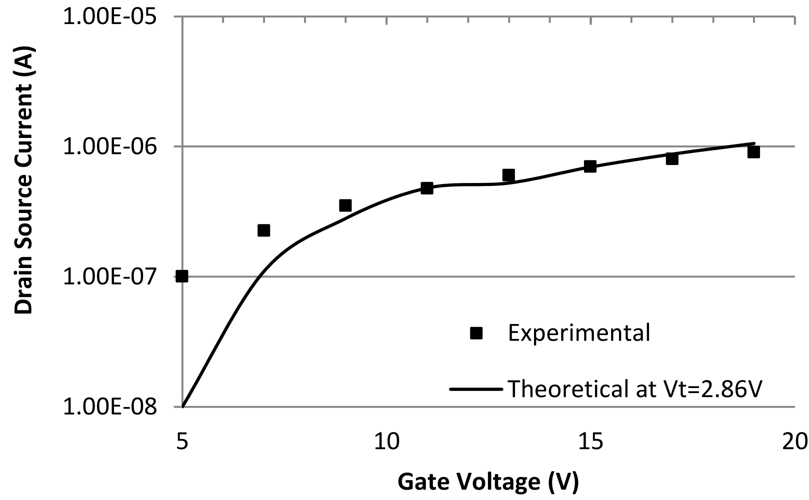


Fig. 5.11. Plot of the transfer characteristics of n-channel nc-Si:H TFT (W=200µm, L=50µm) calculated at V_{DS}=1V for V_T=2.86V, N_a=10^{16}cm^{-3} and N_t= 2×10^{16}cm^{-3}. Solid dark line shows the result of C.H.Lee et. al. [30]

Table 5.1 shows the values of the parameters used in the calculations. For the calculation of n_t, the experimental data [30] was used to plot $\ln\left(\frac{I_D}{V_{GS}}\right) \mathrm{vs} \left(\frac{1}{V_{GS}}\right)$, which happens to be a straight line. Using MATLAB Linear Regression Analysis, the slope of this straight line

was found to be -6.226 and from equation (5.20), slope = $\left(-\frac{q^3 n_t^2 t_{si}}{8\varepsilon_i kTC_i}\right)$. Therefore,

$\left(-\frac{q^3 n_t^2 t_{si}}{8\varepsilon_i kTC_i}\right)$=-6.229 which gives n_t = 3.5 x 10^{11} /cm^2.

To validate the model, the variation of drain current versus gate voltage of n-channel nc-Si:H TFT calculated at V_{DS}=1V for V_T=2.86V is shown in Fig. 5.11 and is compared with experimental values of Lee et. al. [30].

It can be seen that in the higher gate voltage region (V_{GS}> 8V), the computed variation are in excellent agreement with experimentally observed values, however in the region (V_{GS}< 8V) there is a slight deviation from experimental variation. This may be due to the effect of grain boundaries which is more pronounced at low gate voltages and also the channel used for experiments may be slightly different in terms of purity of nc-Si:H material.

Table 5.1: Parameters used in the calculations [30]

Parameters	**Symbols**	**Values**
Channel length	L	50μm
Channel width	W	200μm
Grain size	D_G	25nm
Grain boundary width	D_{GB}	2.5nm
Drain voltage	V_{DS}	1V
nc-Si:H inversion layer thickness	t_{si}	80nm
Bulk grain mobility	μ_G	203cm^2 Vs^{-1}
Grain boundary mobility	μ_{GB}	0.3cm^2 Vs^{-1}
Mobility degradation factor	M = exp(γ)	γ= 0.7 at V_G< 11V γ= 1 at V_G> 11V

5.3. CONCLUSION

The effects of various physical parameters i.e. trapping state density, doping density, temperature and gate insulator thickness on the threshold voltage are analyzed and the model for determining the threshold voltage of nc-Si:H TFT is proposed. The results revealed that the decrease in gate insulator thickness and increase in temperature causes the decrease in the threshold voltage. The results also demonstrate that the threshold voltage increases with increase in trap density and doping concentration for a particular value of gate insulator thickness.

In addition, the model for effective mobility is also proposed in this chapter by considering the effects of perpendicular and parallel grain boundaries. It is observed that parallel mobility is much greater that perpendicular mobility for all values of gate voltage and therefore mobility due to perpendicular grain boundaries have the dominant effect on the calculation of effective mobility. This mobility model is then used to calculate the drain current.

The validity of proposed models was verified through the satisfactory agreement between theoretical and experimental data.

CHAPTER 6

NON-IDEALITIES IN nc-Si:H TFT

6.1. INTRODUCTION

The TFT provides high mobility and high electrical stability in the ideal condition however transconductance degradation [40, 41] and threshold voltage shift [68, 87, 114] under electrical stress are the two main mechanisms which cause non-idealities in the nc-Si:H TFT performance. Therefore deep analysis on these mechanisms is required in order to design the nc-Si:H TFT with enhanced performance.

In this chapter, detailed study on these mechanisms is provided. The chapter is divided into two main sections. In first section, analysis on threshold voltage shift including the effect of various physical parameters like grain size, gate insulator thickness, doping density and grain boundary trapping state on the threshold voltage shift is discussed. In second section, analysis on transconductance degradation covering the effect of DOS parameters on the performance of nc-Si:H TFT with Si_3N_4 as gate dielectric is presented. The variation in DOS in nc-Si:H material and thus on the TFT device performance occurred by altering the channel length and channel quality is presented. The analysis was performed using ATLAS 2D TCAD simulator from SILVACO.

6.2. THRESHOLD VOLTAGE SHIFT

Limited work on the electrical instability of nc-Si:H TFT are published so far and most of these works focus on the gate bias stability. Esmaeili-Rad et. al. [114] compared the

threshold voltage shift of the nc-Si:H TFTs with that of the a-Si:H TFTs, under similar operation conditions and found two major differences in the behavior of nc-Si:H TFTs as compared to that of the a-Si:H TFTs, first one is the threshold voltage shift in nc-Si:H TFT. saturates at prolonged stress times, but that of a-Si:H TFT does not as shown in Fig. 6.1 and second one is that threshold voltage shift in nc-Si:H TFT is weakly temperature dependent, as compared to that of a-Si:H device as shown in Fig. 6.2. This behavior of threshold voltage shift in nc-Si:H TFTs shows absence of defect state creation. The weak temperature dependence validate that the instability in nc-Si:H TFTs is due to the charge trapping mechanism proposed by Powell et al. [56]. The threshold voltage shift in nc-Si:H TFT thus also follows the stretched exponential time dependence [68, 115]. Kim et. al. [87] proposed that the nc-Si:H TFT shows less threshold voltage shift as compared to a-Si:H TFTs. When the drain bias applied to the nc-Si:H TFT increases, the concentration of channel charge decreases and due to which less defect states are created and thus decreases the threshold voltage shift. In addition to this, they examined that in case of top gated nc-Si:H TFT, the defect state creation is much lower due to the presence of well-crystallize region of the nc-Si:H film. They also proposed that the ratio of depleted charges to the total charges increases with the decreasing channel length. Since short channel TFT has lower concentration of channel charge thus it shows less threshold voltage degradation as compared to long channel TFT.

Since threshold voltage shift (ΔV_T) in nc-Si:H TFT follows the stretched exponential time dependence [68, 115] which basically contains the parameter ΔV_{T0} where $\Delta V_{T0} = V_{gs} - V_T$, and as we already discussed in chapter 5 that the threshold voltage (V_T) in nc-Si:H TFTs is basically affected by various physical parameters. Therefore, in the present work, the effect of these physical parameters like grain size, gate insulator thickness, doping density and grain boundary trapping state which affects the electrical instability of nc-Si:H TFT is analyzed.

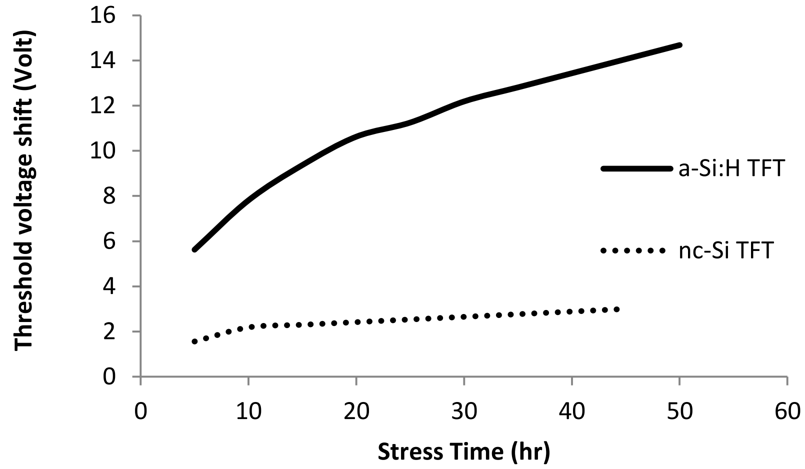


Fig. 6.1. Comparison between the threshold voltage shift in a-Si:H TFT and nc-Si:H TFT as a function of stress time at temperature 75˚C and stress current of 10µA [114]

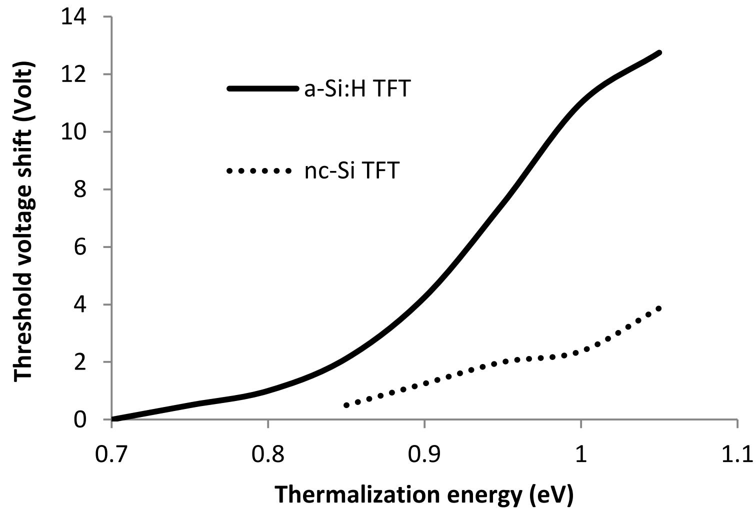


Fig. 6.2. Comparison between the threshold voltage shift in a-Si:H TFT and nc-Si:H TFT as a function of thermalization energy at temperature 75˚C and stress current 15µA[114]

The stretched exponential equation for threshold voltage shift calculation is given as [68]

$$|\Delta V_T| = \left(V_{gs} - V_T\right)\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \tag{6.1}$$

From equation (5.12) and (6.1), the final expression for threshold voltage shift is given as:

$$|\Delta V_T| = \left(V_{gs} - \varphi_s\left[1 + \frac{qt_i\sqrt{N_t}}{\varepsilon_i}\sqrt{1 + \frac{10.4}{1 + \left(\frac{1.38}{D_G \times 10^7}\right)^{1.37}}}\right]\right)\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \tag{6.2}$$

Table 6.1 shows the typical values of the model parameters used in the calculations.

Table 6.1: Model parameters used in the calculations [30, 108, 117, 118]

Parameters	**Symbols**	**Values**
Channel length	L	50 μm
Channel width	W	200 μm
Grain size	D_G	25 nm
Gate voltage	V_{GS}	20 V
Drain voltage	V_{DS}	1 V
Density of trapping states	N_t	$2.5*10^{17}$ cm^{-3} eV^{-1}
Temperature	T	300K
Dielectric strength of insulator layer	ε_i	7.5
Insulator layer thickness	t_i	300 nm
Characteristic trapping time	τ	$1.46*10^6$ sec
Stretched-exponential exponent	β	0.45

Fig. 6.3 illustrate the variation of calculated values for threshold voltage shift as a function of time for different values of trap density. It is observed that at a particular time, the threshold voltage shift decreases with increase in trap density. This is attributed to the fact that the channel charge concentration reduces due to increase in trap states which in turn decreases the threshold voltage shift [87]. Similarly, Fig. 6.4 shows the effect of doping concentration over threshold voltage shift. It is seen that threshold voltage shift decreases with increase in doping concentration. This is due to the fact that bandgap alongwith trap density increases with increase in doping concentration which results into the reduction of threshold volatge shift value.

Fig. 6.5 shows the effect of grain size over threshold voltage shift. It is observed from the Fig. 6.5 that for smaller grain size, threshold volatge shift increases with increase in grain size. This may be attributed to the fact that trap density decreases with increase in grain size [116] and therefore increase the threshold voltage shift values. However, for larger grain size (D_G > 20nm), effect of dopant concentration dominates over the trap density effect and provide stability to the device. This implies that grain size must be larger in order to provide stability to the device by preventing the threshold voltage variation due to various device fabrication processes.

Fig. 6.6 demonstrates the effect of gate dielectric thickness over threshold voltage shift. The result shows that threshold voltage shift reduces with increase in gate insulator thickness. This is due to the fact that as the insulator thickness increases it causes the increase in trap states available at insulator-channel interface which reduces the available carrier for transport and therefore reduces the threshold voltage shift.

Fig. 6.7 shows the effect of bias voltage over threshold voltage shift. It is observed that threshold voltage shift increases with the bias voltage applied to the gate. For all values of bias voltage, threshold voltage shift increases with increase in bias stress time. Furthermore, it was observed that shift of the threshold voltage is symmetric among all the values of gate bias.

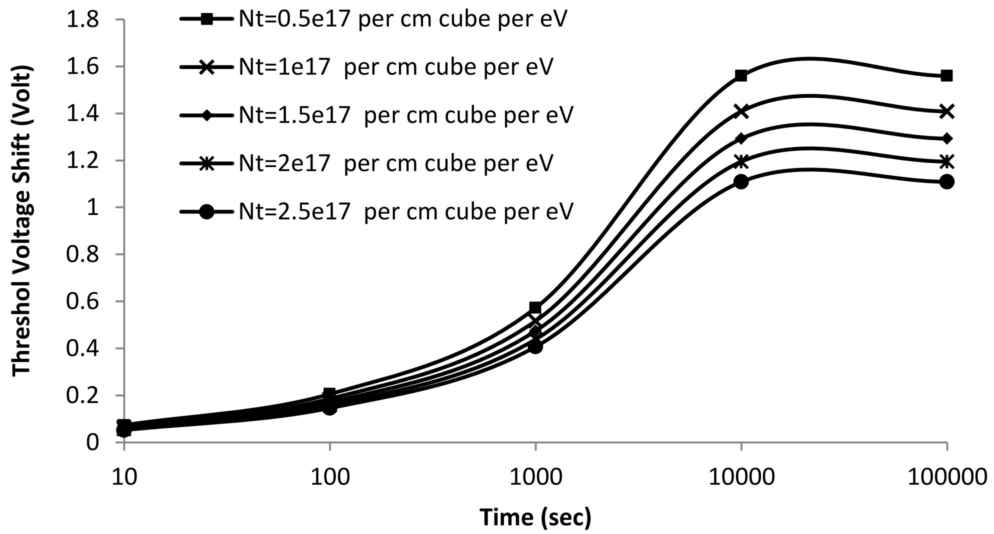


Fig. 6.3. Computed variations of threshold voltage shift in the top gated nc-Si:H TFTs as a function of time for different trap state densities

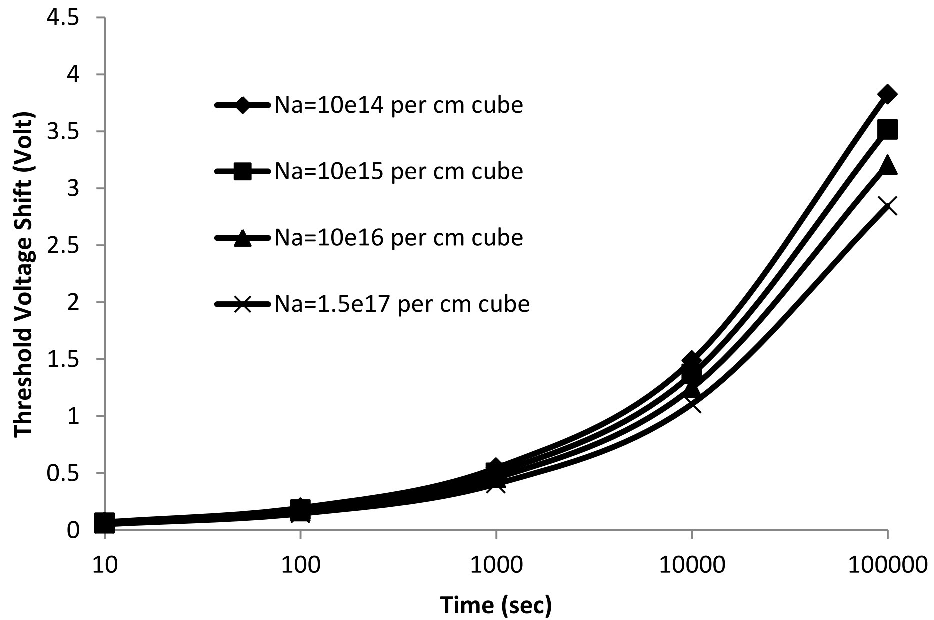


Fig. 6.4. Computed variations of threshold voltage shift in the top gated nc-Si:H TFTs as a function of time for different values of doping concentration

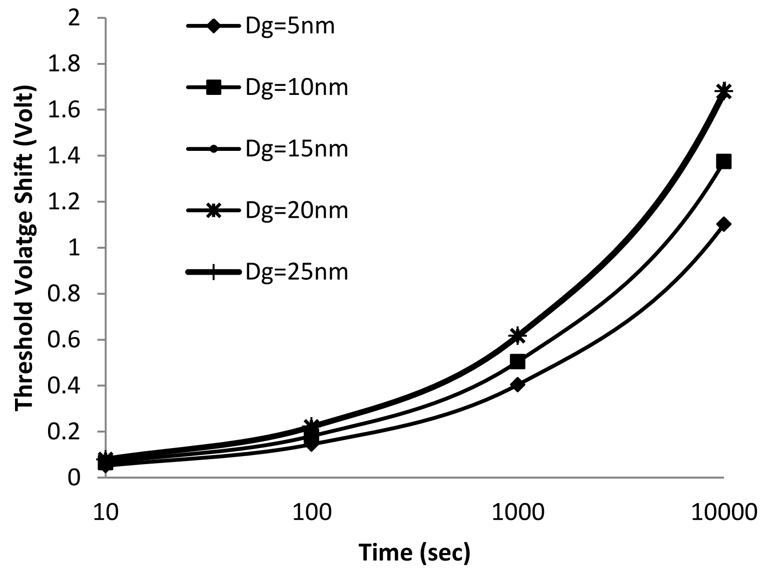


Fig. 6.5. Computed variations of threshold voltage shift in the top gated nc-Si:H TFTs as a function of time for different grain sizes

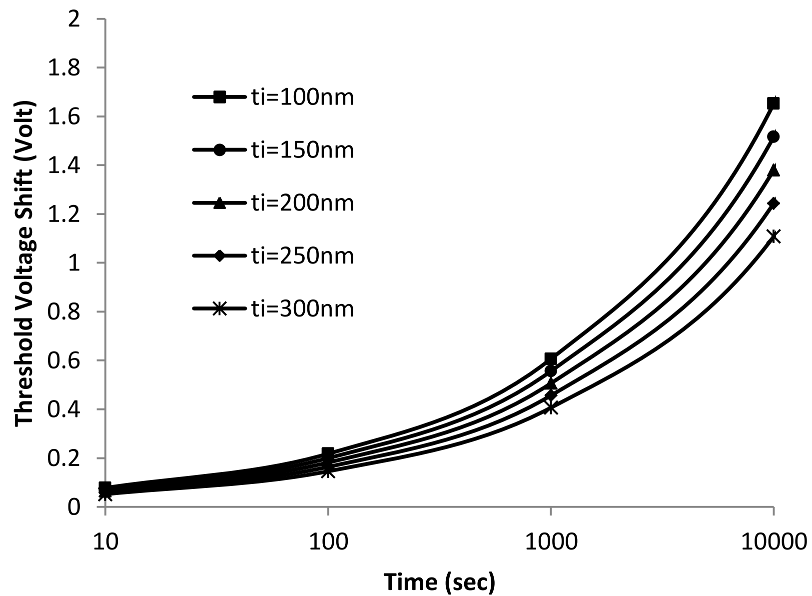


Fig. 6.6. Computed variations of threshold voltage shift in the top gated nc-Si:H TFTs as a function of time for different values of gate insulator thickness

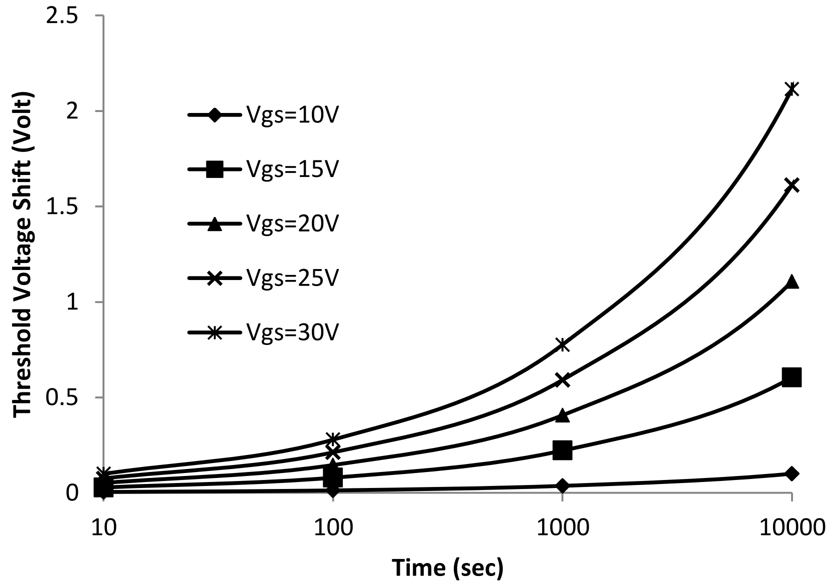


Fig. 6.7. Computed variations of threshold voltage shift in the top gated nc-Si:H TFTs as a function of time under different gate bias stress

The measured values of threshold voltage shift computed using equation (6.2) and the experimental values of Lee et. al. [30] is shown in Table 6.2. It is clearly seen from the Table 6.2 that the results from analytical model using equation (6.2) are in considerable good agreement with experimental data [30]. However, the small difference may be due to the fact that the actual device used for the experiment may be slightly different in terms of purity of nc-Si:H channel layer.

Table 6.2: Calculated and experimental [30] threshold voltage shift at different V_{GS}

	Theoretical ΔV_T	Experimental ΔV_T
V_{GS}=20V	0.42	0.35
V_{GS}=30V	0.81	0.77

6.3. TRANSCONDUCTANCE DEGRADATION

Fig. 6.8 shows equivalent circuit of the TFT used for device simulation where R denotes parasitic resistance components of the n-channel top gated nc-Si:H TFT.

DOS model, which is available in TFT module in ATLAS tool package, is used to extract the density of defects present in the band gap of nc-Si:H. We have considered the case that DOS has a continuous distribution from band tail states to the extended energy states. DOS can be defined as a function of energy as follows:

$$g(E) = g_{GA}(E) + g_{GD}(E) + g_{TA}(E) + g_{TD}(E) \tag{6.3}$$

where

$$g_{GA}(E) = NGA\ \exp\left[-\left(\frac{EGA - E}{WGA}\right)^2\right] \tag{6.4}$$

$$g_{GD}(E) = NGD\ \exp\left[-\left(\frac{E - EGD}{WGD}\right)^2\right] \tag{6.5}$$

$$g_{TA}(E) = NTA\ \exp\left(\frac{E - E_C}{WTA}\right) \tag{6.6}$$

$$\mathrm{g_{TD}(E) = NTD\ \exp\left(\frac{E_V - E}{WTD}\right)} \tag{6.6}$$

where E_C and E_V are the conduction and valence band edge energies, E is the trap energy, N is the edge intercept density, W is the characteristic decay energy and the scripts (T, G, A, D) stand for band tail, Gaussian deep, acceptor and donor states respectively.

Fig. 6.9 shows the virtually fabricated TFT structure used for 2D device simulation on ATLAS by SILVACO. Table 6.3 shows the value of various nc-Si:H TFT parameters used for device simulation.

The nc-Si:H is used as an active layer with a thickness of 80 nm and the 300 nm thick Si_3N_4 layer is used as a gate dielectric. The width of the channel is taken as 200μm and the channel length range varies from 50μm to 100μm. In spite of defining a new layer, the source and drain region is implemented using highly doped (i.e. 10^{20} /cm^3) n$^+$ region and the aluminum metal contact on the top of it. The parasitic resistance is employed as a lumped component in the simulation input desk separately and is not defined in mesh structure.

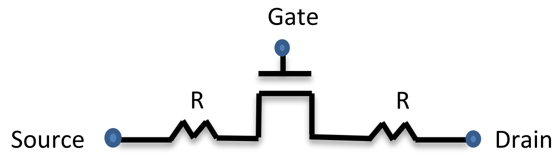


Fig. 6.8. Equivalent circuit of the TFT used for device simulation

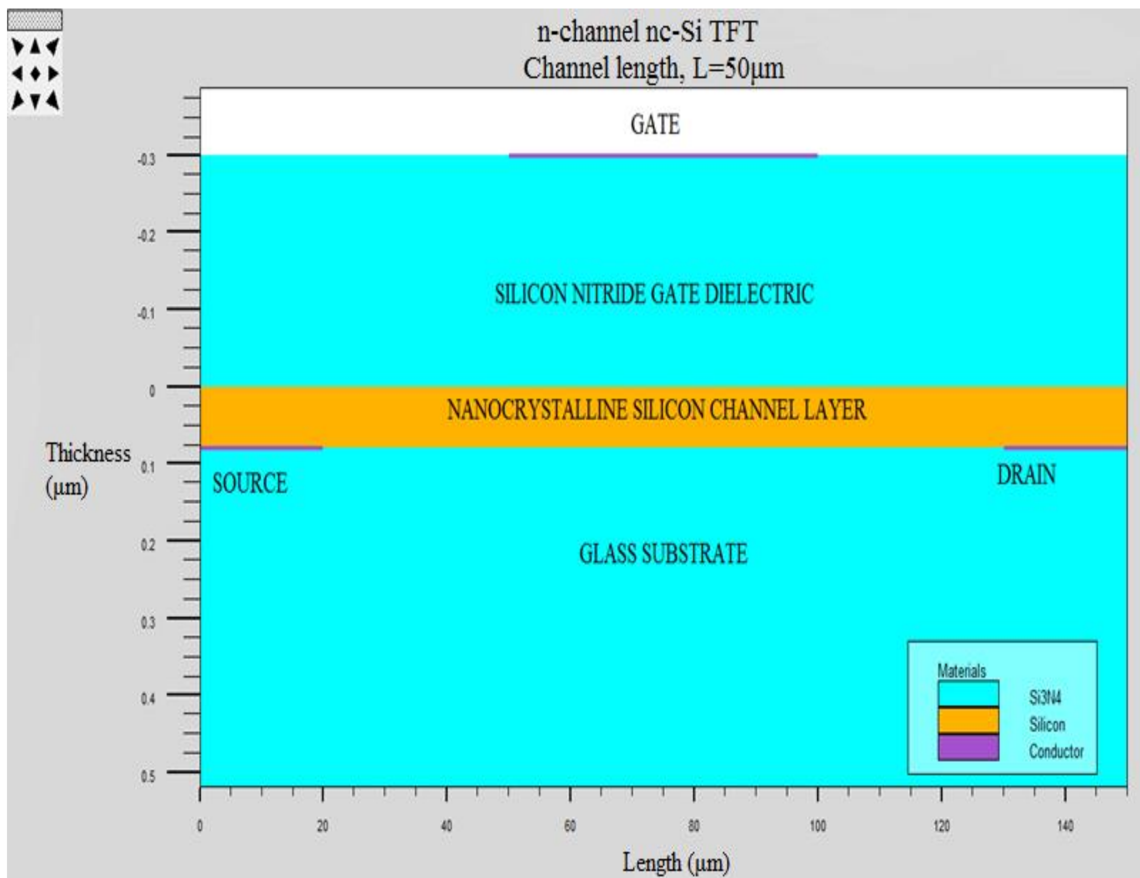


Fig. 6.9. nc-Si:H TFT structure for ATLAS simulation

Table 6.3: ATLAS device simulation parameter for nc-Si:H TFT

Parameter	Description	nc-Si:H
NTA	Conduction band edge intercept tail states density	$1x10^{20}$ cm^{-3}
NTD	Valence band edge intercept tail states density	$1x10^{20}$ cm^{-3}
NGA	Conduction band edge intercept deep states density	$3.7x10^{17}$ cm^{-3}
NGD	Valence band edge intercept deep states density	$3.7x10^{17}$ cm^{-3}
EGA	Peak energy of deep states as $E=E_C$	0.4 eV
EGD	Peak energy of deep states as $E=E_V$	0.4 eV
WTA	Characteristic decay energy of tail states as $E=E_C$	0.025 eV
WTD	Characteristic decay energy of tail states as $E=E_V$	0.025 eV
WGA	Characteristic decay energy of deep states as $E=E_C$	0.1 eV
WGD	Characteristic decay energy of deep states as $E=E_V$	0.1 eV

For the present work, V_{DS} =10V (fixed) is considered because at such a high drain voltage only, the effect of contact resistance in nc-Si:H TFT is more prominent [30] and therefore increase the overall parasitic resistance.

The influence of DOS (i.e. the nc-Si:H material properties) on the nc-Si:H TFT performance is investigated by considering different values of characteristic decay energy (WTA) as 0.020, 0.025, 0.033, 0.030, 0.040 eV and keeping parasitic resistance value fixed at 10^6 Ω. The higher value of WTA relates to the wider acceptor like tail states which corresponds to the film which has more amorphous-like properties [21] and thus higher parasitic resistance. Similarly, the lower value of WTA defines that the film is more polycrystalline. The simulation results reveal that the transconductance degradation (as shown in Fig. 6.10) occurs as the film become more amorphous or as the value of WTA increases from 0.020 to 0.040eV. The drain current also decreases (as illustrated in Fig. 6.11) due to increase in total series resistance with the increase in the value of WTA.

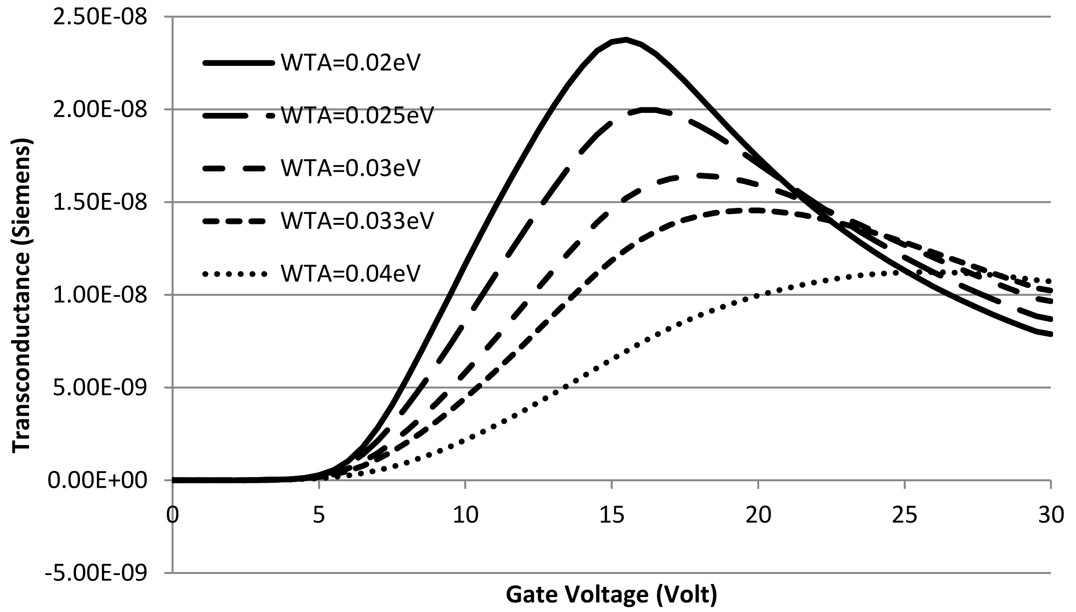


Fig. 6.10. Variation of transconductance as a function of gate voltage for different values of tail states

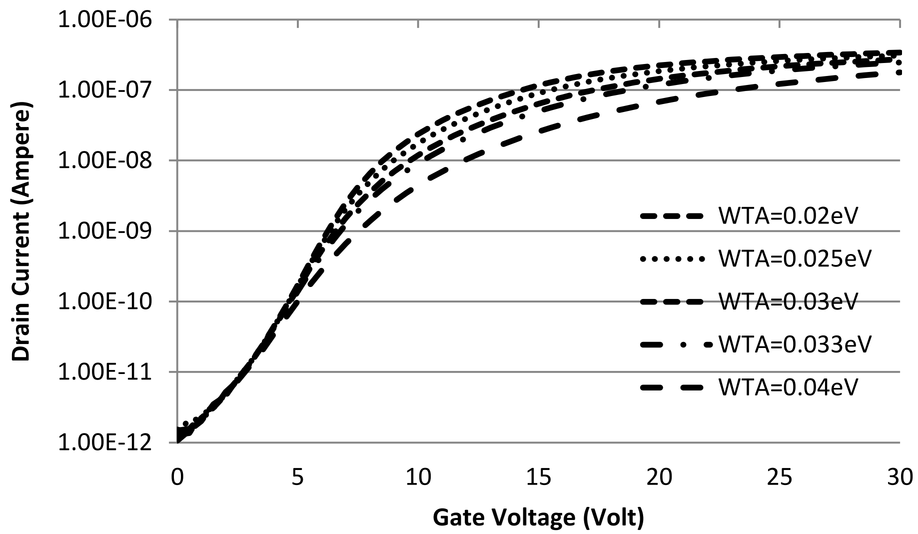


Fig. 6.11. Variation of drain current as a function of gate voltage for different values of tail states

The channel length dependence on the drain current of nc-Si:H TFT is analyzed by varying channel length from 50 to 100μm while maintaining other parameter like DOS as fixed at initial fitting values (i.e. WTA=0.02eV). The simulation results indicate that increase in channel length degrades the transconductance as shown in Fig. 6.12. This degradation is attributed due to the increase in parasitic resistance. Fig. 6.13 shows the drain current degradation with the increase in channel length. This drain current degradation is attributed due to the increase in weight of series resistance of the channel layer which increases the overall parasitic resistance. The drain current degradation can also be explained by the increase of transverse electric field on increasing the channel length even if the channel depth remains fixed. This variation is illustrated in Fig. 6.14 for channel length values of 50μm and 90μm.

The dependence of parasitic resistance, R on the transconductance is analyzed by varying the parasitic resistance from 10^3 to 10^7 Ω and considering fixed value of WTA as 0.02eV. The simulation result shown in Fig. 6.15 reveals that the transconductance decreases as the parasitic resistance increases from 10^3 to 10^7 Ω.

In order to compare the simulated results with the experimental findings [30], a modeling factor F=exp(α) is used where the value of α is taken as 0.27. This factor will compensate the difference between the simulated DOS value and actual DOS in nc-Si:H film used in device fabrication. The comparison between the two, as shown in Fig 6.16, shows the excellent match between the results.

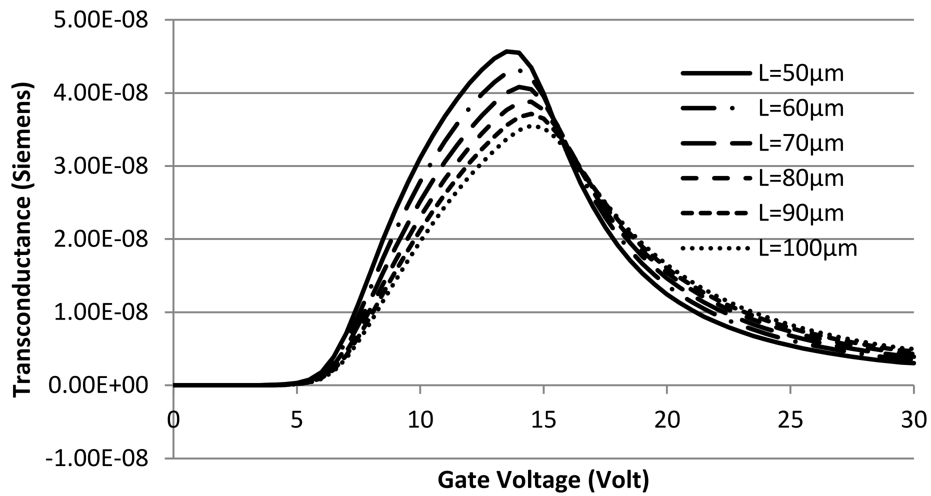


Fig. 6.12. Variation of transconductance as a function of gate voltage for different values of channel length

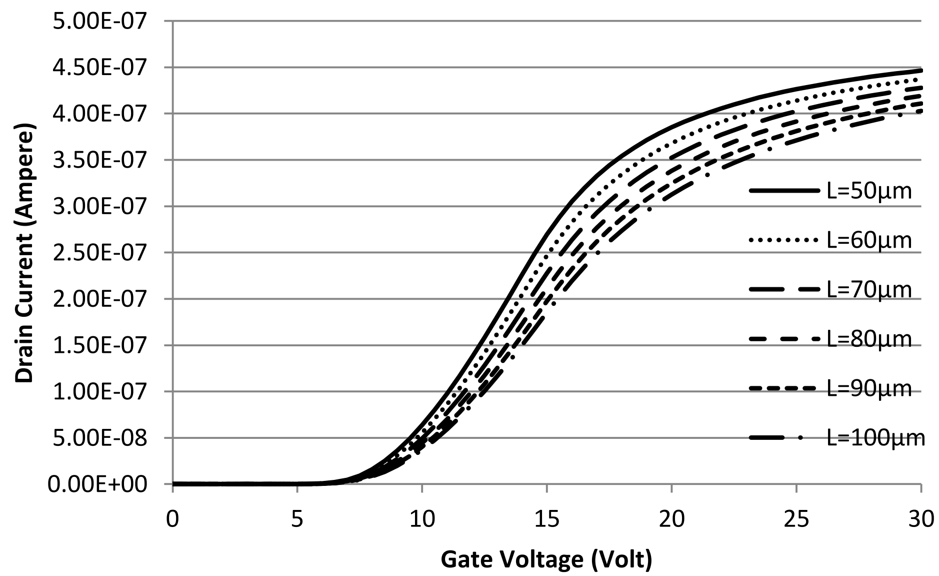


Fig. 6.13. Variation of drain current as a function of gate voltage for different values of channel length

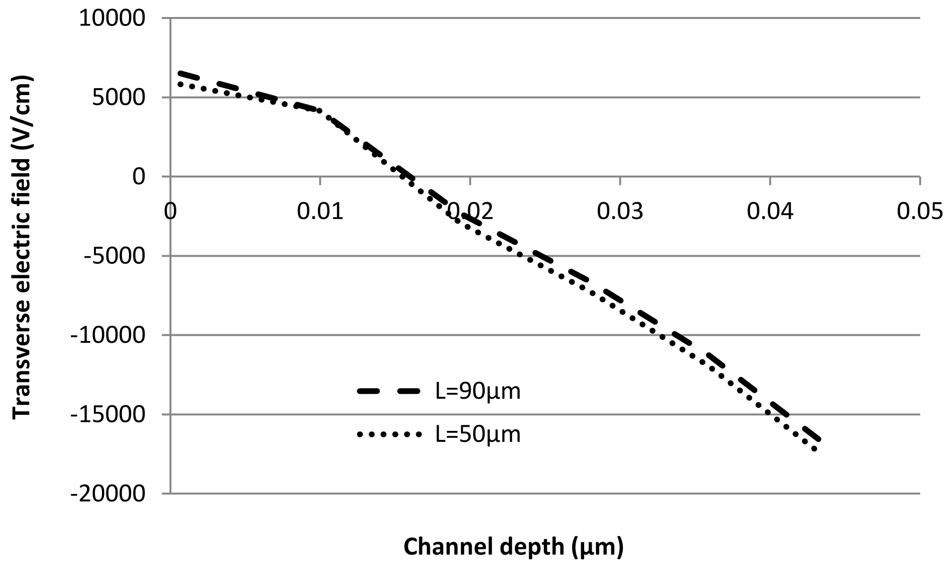


Fig. 6.14. Variation of transverse electric field versus channel length depth for L= 90µm and 50µm

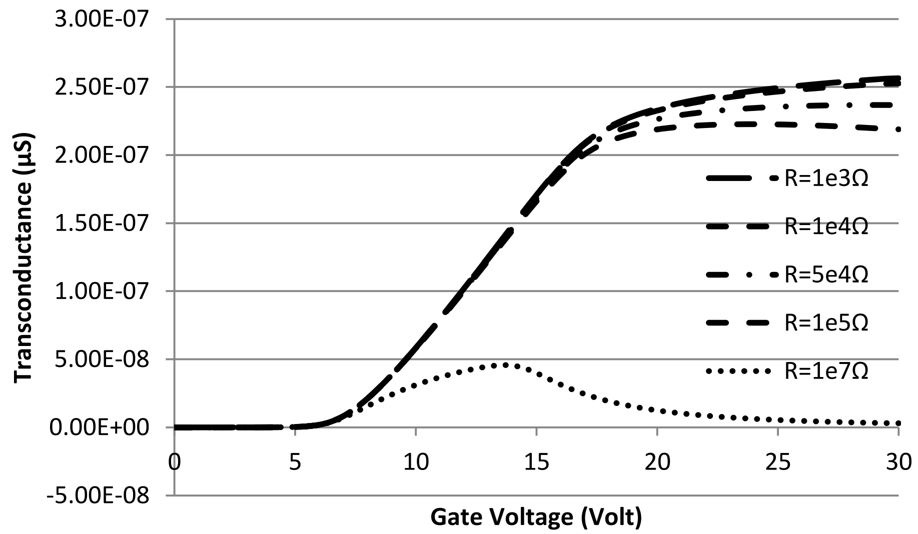


Fig. 6.15. Variation of transconductance as a function of gate voltage for different values of parasitic resistance

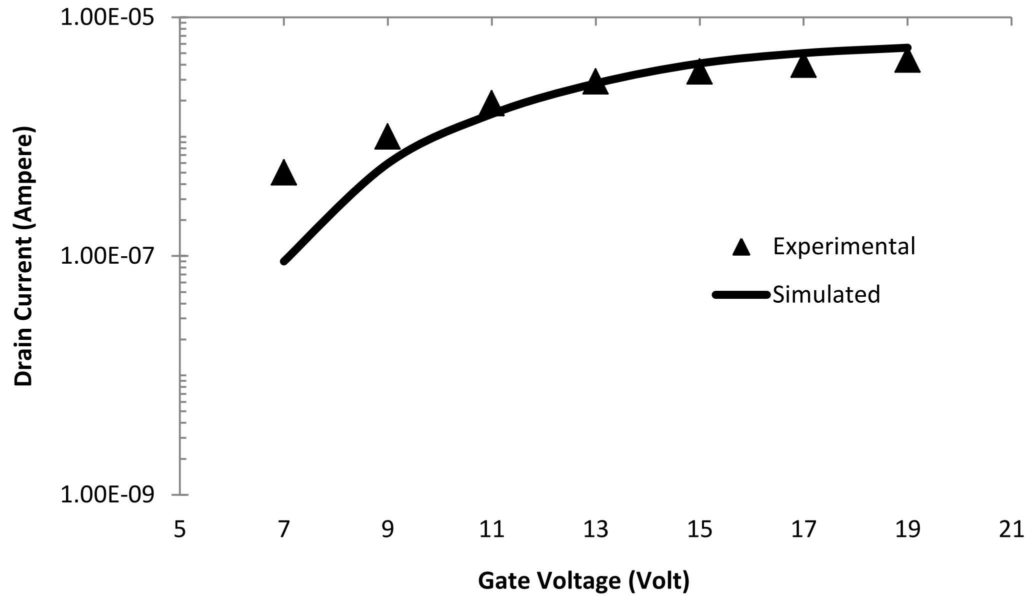


Fig. 6.16. Plot of the transfer characteristic of nc-Si:H top-gated TFT (W=200µm and L=50µm) simulated at V_{DS}=10V for WTA=0.02 and R=10^7 Ω. Triangle shows the experimental results of C. H. Lee et. al. [30] and solid line shows simulated results

6.4. CONCLUSION

In this chapter, the study on threshold voltage instability which includes the effect of various physical parameters like grain size, gate insulator thickness, doping density and grain boundary trapping state on the threshold voltage shift is reported. It is observed that the higher trap density, greater doping concentration and larger gate insulator thickness provide lesser threshold voltage shift. Further, it is found from the results of grain size analysis that if grain size is smaller than threshold voltage shift decreases with decrease in grain size. However, if grain size is larger (D_G > 20nm) then device become stable and shows negligible threshold voltage shift. In this chapter, threshold voltage shift under gate bias voltage is also analyzed and result reveals that threshold voltage shift increases with the bias voltage. The calculated results are compared with experimental data. The close match between the two confirms the validity of proposed study.

In addition to this, the effects of DOS and channel length on the performance of nc-Si:H TFT using ATLAS 2D device simulator by SILVACO was also investigated. The simulation results reveal that the channel material properties affect the device transconductance. The higher value of characteristic decay energy of the channel material causes the increase in DOS and thereby the degradation in drain current which in turn limits the on-state device performance. It has been also observed that the increase in channel length also degrades the transconductance and drain current due to increase in weight of parasitic resistance. The outcome of this study is compared with the experimental data and the similar trend between the two has been observed.

CHAPTER 7

CONCLUSION

7.1 CONCLUSION

The thesis covered the analysis of issues related to device characteristics of n-channel top gate nc-Si TFT for its application in new generation large area displays.

The objective of this thesis was to investigate, analyze and develop a comprehensive study on electronic behaviour of nanocrystalline silicon thin film transistor (nc-Si:H TFT). In order to achieve this research goal, some specific objectives were made: (1) To deposit the nc-Si film on glass substrate for studying the surface morphology of the film. (2) To select a suitable gate dielectric material for nc-Si:H TFT. (3) To develop an analytical model for describing the electronic behaviour of the device. (4) To analyze the non-idealities in the performance of nc-Si:H TFT by developing an analytical model and by doing simulations.

In order to get better understanding and physical insights, an extensive review has been carried out in terms of previous device models, fabrication techniques of top-gate nc-Si:H TFT and electrical instability about the device. Important outcomes of the literature review are reported in chapter 2.

The deposition of nc-Si:H films has been carried to study the structural morphology and conductivity of nc-Si:H film to be used for the modeling of nc-Si:H TFT device. Using e-beam PVD method, the 100 nm thick nc-Si:H films was deposited on Corning glass 1737 substrate in the vacuum of 8 x 10^{-6} Torr with controlled beam current of 90mA and

deposition rate of 1.2 A°/s. The optimized nc-Si:H film exhibited high conductivity of the order of 100 S/cm and small grain sizes in the range of 2-15nm. Therefore this optimized nc-Si:H film can provide high mobility and high on current if used as the channel layer for the fabrication of top-gate nc-Si:H TFT. The results validate that the e-beam PVD process is the cost effective technique for high quality nc-Si:H film deposition. The deposition of nc-Si:H films with different thicknesses (i.e. 100nm, 150nm and 200nm) has also been carried. The FESEM and AFM results show that the grain size increases with increase in film thickness.

Next, gate dielectric material selection using three approaches i.e. Ashby's approach, VIKOR and TOPSIS has been presented in this thesis. Si_3N_4, Al_2O_3, ZrO_2, Ta_2O_5 and HfO_2 materials have been investigated. Two performance indices (i.e. drain current and leakage current) based on four material indices (i.e. dielectric constant, band gap, conduction band offset and interface trap density) to improve the performance of top-gate nc-Si:H TFT were optimized. The investigation shows that Si_3N_4 is the best suitable material and can provide high drain current and less leakage current when used for gate dielectric in top-gate nc-Si:H TFT. The outcome of this analysis shows good agreement between all the three methodologies and the experimental results.

An analytical model for the extraction of threshold voltage in top-gate nc-Si:H TFTs has been proposed. The effect of various physical parameters such as gate insulator thickness, trap density, doping density and temperature on the threshold voltage has been investigated. The results demonstrated that the reduction in gate insulator thickness and the increase in temperature causes the decrease in threshold voltage. The results also illustrated that the threshold voltage increases with increase in trap density and doping concentration.

In addition, an analytical mobility model for effective mobility has also been proposed in this thesis. The effect of perpendicular and parallel grain boundaries on effective mobility has been demonstrated. It is observed that the effect of parallel grain boundaries is less prominent than perpendicular grain boundaries. It is observed that both parallel and perpendicular mobility increases with the increase in gate voltage. This proposed model

has been further used for the accurate estimation of drain current in top-gate nc-Si:H TFTs.

An analytical model for threshold voltage instability in top-gate nc-Si:H TFT has also been proposed in this thesis. In the proposed model, the effects of various physical parameters on threshold voltage shift have been incorporated. It is observed that the higher trap density, greater doping concentration and larger gate insulator thickness provide lesser threshold voltage shift. In addition, it is observed that for smaller grain sizes, threshold voltage shift decreases with decrease in grain size. However, for larger grain sizes ($D_G > 20$nm), negligible threshold voltage shift has been observed. Threshold voltage shift under prolonged gate bias stress has also been analyzed and results of this analysis revealed that threshold voltage shift increases with the increase in gate bias voltage. The close match between the analytically calculated data and experimental data confirms the validity of proposed model.

Lastly, the effect of DOS and channel length on the performance of top-gate nc-Si:H TFT has been analyzed using ATLAS 2D device simulator. It has been confirmed that the channel material properties affect the device transconductance. The higher value of characteristic decay energy reduces the transconductance and drain current and thereby degrades the device performance. It has also been observed that the increase in channel length from 50 to 100μm also degrades the device performance due to increase in weight of parasitic resistance. The result of this analysis is compared with the experimental results and the similar trend between the two has been observed.

The research presented in the thesis has significant implications and contributions to the development of enhanced performance nc-Si:H TFT. The research highlights are listed below:

- In contrast to all previous work, we have shown that it is possible to deposit a high quality nc-Si:H film on glass substrate using e-beam PVD method.
- Si_3N_4 is the best gate dielectric which can provide high drain current and low leakage current for nc-Si:H TFT.

- An analytical model for threshold voltage, effective mobility and drain current has been proposed which incorporates the effects of grains, grain boundaries, trap density, doping density, gate insulator thickness and temperature.
- Model for threshold voltage shift has been proposed and using simulation the transconductance degradation mechanism is analyzed.

Although this thesis has addressed several critical issues aforementioned, nc-Si:H TFT still need to further investigated to overcome other challenges. In the next section the future scope of work is presented.

7.2. FUTURE SCOPE OF WORK

In order to continue and improve the work presented in this thesis, the following improvements as a future scope of work are suggested:

- Apart from material selection methodologies, experimental study is also possible by depositing all possible gate dielectric and analyzing their behaviour on the device characteristics.
- Further, the cause of threshold voltage shift may be deeply studied experimentally by fabricating the device.
- It is also possible to investigate the effects of tilt angle of grain boundaries in the channel and may be incorporating in the analytical device modeling.
- A further refinement of the model is possible by taking total trap concentration and trap level at the grain boundaries from a statistical distribution to account for the differences in grain size and shape.
- In order to have high switching speed of TFT, the effective mobility of the carriers in channel needs to improve. This may be possible by improving the nc-Si:H material itself.

APPENDIX

Simulation Input Desk

I. To analyze the effect of nc-Si material quality

```
go atlas
TITLE Generation of top gate-staggered source/drain TFT structure.

# Define TFT structure: standard (L_off = 0), L = 50 um, t_ch = 80 nm, t_ox = 300 nm
mesh
x.m l=0 spac=2.
x.m l=20 spac=3.
x.m l=35 spac=5.
x.m l=50 spac=0.25
x.m l=75 spac=3.
x.m l=100 spac=0.25
x.m l=115 spac=5.
x.m l=130 spac=3.
x.m l=150 spac=2.

y.m l=-0.3 spac=0.05
y.m l=0 spac=0.0075
y.m l=0.04 spac=0.01
y.m l=0.08 spac=0.0075
y.m l=0.4 spac=0.25
y.m l=10. spac=5.

# Define regions: 1=nitride, 2 and 3=silicon, 4=nitride
region  num=1  y.max=0. nitride
region  num=2  y.min=0. y.max=0.04 silicon
region  num=3  y.min=0.04 y.max=0.08 silicon
region  num=4  y.min=0.08 oxide

# Define electrodes: 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate
elec num=1 x.min=50 x.max=100 y.min=-0.3 y.max=-0.3 name=gate
elec num=2 x.min=0. x.max=20. y.min=0.08 y.max=0.08 name=source
elec num=3 x.min=130. x.max=150. y.min=0.08 y.max=0.08 name=drain

# Define doping
doping reg=2 uniform conc=1.e11 n.type
doping reg=3 uniform conc=1.e11 n.type
doping reg=3 gauss  conc=1.e20 n.type  x.right=50 char=0.3
doping reg=3 gauss  conc=1.e20 n.type  x.left=100 char=0.3

save outf=std_str_l=50.str

mesh inf = str/std_str_l = 50.str

# Set nc-Si:H material parameters
```

```
material material=silicon mun=65 mup=3

defects nta=1.12e21 ntd=4.e20 wta=0.033 wtd=0.033 \
  nga=5.e17 ngd=1.5e17 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
  sigtae=1.e-16 sigtah=1.e-14 sigtde=1.e-14 sigtdh=1.e-16 \
  siggae=1.e-16 siggah=1.e-14 siggde=1.e-14 siggdh=1.e-16 \
  dfile=donors5.dat afile=acceptors5.dat \
  numa=12 numd=12

interface qf=3e11

# Define contact parameters
contact num=1 alum
contact num=2 alum resistance=1.e7
contact num=3 alum resistance=1.e7

# Define models
models srh print trap.coulombic

# Enable the following parameters for study of scattering effects
# mobility en.cvt=1 dn.cvt=0.333 ep.cvt=1 dp.cvt=0.333 kn.cvt=2 kp.cvt=2

method newton
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
solve vdrain=1 vfinal=10 vstep=1 name=drain

log outf = forward_wt4.log
solve vgate=0 vstep=0.5 vfinal=30 name=gate
go atlas

extract init infile="forward_wt4.log"
extract name="forward_wt4" curve(v."gate", i."drain") outf="forward_wt4.dat"
extract name="gm_wt4" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_wt4.dat"
extract name="nvt5" (xintercept(maxslope(curve(v."gate",(i."drain")))))-(ave(v."drain")/2.0)

tonyplot forward_wt4.dat
tonyplot gm_wt4.dat

go atlas
TITLE Generation of top gate-staggered source/drain TFT structure.

# Define TFT structure: standard (L_off = 0), L = 50 um, t_ch = 80 nm, t_ox = 300 nm
mesh
x.m l=0 spac=2.
x.m l=20 spac=3.
x.m l=35 spac=5.
x.m l=50 spac=0.25
x.m l=75 spac=3.
x.m l=100 spac=0.25
x.m l=115 spac=5.
```

```
x.m l=130 spac=3.
x.m l=150 spac=2.

y.m l=-0.3 spac=0.05
y.m l=0 spac=0.0075
y.m l=0.04 spac=0.01
y.m l=0.08 spac=0.0075
y.m l=0.4 spac=0.25
y.m l=10. spac=5.

# Define regions: 1=nitride, 2 and 3=silicon, 4=nitride
region  num=1  y.max=0. nitride
region  num=2  y.min=0. y.max=0.04 silicon
region  num=3  y.min=0.04 y.max=0.08 silicon
region  num=4  y.min=0.08 oxide

# Define electrodes: 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate
elec num=1 x.min=50 x.max=100 y.min=-0.3 y.max=-0.3 name=gate
elec num=2 x.min=0. x.max=20. y.min=0.08 y.max=0.08 name=source
elec num=3 x.min=130. x.max=150. y.min=0.08 y.max=0.08 name=drain

# Define doping
doping reg=2 uniform conc=1.e11 n.type
doping reg=3 uniform conc=1.e11 n.type
doping reg=3 gauss  conc=1.e20 n.type  x.right=50 char=0.3
doping reg=3 gauss  conc=1.e20 n.type  x.left=100 char=0.3

save outf=std_str_l=50.str


mesh inf = str/std_str_l = 50.str

# Set nc-Si:H material parameters

material material=silicon mun=65 mup=3

defects nta=1.12e21 ntd=4.e20 wta=0.025 wtd=0.025 \
  nga=5.e17 ngd=1.5e17 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
  sigtae=1.e-16 sigtah=1.e-14 sigtde=1.e-14 sigtdh=1.e-16 \
  siggae=1.e-16 siggah=1.e-14 siggde=1.e-14 siggdh=1.e-16 \
  dfile=donors4.dat afile=acceptors4.dat \
  numa=12 numd=12

interface qf=3e11

# Define contact parameters
contact num=1 alum
contact num=2 alum resistance=1.e7
contact num=3 alum resistance=1.e7

# Define models
models srh print trap.coulombic
```

```
# Enable the following parameters for study of scattering effects
# mobility en.cvt=1 dn.cvt=0.333 ep.cvt=1 dp.cvt=0.333 kn.cvt=2 kp.cvt=2

method newton
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
solve vdrain=1 vfinal=10 vstep=1 name=drain

log outf = forward_wt3.log
solve vgate=0 vstep=0.5 vfinal=30 name=gate
go atlas

extract init infile="forward_wt3.log"
extract name="forward_wt3" curve(v."gate", i."drain") outf="forward_wt3.dat"
extract name="gm_wt3" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_wt3.dat"
extract name="nvt4" (xintercept(maxslope(curve(v."gate",(i."drain")))))-(ave(v."drain")/2.0)

tonyplot forward_wt3.dat
go atlas
TITLE Generation of top gate-staggered source/drain TFT structure.

# Define TFT structure: standard (L_off = 0), L = 50 um, t_ch = 80 nm, t_ox = 300 nm
mesh
x.m l=0 spac=2.
x.m l=20 spac=3.
x.m l=35 spac=5.
x.m l=50 spac=0.25
x.m l=75 spac=3.
x.m l=100 spac=0.25
x.m l=115 spac=5.
x.m l=130 spac=3.
x.m l=150 spac=2.

y.m l=-0.3 spac=0.05
y.m l=0 spac=0.0075
y.m l=0.04 spac=0.01
y.m l=0.08 spac=0.0075
y.m l=0.4 spac=0.25
y.m l=10. spac=5.

# Define regions: 1=nitride, 2 and 3=silicon, 4=nitride
region  num=1  y.max=0. nitride
region  num=2  y.min=0. y.max=0.04 silicon
region  num=3  y.min=0.04 y.max=0.08 silicon
region  num=4  y.min=0.08 oxide

# Define electrodes: 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate
elec num=1 x.min=50 x.max=100 y.min=-0.3 y.max=-0.3 name=gate
elec num=2 x.min=0. x.max=20. y.min=0.08 y.max=0.08 name=source
elec num=3 x.min=130. x.max=150. y.min=0.08 y.max=0.08 name=drain
```

```
# Define doping
doping reg=2 uniform conc=1.e11 n.type
doping reg=3 uniform conc=1.e11 n.type
doping reg=3 gauss  conc=1.e20 n.type  x.right=50 char=0.3
doping reg=3 gauss  conc=1.e20 n.type  x.left=100 char=0.3

save outf=std_str_l=50.str


mesh inf = str/std_str_l = 50.str

# Set nc-Si:H material parameters

material material=silicon mun=65 mup=3

defects nta=1.12e21 ntd=4.e20 wta=0.03 wtd=0.03 \
  nga=5.e17 ngd=1.5e17 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
  sigtae=1.e-16 sigtah=1.e-14 sigtde=1.e-14 sigtdh=1.e-16 \
  siggae=1.e-16 siggah=1.e-14 siggde=1.e-14 siggdh=1.e-16 \
  dfile=donors3.dat afile=acceptors3.dat \
  numa=12 numd=12

interface qf=3e11

# Define contact parameters
contact num=1 alum
contact num=2 alum resistance=1.e7
contact num=3 alum resistance=1.e7

# Define models
models srh print trap.coulombic

# Enable the following parameters for study of scattering effects
# mobility en.cvt=1 dn.cvt=0.333 ep.cvt=1 dp.cvt=0.333 kn.cvt=2 kp.cvt=2

method newton
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
solve vdrain=1 vfinal=10 vstep=1 name=drain

log outf = forward_wt2.log
solve vgate=0 vstep=0.5 vfinal=30 name=gate
go atlas

extract init infile="forward_wt2.log"
extract name="forward_wt2" curve(v."gate", i."drain") outf="forward_wt2.dat"
extract name="gm_wt2" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_wt2.dat"
extract name="nvt3" (xintercept(maxslope(curve(v."gate",(i."drain")))))-(ave(v."drain")/2.0)

tonyplot forward_wt2.dat
tonyplot gm_wt2.dat
```

```
go atlas
TITLE Generation of top gate-staggered source/drain TFT structure.

# Define TFT structure: standard (L_off = 0), L = 50 um, t_ch = 80 nm, t_ox = 300 nm
mesh
x.m l=0 spac=2.
x.m l=20 spac=3.
x.m l=35 spac=5.
x.m l=50 spac=0.25
x.m l=75 spac=3.
x.m l=100 spac=0.25
x.m l=115 spac=5.
x.m l=130 spac=3.
x.m l=150 spac=2.

y.m l=-0.3 spac=0.05
y.m l=0 spac=0.0075
y.m l=0.04 spac=0.01
y.m l=0.08 spac=0.0075
y.m l=0.4 spac=0.25
y.m l=10. spac=5.

# Define regions: 1=nitride, 2 and 3=silicon, 4=nitride
region  num=1  y.max=0. nitride
region  num=2  y.min=0. y.max=0.04 silicon
region  num=3  y.min=0.04 y.max=0.08 silicon
region  num=4  y.min=0.08 oxide

# Define electrodes: 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate
elec num=1 x.min=50 x.max=100 y.min=-0.3 y.max=-0.3 name=gate
elec num=2 x.min=0. x.max=20. y.min=0.08 y.max=0.08 name=source
elec num=3 x.min=130. x.max=150. y.min=0.08 y.max=0.08 name=drain

# Define doping
doping reg=2 uniform conc=1.e11 n.type
doping reg=3 uniform conc=1.e11 n.type
doping reg=3 gauss  conc=1.e20 n.type  x.right=50 char=0.3
doping reg=3 gauss  conc=1.e20 n.type  x.left=100 char=0.3

save outf=std_str_l=50.str

mesh inf = str/std_str_l = 50.str

# Set nc-Si:H material parameters

material material=silicon mun=65 mup=3

defects nta=1.12e21 ntd=4.e20 wta=0.04 wtd=0.04 \
  nga=5.e17 ngd=1.5e17 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
  sigtae=1.e-16 sigtah=1.e-14 sigtde=1.e-14 sigtdh=1.e-16 \
  siggae=1.e-16 siggah=1.e-14 siggde=1.e-14 siggdh=1.e-16 \
  dfile=donors2.dat afile=acceptors2.dat \
  numa=12 numd=12
```

```
interface qf=3e11

# Define contact parameters
contact num=1 alum
contact num=2 alum resistance=1.e7
contact num=3 alum resistance=1.e7

# Define models
models srh print trap.coulombic

# Enable the following parameters for study of scattering effects
# mobility en.cvt=1 dn.cvt=0.333 ep.cvt=1 dp.cvt=0.333 kn.cvt=2 kp.cvt=2

method newton
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
solve vdrain=1 vfinal=10 vstep=1 name=drain

log outf = forward_wt1.log
solve vgate=0 vstep=0.5 vfinal=30 name=gate
go atlas

extract init infile="forward_wt1.log"
extract name="forward_wt1" curve(v."gate", i."drain") outf="forward_wt1.dat"
extract name="gm_wt1" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_wt1.dat"
extract name="nvt2" (xintercept(maxslope(curve(v."gate",(i."drain")))))-(ave(v."drain")/2.0)

tonyplot forward_wt1.dat
tonyplot gm_wt1.dat

go atlas
TITLE Generation of top gate-staggered source/drain TFT structure.

# Define TFT structure: standard (L_off = 0), L = 50 um, t_ch = 80 nm, t_ox = 300 nm
mesh
x.m l=0 spac=2.
x.m l=20 spac=3.
x.m l=35 spac=5.
x.m l=50 spac=0.25
x.m l=75 spac=3.
x.m l=100 spac=0.25
x.m l=115 spac=5.
x.m l=130 spac=3.
x.m l=150 spac=2.

y.m l=-0.3 spac=0.05
y.m l=0 spac=0.0075
y.m l=0.04 spac=0.01
y.m l=0.08 spac=0.0075
y.m l=0.4 spac=0.25
y.m l=10. spac=5.
```

```
# Define regions: 1=nitride, 2 and 3=silicon, 4=nitride
region  num=1  y.max=0. nitride
region  num=2  y.min=0. y.max=0.04 silicon
region  num=3  y.min=0.04 y.max=0.08 silicon
region  num=4  y.min=0.08 oxide

# Define electrodes: 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate
elec num=1 x.min=50 x.max=100 y.min=-0.3 y.max=-0.3 name=gate
elec num=2 x.min=0. x.max=20. y.min=0.08 y.max=0.08 name=source
elec num=3 x.min=130. x.max=150. y.min=0.08 y.max=0.08 name=drain

# Define doping
doping reg=2 uniform conc=1.e16 n.type
doping reg=3 uniform conc=1.e16 n.type
doping reg=3 gauss  conc=1.e20 n.type  x.right=50 char=0.3
doping reg=3 gauss  conc=1.e20 n.type  x.left=100 char=0.3

save outf=std_str_l=50.str


mesh inf = str/std_str_l = 50.str

# Set nc-Si:H material parameters

material material=silicon mun=65 mup=3

defects nta=1.12e21 ntd=4.e20 wta=0.02 wtd=0.02 \
  nga=5.e17 ngd=1.5e17 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
  sigtae=1.e-16 sigtah=1.e-14 sigtde=1.e-14 sigtdh=1.e-16 \
  siggae=1.e-16 siggah=1.e-14 siggde=1.e-14 siggdh=1.e-16 \
  dfile=donors1.dat afile=acceptors1.dat \
  numa=12 numd=12

interface qf=3e11

# Define contact parameters
contact num=1 alum
contact num=2 alum resistance=1.e7
contact num=3 alum resistance=1.e7

# Define models
models srh print trap.coulombic

# Enable the following parameters for study of scattering effects
# mobility en.cvt=1 dn.cvt=0.333 ep.cvt=1 dp.cvt=0.333 kn.cvt=2 kp.cvt=2

method newton
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
solve vdrain=1 vfinal=10 vstep=1 name=drain
```

```
log outf = forward_wt.log
solve vgate=0 vstep=0.5 vfinal=30 name=gate
go atlas

extract init infile="forward_wt.log"
extract name="forward_wt" curve(v."gate", i."drain") outf="forward_wt.dat"
extract name="gm_wt" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_wt.dat"
extract name="nvt1" (xintercept(maxslope(curve(v."gate",(i."drain")))))-(ave(v."drain")/2.0)

tonyplot forward_wt.dat
tonyplot gm_wt.dat

quit
```

II. To analyze the effect of channel length variation

```
go atlas
TITLE Generation of top gate-staggered source/drain TFT structure.

# Define TFT structure: standard (L_off = 0), L = 50 um, t_ch = 80 nm, t_ox = 300 nm
mesh
x.m l=0 spac=2.
x.m l=20 spac=3.
x.m l=35 spac=5.
x.m l=50 spac=0.25
x.m l=75 spac=3.
x.m l=100 spac=0.25
x.m l=115 spac=5.
x.m l=130 spac=3.
x.m l=150 spac=2.

y.m l=-0.3 spac=0.05
y.m l=0 spac=0.0075
y.m l=0.04 spac=0.01
y.m l=0.08 spac=0.0075
y.m l=0.4 spac=0.25
y.m l=10. spac=5.

# Define regions: 1=nitride, 2 and 3=silicon, 4=nitride
region  num=1  y.max=0. nitride
region  num=2  y.min=0. y.max=0.04 silicon
region  num=3  y.min=0.04 y.max=0.08 silicon
region  num=4  y.min=0.08 oxide

# Define electrodes: 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate
elec num=1 x.min=50 x.max=100 y.min=-0.3 y.max=-0.3 name=gate
elec num=2 x.min=0. x.max=20. y.min=0.08 y.max=0.08 name=source
elec num=3 x.min=130. x.max=150. y.min=0.08 y.max=0.08 name=drain

# Define doping
doping reg=2 uniform conc=1.e11 n.type
doping reg=3 uniform conc=1.e11 n.type
```

```
doping reg=3 gauss  conc=1.e20 n.type  x.right=50 char=0.3
doping reg=3 gauss  conc=1.e20 n.type  x.left=100 char=0.3

save outf=std_str_l=50.str


mesh inf = str/std_str_l = 50.str

# Set nc-Si:H material parameters

material material=silicon mun=65 mup=3

defects   nta=1.e20 ntd=1.e20 wta=0.025 wtd=0.025 \
          nga=3.7e17 ngd=3.7e17 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
          sigtae=1.0e-16 sigtah=1.0e-14 sigtde=1.0e-14 sigtdh=1.0e-16 \
          siggae=1.0e-16 siggah=1.0e-14 siggde=1.0e-14 siggdh=1.0e-16 \

dfile=donors.dat afile=acceptors.dat \
numa=36 numd=36
interface qf=1.5e11

# Define contact parameters
contact num=1 alum
contact num=2 alum resistance=1.e7
contact num=3 alum resistance=1.e7

# Define models
models srh print trap.coulombic

# Enable the following parameters for study of scattering effects
# mobility en.cvt=1 dn.cvt=0.333 ep.cvt=1 dp.cvt=0.333 kn.cvt=2 kp.cvt=2

method newton
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
solve vdrain=1 vfinal=10 vstep=1 name=drain

log outf = forward_l=50.log
solve vgate=0 vstep=0.5 vfinal=30 name=gate
go atlas

extract init infile="forward_l=50.log"
extract name="forward_l=50" curve(v."gate", i."drain") outf="forward_l=50.dat"
extract name="gm_l=50" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_l=50.dat"
extract name="nvt" (xintercept(maxslope(curve(v."gate",(i."drain")))))-(ave(v."drain")/2.0)

go atlas
TITLE Generation of top gate-staggered source/drain TFT structure.

# Define TFT structure: standard (L_off = 0), L = 70 um, t_ch = 80 nm, t_ox = 300 nm
mesh
x.m  l=0  spac=2.
```

```
x.m  l=20  spac=3.
x.m  l=35  spac=5.
x.m  l=50  spac=0.25
x.m  l=85  spac=3.
x.m  l=120  spac=0.25
x.m  l=135  spac=5.
x.m  l=150  spac=3.
x.m  l=170  spac=2.

y.m l=-0.3 spac=0.05
y.m l=0 spac=0.0075
y.m l=0.04 spac=0.01
y.m l=0.08 spac=0.0075
y.m l=0.4 spac=0.25
y.m l=10. spac=5.

# Define regions: 1=nitride, 2 and 3=silicon, 4=nitride
region  num=1  y.max=0. nitride
region  num=2  y.min=0. y.max=0.04 silicon
region  num=3  y.min=0.04 y.max=0.08 silicon
region  num=4  y.min=0.08 oxide

# Define electrodes: 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate
elec num=1 x.min=50 x.max=120 y.min=-0.3 y.max=-0.3 name=gate
elec num=2 x.min=0. x.max=20. y.min=0.08 y.max=0.08 name=source
elec num=3 x.min=150. x.max=170. y.min=0.08 y.max=0.08 name=drain

# Define doping
doping reg=2 uniform conc=1.e11 n.type
doping reg=3 uniform conc=1.e11 n.type
doping reg=3 gauss  conc=1.e20 n.type  x.right=50 char=0.3
doping reg=3 gauss  conc=1.e20 n.type  x.left=120 char=0.3

save outf=std_str_l=70.str

mesh inf = str/std_str_l = 70.str

# Set nc-Si:H material parameters

material  material=silicon mun=65 mup=3

defects   nta=1.e20 ntd=1.e20 wta=0.025 wtd=0.025 \
              nga=3.7e17 ngd=3.7e17 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
              sigtae=1.0e-16 sigtah=1.0e-14 sigtde=1.0e-14 sigtdh=1.0e-16 \
              siggae=1.0e-16 siggah=1.0e-14 siggde=1.0e-14 siggdh=1.0e-16 \

dfile=donors.dat afile=acceptors.dat \
numa=36 numd=36
interface qf=1.5e11

# Define contact parameters
contact num=1 alum
contact num=2 alum resistance=1.e7
```

```
contact num=3 alum resistance=1.e7

# Define models
models srh print trap.coulombic

# Enable the following parameters for study of scattering effects
# mobility en.cvt=1 dn.cvt=0.333 ep.cvt=1 dp.cvt=0.333 kn.cvt=2 kp.cvt=2

method newton
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
solve vdrain=1 vfinal=10 vstep=1 name=drain


log outf = forward_l=70.log
solve vgate=0 vstep=0.5 vfinal=30 name=gate
go atlas

extract init infile="forward_l=70.log"
extract name="forward_l=70" curve(v."gate", i."drain") outf="forward_l=70.dat"
extract name="gm_l=70" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_l=70.dat"
extract name="nvt" (xintercept(maxslope(curve(v."gate",(i."drain")))))-(ave(v."drain")/2.0)


go atlas
TITLE Generation of top gate-staggered source/drain TFT structure.

# Define TFT structure: standard (L_off = 0), L = 60 um, t_ch = 80 nm, t_ox = 300 nm
mesh
x.m  l=0  spac=2.
x.m  l=20  spac=3.
x.m  l=35  spac=5.
x.m  l=50  spac=0.25
x.m  l= 80 spac=3.
x.m  l=110  spac=0.25
x.m  l=115  spac=5.
x.m  l=130  spac=3.
 x.m  l=150  spac=2.

y.m l=-0.3 spac=0.05
y.m l=0 spac=0.0075
y.m l=0.04 spac=0.01
y.m l=0.08 spac=0.0075
y.m l=0.4 spac=0.25
y.m l=10. spac=5.

# Define regions: 1=nitride, 2 and 3=silicon, 4=nitride
region  num=1  y.max=0. nitride
region  num=2  y.min=0. y.max=0.04 silicon
region  num=3  y.min=0.04 y.max=0.08 silicon
region  num=4  y.min=0.08 oxide
```

```
# Define electrodes: 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate
elec num=1 x.min=50 x.max=110 y.min=-0.3 y.max=-0.3 name=gate
elec num=2 x.min=0. x.max=20. y.min=0.08 y.max=0.08 name=source
elec num=3 x.min=130. x.max=150. y.min=0.08 y.max=0.08 name=drain

# Define doping
doping reg=2 uniform conc=1.e11 n.type
doping reg=3 uniform conc=1.e11 n.type
doping reg=3 gauss  conc=1.e20 n.type  x.right=50 char=0.3
doping reg=3 gauss  conc=1.e20 n.type  x.left=110 char=0.3

save outf=std_str_l=60.str

mesh inf = str/std_str_l = 60.str

# Set nc-Si:H material parameters

material material=silicon mun=65 mup=3

defects   nta=1.e20 ntd=1.e20 wta=0.025 wtd=0.025 \
                    nga=3.7e17 ngd=3.7e17 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
                    sigtae=1.0e-16 sigtah=1.0e-14 sigtde=1.0e-14 sigtdh=1.0e-16 \
                    siggae=1.0e-16 siggah=1.0e-14 siggde=1.0e-14 siggdh=1.0e-16 \

dfile=donors.dat afile=acceptors.dat \
numa=36 numd=36
interface qf=1.5e11

# Define contact parameters
contact num=1 alum
contact num=2 alum resistance=1.e7
contact num=3 alum resistance=1.e7

# Define models
models srh print trap.coulombic

# Enable the following parameters for study of scattering effects
# mobility en.cvt=1 dn.cvt=0.333 ep.cvt=1 dp.cvt=0.333 kn.cvt=2 kp.cvt=2

method newton
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
solve vdrain=1 vfinal=10 vstep=1 name=drain


log outf = forward_l=60.log
solve vgate=0 vstep=0.5 vfinal=30 name=gate
go atlas

extract init infile="forward_l=60.log"
extract name="forward_l=60" curve(v."gate", i."drain") outf="forward_l=60.dat"
```

```
extract name="gm_l=60" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_l=60.dat"
extract name="nvt" (xintercept(maxslope(curve(v."gate",(i."drain")))))-(ave(v."drain")/2.0)


go atlas
TITLE Generation of top gate-staggered source/drain TFT structure.

# Define TFT structure: standard (L_off = 0), L = 80 um, t_ch = 80 nm, t_ox = 300 nm
mesh
x.m  l=0  spac=2.
x.m  l=20  spac=3.
x.m  l=35  spac=5.
x.m  l=50  spac=0.25
x.m  l=90 spac=3.
x.m  l=130  spac=0.25
x.m  l=145  spac=5.
x.m  l=160  spac=3.
 x.m  l=180  spac=2.

y.m l=-0.3 spac=0.05
y.m l=0 spac=0.0075
y.m l=0.04 spac=0.01
y.m l=0.08 spac=0.0075
y.m l=0.4 spac=0.25
y.m l=10. spac=5.

# Define regions: 1=nitride, 2 and 3=silicon, 4=nitride
region  num=1  y.max=0. nitride
region  num=2  y.min=0. y.max=0.04 silicon
region  num=3  y.min=0.04 y.max=0.08 silicon
region  num=4  y.min=0.08 oxide

# Define electrodes: 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate
elec num=1 x.min=50 x.max=130 y.min=-0.3 y.max=-0.3 name=gate
elec num=2 x.min=0. x.max=20. y.min=0.08 y.max=0.08 name=source
elec num=3 x.min=160. x.max=180. y.min=0.08 y.max=0.08 name=drain

# Define doping
doping reg=2 uniform conc=1.e11 n.type
doping reg=3 uniform conc=1.e11 n.type
doping reg=3 gauss  conc=1.e20 n.type  x.right=50 char=0.3
doping reg=3 gauss  conc=1.e20 n.type  x.left=130 char=0.3

save outf=std_str_l=80.str


mesh inf = str/std_str_l = 80.str

# Set nc-Si:H material parameters

material material=silicon mun=65 mup=3

defects   nta=1.e20 ntd=1.e20 wta=0.025 wtd=0.025 \
```

```
                              nga=3.7e17 ngd=3.7e17 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
                              sigtae=1.0e-16 sigtah=1.0e-14 sigtde=1.0e-14 sigtdh=1.0e-16 \
                              siggae=1.0e-16 siggah=1.0e-14 siggde=1.0e-14 siggdh=1.0e-16 \

dfile=donors.dat afile=acceptors.dat \
numa=36 numd=36
interface qf=1.5e11

# Define contact parameters
contact num=1 alum
contact num=2 alum resistance=1.e7
contact num=3 alum resistance=1.e7

# Define models
models srh print trap.coulombic

# Enable the following parameters for study of scattering effects
# mobility en.cvt=1 dn.cvt=0.333 ep.cvt=1 dp.cvt=0.333 kn.cvt=2 kp.cvt=2

method newton
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
solve vdrain=1 vfinal=10 vstep=1 name=drain

log outf = forward_l=80.log
solve vgate=0 vstep=0.5 vfinal=30 name=gate
go atlas

extract init infile="forward_l=80.log"
extract name="forward_l=80" curve(v."gate", i."drain") outf="forward_l=80.dat"
extract name="gm_l=80" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_l=80.dat"
extract name="nvt" (xintercept(maxslope(curve(v."gate",(i."drain")))))-(ave(v."drain")/2.0)

go atlas
TITLE Generation of top gate-staggered source/drain TFT structure.

# Define TFT structure: standard (L_off = 0), L = 90 um, t_ch = 80 nm, t_ox = 300 nm
mesh
x.m  l=0  spac=2.
x.m  l=20  spac=3.
x.m  l=35  spac=5.
x.m  l=50  spac=0.25
x.m  l=90 spac=3.
x.m  l=140  spac=0.25
x.m  l=155  spac=5.
x.m  l=170  spac=3.
 x.m  l=190  spac=2.

y.m l=-0.3 spac=0.05
y.m l=0 spac=0.0075
y.m l=0.04 spac=0.01
y.m l=0.08 spac=0.0075
```

```
y.m l=0.4 spac=0.25
y.m l=10. spac=5.

# Define regions: 1=nitride, 2 and 3=silicon, 4=nitride
region  num=1  y.max=0. nitride
region  num=2  y.min=0. y.max=0.04 silicon
region  num=3  y.min=0.04 y.max=0.08 silicon
region  num=4  y.min=0.08 oxide

# Define electrodes: 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate
elec num=1 x.min=50 x.max=140 y.min=-0.3 y.max=-0.3 name=gate
elec num=2 x.min=0. x.max=20. y.min=0.08 y.max=0.08 name=source
elec num=3 x.min=170. x.max=190. y.min=0.08 y.max=0.08 name=drain

# Define doping
doping reg=2 uniform conc=1.e11 n.type
doping reg=3 uniform conc=1.e11 n.type
doping reg=3 gauss  conc=1.e20 n.type  x.right=50 char=0.3
doping reg=3 gauss  conc=1.e20 n.type  x.left=140 char=0.3

save outf=std_str_l=90.str

mesh inf = str/std_str_l = 90.str

# Set nc-Si:H material parameters

material material=silicon mun=65 mup=3

defects   nta=1.e20 ntd=1.e20 wta=0.025 wtd=0.025 \
              nga=3.7e17 ngd=3.7e17 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
              sigtae=1.0e-16 sigtah=1.0e-14 sigtde=1.0e-14 sigtdh=1.0e-16 \
              siggae=1.0e-16 siggah=1.0e-14 siggde=1.0e-14 siggdh=1.0e-16 \

dfile=donors.dat afile=acceptors.dat \
numa=36 numd=36
interface qf=1.5e11

# Define contact parameters
contact num=1 alum
contact num=2 alum resistance=1.e7
contact num=3 alum resistance=1.e7

# Define models
models srh print trap.coulombic

# Enable the following parameters for study of scattering effects
# mobility en.cvt=1 dn.cvt=0.333 ep.cvt=1 dp.cvt=0.333 kn.cvt=2 kp.cvt=2

method newton
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
```

```
solve vdrain=1 vfinal=10 vstep=1 name=drain


log outf = forward_l=90.log
solve vgate=0 vstep=0.5 vfinal=30 name=gate
go atlas

extract init infile="forward_l=90.log"
extract name="forward_l=90" curve(v."gate", i."drain") outf="forward_l=90.dat"
extract name="gm_l=90" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_l=90.dat"
extract name="nvt" (xintercept(maxslope(curve(v."gate",(i."drain")))))-(ave(v."drain")/2.0)
go atlas
TITLE Generation of top gate-staggered source/drain TFT structure.

# Define TFT structure: standard (L_off = 0), L = 100 um, t_ch = 80 nm, t_ox = 300 nm
mesh
x.m  l=0  spac=2.
x.m  l=20  spac=3.
x.m  l=35  spac=5.
x.m  l=50  spac=0.25
x.m  l=100 spac=3.
x.m  l=150  spac=0.25
x.m  l=165  spac=5.
x.m  l=180  spac=3.
 x.m  l=200  spac=2.

y.m l=-0.3 spac=0.05
y.m l=0 spac=0.0075
y.m l=0.04 spac=0.01
y.m l=0.08 spac=0.0075
y.m l=0.4 spac=0.25
y.m l=10. spac=5.

# Define regions: 1=nitride, 2 and 3=silicon, 4=nitride
region  num=1  y.max=0. nitride
region  num=2  y.min=0. y.max=0.04 silicon
region  num=3  y.min=0.04 y.max=0.08 silicon
region  num=4  y.min=0.08 oxide

# Define electrodes: 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate
elec num=1 x.min=50 x.max=150 y.min=-0.3 y.max=-0.3 name=gate
elec num=2 x.min=0. x.max=20. y.min=0.08 y.max=0.08 name=source
elec num=3 x.min=180. x.max=200. y.min=0.08 y.max=0.08 name=drain

# Define doping
doping reg=2 uniform conc=1.e11 n.type
doping reg=3 uniform conc=1.e11 n.type
doping reg=3 gauss  conc=1.e20 n.type  x.right=50 char=0.3
doping reg=3 gauss  conc=1.e20 n.type  x.left=150 char=0.3

save outf=std_str_l=100.str
tonyplot std_str_l=100.str
```

```
mesh inf = str/std_str_l = 100.str

# Set nc-Si:H material parameters

material material=silicon mun=65 mup=3

defects   nta=1.e20 ntd=1.e20 wta=0.025 wtd=0.025 \
                    nga=3.7e17 ngd=3.7e17 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
                    sigtae=1.0e-16 sigtah=1.0e-14 sigtde=1.0e-14 sigtdh=1.0e-16 \
                    siggae=1.0e-16 siggah=1.0e-14 siggde=1.0e-14 siggdh=1.0e-16 \

dfile=donors1.dat afile=acceptors1.dat \
numa=36 numd=36
interface qf=1.5e11

# Define contact parameters
contact num=1 alum
contact num=2 alum resistance=1.e7
contact num=3 alum resistance=1.e7

# Define models
models srh print trap.coulombic

# Enable the following parameters for study of scattering effects
# mobility en.cvt=1 dn.cvt=0.333 ep.cvt=1 dp.cvt=0.333 kn.cvt=2 kp.cvt=2

method newton
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
solve vdrain=1 vfinal=10 vstep=1 name=drain


log outf = forward_l=100.log
solve vgate=0 vstep=0.5 vfinal=30 name=gate
go atlas

extract init infile="forward_l=100.log"
extract name="forward_l=100" curve(v."gate", i."drain") outf="forward_l=100.dat"
extract name="gm_l=100" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_l=100.dat"
extract name="nvt" (xintercept(maxslope(curve(v."gate",(i."drain")))))-(ave(v."drain")/2.0)


tonyplot -overlay forward_l=50.dat forward_l=70.dat  forward_l=60.dat  forward_l=80.dat
forward_l=90.dat forward_l=100.dat
tonyplot -overlay gm_l=50.dat gm_l=70.dat gm_l=60.dat  gm_l=80.dat gm_l=90.dat gm_l=100.dat

quit
```

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LIST OF PUBLICATIONS

Publication in Peer Reviewed Journals:

1. **Prachi Sharma** and Navneet Gupta, "Model for threshold voltage instability in top-gated nanocrystalline silicon thin film transistor" *Journal of Computational Electronics* (*Springer*), pp. 666-671, vol. 15, issue 2, 2016. **[SCI Indexed]**
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3. **Prachi Sharma** and Navneet Gupta, "Threshold Voltage Modeling on Nanocrystalline Silicon Thin-Film Transistors", *Journal of Electron Devices*, pp. 1608-1612, vol. 19, 2014.
4. Abhishek Mukherjee, **Prachi Sharma** and Navneet Gupta, "Modeling of Field Effect Mobility using Grain Boundaries on Nanocrystalline Silicon Thin-Film Transistor (nc-Si TFT)" *Journal of Nano- and Electronic Physics*, pp. 04054-1-3, vol. 5, 2013. **[Scopus Indexed]**
5. **Prachi Sharma** and Navneet Gupta, "Two dimensional simulation and analysis of density-of-states (DOS) in top-gated nanocrystalline silicon thin film transistor (nc-Si TFT)" *Nanotechnology and Nanomaterials Journal*, March, 2016. [SCI Indexed] [communicated]
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1. **Prachi Sharma** and Navneet Gupta, "Investigation of channel material quality effect on the top-gated nanocrystalline silicon thin film transistor (nc-Si TFT) performance using ATLAS SILVACO" 18th International Workshop on the Physics of Semiconductor Devices (IWPSD-2015), IISC Bangalore, December 7-10, 2015.
2. **Prachi Sharma** and Navneet Gupta, "Deposition of Nanocrystalline Silicon (nc-Si) Thin Film by E-beam Evaporation for Display Application" National Conference on Advances in Microelectronics, Instrumentation and Communication (MICOM-2015), BITS Pilani, Pilani Campus, Rajasthan, November 20-22, 2015. **(Best Poster Award)**

3. **Prachi Sharma** and Navneet Gupta, "Nanocrystalline Silicon Thin Film Transistor (nc-si:H TFTs)- A Device for Display Panels" International conference on Communication Systems (ICCS-2013), BKBIET, Pilani, Rajasthan, October 18-21, 2013.
4. **Prachi Sharma** and Navneet Gupta, "Model for Drain Current based on the Exponential Distribution of Tail States for Nanocrystalline Silicon Thin Film Transistor" 3rd IEEE International Advance Computing Conference (IACC-2013), AKGEC, Ghaziabad, U.P., February 22-23, 2013.
5. Abhishek Mukherjee, **Prachi Sharma** and Navneet Gupta, "Modeling of Field Effect Mobility using Grain Boundaries on Nanocrystalline Silicon Thin-Film Transistor (nc-Si TFT)" Second International Symposium on Semiconductor Materials and Devices (ISSMD-2), Jammu University, Jammu, Jammu and Kashmir, January 31 to February 2, 2013.

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