Chapter 7

Hardware Implementation of Simple UPQC

Introduction

To mitigate the power quality issues in DG based MG distribution system, UPQC is proven to be a multipurpose device for solving various PQ issues simultaneously. The design and modeling of the UPQC to provide compensation are analyzed using the models developed in MATLAB/Simulink and the results that are presented in the previous chapter validate the effectiveness of the device against all PQ problems. In addition to the above, to validate the performance of the device experimentally, a mini UPQC has been developed in the laboratory to mitigate the voltage issues of an MG. The MG considered is a PV-Wind emulator which is a scale down experiment setup to replicate the actual MG.

7.1 MG-UPQC in Real Time

An MG containing two DERs, one as a PV generation and the other one as a WECS is considered as shown in Figure 7.1. The considered MG is delivering a source voltage V_{Source} at the common

AC bus and connected to the load circuit. The load voltage V_{load} differs from the supply voltage (reference voltage) due to environmental conditions or load changes. The difference between these two voltages is V_{comp} and is to be compensated by using a compensating device to maintain the output voltage at constant which in turn makes the difference between the voltages as zero. In this work, the device UPQC is considered to provide the compensation for a dip/sag condition in the voltage. A control circuit is implemented in UPQC to provide voltage sag compensation in real time. In this regard, MG hardware setup by using PV-WECS emulator, control unit, UPQC design, the experimental setup of UPQC are discussed further.

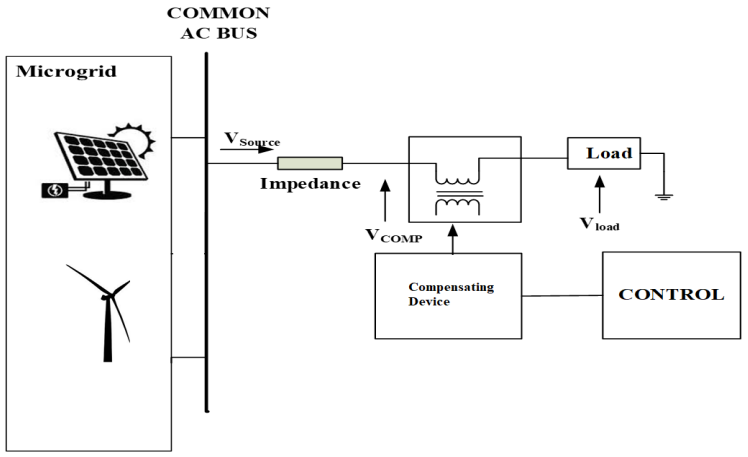


FIGURE 7.1: Block diagram of PV-WECS MG experimental setup

7.1.1 PV-WECS Emulator

A PV-WECS emulator that represents a MG, with an experimental setup of 800 W PV and 1.2 kW wind power emulator is utilized. The experimental setup is shown in Figure 7.2. The major elements of the setup are PV emulator, wind emulator converter circuit, load and user control and interface (UCI) as shown in Figure 7.2.

The details of each element are described below.

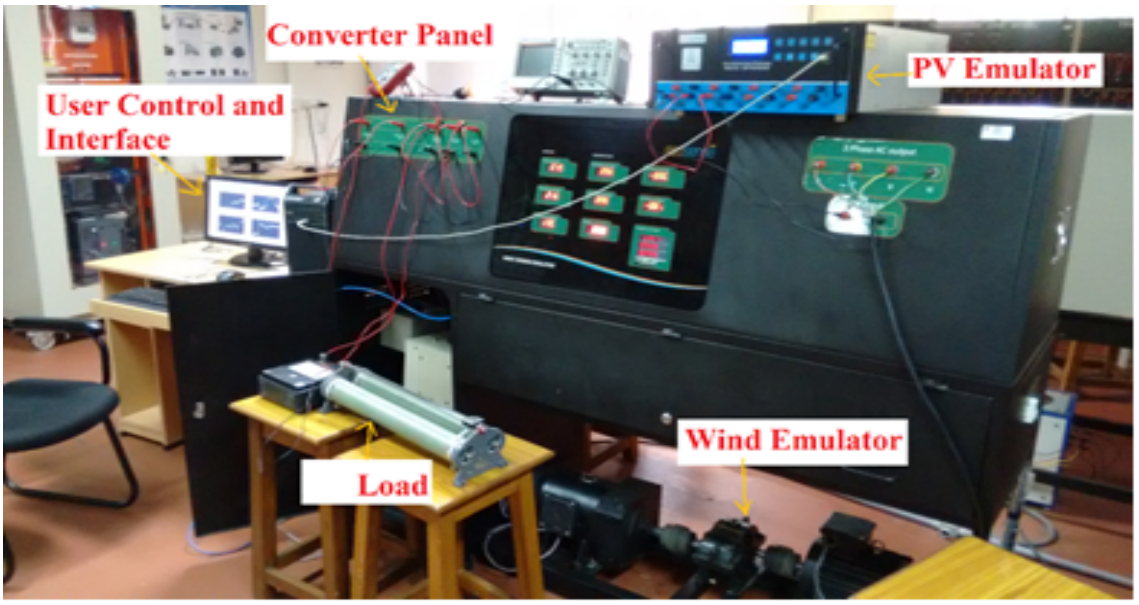


FIGURE 7.2: PV-Wind emulator experimental setup

7.1.2 PV Emulator

The PV emulator has 4 out channels each with 0-50 V that can be connected in series and parallel combination to obtain desired output power as shown in Figure 7.3. The four channels are connected in series for the experimental investigation. It is a programmable power supply designed to emulate solar panels with the fast transient response, the emulator responds to change in load conditions and maintains the output on IV characteristics of the selected panel for a given ambient condition.The PV emulator uses an internal algorithm to adjust V_{OC} (Open Circuit Voltage) and I_{SC} (Short Circuit Current) so as to match the solar panel selected by the user based on ambient temperatures, solar irradiation levels etc. PV emulator takes into account the weather conditions at the time of year specified, the position of the sun at the hour specified, location and position of the panel, manufacturer of the panel. It also includes a user control to test response for a wide range of solar panels from which a panel can be selected that matches the manufacturer's data sheet. In addtion, an appropriate MPPT tarcking algorithm of PV inverter can also be selected. The PV emulator also consists of inbuilt buck-boost converter to step up/down to desired DC and inverter ciruits as shown in Figure 7.4 The ratings of the PV emualtor are listed below in the Table. 7.1.

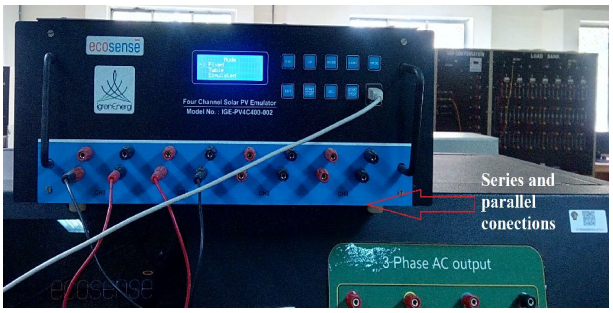


FIGURE 7.3: PV-Wind emulator

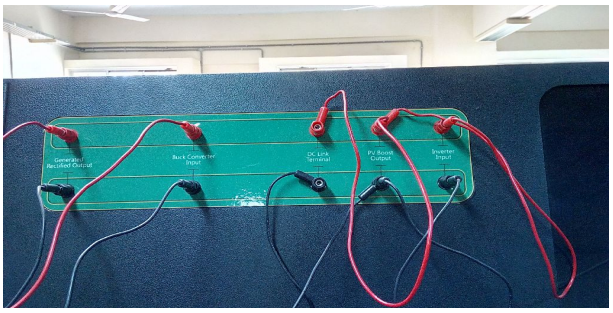


FIGURE 7.4: PV-Wind emulator

TABLE 7.1: PV emulator specifications

No. of Channels = 4		
Input	Supply voltage	230 V AC, 50 Hz
	I_{SC} (Short Circuit Current)	0-8 A
	V_{OC} (Open Circuit Voltage)	0- 50 V DC
	Max. output power/channel	400 W
Output	Maximum channels in Series/parallel	4
	Maximum absolute voltage at the ouput	200 V DC
	Modes of operation	Fixed mode, Table mode, Simulator Mode, Programming mode

7.1.3 WECS Emulator

A WECS emulator mimics the behavior of actual wind turbine under contolled manner. Essentially it simulates the same operating pattern at hardware level in real time similar to what an actual wind turbine does at given operating parameters of wind speed and pitch angle. It consists of a DC shunt motor coupled to electrical generator whih is used as wind power generator as shown in Figure 7.5. FPGA board is utilised for solving the differential eqautions in real time, additionally on board ADC channels and PWM port for power electronic converter/inverter firing. A slip ring induction generator is mechanically coupled to gear box. A power conditioning unit (diode

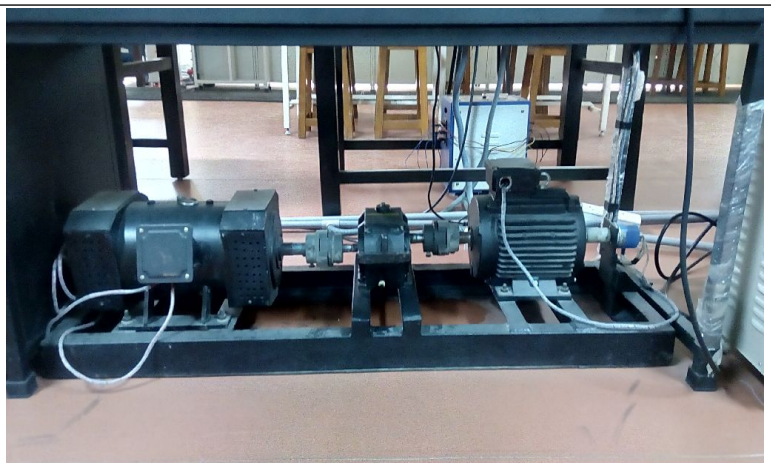


FIGURE 7.5: WECS emulator

TABLE 7.2: Electrical parameters of WECS emulator and converter circuit

Components	**Specifications**	**Components**	**Specifications**
DC motor		**DC drive**	
Output power	3.5 kW (5 HP)	DC link capacitor	3300 F, 450 V DC
Nominal field voltage	220 V DC	Control	Fixed field
Nominal armature voltage	220 V DC	Topology	Buck converter
Speed at rated voltage	1500 rpm	Rating	15A, 250 V DC
AC generator		Switching frequency	60 kHz
Output power	1.2 kW	**Bridge rectifier**	
Line to Line voltage	415 V AC	Rating	10 A, 400 V

bridge rectifier and three phase inverter) is provided along with a sensor board that senses the rectifier DC link voltage, generated voltages/currents. The details of the wind emulator are listed in Table. 7.2.

7.1.4 PV-WECS Emulator Converter and UCI

The PV- wind emulator converter circuit is shown in the Figure 7.6. The details of the converter are given in Table. 7.2. This represents the PV system connected to the WECS and obtaining a 3-phase output at the common AC bus terminals. The interface to the hardware is employed using a software based user control and monitoring system through LabVIEW system design software as shown in Figure 7.7. The real-time data of solar illumination and wind speed are imported into the emulator through the software interface. Voltage quality issues that cause sag due to changes in solar insolation, wind speed, and various load conditions are observed. To

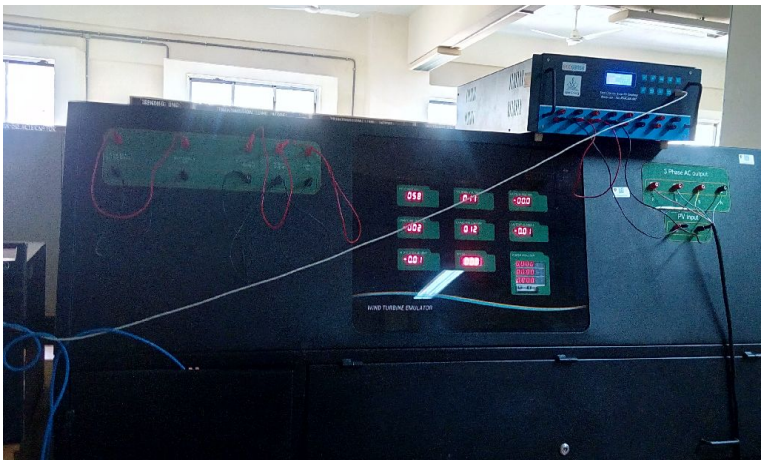


FIGURE 7.6: PV-Wind emulator

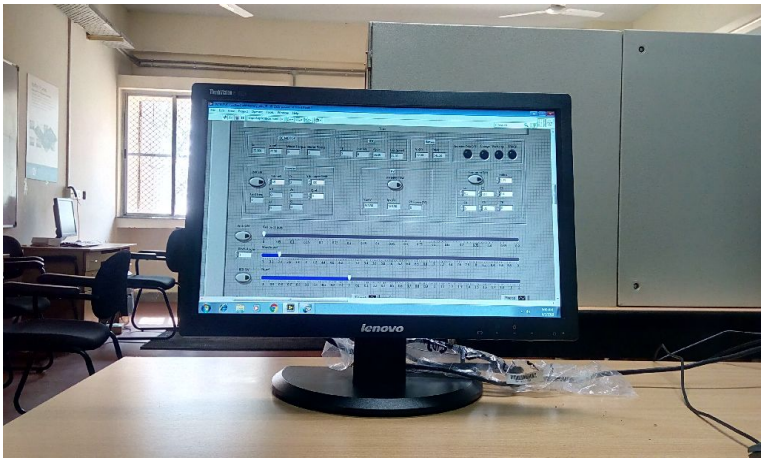


FIGURE 7.7: User control interfacing of PV-Wind emulator

mitigate these concerned issues, a compensating device UPQC has been mathematically modeled, designed and implemented. The details of a hardware implementation of UPQC are discussed in the next section.

7.1.5 UPQC in MG

To deal with the PQ issues in MG, a compensating device, UPQC is considered as shown in the Figure 7.1. The operation of the UPQC is limited to sag mitigation only due to the available laboratory facilities for the experimental setup. UPQC is a combination of series and shunt APF as shown in the Figure 7.8. The series APF mitigates all voltage quality problems whereas shunt converter mitigates all current quality problems. The problem considered in this case is sag, which is based on voltage quality. Hence the modeling and design of UPQC are carried

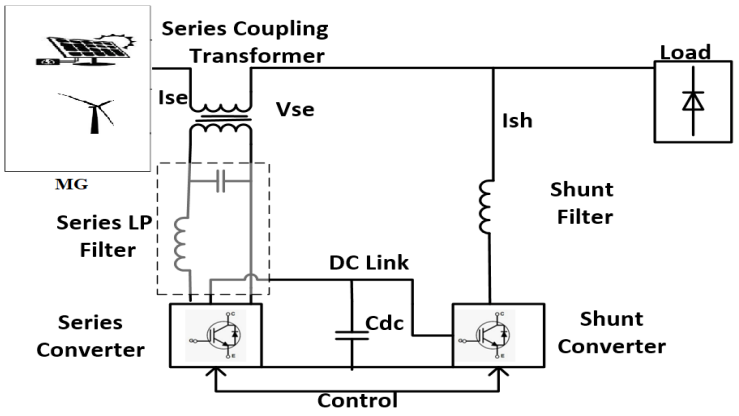


FIGURE 7.8: Block diagram of UPQC in MG

in terms of voltage compensation by its series converter. The DC link voltage is replaced by means of an external DC source. The experimental setup of UPQC in MG is shown in Figure 7.9. The prototype for UPQC system is designed, developed and implemented for a PV-WECS MG compensation in the laboratory as shown in Figure 7.9. The major elements of the prototype consist of : Voltage Source Inverter (VSI) which is realized using Insulated Gate Bipolar Transistor (IGBT) swicthes; Sensors to sense the input and output (Load) voltages; Power Supplies 0-100V DC for inverter DC supply; 0-15 V DC for gate trigger circuit etc.; Injection transformer; Auto transformer vi) Amplifying circuits (no.4) using LM741; DS 1103 controller board viii) PC with RTI (Real Time Interface) of DS 1103; Filter circuit (L= 2 mH and C= 100 μF); PWM logic controller developed in MATLAB/Simulink; Sag generator using Manual switch.

7.1.6 Control Ciruit of UPQC

In order to mitigate the sag in the output voltage, series APF of the UPQC is to be operated. The functioning algorithm (known as feedforward algorithm) to control series VSC of UPQC is shown in the Figure 7.10. The source and load voltages are sensed and compared by using sensing circuits shown in Figure. 7.11(a). Sensing circuits are used to sense the actual source and load voltages and the voltage will be scaled down to 5 V to suit the DSPACE I/O ADCs to read the values. The source voltage is considered as a reference voltage. If there exists any difference between both the voltages, the difference voltage (positive in case of sag, negative in

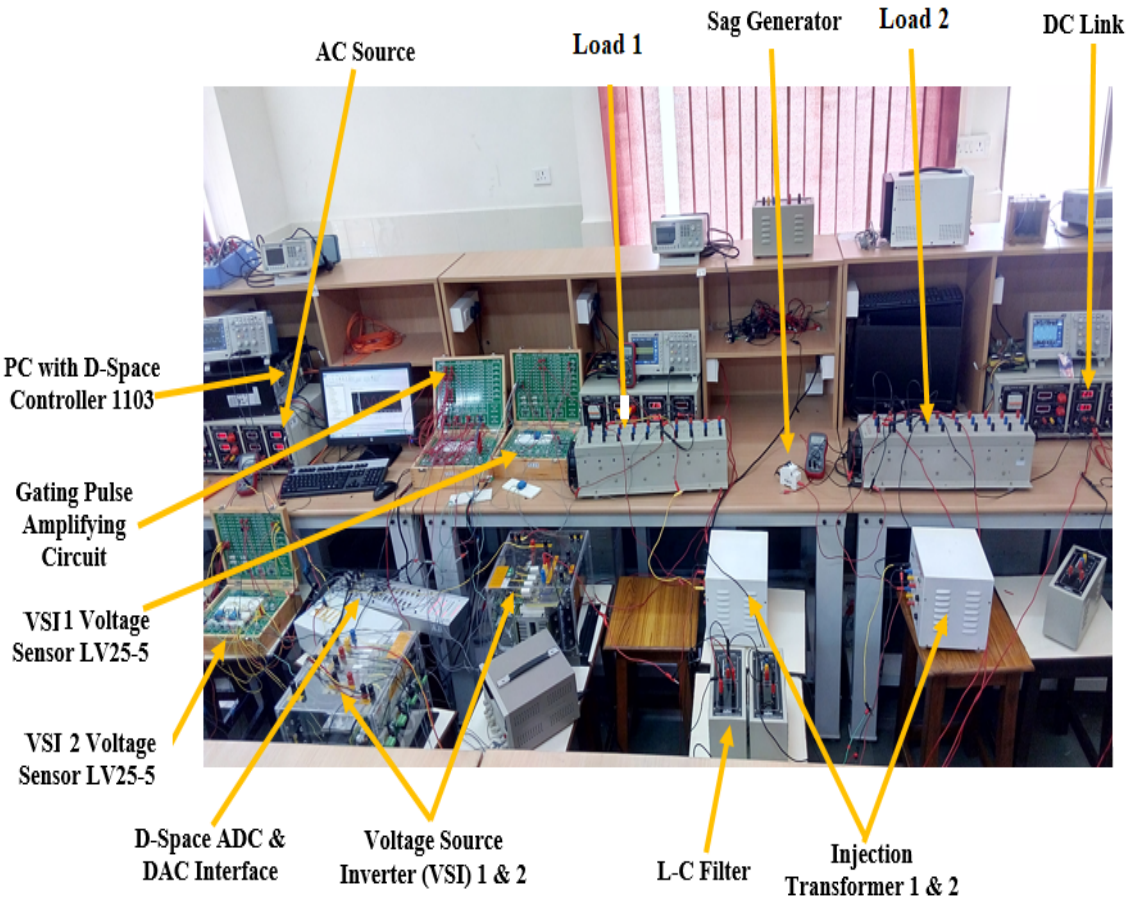


FIGURE 7.9: MG-UPQC experimental setup

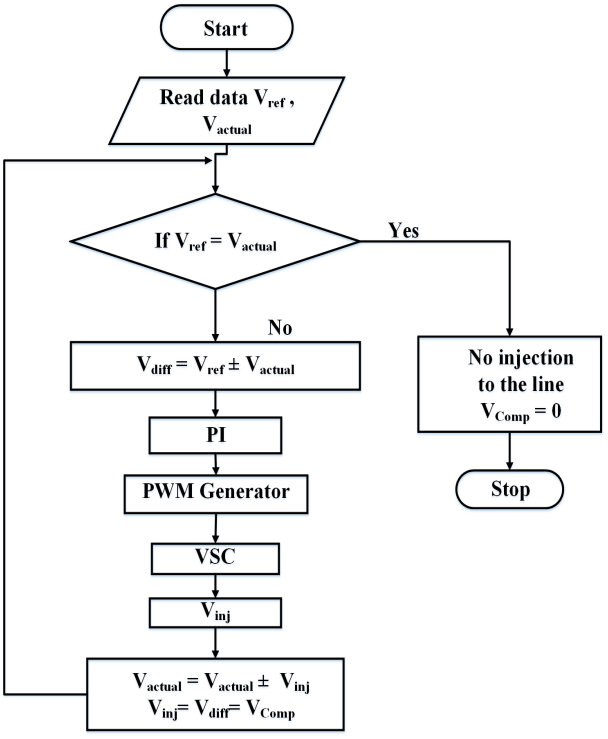
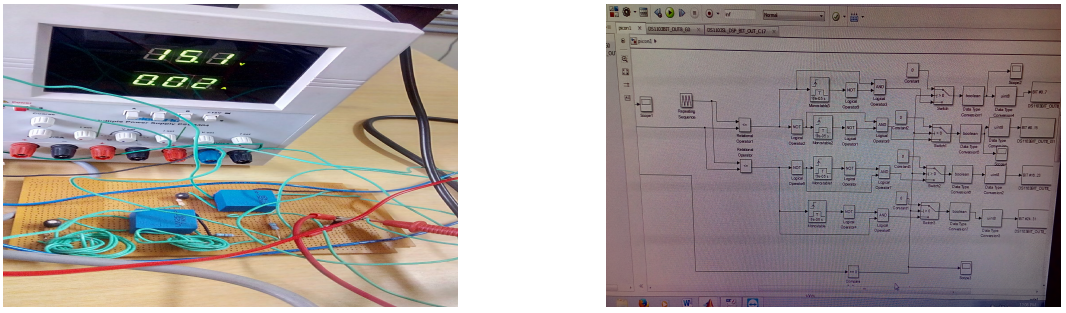


FIGURE 7.10: Flow chart for the control of UPQC in MG

case of swell) is computed. Further, these values are fed to PWM logic control using real-time interface (RTI) in MATLAB/Simulink to perform PWM generation. The error(difference) signal between the actual and reference voltage is used as a modulation signal, that allows, to generate a commutation pattern for the power switches (IGBT's) of series VSC of the UPQC. Injected voltage magnitude is controlled through this modulation. Thus the PWM gate pulses are derived from PWM are taken using RTI and fed to DSPACE 1103 control board as shown in Figure 7.12(a). From this, the gate pulses are taken and fed to amplifier circuits to get amplified as the minimum required voltage for the gate circuit to trigger is 13.5 V. The gate signals from DSPACE and connected to amplifiers are shown in Figure 7.12(b). These amplified signals are fed to the VSC of the UPQC shown in Figure 7.13(a) to generate the voltage to be injected. The voltage will be injected into the circuit to retain the output voltage near to the reference voltage, however, contains harmonics. To eliminate these injection harmonics, a filter shown in Figure 7.13(b)is connected to the inverter. The output of the filter circuit of the series VSC of UPQC is the required voltage and injected into the circuit using injection transformer shown in Figure 7.13(c). The overall circuit diagram of the complete series APF of UPQC to mitigate the sag is shown in Figure 7.14.

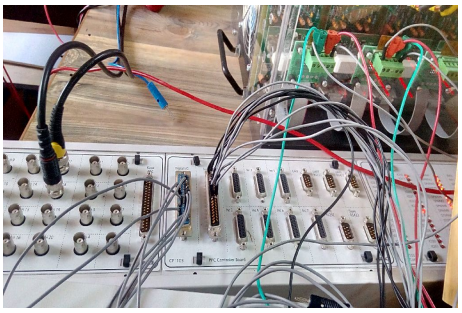


(a) I/O Sensor (b) RTI to DSPACE

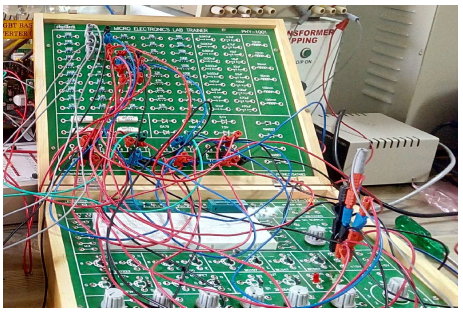
FIGURE 7.11: Sensing circuit and RTI

7.1.7 Design of UPQC for Sag Mitigation

The actual sag problem in the MG considered as follows: Initially, the MG with 20 V acting as a source with 25 Ω delivers a load of 50 Ω via an autotransformer. The output voltage in this condition is 13 V. Further a load of 100 Ω is connected in addition using a manual switch

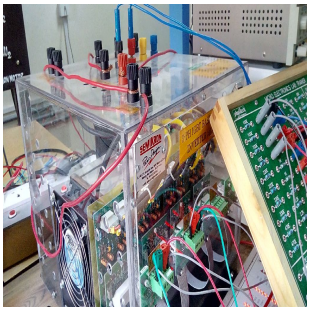


(a) DSPACE controller board



(b) Amplifier circuits of gate signals

FIGURE 7.12: DSPACE contoller board and Amplifier circuits



(a) Inverter of VSC

(b) Filter connected to VSC

(c) Injection transformer of VSC

FIGURE 7.13: VSC circuit of UPQC

as shown in the Figure 7.15 to create a sag such that the output voltage is dropped to 11 V. Now the aim is to mitigate these drop and sag in the load voltage. Hence a mini UPQC with scale down experimental setup has been designed and developed in the laboratory. The design of UPQC includes the voltage rating of the VSC of the series APF, the current rating of the VSC, injection transformer rating, DC bus voltage, DC bus capacitance, AC interfacing inductance, and ripple factor. The UPQC for voltage compensation has been designed relatively using the same design procedure mentioned in 4.6.4. In the present case, the design of UPQC is downscaled to lower level based on the nature of load connected.

The voltage rating of the VSC of UPQC:

Consider a voltage fluctuation of 52% voltage dip in an MG acting as a 20 V source(MG) with 25 Ω delivers a load of 50 Ω via an autotransformer. Further, a load of 100 Ω is connected using a manual switch to create a sag. Due to this, initially the load voltage is dropped to 13 V when the switch is closed for a while to create the sag, it is further dropped to 11 V. The voltage rating of the VSC of UPQC depends on the maximum voltage to be injected in this condition. However in

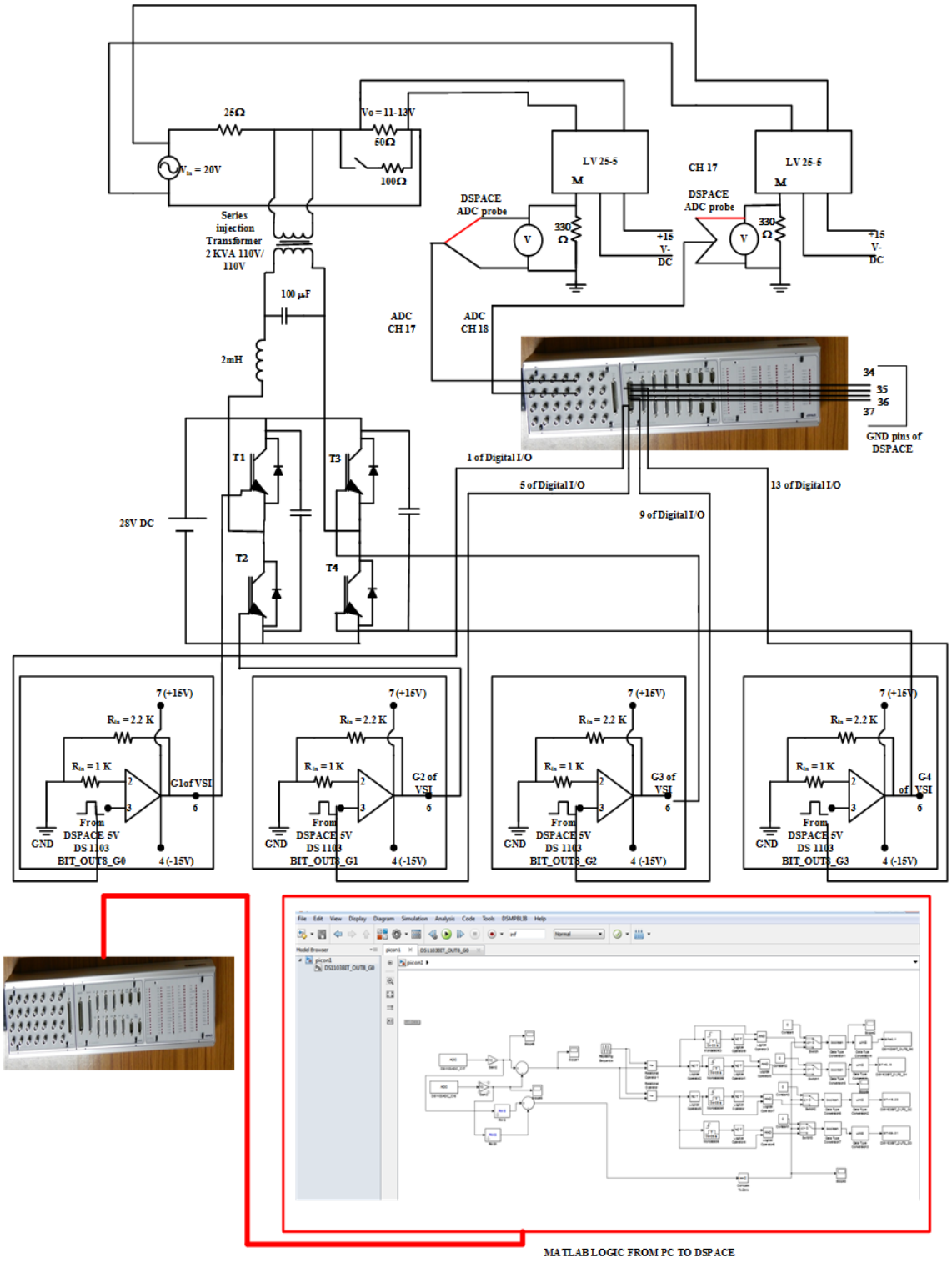


FIGURE 7.14: Prototype circuit of UPQC in MG

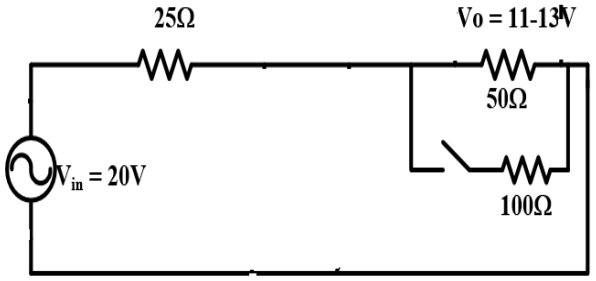


FIGURE 7.15: The basic electrical circuit of the scale down MG with load

a self supported VSC based UPQC, the VSC rating will be calculated as per the requirement of the load. The maximum sag 52% in the terminal voltage is obtained as $20 \times 0.5238 = 11$ V. Therefore the injected voltage V_C is estimated as

$$V_C = \sqrt{V_S^2 - V_L^2} = \sqrt{20^2 - 11^2} = 16.7V = 17V(approx.) \tag{7.1}$$

This voltage is to be injected into the system from UPQC.

Current rating of the VSC of UPQC:

The current rating of the UPQC depends on the load current to the downstream of a UPQC. For a load (25 Ω source resistance and a load of 50 Ω and further a load of 100 Ω), the current is calculated by applying KVL to the circuit shown in Figure 7.15, the current is obtained as 0.3428 A and the load is 6.856 VA (0.3428×20)

$$I_S = \frac{20}{25 + 33.33} = 0.3428A \tag{7.2}$$

where I_S is the current and V_S is the line voltage. Therefore, the current rating of the UPQC is $I_S = 0.3428$ A.

kVA rating of the VSC of UPQC:

The VA rating of the VSC of a UPQC is calculated as

$$S = V_S I_S/1000 = 11 \times 0.3428 = 3.7708VA. \tag{7.3}$$

Rating of injection transformer of UPQC:

The injection transformer is designed considering the optimum voltage level of the VSC. For this, the voltage of VSC is to be calculated. The voltage of VSC is considered as the difference between the actual and desired voltage. i.e 9 V (= 20-11 V) The primary side voltage of injection transformer will be 17 V and the secondary side voltage will be 9 V. The kVA rating of injection transformer can be calculated as

$$VA = V_C I_S/1000 = \times 17 \times 0.3428 = 5.8276VA. \tag{7.4}$$

Hence, the rating of injection trnasformer is 5.8276 VA i.e, 6 VA , n= 9 V/ 11 V.

DC capacitor voltage of VSC of UPQC:

$$V_{DC} > 2\sqrt{2}V_{VSC} \tag{7.5}$$

where the VSC voltage is 9 V The value of V_{DC} is obtained as 26 V and a V_{DC} of 30 V is selected for the UPQC.

DC bus capacitance of UPQC

The DC bus capacitance is selected based on the transient energy required during the change in the load. Considering energy stored in the DC bus capacitor for meeting the energy demand of the load for a fraction of power cycle, the relation can be expressed as

$$\frac{1}{2}C_d(V_{DC}^2 - V_{DC1}^2) = 3V_C I_S \Delta t \tag{7.6}$$

where V_{DC} is rated DC bus voltage, V_{DC1} is the drop in the DC bus voltage allowed during transients, and Δ t is the time for which support is required. considering Δ t = 200 μ sec, V_{DC} =30 V, V_{DC1} = 30 - 5% of 30 V= 28.5 V, the DC bus capacitance can be calculated as $\frac{1}{2}C_d(30^2 - 28.5^2) = 3 \times V_C I_S \Delta t$. It give C_D as 55.68 μF. Hence a DC bus capacitor of 100 μF, 30 V is selected.

Interfacing inductor for the VSC of UPQC

The interfacing inductor L_r is selected based on the current ripple in the current of the UPQC

($\Delta\ I_S$). Considering the ripple current in the inductor is 2%, modulation index m is 1, and overloading factor a =1.2, the inductor is calcuated as

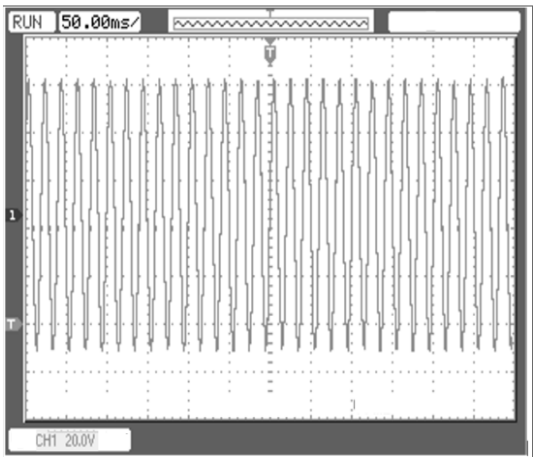
$$L_{r,interface} = \frac{\sqrt{3}nmV_{DC}}{2 * 6 * af_s * \Delta I_s} \tag{7.7}$$

Hence the interfacing inductor is estimated as 2 mH. Hence, an interfacing inductor of L_r of 2 mH and 1 A current carrying capacity is selected for the UPQC. Based on the above calculations, the UPQC is designed to mitigate the sag problem in MG in real time.

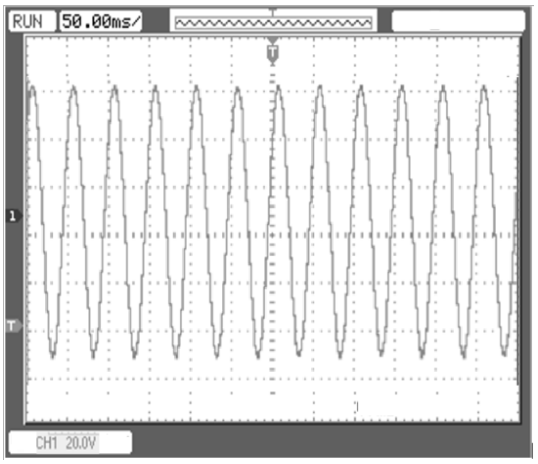
7.2 Results

A PV-WECS experimental has been established and PQ issues in terms of voltage due to supply and load changes are investigated. To mitigate the power quality issues of the MG, the need for a compensating has been identified. In this regard, UPQC is considered as a compensating device. The prototype of UPQC is developed in the laboratory based on the available facilities and analyzed for voltage sag mitigation in real time.

In this regard, the voltage is scaled down to a value of 20 V. The reference voltage (20 V) in actual form and expanded form from PV-WECS MG are shown in Figure 7.16(a) and Figure 7.16(b). The voltage is dropped to 13V due to load connected as shown in Figure 7.17(a) and



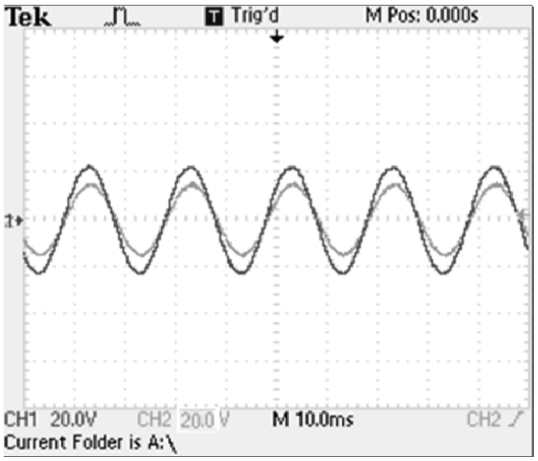
(a) source voltage



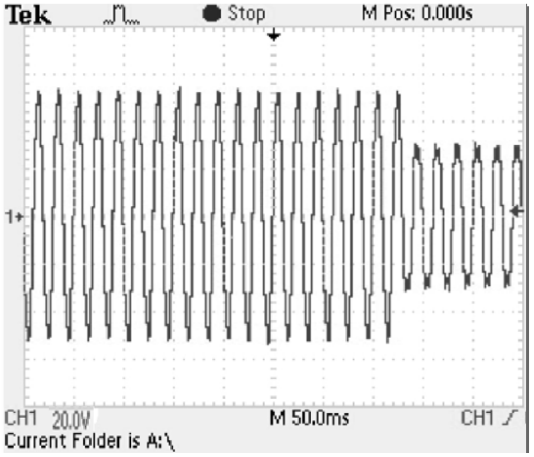
(b) Expanded source voltage

FIGURE 7.16: Source or reference voltage

further a sag of 9V (i.e load voltage =11V) is created using manual sag generator as shown in Figure 7.17(b). The expanded output during sag is shown in Figure 7.18(a). The UPQC using



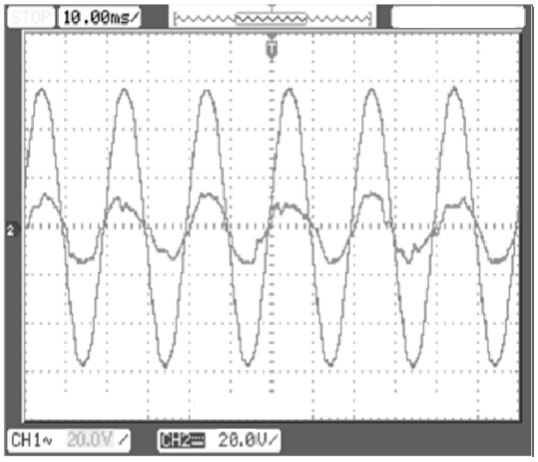
(a) Source and load voltage drop(only resistive load)



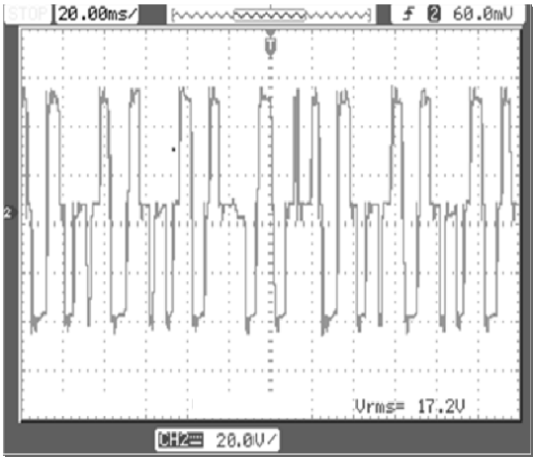
(b) sag

FIGURE 7.17: Drop and sag in the output voltage

the proposed logic generates the required voltage to be injected and the injection voltage is shown in the Figure 7.18(b) and thus the voltage will be compensated.



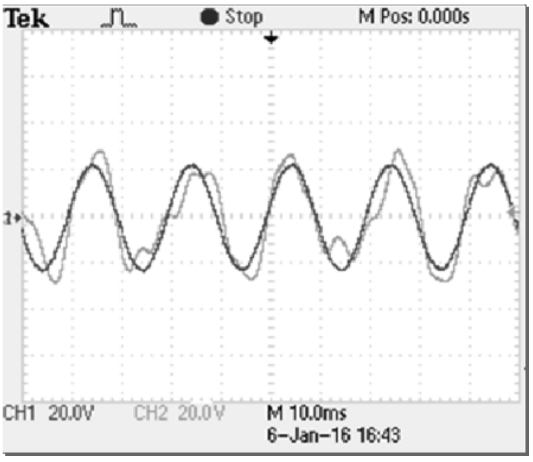
(a) source and load sag voltage



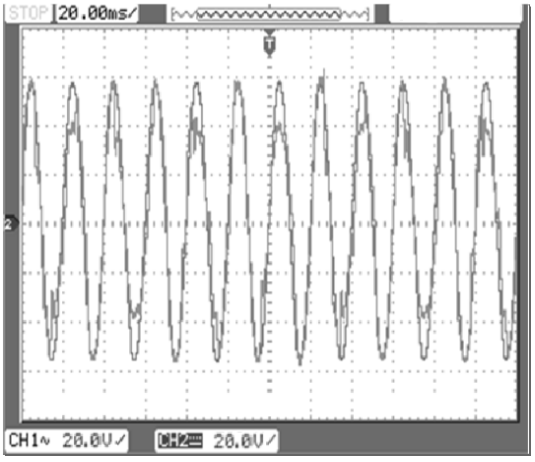
(b) inverterop voltage

FIGURE 7.18: sag voltage and inverter output voltage

However, the output voltage contains harmonics as shown in Figure 7.19(a). A low pass filter has been designed and used to suppress these harmonics and the resultant compensated output nearer to the reference (source) is shown in the Figure 7.19(b). Thus the performance of series



(a) source and compensated load without filter



(b) source and compensated load with filter

FIGURE 7.19: Compensated voltage without and with filter

APF in PV-WECS MG in providing voltage compensation is verified using both simulation and experimental set up.

7.3 Conclusion

This chapter discusses the real-time implementation of the custom power device specifically UPQC in mitigating the problem of voltage sags occurring in the microgrid. In this situation, a PV-WECS MG experimental setup is established with real-time data of environmental conditions. The MG is developed using PV-WECS emulator which is a scale down experiment setup. A prototype of UPQC is modeled, designed and connected to the MG setup to mitigate the aforementioned power quality problem i.e sag. From the experimental study, the effective performance of the UPQC is validated in real time to maintain the output voltage constant irrespective of environmental and load conditions.