Chapter 4

PQ Compensation using Dynamic Voltage Restorer

Introduction

Microgrids utilize freely available renewable energy sources (RES) to generate power and are installed at consumer's sites, i.e, the distribution end. Power quality issues have been observed in these MGs. Some of them are voltage swells and sags, and low power factor requiring reactive power compensation which would be possible with a compensating device. This chapter presents the utilization of the custom power device specifically Dynamic Voltage Restorer (DVR) in mitigating the problem of voltage sags and swells occurring in MG. The DVR in addition to voltage magnitude compensation provides harmonic mitigation. This is achieved by further enhancing the DVR as a series active filter with proposed control technique. A novel control technique based on IVTG approach is proposed to improve its performance in providing harmonic compensation and compared with control techniques like PI, SRF theory with varying load conditions in the MG.

4.1 DVR in MG Distribution Systems

The power distribution systems suffer from many power quality issues that are based on voltage quality. In this thesis, the main voltage quality issues considered are sags, swells, and harmonics. The DVRs provide compensation to these voltage based issues. They inject voltage in series into the system. This can be achieved generally by using insulated gate bipolar transistor based PWM (pulse width modulated) voltage source converters (VSCs) which are the main building block of DVR. The voltage will be injected by VSC against to this voltage by using DVR with an equal amount of magnitude. However, this is varying and comprises the three sequence components and in addition to harmonic components. Similarly, the nonlinear loads connected to the MG also draw harmonics and reactive power components of current in addition to fundamental power component of the current from the AC mains. Such voltage fed non-linear converter loads, in turn, draw peaky and of this type of voltage-fed nonlinear loads (such as diode rectifier with a large DC bus capacitor filter), requiring a DC voltage source with the DC capacitor, has increased nowadays in many applications. Hence the mitigation of voltage for sag, swell in terms of magnitude is just not sufficient but the compensation against to the system harmonics is also required. Consequently, an active power filtering scheme is introduced, operating in this direction thus protecting the mains (MG) and the other equipment (load). The series APF is used to filter and mitigate harmonics. The APF feature is spreading widely due to its fast acting power electronic elements. The actual series compensator, DVR is recently reported as a series APF by adapting active power filtering feature. It is used as active power filter to eliminate harmonics due to nonlinear loads fed by voltage, to provide voltage compensation and became a custom power device (CPD) [145]. Hence, the device DVR with active power filter modified as series APF is considered in this chapter to provide power quality compensation for voltage disturbances. Accordingly, the analysis, design, and control of the DVR and its additional active filtering feature (i.e Series. APF) for voltage quality improvement are presented.

4.1.1 State of the Art on DVR and Series APF

The phenomenon of sags and swell in detail are discussed in 1.1.1. These are also caused due to the output variations from the RES generation, i.e the supply side disturbances to the loads. These common disturbances in the MG can be due to (i) disturbances arising due to environmental changes (ii) nature of loads and (iii) fuse or breaker operation. The voltage disturbances are also caused by symmetrical and non-symmetrical faults. The performance of the sensitive equipment in industries, hospitals, business centers is adversely affected by the disturbances in the source voltages. In such case, voltage sags for a short duration of few cycles may cause a great damage to the sensitive equipment. The voltage fluctuations are additionally caused by loads. The nonlinear nature of the loads and AC loads demanding reactive power at the time of starting are few scenarios which cause harmonics. The series compensator DVR is proposed to mitigate these voltage disturbances. The primary application of DVR in the distribution system is to compensate for sags and swells in the voltages in terms of its magnitude. The first DVR entered commercial service on the Duke Power System in the U.S.A. in August 1996 [146] to compensate 50 % voltage sag for a period of 0.5 seconds. However, DVR has been studied extensively in mitigating disturbances such as voltage sags, swells, unbalance and harmonics in the conventional power system [147] but not for voltage compensation in the MG. Though its usage has been investigated in the fault ride through, in a wind generation source connected to the grid on the occurrence of a fault in the grid [148]. A series compensator was designed to provide fault protection in microgrid in [149, 150] and to improve power quality in microgrid a DVR with its DC link charged with photovoltaic (PV) generation/battery units were proposed in [151] but harmonics mitigation was neglected

In order to enhance the DVR to compensate all voltage problems, it is necessary to add additional features requiring the modeling of DVR. The following section describes the building blocks of DVR.

4.2 Dynamic Voltage Restorer

The four major components of DVR are: 1. VSC with the control unit, 2. Injection transformer, 3. Filter, and 4. Energy storage. The block diagram of DVR is represented in Figure 4.1.

1. Voltage source converter (VSC):

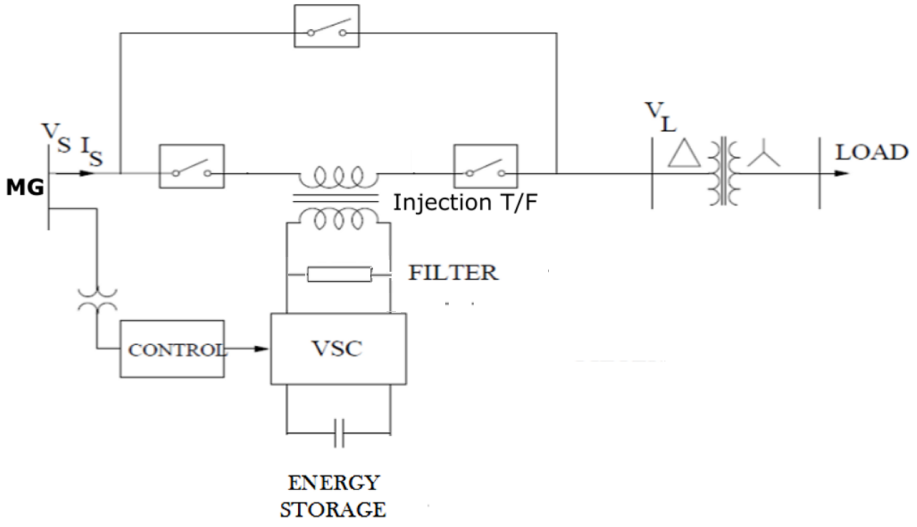


FIGURE 4.1: Block diagram of DVR

A VSC is used to convert DC-AC using the group of IGBT/MOSFET switches (2,4,6,12 etc). The required output AC voltage is injected to compensate the voltage sag in the transmission line. The DC input voltage is obtained from an energy storage which would be a battery or output of the controlled rectifier.

• Control unit:

A control unit is designed to find the difference between the reference load voltage and actual load voltage (in the case of sag and swell condition) utilizing which it modulates the Pulse Width Modulation (PWM) signals to control the switches to generate the required injection voltage. Thus the VSI generates a required three phase 50 Hz sinusoidal voltages and injects into the system.

2. Injection transformer:

The injection transformer is a two winding transformer and is used to inject the required voltage generated from VSC for sag/swell mitigation in series with the line. The injection transformer can be a 3-phase transformer or 3, 1-phase transformers connected together. The selection is

based on the requirement of zero sequence currents compensation. The injection transformer also helps in isolating the line from the DVR system.

3. Filters: The filters are used to remove the harmonics during voltage injection. The location of the filter can be online side or inverter side of the injections transformers. The inverter side filters are of a lower rating compared to line side filter but the inductance used for filtering drops the injected voltage. The line side filters require a high rating, however, do not cause any voltage drop or phase deviation in the injected voltage.

4. Energy Storage: The purpose of the energy source is to supply the necessary energy to the VSI which will be converted to alternating quantity and fed to the injection transformer. Batteries are most commonly used and the capacity of the battery determines the duration of the sag which can be compensated by the DVR. An auxiliary bridge converter can also provide the required DC supply to the DVR [152]. DVR, based on photovoltaic (PV) generation/battery units acting as DC source is proposed in [151]. However, the necessary active power can also be supplied using a self-controlled DC link acting as an energy storage [153, 154]. The DVR constituted with the components, is generally operated in two modes. The two modes are:

1. Standby (also termed as short circuit operation (SCO)) mode where the voltage injected has zero magnitude.

2. Boost mode (when the DVR injects a required voltage of appropriate magnitude and phase to restore the pre-fault load bus voltage).

4.3 Voltage Compensation Methods

A specified control is required for proper operation of DVR system. DVR detects the presence of voltage sags/ swells and operates to mitigate the voltage dip/rise. The control technique is applied to generate Pulse Width Modulation (PWM) control signals to IGBTs switches to develop the required voltage to be injected. The generation of PWM signals, in turn, is based on the control logic applied for inverter switching. Thus the VSI generates a required three phase 50

Hz sinusoidal voltages and injects into the system [146]. Compensation is provided by using 3 control strategies as given below:

4.3.1 Pre-Sag Compensation

The reference or supply voltage, load voltage are measured and compared. The compensation is provided such that the resultant voltage is equal to the pre-sag voltage. This produces undisturbed load voltage. However, a higher rating VSC is required. Prior to sag, $V_S = V_L = V_0$. Due to sag, the voltage is dropped in magnitude to V_{S1} which further shifts the supply phase angle as shown in Figure 4.2. The VSC injects a voltage V_{C1} in magnitude and phase such that the load voltage ($V_L = V_{S1} + V_{C1}$) remains at V_0 (both in magnitude and phase). It is claimed that some loads are sensitive to phase jumps and it is necessary to compensate for both the phase jumps and the voltage sags.

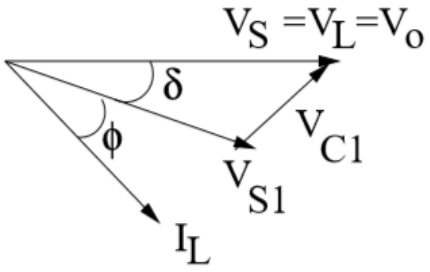


FIGURE 4.2: Pre-sag compensation

4.3.2 In-Phase Compensation

In this strategy, supply voltage and DVR injected voltage are in phase without considering load current and is given by V_{C2} as shown in Figure 4.3. The injected voltage is minimum in magnitude in this case but results in a phase shift of load voltage. This can be applied to loads insensitive to phase jumps. However, the DVR requires power rating in this method.

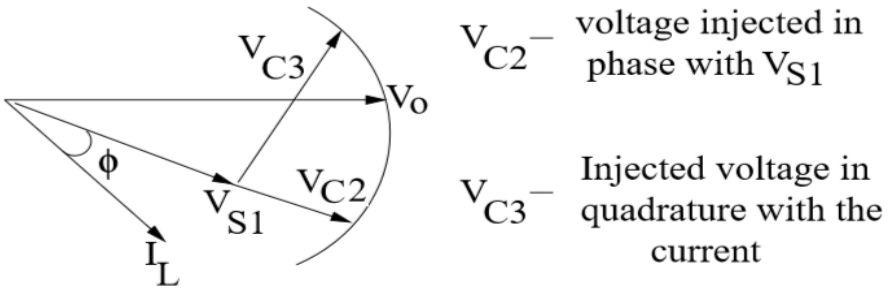


FIGURE 4.3: Phasor diagram showing in-phase, minimum energy compensation

4.3.3 Minimum Energy Compensation

There is no power requirement for the DVR, if DVR injects the voltage (V_{C3}) in quadrature with load current assuming there are no losses. The DVR voltage acts in capacitive mode and ensure that V_L leads V_{S1} as shown in Figure 4.3. Based on voltage of the load and p.f, the load current will be defined. This compensation measures the load current in addition to supply and load voltages. The compensated voltage V_{C3} is in quadrature with the load current which also injects the reactive power into the system. However, minimum supply voltage is to be maintained for full compensation [155, 156]. The DVR provides compensation to the voltage problems in terms of magnitude only. However, the harmonics are also observed with varying loads at the load side. The filter in the DVR only removes injected harmonics caused by inverter action. Consequently, to enhance its performance especially when nonlinear loads are connected, the DVR is modified as series APF [157, 158] by adapting active power filtering feature to mitigate harmonics along with magnitude compensation. This is implemented in the control unit of DVR.

4.4 Control Strategies for Active Filtering

The series power compensator DVR is designed with APF technique to provide harmonic compensation in addition to RPC. The equivalent circuit employed with series compensation is shown in Figure. 4.4. A harmonic current and voltage of I_{Lh} and V_{Lh} start flowing due to nonlinear load. The harmonic impedance is Z_{Fh}. From the supply side, the Thevenin (harmonic) voltage, current, and impedance are given by V_{Th}, I_{Sh} and Z_{Th}. As a result, the harmonic voltage

injected in series is V_{Ch}. To mitigate this voltage an equal and opposite voltage to be injected by the series APF which is represented by using V_{Sh}. The filtering feature can be implemented in

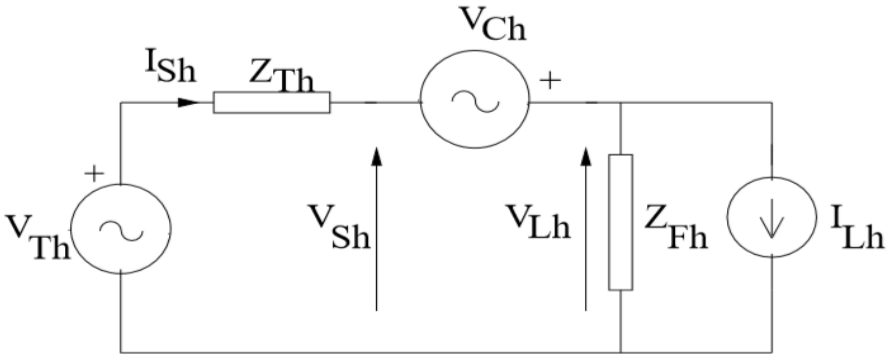
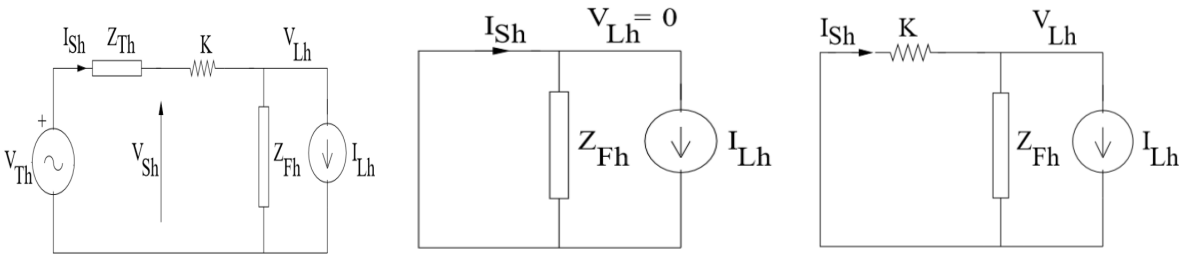


FIGURE 4.4: Harmonic equivalent circuit for series active filtering

three ways for the series active filter as shown in Figure. 4.5 are : [146],



(a) Current detecting method (b) Voltage detecting method (c) Combined method

FIGURE 4.5: Equivalent circuits for three differrent filtering approaches

1. **Current detection method**.
2. **Voltage detection method.**
3. **Combined method.**

The equivalent circuits for the three differrent filtering approaches are shown in Figure. 4.5. The harmonic load voltage and the harmonic source current (V_{Lh}) (I_{Sh}) are deduced as:

1. **Current detection method** The compensation voltage V_{Ch} control is given by

$$V_{Ch} = -K\, I_{Sh} \tag{4.1}$$

$$V_{Lh} = \frac{Z_{Fh}}{Z_{Th} + Z_{Fh} + K} V_{Th} - \frac{(Z_{Th} + K) Z_{Fh}}{Z_{Th} + Z_{Fh} + K} I_{Lh} \tag{4.2}$$

$$I_{Sh} = \frac{1}{Z_{Th} + Z_{Fh} + K} V_{Th} - \frac{Z_{Fh}}{Z_{Th} + Z_{Fh} + K} I_{Lh} \tag{4.3}$$

K represents gain of the proportional controller and h is for harmonic order.

2. **Voltage detection method** Here V_{Ch} is controlled as

$$V_{Ch} = -V_{Sh} \tag{4.4}$$

$$V_{Lh} = 0 \tag{4.5}$$

$$I_{Sh} = I_{Lh} \tag{4.6}$$

The voltage detection method compensates for voltages (load), however, the source current harmonics remain uncompensated.

3. **Combined method** Here V_{Ch} is obtained as

$$V_{Ch} = -K I_{Sh} - V_{Sh} \tag{4.7}$$

$$V_{Lh} = -\frac{K Z_{Fh}}{Z_{Fh} + K} I_{Lh} \tag{4.8}$$

$$I_{Sh} = \frac{Z_{Fh}}{Z_{Fh} + K} I_{Lh} \tag{4.9}$$

The combined method eliminates the disadvantages of the first two methods. Not only the source voltage disturbances have no effect on the load bus voltage, the source current harmonics are eliminated if $K \gg |Z_{Fh}|$. This is easy to arrange for harmonic frequencies of 5 f_0 and above, where f_0 is the fundamental (supply) frequency.

4.5 Classification of Series Active Power Filters

Series APFs can be classified based on the type of converter used, topology and the number of phases. Based on converter used, the series APFs are claissfied as current source and voltage source (CSC and VSC) APFs. CSC-series APF is reliable but lossy and power capacitors with high raing are required. Due to this, can not be applied in case of multilevel mode. Whereas VSC based APF has a self-supporting DC voltage bus. It is preeferred due to its light weight, cheap, and can be extended to multilevel. Based on topology the two types are : Half-bridge and Full bridge VSC based series APFs. Similalry, based on number of phases the series APF systems are: 1-phase 2-wire, 3-phase 3-wire, and 3-phase 4-wire.

4.6 Control and Design of Series Active Filters

The series APFs are used provide compensation for voltage quality issues including harmonics in the MG. In turn the APFs are driven by using self supporting DC bus or battery energy storage system (BESS). They are used to inject required voltages in series between the source(DGs) and load for voltage magnitude compensation or for obtaining balanced sinusoidal voltages across the load. These objectives are selected either individually or in combination to maintain stable voltage profile in the MG. The control algorithms considered are:

- **PI control**
- **Synchronous reference frame (SRF) theory, also known as a d-q theory.**
- **Identity vector template generation (IVTG) technique.**

4.6.1 PI Control

The PI control is used to generate the difference between the actual and reference voltage, and whose output is utilized to generate corresponding PWM signals to be given to the VSC to obtain

the required injected voltage. This control is simple and does not involve complex control circuit. PI control is an integral error compensation scheme, the output response depends in upon the integral of the actuating signal. This type of compensation is introduced by a using a controller which produces an output signal consisting of two terms, one proportional to the actuating signal and the other proportional to its integral. Such a controller is called proportional plus integral controller or PI controller. Figure 4.6 is the block diagram of the PI control used in DVR-MG setup. The algorithm of PI control is shown in Figure 4.7. K_p and K_i values of proposed PI

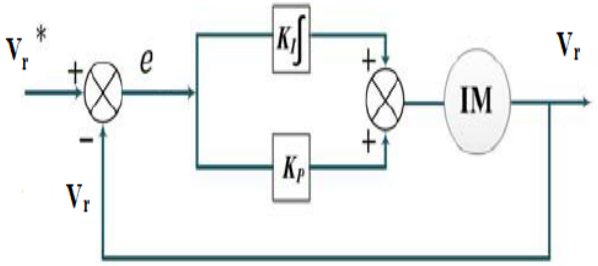


FIGURE 4.6: PI control of DVR

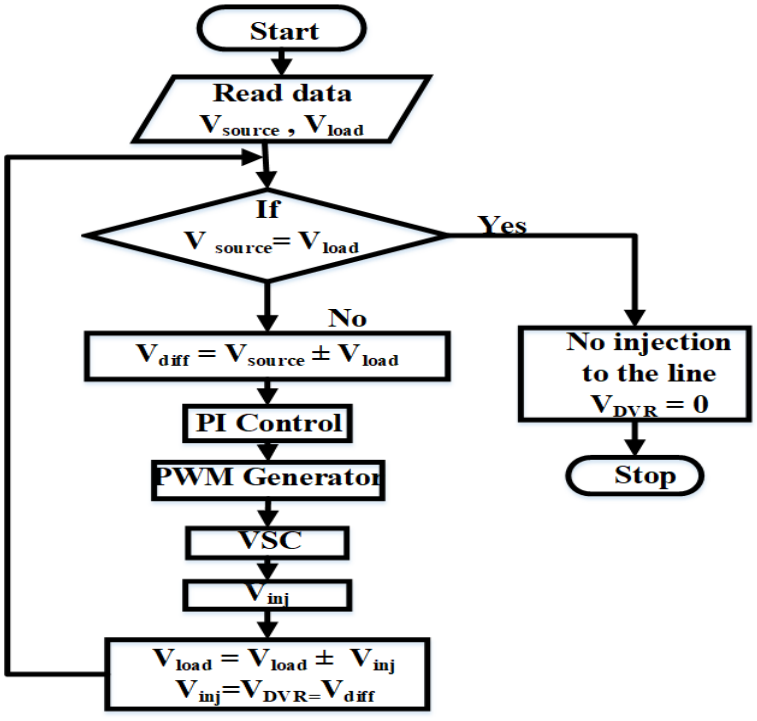


FIGURE 4.7: Flowchart for PI control of DVR

controller considered in continuous time mode are 0.5 and 10 respectively.

$$v_r(t) = K_p\, e(t) + K_i \int e(t) \tag{4.10}$$

where

$$e(t) = v_r^*(t) - v_r(t) \tag{4.11}$$

At present, the PI controller is most widely adopted in industrial application due to its simple structure, easy to design and low cost. Despite these advantages, the PI controller fails, when the controlled object is highly nonlinear and uncertain. PI controller cannot eliminate harmonics resulted from non-linear loads. It is mainly applicable where the voltage compensation is to be provided mainly in terms of magnitude. Moreover, changing the gains of proportional and integral modes has a negative effect on the speed of the response and overall stability of the system. Thus, PI controller is not relied on to provide the complete compensation for voltage disturbances in the MG.

4.6.2 SRF Theory

The voltage compensation is achieved by injecting/absorbing P or Q, or both P and Q. In minimum energy compensation mode, the compensating voltage is in quadrature with the load voltage and injects reactive power into the system thus provides compensation. However, it requires minimum value of the voltage. For in-phase compensation, the DVR needs power (both P and Q) which is to be provided by external DC source such as a battery on its DC side. However, if the external source is replaced by a self-supported DC bus, the performance of the DVR during in-phase compensation becomes effective. The SRF theory can be operated in both ways, i.e., with battery and self-supported DC bus. The control is mainly used to energize the DC bus based on the working condition (normal/sag-swell). SRF theory based control considers all these conditions and provide compensation in this mode. Initially, the control technique is discussed for battery energy storage system (BESS) support and the subsequent section discusses the control for self-supporting DC bus.

4.6.2.1 Control of DVR with BESS

The control algorithm of the series APF using SRF theory for reference signals estimation is shown in Figure 4.8. The voltages at PCC, MG supply (v_{Sa}, v_{Sb}, v_{Sc}) and the terminal voltages (v_{La}, v_{Lb}, v_{Lc}) are sensed. The measured of components $(v_S, v_L$ are first transferred into two-phase stationary co-ordinates using $\alpha - \beta$ transformation. After that, the stationary frame quantities are transferred into the synchronous rotating frame using cos and sin functions from the PLL. The sin and cos functions help to maintain the synchronization with supply system. From the desired load vectors reference voltage signals $(v^*_{La}, v^*_{Lb}, v^*_{Lc})$ are extracted. The computed error between the generated reference signals and actual signals is fed to PI controller to drive the IGBT signals. Using inverse transformation, the signals from PI controller are again converted into abc frame and generates the required PWM signals to drive the IGBT switches of VSC. The

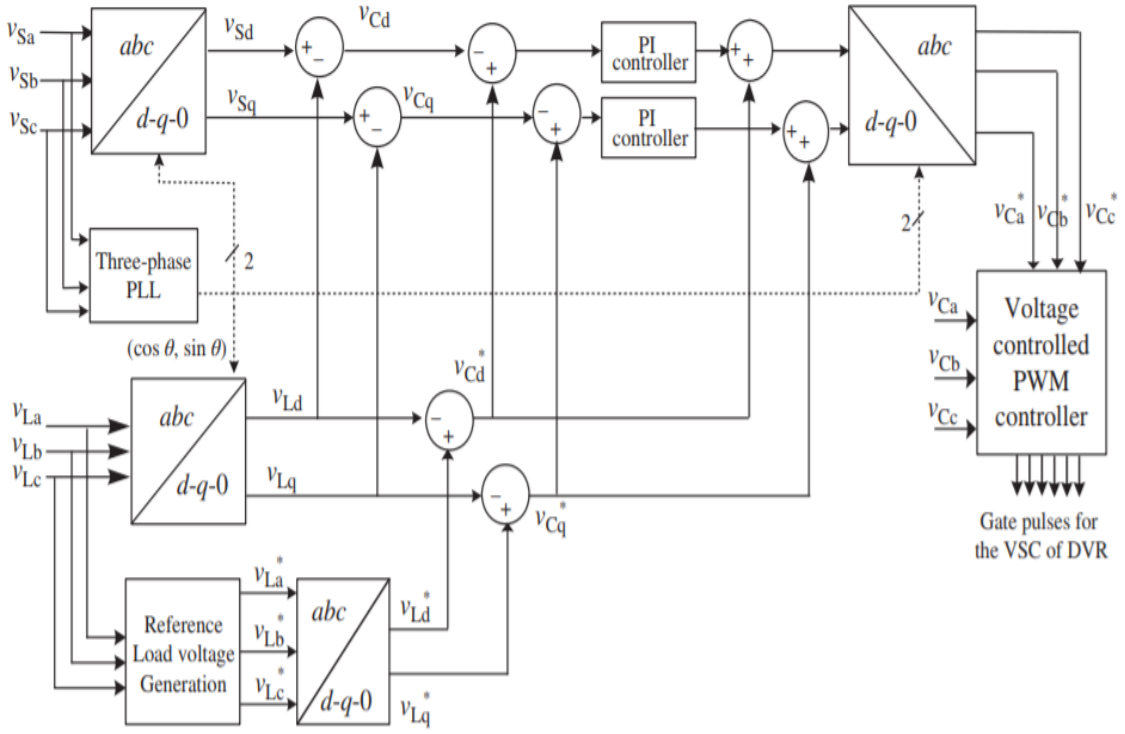


FIGURE 4.8: SRF theory based method for control of BESS supported DVR [1]

flowchart of SRF theory control is given in Figure 4.9

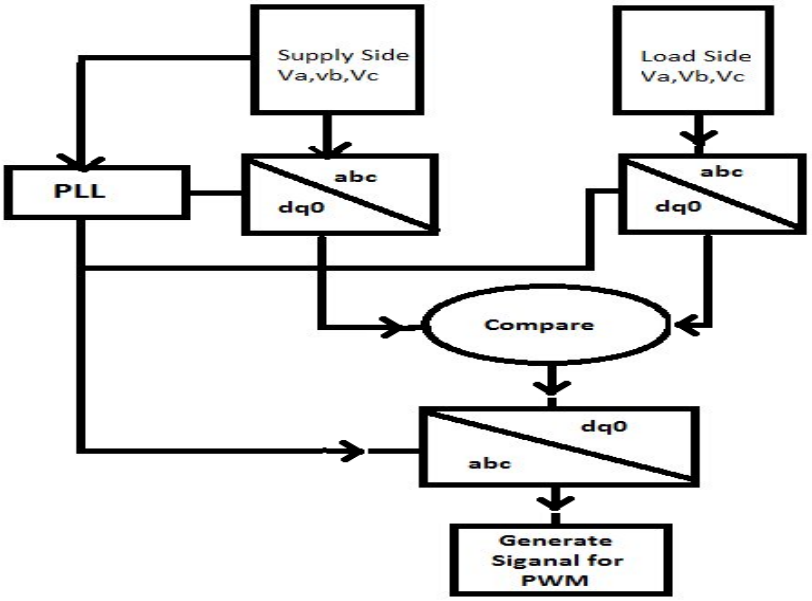


FIGURE 4.9: Flow chart of SRF theory based method for control of BESS supported DVR

The load voltage v_L at PCC is given by

$$V_L = \left(\frac{2}{3}\right)^{1/2} (v_{La}^2 + v_{Lb}^2 + v_{Lc}^2)^{1/2} \tag{4.12}$$

and the identity vectors are obtained as

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \frac{1}{V_L} \begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix} \tag{4.13}$$

The resultant estimated reference load voltages are

$$\begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix} = V_L^* \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{4.14}$$

Using PLL, PARK's transformation,

$$\begin{bmatrix} v_{Ld} \\ v_{Lq} \\ v_{L0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\,\theta & -sin\,\theta & \frac{1}{2} \\ cos(\theta - \frac{2\pi}{3}) & -sin(\theta - \frac{2\pi}{3}) & \frac{1}{2} \\ cos(\theta + \frac{2\pi}{3}) & sin(\theta + \frac{2\pi}{3}) & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix} \tag{4.15}$$

The reference load voltages $(v^*_{La}, v^*_{Lb}, v^*_{Lc})$ and the voltages at PCC (v_S) are also estimated using SRF theory. The resultant DVR voltages (dq) are

$$v_{Cd} = v_{Sd} - v_{Ld} \tag{4.16}$$

$$v_{Cq} = v_{Sq} - v_{Lq} \tag{4.17}$$

The dq frame voltages from DVR are calculated as

$$v^*_{Cd} = v_{Ld}* - v_{Ld} \tag{4.18}$$

$$v_{Cq} = v^*_{Lq} - v_{Lq} \tag{4.19}$$

PI controllers are used to regualte the difference between the actual DVR voltages and reference voltage. Later reverse Park's transformation is used to convert again to abc frame from Eq. (4.19) and considering v^*_{Co} as zero:

$$\begin{bmatrix} v^*_{Ca} \\ v^*_{Cb} \\ v^*_{Cc} \end{bmatrix} = \begin{bmatrix} cos\,\theta & -sin\,\theta & 1 \\ cos(\theta - \frac{2\pi}{3}) & -sin(\theta - \frac{2\pi}{3}) & 1 \\ cos(\theta + \frac{2\pi}{3}) & sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} v^*_{Cd} \\ v^*_{Cq} \\ v^*_{Co} \end{bmatrix} \tag{4.20}$$

The reference DVR voltages $(v^*_{Ca}, v^*_{Cb}, v^*_{Cc})$ and the sensed DVR voltages (v_{Ca}, v_{Cb}, v_{Cc}) are fed to gate circuit of the VSC of DVRs.

4.6.2.2 Control of Self Supported DVRs

The SRF theory control implemented with self supported DC bus is hown in Figure 4.10. The compensation strategy is similar to that of battery supported DVR in addition to harmonic compensation using LPF. The components of voltages in d- and q- axes are

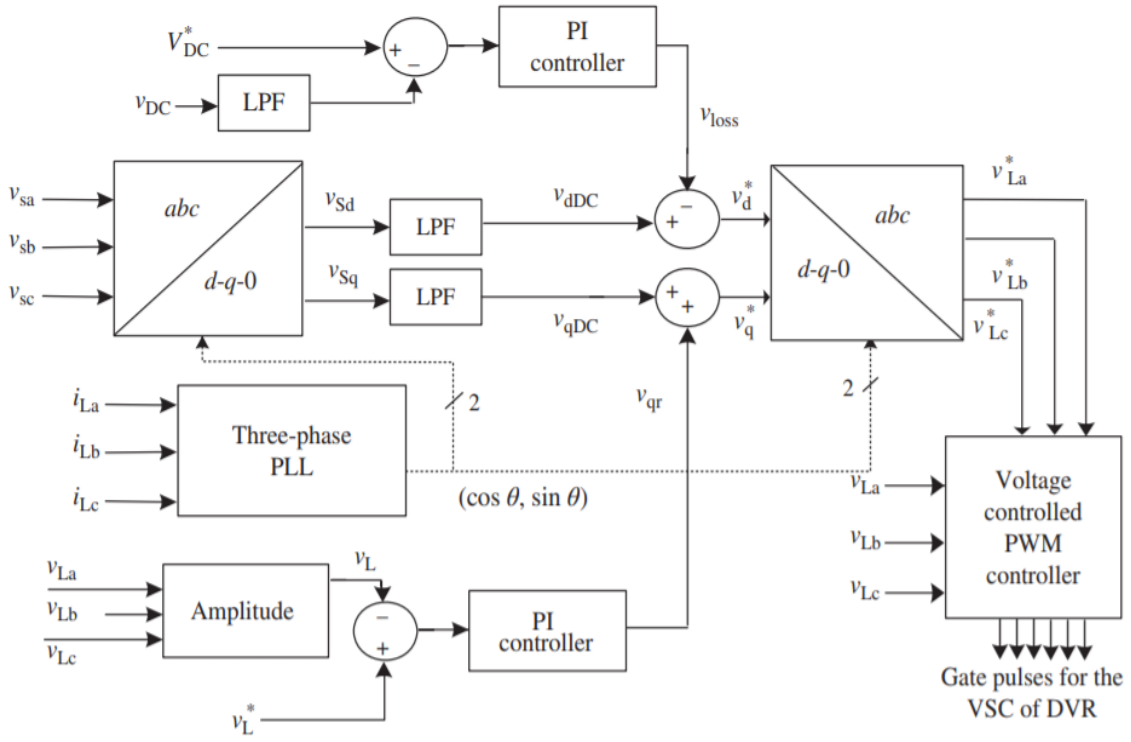


FIGURE 4.10: SRF theory based method for control of self-supported DVR [2]

$$v_{Sd} = v_{dDC} - v_{dAC} \tag{4.21}$$

$$v_{Sq} = v_{qDC} - v_{qAC} \tag{4.22}$$

The control of DC bus employed with self support is acheived by using PI controller and measures the voltage loss (v_{loss}) which is to be compensated as:

$$v_{loss(n)} = v_{loss(n-1)} + K_{p1}\,(v_{de(n)} - v_{de(n-1)} + K_{i1}\,v_{de(n)} \tag{4.23}$$

where $v_{de(n)} = v^*_{DC} - v_{DC(n)}$, sensed DC voltage is ($v_{DC}$) and the reference DC voltage is (v^*_{DC}), $v_{de(n)}$ is the error between them for the nth sampling instant. K_{p1} and K_{i1} are DC bus control

proportional and the integral gains.

w.r.to d-axis, the reference is

$$v_d^* = v_{dDC} - v_{loss} \tag{4.24}$$

The control load voltagr v_L to its reference v_L^* is obtained by using another PI controller. However, the output of this controller represents the reactive component of voltage (v_{qr}) and is considered to regulate v_L. Initially, the amplitude of v_L at PCC is deduced from the actual voltages (v_{La}, v_{Lb}, v_{Lc}) as in Eq.(4.12). Using PI controller, the regulated voltage to its reference is given by,

$$v_{qr(n)} = v_{qr(n-1)} + K_{p2}\left(v_{te(n)} - v_{te(n-1)}\right) + K_{i2}\, v_{te(n)} \tag{4.25}$$

The reference load voltage is (v_L^*), actual load voltage is ($v_{L(n)}$) and $v_{te(n)} = v_L^* - v_{L(n)}$ is the error for nth instant. K_{p2} and K_{i2} are the DC bus proportional and the integral gains.

w.r.to q-axis, the reference is

$$v_q^* = v_{qDC} - v_{qr} \tag{4.26}$$

The reference load voltages ($v_{La}^*, v_{Lb}^*, v_{Lc}^*$) in abc frame are obtained from the reverse Park's transformation as in (4.20) . The errors between the sensed load voltages (v_{La}, v_{Lb}, v_{Lc}) and reference load voltages are used in the PWM controller to generate gate pulses for the VSC of the DVR. This type of control is used in series APF. The flowchart of SRF theory control is given in Figure 4.11.

Thus, the SRF theory transforms components at PCC in the synchronous frame and consists of a PLL circuit which senses phase and frequency. Thus, the circuit is complex and is slow in transient response as the delay depends on PLL and the filter [159] only. Application of this control theory for series SPF is limited while handling nonlinear loads that require fast corrective actions. Subsequently, new technique Identity vector template generation (IVTG) is proposed.

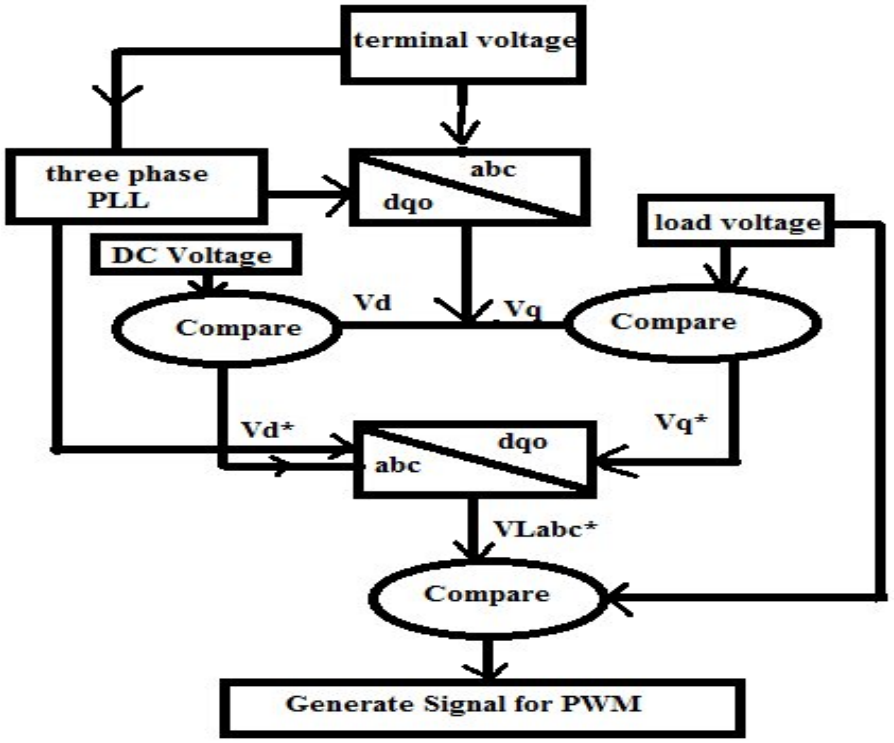


FIGURE 4.11: Flow chart of SRF theory with self supported DC link control of DVR

4.6.3 IVTG Technique

The effectiveness of the compensation depends on its controller's ability to calculate the reference signals for the series inverter with a minimum error and time delay to compensate for the current and voltage distortion, voltage variation, or any other undesirable condition. The major function of series APF is to strictly maintain the voltage at load bus sinusoidal and at the rated value (magnitude). Therefore, the simplest approach to generate reference signals for series inverter would be directly imposing the load bus voltage to be perfect sinusoidal. On a particular distribution system the standard magnitude of voltage being supplied is fixed. For example, high power rated industrial loads are supplied with three-phase 11kV/440V AC, 50Hz voltages and a typical household consumer is supplied by single-phase 220VAC, 50Hz voltage. Therefore two important factors to maintain the precise regulation at load bus, especially for sensitive loads to be protected are i) perfect sinusoidal voltage at 50Hz and ii) fixed load voltage magnitude. The supply voltages can be distorted, may show some dips or rise in voltage due to switching of high rated load connected to the same feeder, or may get unbalanced due to severe unbalanced load

on the network, etc. Under such undesirable conditions, if we could force the load voltages to be perfectly sinusoidal and at fixed load voltage magnitude, the unwanted events/ problem can be solved easily. Assuming that the terminal voltages at point of common coupling (PCC) are distorted, they can be decomposed as sum of fundamental and harmonics components. Hence a simple new approach is explained to extract the reference voltage and current signals for voltage source inverters. In this situation, a novel control methodology for series APF is proposed i.e., the IVTG technique given in Figure 4.12, in which fundamental identity vector templates are generated to eliminate the harmonic content in the MG voltages at PCC. The source voltage or

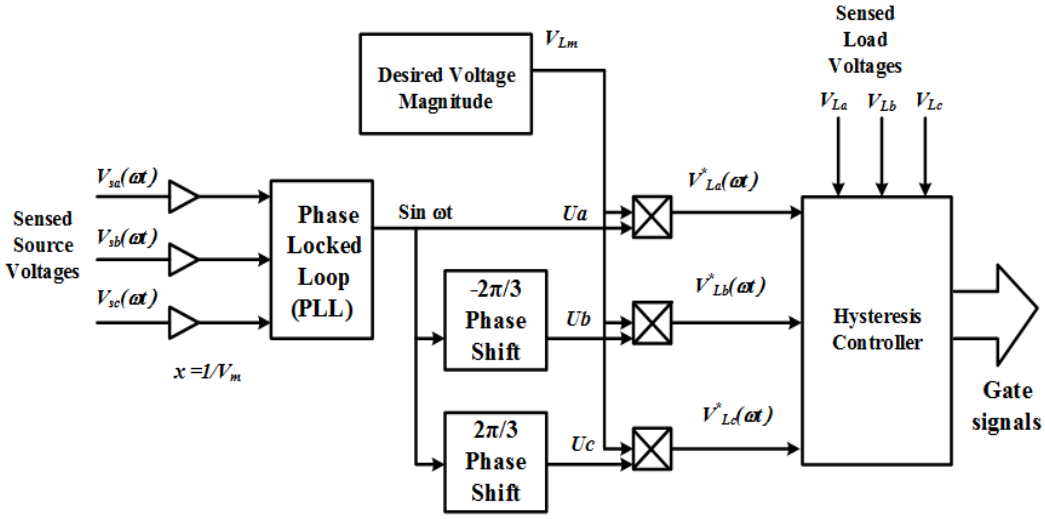


FIGURE 4.12: IVTG control

MG reference voltage for phase 'a' V_s can be expressed as

$$V_{Sa}(\omega t) = V_{Sa,1} + V_{Sa,2} + V_{Sa,0} + V_{Sa,h} \tag{4.27}$$

where $V_{Sa,1}, V_{Sa,2}, V_{Sa,0}, V_{Sa,h}$ are fundamental positive, negative, zero sequence and harmonic components of phase 'a' voltage. The harmonic component of phase a can be expressed as

$$V_{Sa,h} = \sum_{n=2}^{\infty} V_{Sa,n} \sin(n\omega t + \theta_{na}) \tag{4.28}$$

Similarly, for other two phases, the voltages can be expressed as

$$V_{Sb}(\omega t) = V_{Sb,1} + V_{Sb,2} + V_{Sb,0} + V_{Sb,h} \tag{4.29}$$

$$V_{Sc}(\omega t) = V_{Sc,1} + V_{Sc,2} + V_{Sc,0} + V_{Sc,h} \tag{4.30}$$

In MG, the voltages at PCC i.e, both source and load voltages are required to be sinusoidal. Except the positive sequence components, the other components like negative, zero and harmonic content should be nullified. To achieve this, identity amplitude sinusoidal voltages at PCC are generated from sensed voltages representing A, B and C phase voltages respectively and compared with desired voltage magnitude. The voltage vectors generated by using this approach are termed as identity vector templates and are specified by the following equations:

$$U_a = \sin(\omega t) \tag{4.31}$$

$$U_b = \sin(\omega t - 120^\circ) \tag{4.32}$$

$$U_c = \sin(\omega t + 120^\circ) \tag{4.33}$$

Let V_{Lm} represents the peak value of the load voltage. Now, the above set of equations is multiplied by the constant term V_{Lm} to yield the required load voltages. These are given by,

$$V^*_{La}(\omega t) = V_{Lm}.U_a = V_{Lm}\sin(\omega t) \tag{4.34}$$

$$V^*_{Lb}(\omega t) = V_{Lm}.U_b = V_{Lm}\sin(\omega t - 120^\circ) \tag{4.35}$$

$$V^*_{Lc}(\omega t) = V_{Lm}.U_c = V_{Lm}\sin(\omega t + 120^\circ) \tag{4.36}$$

The flowchart of IVTG control is given in Figure 4.13 A hysteresis controller generates the firing pulses for the VSI acting as Series APF by comparing these reference load voltages with the actual load voltages. If the load voltages follow their reference values, then, the aforementioned voltage quality issues will be eliminated. The schematic diagram of series APF employed with hysteresis control of a series APF is shown in the Figure 4.14. The Figure 4.14 represents the MG connected to a nonlinear load and is provided compensation by using series APF using IVTG control. The PWM signals generated from Hysteresis controller driven by IVTG technique are further fed to VSC circuit of series APF to produce the required voltage to be injected.

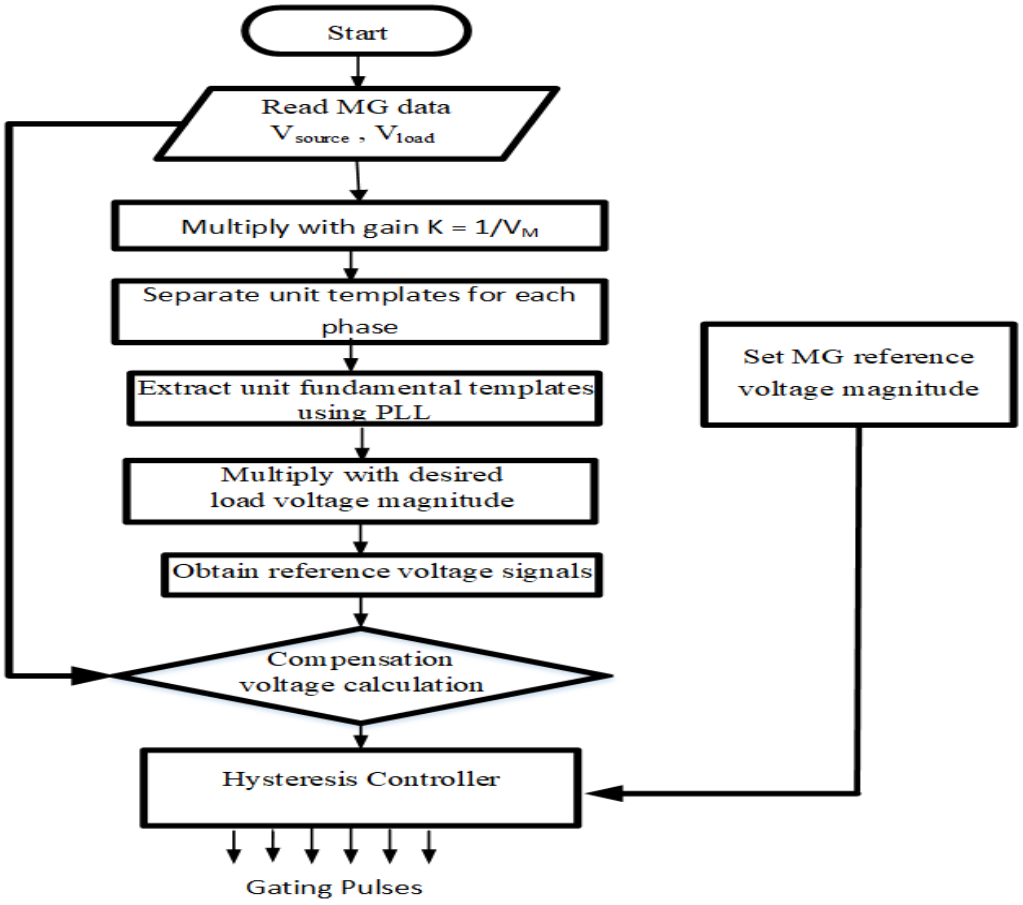


FIGURE 4.13: Flow chart of proposed IVTG control for DVR

The overall design of DVR is mainly based on sag/ swell percentage, duration, a rating of the load etc. The active filtering using series APF (enhanced DVR) is explained mathematically in the next section.

4.6.4 Analysis and Design of Series APF

The ratings that are required to be calculated in the design of series APF are: voltage, current and VA rating of the VSC, injection transformer, DC bus voltage, DC bus capacitance, AC interfacing inductance, and ripple factor. The design of series APF is for the MG connected to the load as shown in Figure 4.14 when operated in islanded mode. However if the MG is with the different rating or the MG is in grid interconnected mode and delivering a heavy load, the series APF has to be designed relatively using the same design procedure. In the present case, the design of series APF is downscaled to lower level based on the nature of load connected.

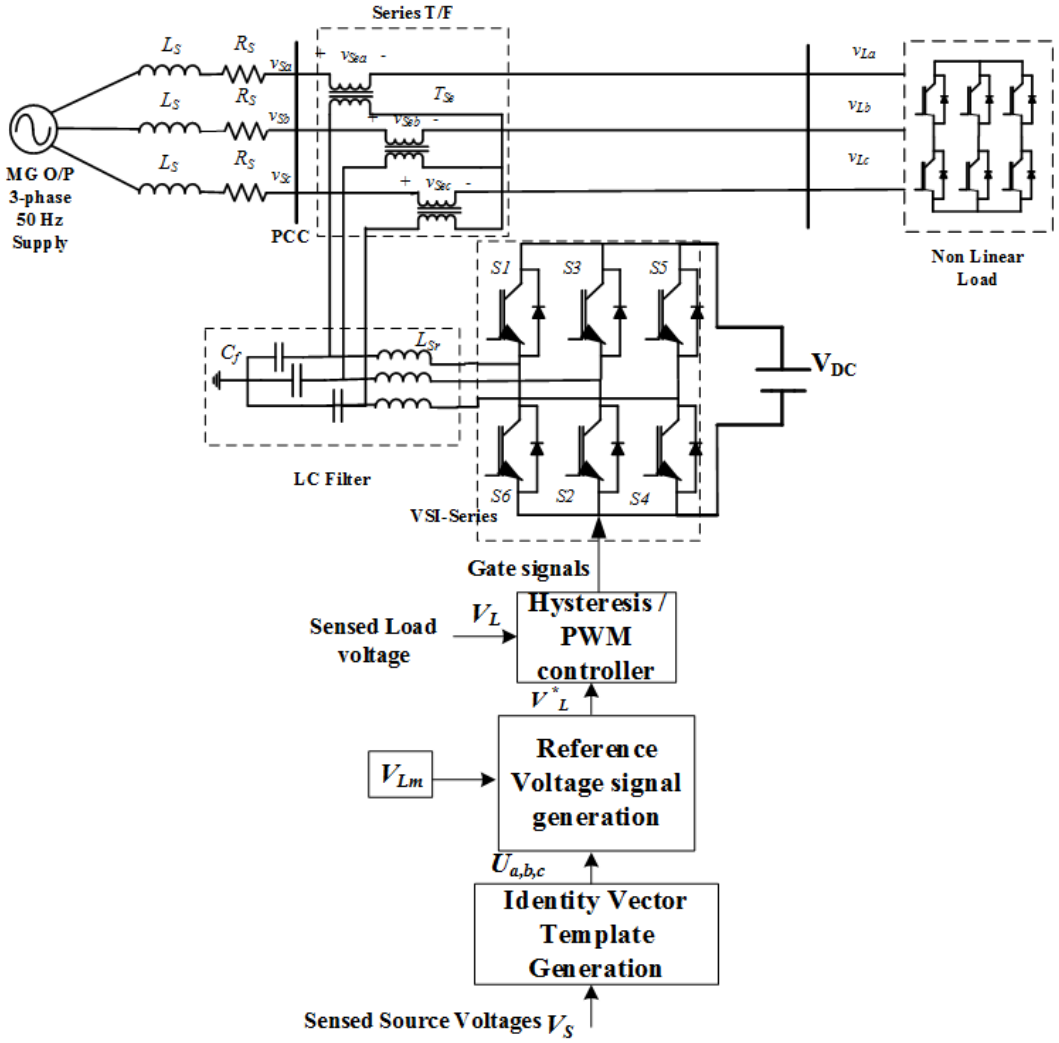


FIGURE 4.14: Schematic diagram of IVTG controlled series APF

4.6.4.1 Voltage Rating of the VSC of DVRs

Consider a voltage sag of 25% in a MG connected to common AC bus bar at 415 V, 2.5 kW, 1.5 kVAR critical load. The load voltage due to sag is obtained as 179.925 V. The required injected voltage for compensation V_C is estimated as,

$$V_C = \sqrt{V_S^2 - V_L^2} \tag{4.37}$$

4.6.4.2 Current Rating of the VSC of DVRs

The current rating of the DVR depends on the fundamental component of load current. For a 3 KVA load (P=2.5 kW, Q=1.5 kVAR), the current is related by,

$$\sqrt{3}\, V_S I_S \, = 3000 \tag{4.38}$$

Hence, the current rating of the DVR is $I_S = 4.173$ A.

4.6.4.3 kVA Rating of the VSC of DVRs

The kVA rating of the VSC of a DVR is calculated as

$$S = \, 3V_S I_S/1000 = 3 \times 158.67 \times 4.173/1000 = 1.9866 kVA. \tag{4.39}$$

4.6.4.4 Rating of Injection Transformer of DVR

Based on the voltage rating of VSC, injection transformer rating is calculated. The voltage of VSC is calculated based on the type of load connected. If the load connected is of nonlinear nature (like voltage fed three-phase rectifier) the design of series APF is based on the DC bus voltage of the non-linear load. If V_d is the DC load voltage of non linear load and is calculated from its fundamental component of AC voltage as given by:

$$V_{LL} = \frac{\sqrt{6}}{\pi} V_d \, = \, 0.779 V_d \tag{4.40}$$

From this the phase voltage V_{ph} can be obtained as $\frac{V_{LL}}{\sqrt{3}}$.

From all these, the voltage rating of VSC is calculated by,

$$\begin{aligned} V_{VSC} = \quad & \Big[\tfrac{1}{\pi}\int_0^{\pi/3}(V_{ph}\sqrt{2}\sin\theta - V_d)^2 d\theta \\ & + \int_{\pi/3}^{2\pi/3}(V_{ph}\sqrt{2}\sin\theta - 2V_d)^2 d\theta \\ & + \int_{2\pi/3}^{\pi}(V_{ph}\sqrt{2}\sin\theta - V_d/3)^2 d\theta\Big]^{1/2} \end{aligned} \tag{4.41}$$

For the non linear load specified in this case, the value of V_{VSC} is obtained as 75.64 V. The primary side voltage of injection transformer will be 158.6 V and the secondary side voltage will be 75.64 V. The kVA rating of injection transformer can be calculated as

$$kVA = 3V_C I_S/1000 = 3 \times 158.67 \times 4.173/1000 = 1.9866kVA. \tag{4.42}$$

Hence, the rating of injection trnasformer is 1.9866 kVA i.e, 2 kVA , n= 75.64 V/158.67 V.

4.6.4.5 DC Capacitor Voltage of VSC of DVR

The voltage of the DC capacitor of VSC is calculated by

$$V_{DC} > 2\sqrt{2}V_{VSC} \tag{4.43}$$

where the VSC voltage is 75.64 V The value of V_{DC} is 212 V and a V_{DC} of 220 V.

4.6.4.6 DC Bus Capacitance of DVR

The DC bus capacitance is estimated based on change in energy caused due to load change which is given by,

$$\frac{1}{2}C_d(V_{DC}^2 - V_{DC1}^2) = 3V_C I_S \Delta t \tag{4.44}$$

where V_{DC} is rated DC bus voltage, V_{DC1} is the DC bus voltage change when load changes, and Δ t is the time required for support. Considering Δ t = 200 μ sec, V_{DC} =220 V, V_{DC1} = 220 - 5%

of 220 V= 209 V, the DC bus capacitance can be calculated as $\frac{1}{2}C_d(220^2 - 209^2) = 3 \times V_C I_S \Delta t$. It give C_D as 2916.38 μF. Hence a DC bus capacitor of 3000 μF, 200 V is selected.

4.6.4.7 Interfacing Inductor for the VSC of DVR

The interfacing inductor L_{Sr} shown in Figure 4.14 is selected based on the current ripple in the current of the DVR ($\Delta\ I_S$). Considering the ripple current in the inductor is 2%, modulation index 'm' of VSC is 1, and with overloading factor a =1.2, the inductor is calculated as [160],

$$L_{Sr,interface} = \frac{\sqrt{3}nmV_{DC}}{2 * 6 * af_s * \Delta I_s} \tag{4.45}$$

Hence the interfacing inductor is estimated as 8.02 mH. Henceforth, an interfacing inductor design is L_r of 8 mH. Based on the above calculations, the series APF is designed for both linear and non-linear loads mentioned below in Table 4.1.

4.7 Simulation of DVR in MG for Voltage Compensation

A microgrid model is developed with 2 DERS, a PV generator of 1.5 kW and a wind generator 2 kW along with storage to deliver an output voltage of 3-phase, 415 V Line-Line RMS (phase to ground voltage of 338 V), 50 Hz, which is at common AC bus in MATLAB Simulink. The reference voltage is shown in Figure 4.15. The loads that are connected to the MG are given in

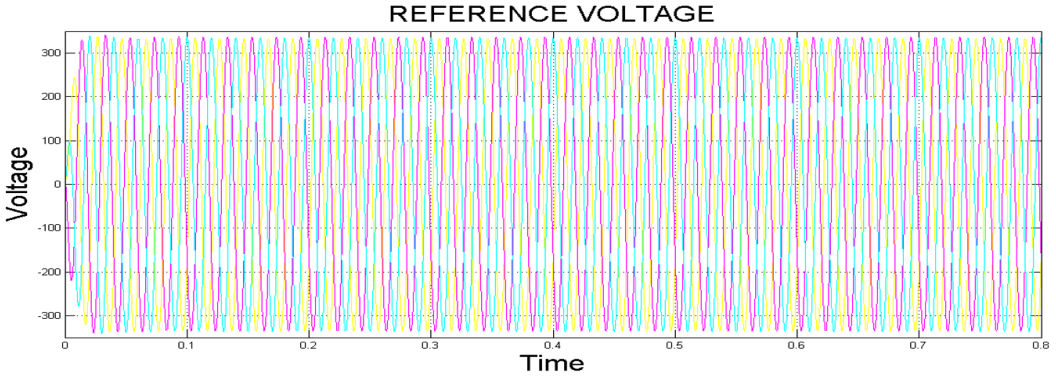


FIGURE 4.15: MG reference voltage

TABLE 4.1: System parameters and constants

System parameters	**Constants**
Microgrid voltage	415 V
VSI	Double 3-arm bridge (12 pulse)
DC Voltage (BESS)	100 V
Load 1 (Δ connected)	1500 W
Load 2 (Δ connected)	100 W, 1000 VAR Inductive
Load 3 (Δ connected)	100 W, 1500 VAR Capacitive

the Table 4.1. Due to resistive load 1 given in Table 4.1, the output voltage is dropped from 338 V to 247 V and further, it is dipped to a value of 187 V when the inductive load (Load 2) that creates a sag when introduced into the system between 0.2 to 0.6 sec. The sag in the load voltage is shown in Figure. 4.16. Similarly capacitive load (Load 3) is connected to MG, a swell

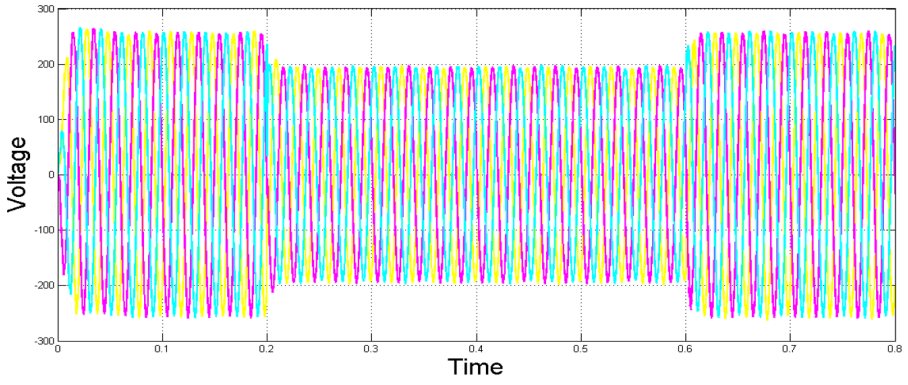


FIGURE 4.16: Sag in output voltage

in output voltage is created. The load is introduced into the sytem between 0.2 to 0.6 sec as shown in the Figure. 4.17. In order to mitigate these two issues in the MG, the compensating

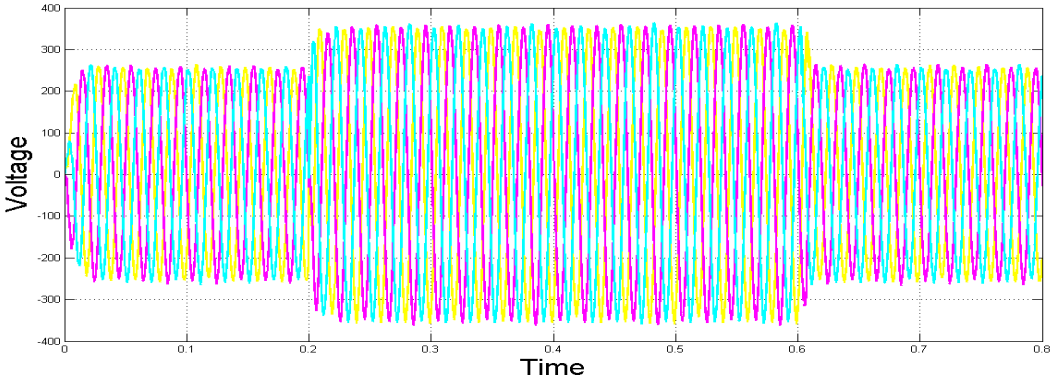


FIGURE 4.17: Swell in output voltage

device DVR has been connected just before the load as shown in Figure. 3.24. When the DVR

is controlled by using PI control and considering K_p and K_i as discussed in section 4.6.1, the output voltage is compensated to its reference value as shown in the Figure 4.18. However, the output at peak is not compensated to its full value i.e, 415 V Line-Line RMS (phase to ground voltage of 338 V) as the tips of the results are not following sinusoidal form. The compensated load voltage using PI control is shown in Figure. 4.18. The zoomed picture(sub) of Figure 4.19 shows the partially compensated output voltage at tips for both sag and swell problems when the corresponding reactive loads are connected to the MG. The PI control works only for specific values of K_p and K_i that is obtained by trial and error method. However, the values may not be suitable if different operating conditions like a change in nature of load and amount of load. Hence the control theory mentioned in section 4.6.1 fails to measure the fast acting changes in load which make the output from the MG varying. Similarly, the performance of the control is

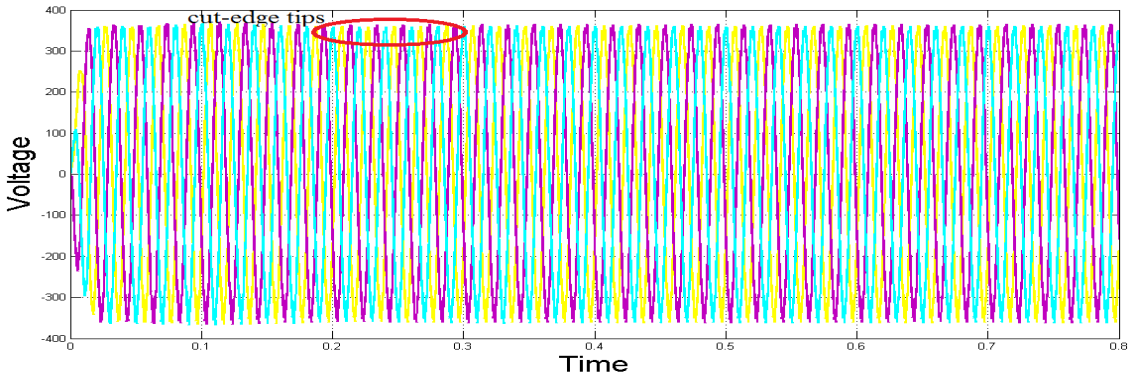


FIGURE 4.18: Voltage compensation using PI control

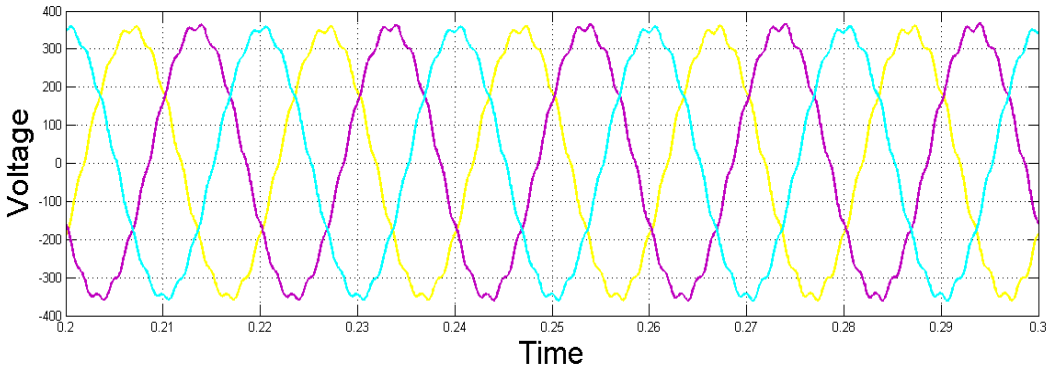


FIGURE 4.19: Partial voltage compensation at the edges using PI control

also analyzed for the supply changes. The supply side, sources being RESs, and due to changes in environmental conditions as mentioned in sections 3.4, 3.5, the output voltage at load cannot

be maintained at constant desired level of 415 V. The continuous changes in the input (both V & I) i.e, MG supply voltage & current disturbances are shown in the Figure 4.20 & Figure 4.21. When PI control discussed in section 4.6.1 is implemented to deal with these concerned supply disturbances, the output voltage is mitigated as shown in the Figure. 4.22. However, the tips of the output voltage do not get compensated well to the required sinusoidal form and contain many hitches in the output voltage. This is due to the fact that K_p and K_i, the gains of PI control are fixed for one condition and are not automatically tuned under dynamic varying conditions of the system. Hence, due to the improper tuning of the PI control in accordance with varying supply and load conditions, the output voltage is partially compensated. Hence, in

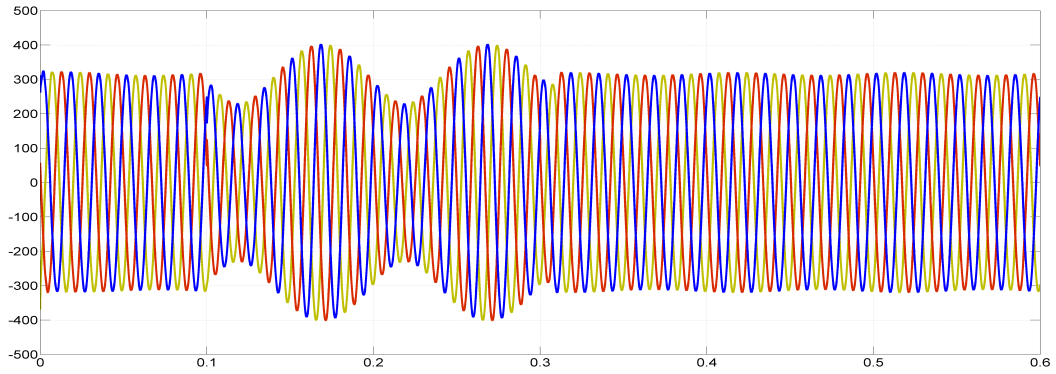


FIGURE 4.20: Voltage disturbances in the supply

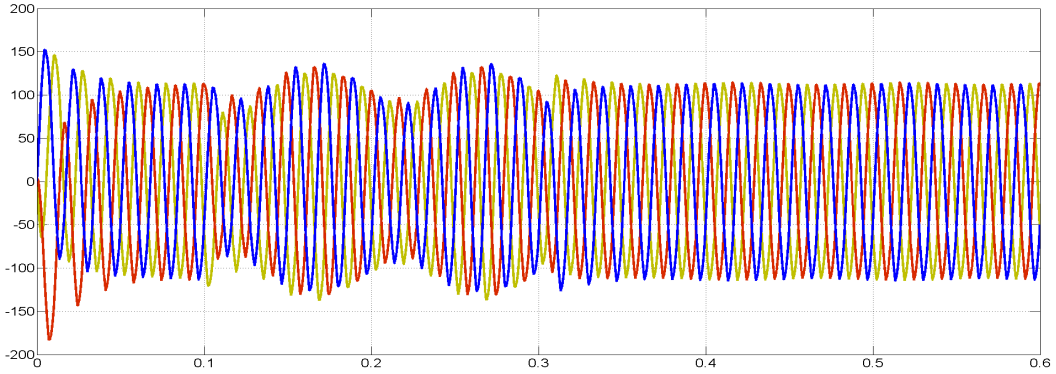


FIGURE 4.21: Change in current due to change in the supply

order to overcome this problem, and also to achieve quick response for the fast acting changes in the source and load, to obtain desired output wave for all operating conditions, SRF theory discussed in the section 4.6.1 is considered and implemented.

Using SRF theory, load voltage is compensated well without changing any of its parameters

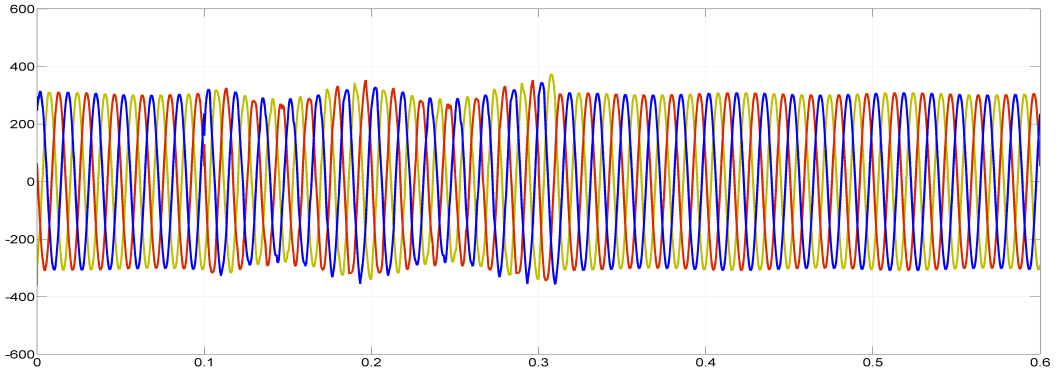


FIGURE 4.22: The compensated output voltage for supply disturbances using PI control

under different varying loads and is shown in Figure. 4.23. Sinusoidal voltage compensation at the edges using SRF theory control is shown in Figure. 4.24 and it represents the fine response of output voltage without any hitch. The control is also tested for its effective performance due to varying supply disturbances.The output voltage is also compensated for the continuous supply changes as shown in Figure 4.25. Further, the maximum value of possible variations in the

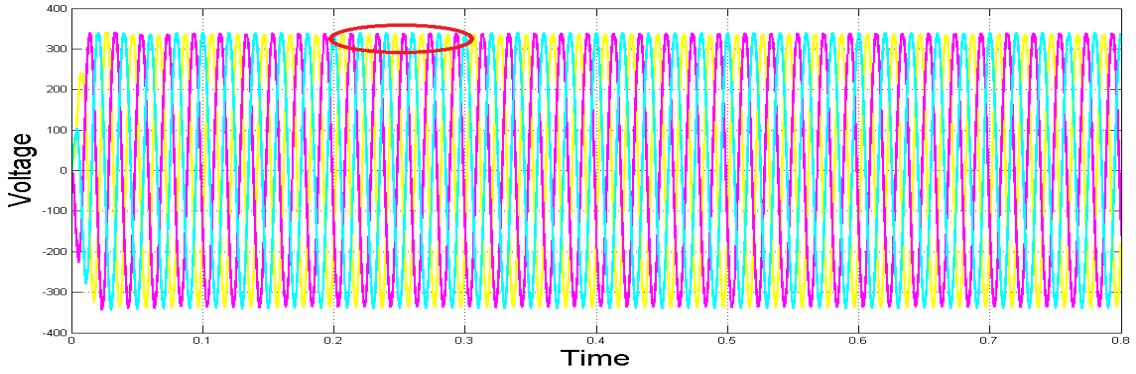


FIGURE 4.23: Voltage compensation using SRF theory control

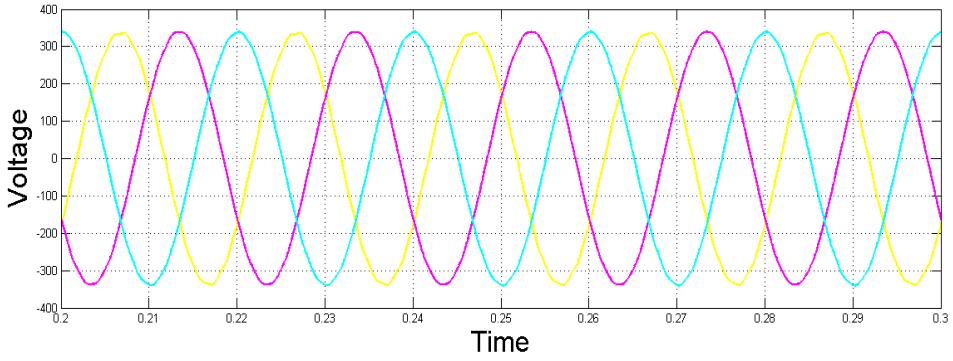


FIGURE 4.24: Voltage compensation at the edges using SRF theory control

supply voltage are approximated as 25% and simulated in the MG. Hence a supply disturbance

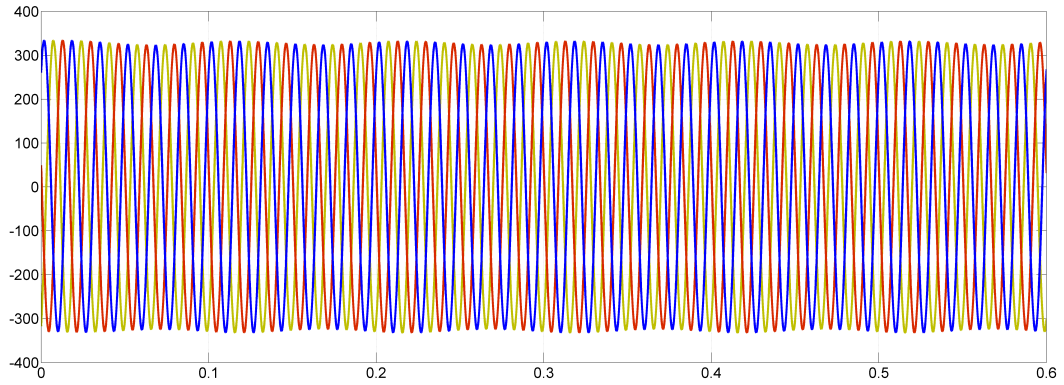


FIGURE 4.25: Compensated output voltage for supply disturbances using SRF theory control

to reduce and increase its peak value by 87.5V (X = 25%) to create both sag and swell within a short time span is created and observed for the duration from 0.1 to 0.8 sec. The sag (25%) in the supply voltage is shown in Figure 4.26 and Figure 4.27. When DVR is connected, the

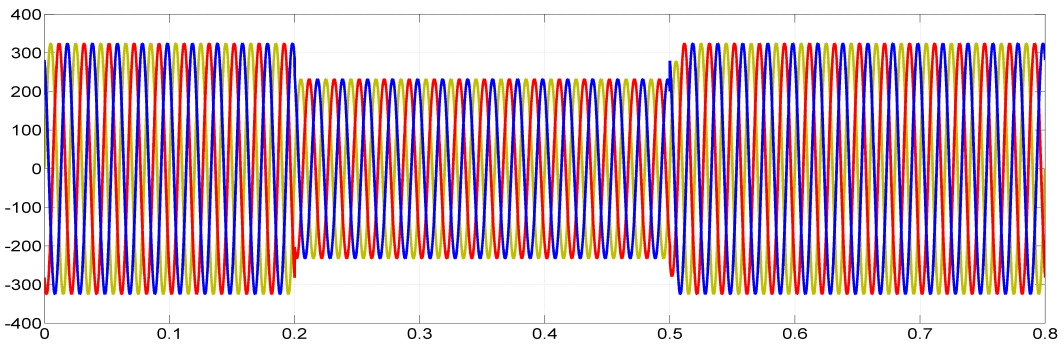


FIGURE 4.26: Sag in supply voltage

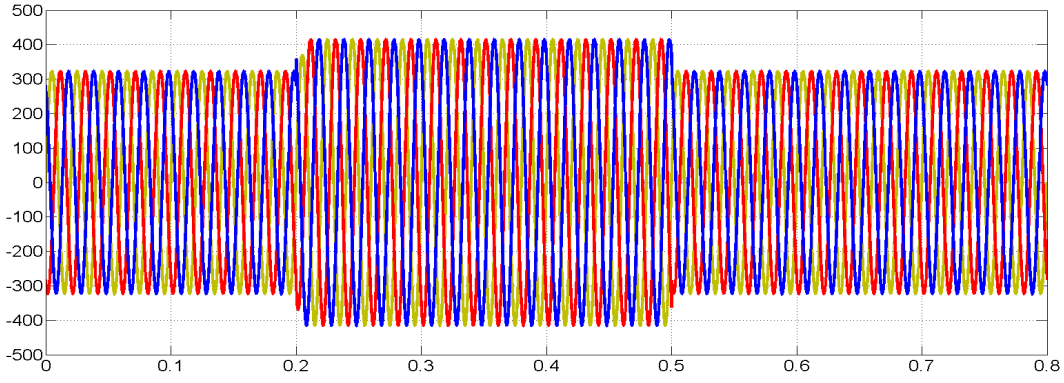


FIGURE 4.27: Swell in supply voltage

dip and rise in the supply voltage are mitigated. The injected voltages during sag and swell conditions are shown in Figure 4.28 and Figure 4.29 respectively. The corresponding changes in the currents of DVR during its working condition is shown in Figure 4.30 and Figure 4.31.

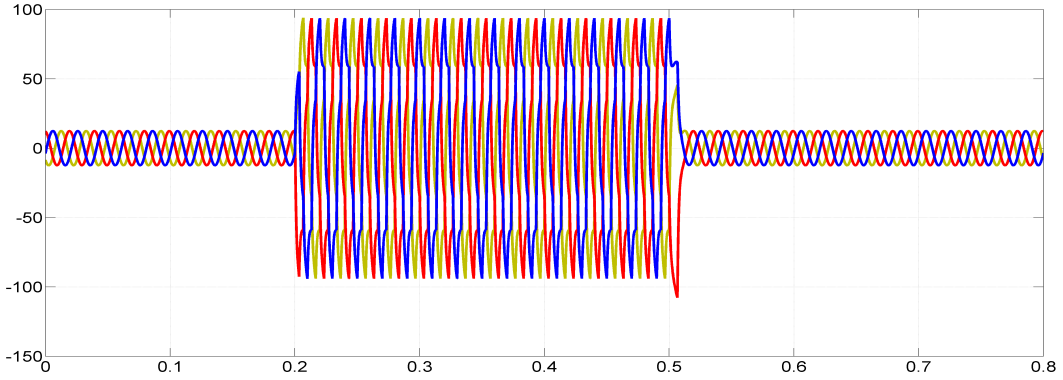


FIGURE 4.28: Injected voltage by series APF in sag condition using SRF theory control

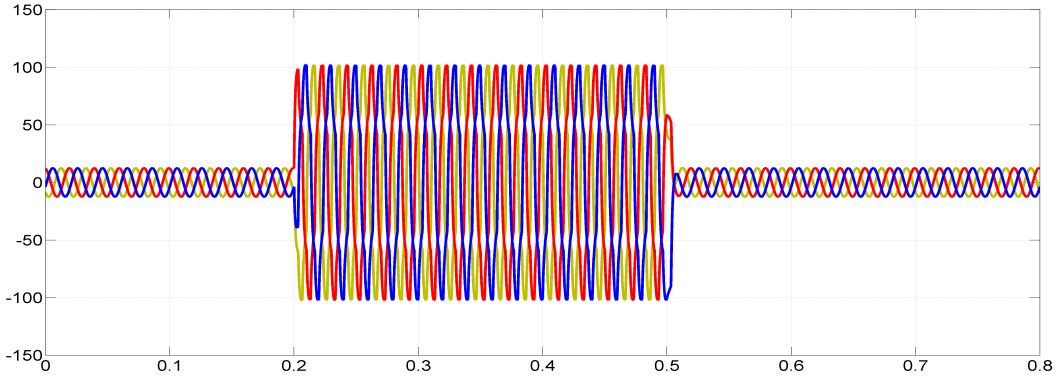


FIGURE 4.29: Injected voltage by series APF in swell condition using SRF theory control

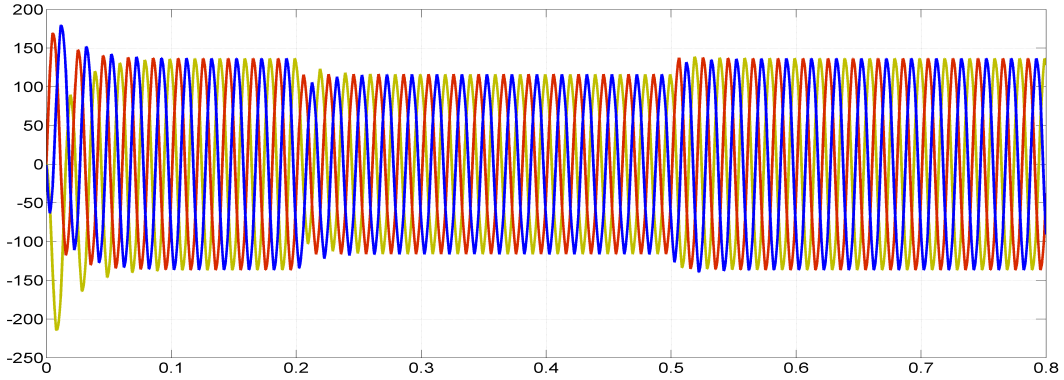


FIGURE 4.30: Current from series APF during sag compensation

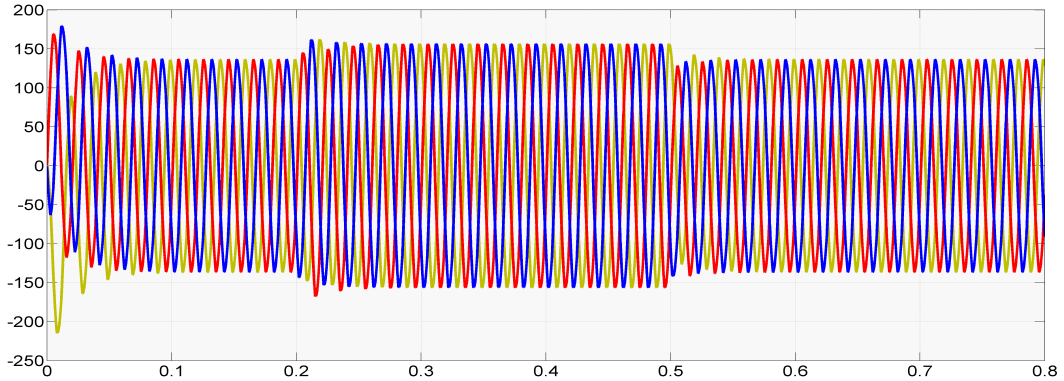


FIGURE 4.31: Current from series APF during swell compensation

Hence, the supply voltage disturbances which further disturb the load voltage in the similar way have been effectively mitigated using using SRF theory control of series APF into the system. The compensated load output voltage is shown in Figure 4.32.

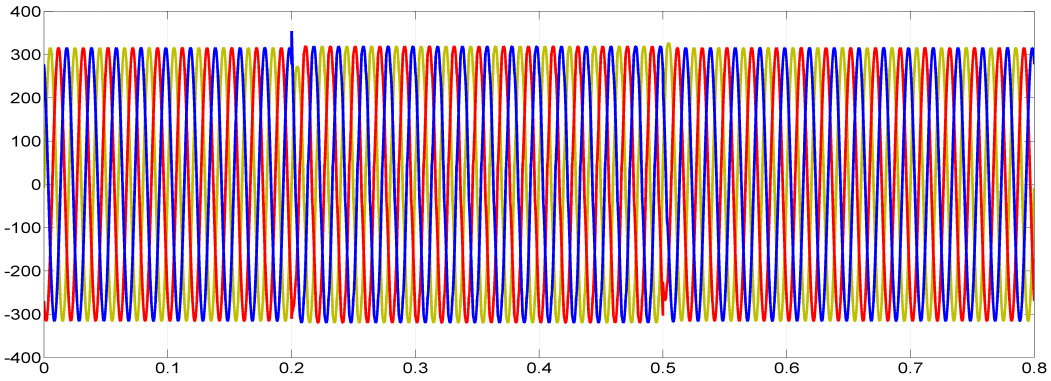


FIGURE 4.32: Compensated output(load) voltage using SRF theory control

Using the above two theories, the dips and swells in the output voltage due to supply voltage variations and also due to different loads are mitigated. The series APF controlled by SRF theory based control is compensating the output voltage to the desired sinusoidal when compared to conventional PI control. However, these two methods are found to be applicable in providing compensation by mitigating voltage disturbances in terms of magnitude and only for linear loads. The issue of stability of time-delay systems has been divided into two classes: delay-dependent and delay-independent and also, the delay-dependent stability criterion is less conservative than the delay-independent criterion when the size of delay is small. The considered MG has been treated as delay-independent as all the voltage problems are solved by using simple IVTG control and complex current problems are dealt by using shunt APF (for which the delay size can be approximated as small especially in case of distribution systems). Hence the condition of delay is ignored in the considered MG PQ compensation. As mentioned in section 2.1.2, loads that give nonsinusoidal outputs and containing harmonics also demand reactive power compensation. Hence the performance of MG is further assessed for nonlinear loads. The MG is connected to a nonlinear load containing a 3-phase full bridge diode rectifier delivering an RL load of 10 Ω + 0.15 mH combined with a series RL load of 0.4 Ω + 15 mH as shown in the Figure 4.33. It is observed that when the MG is delivering this nonlinear load, harmonics are developed in the load voltage as shown in the Figure 3.30. A THD of 24.48% is present in the resultant voltage as

shown in the Figure 4.35. When PI control is used in the series APF, these harmonics in the voltage are raised instead of mitigating. The % THD is increased to a value of 25.40 from 24.48 as shown in Figure 4.36. Similarly, when SRF theory is used as a control in the series APF, % THD is further increased to 47.44 Figure 4.37. From all these, it can be comprehended that the existing PI and SRF theory based controls are used to improve the voltage quality in terms of magnitude. Using these two controls for harmonic loads, the actual harmonic content in the load voltage is aided with the harmonics developed during injection. The injection harmonics are more in case of SRF based control due to its complex circuitry compared to PI control. Hence, % THD is raised in case of SRF theory based control compared to PI control. However, PI control is a simple conventional control that can provide compensation in terms of magnitude only. Hence the harmonics are not eliminated with PI control, more or less remains the same. In this situation,

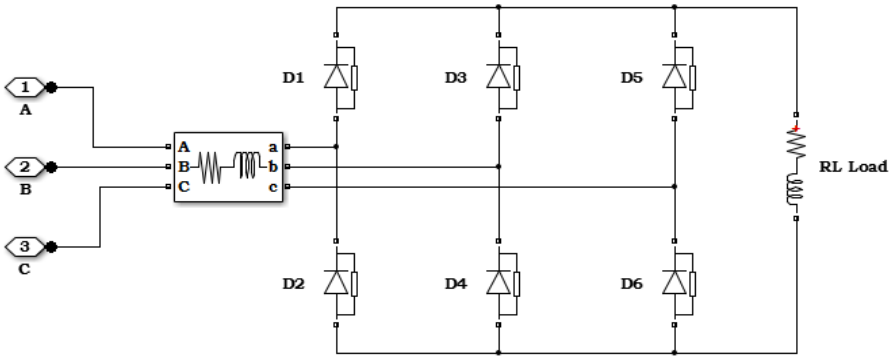


FIGURE 4.33: Diode rectifier connected as non-linear load in MG

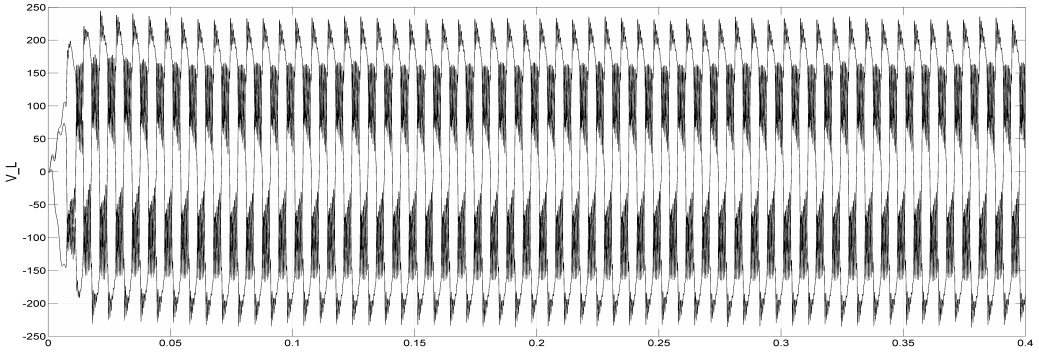


FIGURE 4.34: Harmonic load voltage

the proposed technique base on IVTG discussed in section 4.6.3 is considered and analyzed to provide compensation against the harmonics in the MG especially when it is delivering non

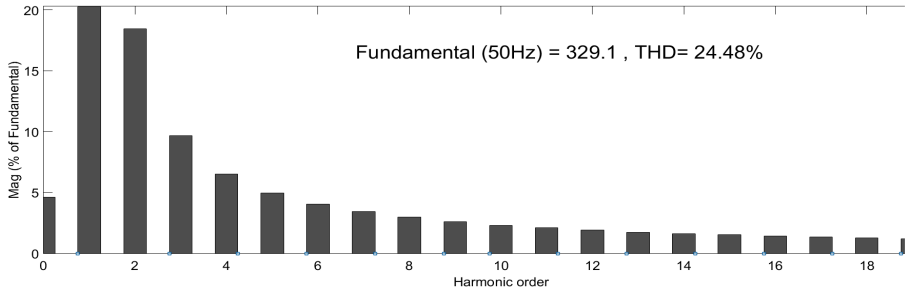


FIGURE 4.35: Harmonics in load voltage due to non-linear load

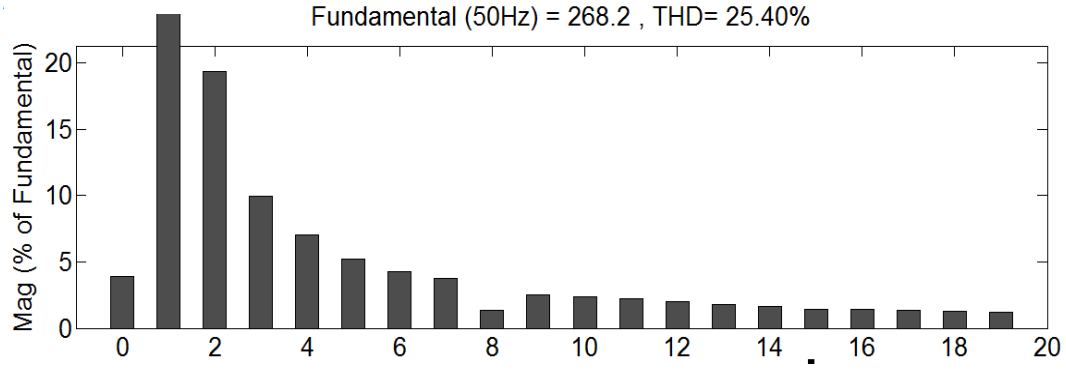


FIGURE 4.36: %THD of load voltage with PI control

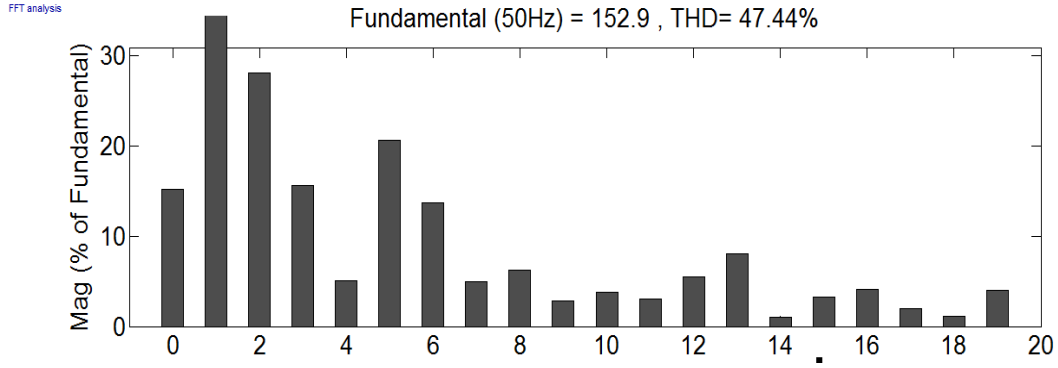


FIGURE 4.37: %THD of load voltage with SRF theory control

linear loads (power electronic loads). The proposed control IVTG control provides compensation based on the calculation of identity templates generated w.r.to reference fundamental frequency and magnitude. Hence the same is considered and implemented in the series APF connected to MG. The simulink diagram of IVTG control is shown in the Figure 4.38. However, with the implementation of proposed IVTG technique, % THD has been improved to 0.94 as shown in Figure 4.40. Similarly, the performance of the designed system with proposed control techniques is also verified in providing compensation for greater variations (182.5 V, i.e 54 %). The results is

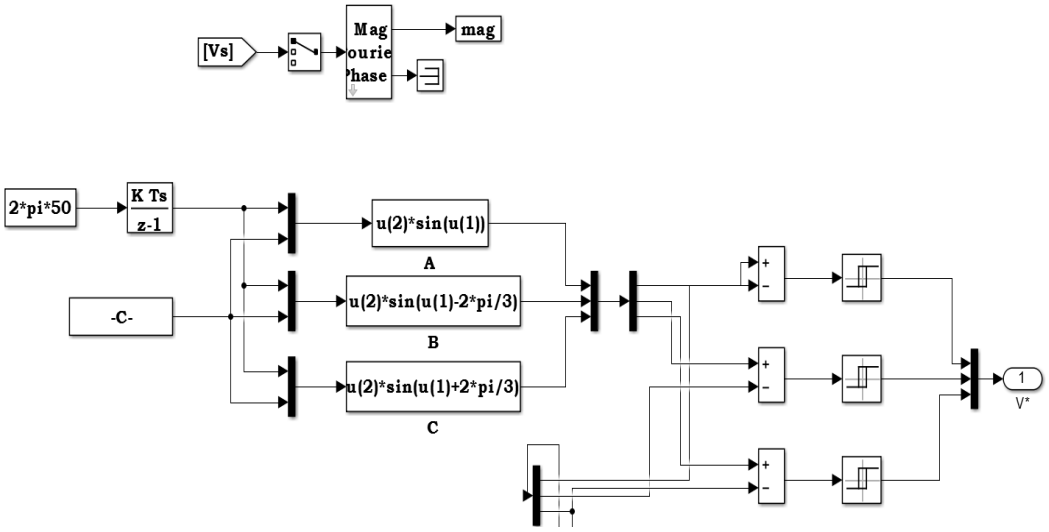


FIGURE 4.38: Simulink diagram of IVTG control

shown in Figure 4.39. Hence The performance of the system is also verified for LVRT condition in case of WECS (which is more prone to) by reducing the voltage to less than half of its value for a period of 0.2 sec. (similar to the case of sag more than 25 %) and also in flicker conditions, it is observed that the system can retain its voltage even in LVRT condition.

The simulation results prove that sag, swell, harmonics in output voltage due to supply and

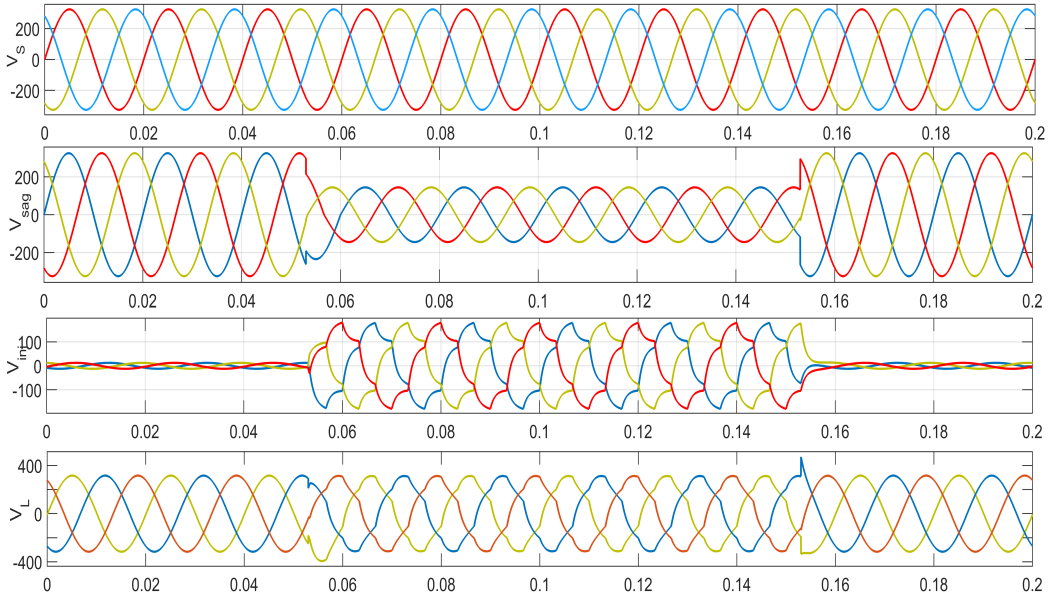


FIGURE 4.39: Mitigation of load voltage for more sag

load changes caused by reactive, harmonic loads and RESs input parameters are compensated well with series APF and is able to maintain its load voltage near to reference voltage in MG.

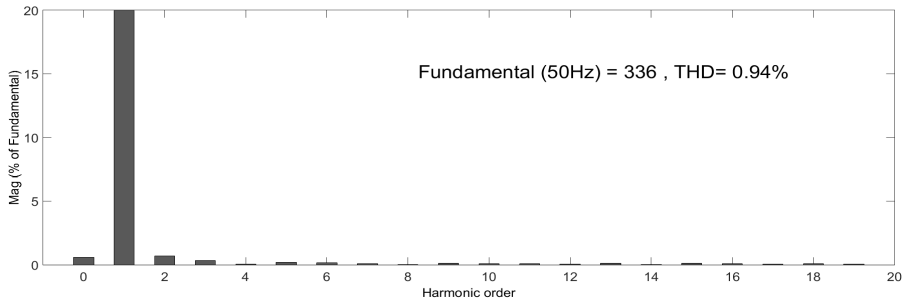


FIGURE 4.40: Compensated voltage for voltage harmonics using IVTG control

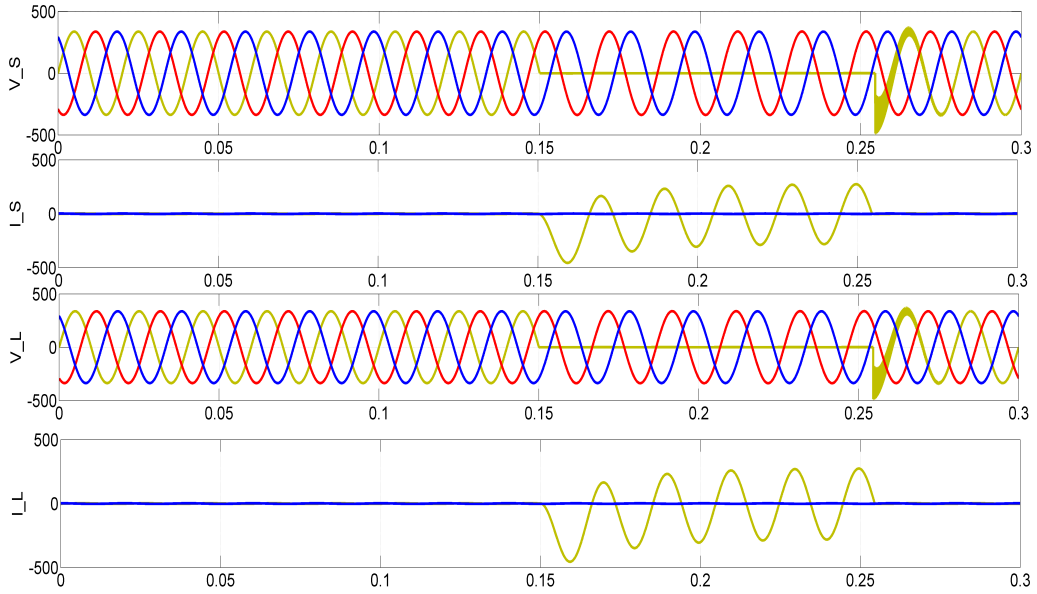


FIGURE 4.41: V & I of supply and load during LG fault without DVR

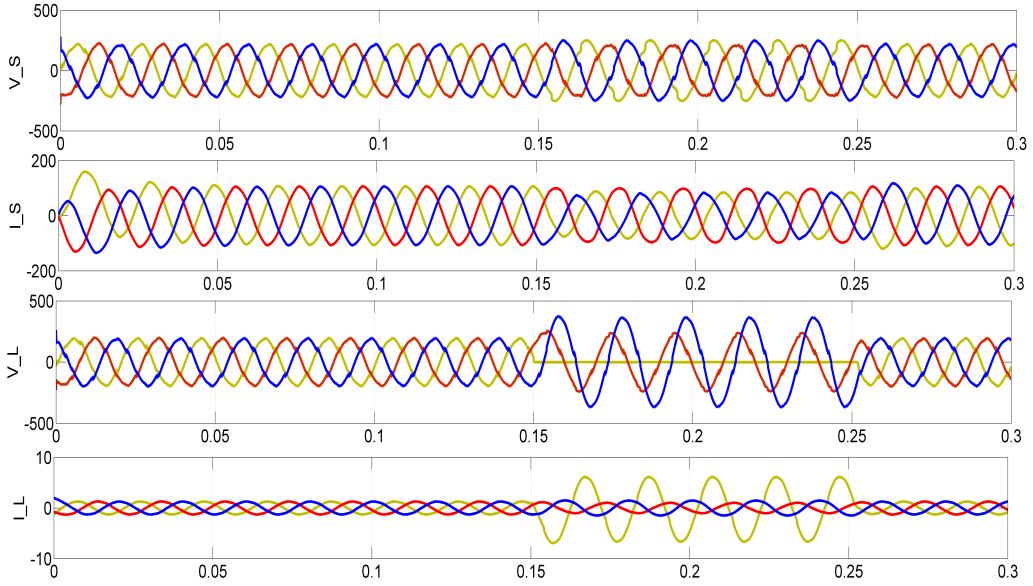


FIGURE 4.42: V & I of supply and load during LG fault with DVR

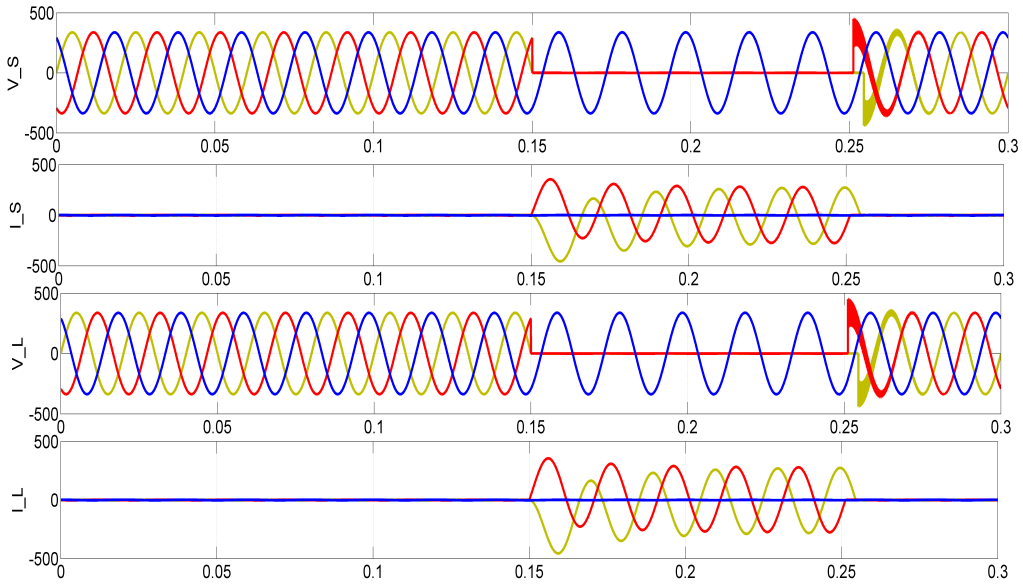


FIGURE 4.43: V & I of supply and load during LLG fault without DVR

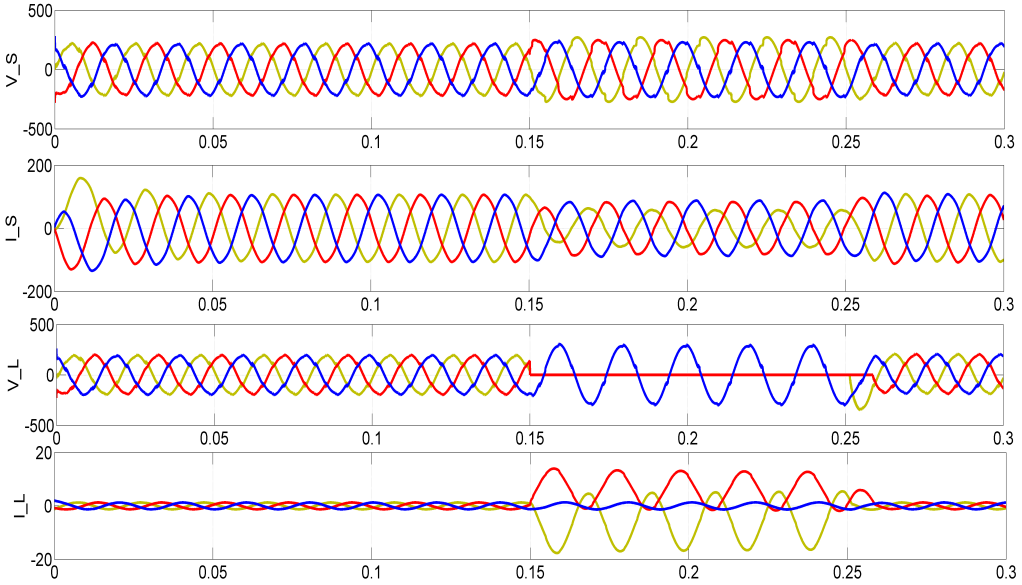


FIGURE 4.44: V & I of supply and load during LLG fault with DVR

Similarly, the performance of MG is also analyzed for symmetrical and unsymmetrical faults. The MG is connected to a 3-phase resistive load of 1 kW along with an inductive load of 600 VAR. Different faults LG, LLG and LLLG faults are simulated in the MG during 0.15 sec - 0.25 sec. The corresponding load voltage and current profiles are presented. When LG fault occurs in MG, the load voltage of phase-a becomes zero due to the short circuit from the line to ground shown by V_L, the supply current of phase -a is raised almost up to 250-300 A shown by I_L represented

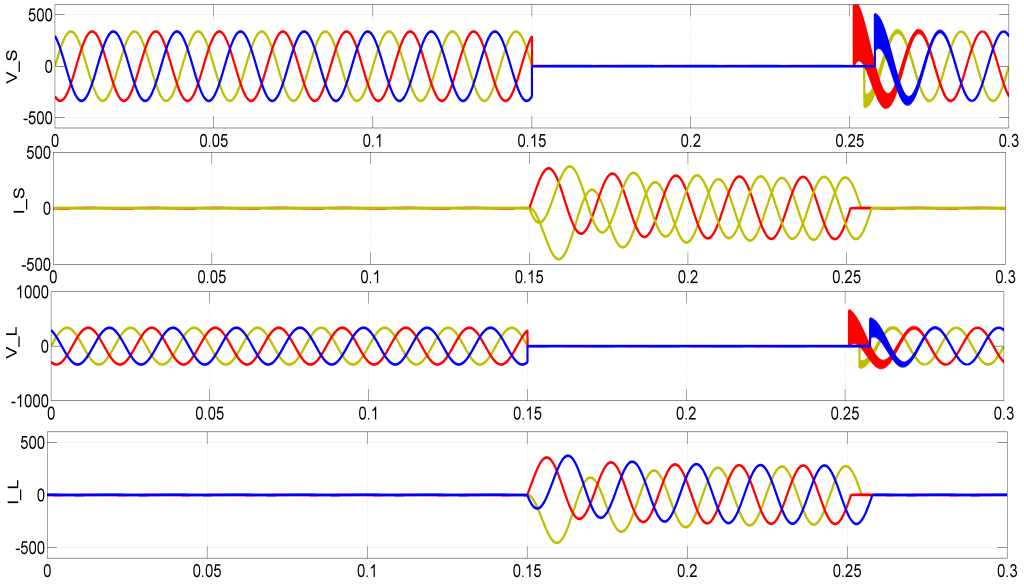


FIGURE 4.45: V & I of supply and load during LLLG fault without DVR

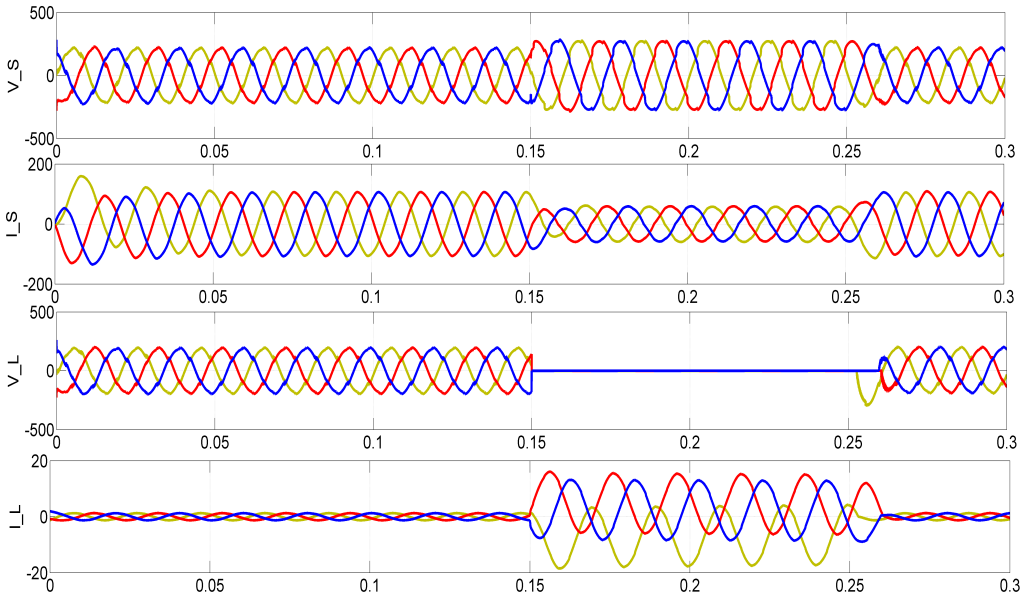


FIGURE 4.46: V & I of supply and load during LG fault with DVR

in Figure 4.41. If there is no compensating device connected to limit this current, the same V & I are flown towards supply as indicated by V_S and I_S as shown in Figure 4.41. When series APF is connected, the load current given by I_L is limited to a safer value below 10 A as shown in Figure 4.42. The supply voltage can be retained better to the normal value indicated by V_S as shown in Figure 4.42. However V_L of phase - a cannot be normal as that phase is short-circuited. When LLG fault occurs in MG, the load voltage of phase- a,b becomes zero due to the short

circuit from the line to ground shown by V_L, the supply currents of phase -a,b are raised almost up to 250-300 A shown by I_L represented in Figure 4.43. If there is no compensating device connected to limit this current, the same V & I are flown towards supply as indicated by V_S and I_S as shown in Figure 4.43. When series APF is connected, the load current given by I_L is limited to a safer value below 20 A as shown in Figure 4.44. The supply voltage can be retained better to the normal value indicated by V_S as shown in Figure 4.44. However V_L of phase - a,b cannot be normal as the corresponding phases are short-circuited. Similarly, When LLLG fault occurs in MG, the load voltage of phase- a,b becomes zero due to the short circuit from the triple line to ground shown by V_L, the supply currents of phase -a,b are raised almost up to 250-300 A shown by I_L represented in Figure 4.45. If there is no compensating device connected to limit this current, the same V & I are flown towards supply as indicated by V_S and I_S as shown in Figure 4.45. When series APF is connected, the load current given by I_L is limited to a safer value below 20 A as shown in Figure 4.46. The supply voltage can be retained better to the normal value indicated by V_S as shown in Figure 4.46. However V_L of phase - a,b,c cannot be normal as the corresponding phases are short-circuited.

4.8 Conclusion

With continuation of various power quality issues that are resulted from supply and load changes mentioned in section 3.5, a dynamic voltage restorer is applied to provide compensation. In this regard, harmonic and reactive compensation in MG for different load conditions and supply variations is observed and presented. The DVRs are mainly used for dynamic compensation of these voltage quality problems. However, the series active power filter (APF) protects the sensitive loads from the harmonics distortions in the voltage of the MG. As its name represents, a series active filter is expected to filter voltage harmonics in the supply systems, in addition, reactive power compensation. Hence the series compensator DVR is enriched with active filter topology and is converted into series APF by designing appropriate filter. The series APF was designed with proper control and incorporated into the MG and simulated. A controller using

PI, SRF techniques that give a scaled error between MG reference and actual load voltages are applied for providing RPC using series APF in MG. It is observed that using these two theories, the dips and swells in the output voltage due to supply voltage variations and also due to different loads are mitigated. However, the series APF controlled by SRF theory based control is compensating the output voltage to the desired sinusoidal when compared to conventional PI control and these two methods are found to be applicable in providing compensation by mitigating voltage disturbances in terms of magnitude and only for linear loads. Consequently, the loads that give nonsinusoidal outputs and containing harmonics also demand reactive power compensation. Hence, a unique technique named IVTG approach has been applied to provide harmonic compensation in MG. The simulation shows that the series APF effectively provides harmonic compensation and substantially, the performance is also satisfactory with quick response and excellent voltage regulation for all voltage disturbances. The performance of the device is also analyzed for fault ride through by limiting fault current to a safe value under different symmetrical and unsymmetrical conditions in the MG. From all these, it is comprehended that the enhanced DVR provides voltage quality in the MG effectively.