

Novel Control Strategies for Multilevel Inverter Fed Three-Phase Induction Motor Drives

THESIS

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*Dedicated to my Parents, my Husband,
and
my daughter Avighna*

CERTIFICATE

This is to certify that the thesis entitled **Novel Control Strategies for Multilevel Inverter Fed Three-Phase Induction Motor Drives** and submitted by **HIMABINDU.T**, ID No 2012PHXF0402H for award of Ph.D. of the Institute embodies original work done by her under our supervision.



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HIMABINDU.T

Declaration of Academic Integrity

I, **HIMABINDU.T**, declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be cause for disciplinary action as per rules of regulations of the Institute.

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Abstract

Direct Torque Control (DTC) is the state-of-the-art control strategy for 3-phase AC motor drives which allows direct control of torque and flux without involving very intensive computations that are inevitable for field oriented control (FOC). It is well known that DTC has more torque and flux ripples as compared to FOC as the former is based on voltage vector selection from a 3-phase 2-level inverter that offers only 6 non-zero voltage vectors as possible choices. Increasing the number of levels in a 3-phase inverter will allow more choices of voltage vectors and hence torque pulsations can be minimized in high performance drives; however, this also increases the complexity of computations and the number of components in the power circuit. The three-level inverter used in this work involves only three extra bi-directional switches as compared to the number of devices in a two-level inverter and hence the cost increase is insignificant as compared to a two-level voltage source inverter (VSI). The major advantages of DTC such as no requirement of current controllers, axes transformation, rotor position sensors- are still preserved when we use a three-level VSI. DTC's lesser parameter dependency and fast torque response has made this control technique more popular in industrial motor control. The objective of this research work is to evaluate and compare the performance of a DTC based three-phase induction motor drive (IMD) while it is being fed by two-level and three-level VSIs. A two-level hysteresis band controller is used as a flux comparator and a three-level and five level hysteresis controllers are used as torque comparators in the two-level VSI and three-level VSI fed drives, respectively. The performance of the drive in these two cases are compared in terms of starting current and torque, response time, responses during speed and load disturbances. The amount of pulsations in the torque and current are estimated for the two-level and three-level VSI fed cases.

The minimization of torque and current ripples has become one of the most important challenges especially in the case of a DTC fed IMD. In extension to the classical DTC, this work also proposes a novel predictive torque control (PTC) algorithm for an induction motor that is simple to implement and also minimizes switching loss by efficient voltage vector placement. An algorithm for selecting the nearest zero/redundant vector is presented. The aim of this portion of the research work is to evaluate and compare the performances of the DTC and PTC algorithms both applied to a three phase induction motor fed by a three-level diode clamped VSI. The comparison has been made based on the torque and current ripples, settling time, and response times during speed and load disturbances and Total Harmonic distortion (THD) of the motor current. The algorithms are simulated using Matlab/Simulink and the results

are presented. It is observed that the implementation of PTC scheme yields better performance with reduced torque ripple than the classical DTC. An experimental setup using an FPGA based controller is developed in the laboratory to implement the DTC based IMD on a 5.7 kW 3-phase induction motor. A novel direct power control (DPC) scheme, with virtual flux orientation based on the grid voltages, has been implemented for an active front end converter (AFEC) feeding the DC link of the VSI. The inverter feeding the induction motor is a multilevel inverter controlled by predictive torque control (PTC). Estimation of instantaneous active (P) and reactive power (Q) for the AFEC is carried out using virtual flux from the mains supply. Optimal switching states are selected from the switching table based on the errors in P and Q and hence the active and reactive power control is directly accomplished by the device switching states of the front end rectifier. The proposed PTC algorithm predicts the behavior of the drive under various load conditions which accordingly sets the power requirement for the AFEC. The proposed optimal voltage vector selection algorithm is applied to both rectifier and inverter, which reduces the number of switchings and therefore results in distinguishable reduction in the switching losses. Four quadrant operation of this multi-level inverter fed IMD with DPC at the front end and PTC at the load end is modeled and simulated in Matlab/Simulink environment and the results are presented. The performance obtained for the drive with the proposed control configuration under various steady state and transient operating conditions show that the drive possesses a very good dynamic response apart from having an acceptable power quality at the point of common coupling.

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Nomenclature

Symbol	Quantity
v_s	Stator Voltage
v_{ds}, v_{qs}	Stator Voltages along d and q -axes
v_a, v_b, v_c	Stator phase Voltages
V_a, V_b, V_c	Three phase Source Voltages
i_s	Stator Current
i_a, i_b, i_c	Stator phase Currents
i_{ds}, i_{qs}	Stator Currents along d and q -axes
$\mathbf{i}_a, \mathbf{i}_b, \mathbf{i}_c$	Three phase line Currents
I	Peak of the input current
$i_s^p(k+1)$	Predictive Stator Current
τ_e	Electromagnetic Torque
τ_{err}	Torque error
$\tau_{estimated}$	Estimated Torque
τ_{HBW}	Torque hysteresis band width
H_τ	Output of the Torque hysteresis controller
$\tau^p(k+1)$	Predictive Torque
ψ_{ref}	Reference Stator flux
ψ_{actual}	Actual Stator flux
$\psi_{estimated}$	Estimated Flux
ψ_{err}	Flux error
ψ_{ds}, ψ_{qs}	Stator flux along d and q -axes
ψ_s	Stator flux
$\psi_s^p(k+1)$	Predictive Stator flux

Symbol	Quantity
ψ_α, ψ_β	Stator flux vector along alpha and beta axes
ψ_r	Rotor flux
$\psi_r^p(k+1)$	Predictive Rotor flux
f_{HBW}	Flux Hysteresis band width
H_ψ	Output of the Flux Hysteresis controller
ω_0	Angular frequency
V_{ph}	Phase Voltage
V_{dc}	DC bus Voltage
R	Stator winding (per-phase) Resistance
R_{ag}, R_{bg}, R_{cg}	Stator winding (per-phase) Resistances of the Grid
L_m	Per-phase Magnetizing inductance
I_m	Per-phase Magnetizing current
α	Angle of flux
P	Number of poles
k_p, k_i	Proportional and Integral Gains
V_s	Inverter Voltage
S_a, S_b, S_c	Switching States
T_s	Sample Time
ϵ_h	Error Minimization
λ_ψ	Weighting Factor
p	Active/Real Power
P^*	Active/Real Power Command
q	Reactive Power
Q^*	Reactive Power Command
θ	Sector Angle

Abbreviation

AFE	Active Front End Converter
DBR	Diode Bridge Rectifier
DC	Direct Current
DTC	Direct Torque Control
DPC	Direct Power Control
IM	Induction Motor
IMD	Induction Motor Drive
NPC	Neutral Point Clamped inverter
PPR	Pulses Per Revolution
PTC	Predictive Torque Control
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
THD	Total Harmonic Distortion
UPF	Unity Power Factor

Chapter 1

Introduction

1.1 Introduction

Electric drives are motion control mechanism which make use of electrical machines, the input to which is modulated by power electronic converters using software tools and suitable control configuration implemented on an embedded platform. Generally, the main objective of the electric drive is to control the output load torque and speed, while converting the electrical energy from the power source into mechanical form. Fig. 1.1 shows the block diagram of an electric drive system along with its control configuration wherein the control can be implemented by analog controllers or digital processors such as digital signal processors (DSPs) or microprocessors/ microcontrollers [1]- [2].

The increasing demand over the years for advanced motion control technologies have resulted in the development of many control strategies for electric motor drive systems. This is because of the fact that medium voltage drives are immensely employed in the industry. Proper integration of motor drives with suitable control schemes improves the performance and efficiency of an electric motor and its input power quality (PQ) too [3]. Also, the advent of a plethora of high power, high frequency, less lossy power semiconductor devices, novel circuit topologies and processors with immense computational capability have contributed to the development of high performance electric drives. Among all the conventional electric motors, squirrel cage induction machines (SCIMs) have really attracted a lot of attention due to their advantages like low maintenance requirement, high power-to-weight ratio, high reliability, etc. With the advent of different control schemes such as field-oriented control (FOC) and direct torque control (DTC), SCIMs are replacing dc motor drives even for adjustable speed applications [4]. Classification of various control schemes for induction motor drives (IMDs) are shown in Fig. 1.2. The main objective behind applying these techniques is to achieve high performance in motor drives.

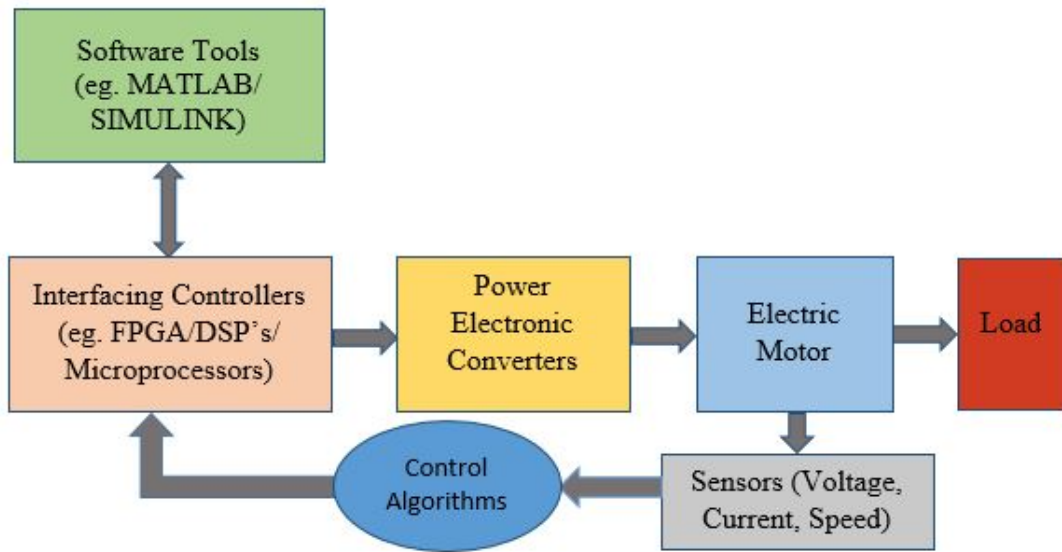


Figure 1.1 Block diagram of an Electric Drive System

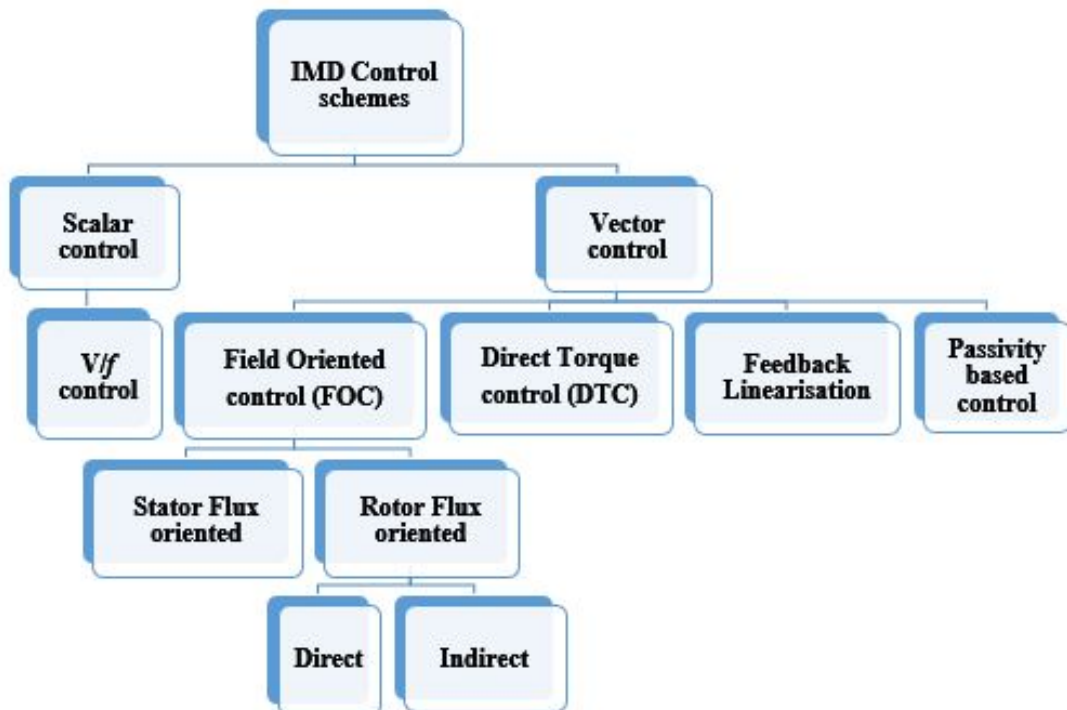


Figure 1.2 Classification of Control Schemes for an IMD

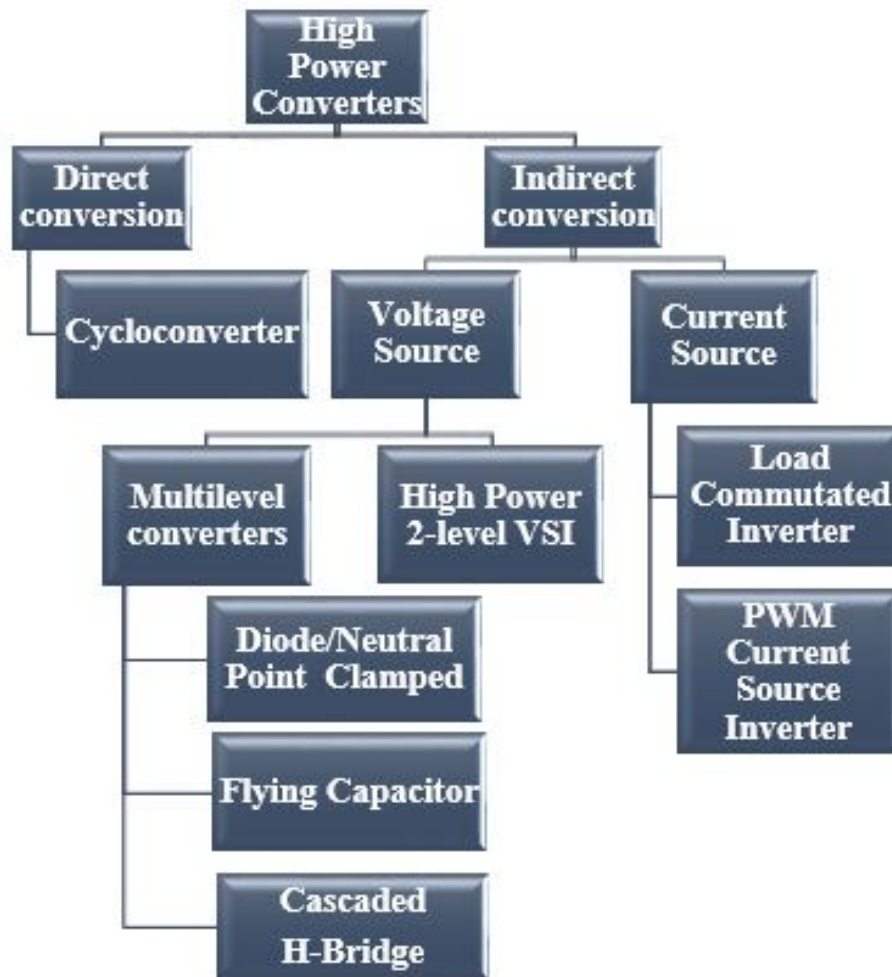


Figure 1.3 Classification of converter topologies

As the name indicates, scalar control changes voltage and frequency magnitudes in proportion to each other to achieve control over the rotor speed until base speed. Above rated speed, field weakening is incorporated to achieve constant power operation. Field oriented control (FOC) strives to emulate DC motor control structure into an induction motor (IM) by decomposing stator current into torque producing and flux producing components of current and control these components independently. On the other hand, direct torque control (DTC) deals with flux linkages and voltages directly rather than dealing with the currents. These control techniques can be implemented by making use of different types of converters. Classification of converter topologies is presented in Fig. 1.3. As shown in the figure, the power conversion could be direct AC-AC conversion using a cycloconverter; otherwise, a fixed frequency, fixed magnitude AC is converted into DC and then in the next stage, it is converted into AC of required frequency and magnitude by making use of voltage source inverters (VSIs) or current source inverters (CSIs).

1.2 State of the Art of Control techniques in Induction Motor Drives

Three-phase SCIMs are extensively used in industries owing to their low cost, simple and rugged structure, self-starting capability and versatility. Due to the advent of power electronic converters, these motors are used for several adjustable speed applications such as electric traction, paper mills, textile mills, process control industries, electric four wheelers, mining and heating, ventilating and air-conditioning (HVAC) systems. Some of the applications like CNC machines, robotics, traction systems and textile mills require very accurate speed and position control mechanisms. Accurate control can be achieved by employing state-of-the-art control techniques like FOC or DTC [5–7]. FOC is capable of generating a good amount of torque even at zero speed condition which is useful in applications such as elevators, cranes and hoists. However, the implementation FOC requires huge amount of calculations to be done in a short span of time and coordinate transformations. On the other hand, DTC is simpler to implement, as it deals with flux linkages and torque directly, rather than dealing with currents as is the case with FOC. DTC does not require coordinate transformation and it is not necessary to determine the exact position of the flux linkage space vector. Because of these advantages, DTC is becoming popular with three-phase IMDs for various applications [8–10]. But, one of the major drawbacks of any DTC drive is the pulsations in its torque [11]. The pulsations are caused by the overshoot and undershoot in the magnitude and position of the flux linkage space phasor. There are only six non-zero voltage vectors available in a two-level voltage source inverter (VSI) out of which two voltage vectors have to be chosen to nullify the flux and torque errors obtained from the DTC algorithm. Due to the constraints imposed by the power converter devices and processor used, the minimum sampling time is restricted to a certain value. So, any voltage vector applied to the stator in a DTC drive, is sustained for a duration of that sampling interval. This causes overshoots and undershoots in the torque and flux values. If there had been more choices of voltage vectors, this situation could have been avoided. One has more choices in voltage vectors by using a multilevel inverter [12]- [13]. Such an inverter, say, a 3-level inverter will have various switching combinations of the devices involved. In a 3 level inverter, 360° space is divided into 12 sectors and one can utilize twelve non-zero vectors out of 27 possible voltage vectors to control the position and magnitude of the flux.

Different types of controllers are employed while implementing DTC or FOC. A unified approach for designing control configuration for switching converters and electrical machines is realized in the form of sliding mode control (SMC) or variable structure control (VSC). This technique is appropriate during the discontinuous control actions i.e. the ON-OFF behavior of power converter switchings [14].

But the main drawback is chattering effect. Because of high frequency switching, the condition of the switches changes so fast that it leads to the change of whole structure of the controller making the chattering effect persist. So, higher order of SMCs are proposed for eliminating these issues and for achieving accurate performance of the system.

Predictive torque control (PTC) is another upcoming robust control technique for both linear and non-linear systems [15]. The availability of fast microprocessors and DSPs has led to better controllability and higher accuracy in power converter fed electric drive systems. PTC as well as model predictive control (MPC) techniques require intensive computations; but, these are capable of achieving high performance control in AC drives [16]. The concept of predictive control involves in predicting the future behavior of the system for different kinds of inputs. Though there are many innovations and control techniques proposed in the literature for the speed control of drives, still there is scope for simplifying the control architecture and topological configurations for AC motor drives.

1.3 Research Gaps

High performance AC motor drives employ FOC and DTC commonly either using a VSI or CSI. In a typical FOC algorithm, the stator current is decomposed into flux and torque producing components. For achieving this, estimation of the exact position and magnitude of the air gap flux is essential which is done by making use of complex coordinate transformations [5]. On the contrary, DTC has gained prominence with adjustable speed IMDs due to its fast torque response and simplicity in implementation; but, the conventional DTC algorithm causes high torque and current ripples especially at lower speeds. A modified DTC technique based on stator voltage vector prediction is proposed in [17]- [18], where the drawbacks such as current distortion and torque ripple are minimized. However, power quality improvement achieved due to these algorithms are not highlighted in these papers. An improved DTC technique with space vector modulation (SVM) is proposed in [9] which eliminates undesired torque and current ripples effectively. A performance comparison of DTC based IMD with P and PI controllers is presented in [19]. A neuro-fuzzy based adaptive controller for accurate speed estimation in a sensorless direct torque controlled IMD, working at low speeds, is discussed in [20] wherein model reference adaptive controller is being employed as a rotor flux observer. There are a large number of papers on the modeling and simulation of IMDs in MATLAB, whereas [21] describes complex real-time simulation of IMD using RT-Lab software while it is running simultaneously on several personal computers.

A few papers discuss specially designed model predictive DTC to provide fast dynamic and good

steady state performances for an IMD by reducing rotor flux and electromagnetic torque ripples [22–25]. However, many of these control algorithms are applicable while operating the converter at high switching frequencies. On the other hand, PTC using immediate flux control (IFC) [26] allows the converter to operate with a low average switching frequency, with slightly higher current and torque ripples. In the second variant of IFC, these ripples have been reduced drastically, but with a considerable increase in the average switching frequency. In [27], an objective comparison of model predictive direct torque and current control methodologies has been done. A comparative study between PTC and DTC for a permanent magnet synchronous machine (PMSM) is presented in [28]. Based on the control techniques discussed above for various adjustable speed AC motor drives, some research gaps have been identified and they are being addressed in the present work. The work carried out in this thesis are as follows:

- Analysis on various control strategies for the performance improvement of Multilevel Inverter fed IMDs.
- Implementation of the above control strategies in Simulink/MATLAB platform and identification of the limitations with the existing control strategies.
- Proposing a suitable control strategy to overcome these limitations especially with reference to multi-level inverter fed IMD to reduce switching losses and to improve performance.
- Implementing this IMD scheme experimentally using an FPGA to achieve compact hardware setup with high performance capability.

1.4 Scope of the work

In most of the DTC drives, high switching frequency due to the use of hysteresis controllers and associated switching losses are major issues, especially when a multi-level inverter is used to feed the IMD. Furthermore, the ripples observed in torque and flux, particularly in low speed operation, pose a major problems to sensitive loads. Some remedial measures are proposed to overcome these issues in the present work. Initially, the performance of a DTC based IMD fed by a 2-level and 3-level inverters are compared in terms of their starting and steady state responses, flux and torque ripples, overshoots and undershoots during speed and torque perturbations. The three level inverter used here has reduced number of devices and yet capable of yielding a voltage with low output distortion. A modified DTC strategy incorporating predictive algorithm is proposed for the three level reduced switch (nine switches) VSI fed IMD. This inverter topology is less costly than a regular three level inverter due to the use of

only one additional device per leg as compared to the normal two-level VSI. The future behaviour of the system in terms of flux, current, and torque are predicted using mathematical model equations and the voltage vector that minimizes the future error is deduced; this particular voltage vector is applied to the motor drive to achieve a better performance. The complete system is studied for different speed and load conditions by modelling the drive system in Simulink/MATLAB. The torque and current ripples, settling times and overshoot, total harmonic distortion (THD) etc. are analysed and also compared with the classical DTC method and the results are presented. A novel predictive control scheme for a three-level diode clamped VSI fed IMD is presented for reducing the torque ripples; further, its performance is compared with a two-level inverter fed drive. For implementing predictive control, the present values of drive parameters such as its current and flux are utilized to predict the behavior of the complete drive system during the next time step. This enables the controller to apply a suitable combination of voltage vector(s) such that the torque ripples could be minimized. The proposed predictive control algorithm is analyzed and the responses are studied for different load and speed conditions of the IMD using Simulink/MATLAB. Whenever there is a redundancy in the switching states of the devices to obtain a particular voltage space vector, suitable choice is made so that the number of switching transitions is kept to a minimum. The switching losses, THD in the stator current, current and torque ripples, overshoot and settling time are analyzed in detail, in this work. The present work combines the optimal zero vector placement strategy for switching loss reduction for the multi-level inverter with direct power control of the active front end (AFE) rectifier. Direct power control of three phase AFE rectifier achieved by optimal voltage vector selection based on the estimation of grid virtual flux. This enables the control strategy to calculate instantaneous active and reactive powers. On the load side, three level neutral point clamped inverter fed IMD is controlled using the proposed PTC algorithm with optimal zero vector placement that reduces the switching losses. This analysis is carried out in Simulink/ MATLAB/ environment for dynamic operating conditions in all four quadrants of drive operation. Finally PTC based IMD has been implemented using an FPGA module. The performance of the drive has been recorded for different operating conditions.

1.5 Organization of Thesis

The work done during the course of this doctoral study has been organized in the form of a dissertation in the following chapters:

Chapter 1 introduces classification and state of the art of control schemes for an IMD and converter

topologies. This chapter also identifies research gaps and then presents the scope of this thesis work.

Chapter 2 gives an account of the literature survey carried out during the course of this research work. The focus is mainly on the control techniques and circuit topologies of the converters for IMDs.

Chapter 3 elucidates the system configuration for both the front end converter and machine side converter and their control methodologies.

Chapter 4 presents modeling and simulation of the proposed control schemes for inverter fed IMDs. This includes both two-level and three-level inverter fed IMDs.

Chapter 5 discusses the results obtained from the simulation models for the proposed control techniques for the reduced switch multilevel inverter fed IMD.

Chapter 6 presents the hardware setup for a FPGA controlled inverter fed IMD followed by experimental results in *Chapter 7*.

Chapter 8 presents the main conclusions drawn from this research work. It also presents scope for future work.

Chapter 2

Literature Review

2.1 Introduction

Higher efficiency, quick response and accurate control are the requirements of many of the industrial drives today. Adjustable speed AC motor drives based on FOC and DTC are able to provide high dynamic performance with maintenance-free operation. In the last two decades, due to the advent of high speed processors and high power semiconductor devices and converters, many novel control configurations have been implemented for IMDs catering to the needs of various applications such as e-mobility, paper mills, textile mills and process control industries. This research work primarily concentrates on multi-level converter fed IMDs with DTC and PTC techniques. An account of the literature survey carried out during the course of this research work has been presented in the following sections. The papers surveyed have been categorized under two specific topics namely, converter topologies and control techniques for IMDs. Based on the material available on these two topics, research gaps have been identified and subsequently, scope of work to be carried out during the course of this dissertation has been outlined.

2.2 Converters for Adjustable Speed Induction Motor Drives

In literature, articles [29] - [30] have discussed power converters and control systems for IMDs because most of the industries use induction motors as their back bone especially for motion control applications. A plethora of high performance, high rated power devices have been developed in the recent past, which have given rise to a huge variety of converters thus improving the performance of the motor drives significantly [3]. Among the different types of DC to AC inverters, two level voltage source inverters (VSIs) are used for medium power drives whereas current source inverters (CSIs) are

commonly employed in very large capacity drives. For drives of high voltage rating, multilevel inverters (MLIs) are commonly used.

2.2.1 Two level Voltage Source Inverters

Most of the two level VSI fed IMDs are used in medium and low power applications. Generally, the number of levels of the converter is decided by the number of steps in the output voltage or current (either zero or $+V_{dc}/-V_{dc}$) generated by the converter. This inverter output voltages or currents can be generated using sine pulse width modulation (SPWM) technique. However, there are certain limitations with SPWM [31]. The output voltage and current are distorted if the switching frequency is not high enough and the total harmonic distortion (THD) of the voltage will be beyond the limits stipulated by international power quality standards. Two level inverters have to be operated at high switching frequencies if overall harmonic content in the output has to be reduced which is not possible for high power and high voltage applications [32]. Most of the PWM techniques require high speed processors for successful implementation [33–35]. One more modulation technique called space vector PWM (SVPWM) is commonly used in VSIs for better utilization of DC link voltage as explained in [36]. As two-level inverters normally have only 6 possible (non-zero) voltage vectors, the choices are limited while implementing a drive control scheme. From the point of view of increasing the choices available, MLIs provide a better flexibility of control [37].

2.2.2 Multilevel Voltage Source Inverters

Multilevel converters are considered today as the state-of-the-art power-conversion systems for high-power and power-quality sensitive applications [38]. An overview of multilevel converter topologies is presented in [39] and recent advances made in modulation and control of such converters are discussed in [40]. These multilevel converters are employed in controlling motor drives and utility interface systems. It is easy to produce high power, high voltage with the help of multilevel structure because of the way in which device voltage stresses are controlled in the structure. MLIs include an array of power semiconductor devices and capacitor voltage sources, the output of which generate voltages with stepped waveforms. Hence, power rating is increased by increasing the number of voltage levels in the inverter without requiring higher rating on individual devices. Medium-voltage multilevel converters with a focus on achieving low harmonic distortion and high efficiency at low switching frequency operation has been proposed in [41]. The main disadvantage of MLIs is the requirement of a

large number of power semiconductor switches. As number of levels increases, the number of switches and gate drive circuits increase which makes the overall system more expensive, complex and less reliable. Most of the inverters are controlled by Pulse Width Modulation (PWM) signals of various forms. PWM methods for the most commonly used VSIs impress either voltages, or currents with low THD, into the stator windings of the machine [42]- [43]. Modern inverter control techniques for the power converters are capable of addressing issues such as power quality improvement, taking care of voltage imbalances and enhancing efficiency of the system [44]- [45]. A PWM scheme for a dual-inverter-fed open-end winding IMD is designed in [46] to eliminate harmonic currents. Simplified SVM techniques for an MLI have been presented in [47]. Initially, cascaded MLI structure was introduced by McMurray in the 1970's [48]. But, the major problem with the cascaded H bridge inverter is the requirement for multiple numbers of DC sources. Diode clamped or neutral point clamped (NPC) MLI was proposed in early 1980's [12], where all phases share a common DC bus, which minimizes the number of capacitors of the converter and hence they are used in applications such as an interface between DC and AC transmission lines and in adjustable speed drives. Another topology called flying capacitor MLI was introduced subsequently [49] and there have been many papers on balancing the capacitor voltages in that topology [50]. The flying capacitor inverter is similar to a diode clamped inverter; but instead of clamping diodes, the inverter uses capacitors. A survey of existing MLI topologies and control configurations are presented in [51]. Classical cascaded MLIs cannot provide regenerative operation in various applications like transportation systems and downhill conveyors where bidirectional power flow is necessary. In order to accommodate regeneration, a few topologies are proposed in [52]- [53]. A new MLI topology with reduced switch count is proposed in [54]. Hammond has addressed the issue of DC link voltage balancing in an MLI [55] as the intermediate DC levels tend to overcharge or discharge if there is no precise monitoring and control. A 5-level inverter for a medium voltage drive has been presented in [56] whereas a grid-tied MLI with higher efficiency is presented in [57]. Multi-level converters for DC-DC applications are detailed in [58]. One major advantage of MLIs is that they can successfully reduce the output THD even at lower switching frequencies [59]. The analysis of an MLI operating over a wide range of modulation indices is discussed in [60]. Modular multi-level converters (MMC) [61] are a new breed of MLIs that are used in off-shore oil-drilling applications. Ever since, there has been a number of researchers working on MMC for various high power applications.

2.2.3 Current Controlled VSIs (CC-VSIs)

Current controlled PWM converters are extensively discussed in the literature due to their merit of having control over the output current despite the PWM controller directly controlling voltage waveform only [62–64]. Various current control techniques have been known for several years. They can be grouped into the following classes: PI controllers, Hysteresis current controllers (HCCs) and Predictive controllers. PI current controllers could predict the harmonics present in the output of an inverter due to which the design of filters becomes simple. But, HCCs operate at variable switching frequencies making the filter design difficult. Predictive controllers are quite complex to implement; so, the processors have to be really powerful for implementing the predictive control technique. [65–67].

2.3 Control Techniques for Adjustable Speed Drives

The induction machines find ubiquitous application in industrial domain due to their maintenance-free and rugged nature. Many upcoming control techniques like field oriented control (FOC) and direct torque control (DTC) have allowed induction machines to be used in adjustable speed applications, especially with excellent dynamic response. These control techniques contribute to improvements in efficiency and accuracy. Various control schemes reported in the literature for the accurate control of IMDs are discussed in the following sections.

2.3.1 Field Oriented Control (FOC)

Most of the industrial applications such as electric traction, textile mills, paper mills, printing presses, cement mills, oil drilling, process control, transport sectors, electric vehicles, conveyer belts, pumps etc., make use of adjustable speed drives (ASDs). Some of them require accurate position control whereas others may need exact speed tracking. ASDs are also widely used in commercial sectors especially for heating, ventilating and air-conditioning (HVAC) systems. The crux of FOC is to find the air gap flux vector position at any instant of time and then decompose the stator current space phasor along and perpendicular to the airgap flux so that these two components can be controlled independent of each other. Decomposing the current (with respect to the air gap flux vector position) involves coordinate transformations; it requires the exact position of the air gap flux vector. But, DTC is not as computation intensive as FOC; so, DTC is preferred in many of the ASD applications where low speed operation is not very common.

2.3.2 Direct Torque Control (DTC)

It is quite challenging to control the torque and speed of an IMD especially because the phase angle between the stator and rotor fluxes is dependent upon the load torque requirement and also because rotor flux and current are not easily accessible. Scalar control, FOC, DTC, and sensorless DTC are the most commonly used control schemes for IMDs [68–70]. Many advanced control techniques (such as sliding mode controllers and fuzzy logic controllers) are adopted to achieve an excellent dynamic response during load changes and external disturbances [71], [72], [10]. The drive should be insensitive to parameter variations as well. Direct torque and flux control strategy based on variable-structure control and discrete space-vector PWM has been reported in [9]. Objectives such as torque error reduction, high resolution of sector identification and torque & current ripple minimization have been achieved by a high-performance controller for an IMD [73]. A neuro-fuzzy based adaptive controller for accurate speed estimation in a sensorless direct torque controlled IMD, working at low speeds is investigated in [74], wherein model reference adaptive controller is being employed as a rotor flux observer. There are a large number of papers on the modeling and simulation of IMDs in MATLAB, whereas [21] describes complex real-time simulation of IMD using RT-Lab software while it is running simultaneously on several personal computers. Sliding mode control (SMC) is a non-linear control method employed to provide quick and accurate response, with robustness irrespective of motor parameter variations [75]. Sliding mode design methods and their applications in power electronics and motion control systems are explained in [69]. Fuzzy sliding mode structure is developed in [76], which is capable of avoiding chattering effect commonly observed in many ASDs. For high-performance applications of the IM servo drive, a dynamic sliding mode controller (DSMC) with a recurrent radial basis function (RRBF) network is proposed in [77]. In this paper, an adaptive dynamic SMC system (ADSMCS) for IFOC-IM drive that guarantees the robustness in the presence of parameter uncertainties and load disturbances has been discussed. The analysis, design and simulation of the FOC, DTC, and other non-linear methods have always been attempted by various researchers aiming to achieve good dynamic performance of the motor drive using different types of inverters such as VSIs, CSIs and MLIs.

2.3.3 Predictive Torque Control (PTC)

Despite the simplicity of implementation of DTC, its major demerit is high torque and current ripples (in the motor drive) due to the limited choice of forcing function. Various modifications in the control methodologies have been put-forth by the researchers to overcome these disadvantages [8], [78],

[79]. Predictive torque control algorithms [24], [26], [17] advocate estimating the performance of the drive for different forcing functions and ultimately choosing the one with the minimum deviation from the desired operating point. In MLIs, the number of choices available for the forcing functions are more and hence it becomes computationally more intensive to implement a PTC algorithm. A comparison between the classical DTC technique and predictive torque control (PTC) is done in [18]; similarly, the DTC technique has been compared with forced machine current control (FMCC) in [80]. From all these reported works on PTC available in the literature, it is amply clear that PTC offers a number of advantages (over classical control methods such as FOC, DTC, SMC) like lesser torque and current ripples and accurate and faster tracking of speed and torque.

2.3.4 Direct Power Control (DPC)

Active front end (AFE) rectifiers are being employed in a wide range of applications, such as Distributed Generating systems (DGS), Battery Energy Storage Systems (BESS) and adjustable speed drives (ASDs), to improve the power quality at the point of common coupling (PCC). This is because the consumers as well as the utilities are very concerned about maintaining an acceptable level of PQ adhering to the international power quality standards. The quality of power has become a major concern for the consumers as well as utilities due to the proliferation of power converters employed in various applications causing non-sinusoidal currents to be drawn from the power grid. Various control strategies for these AFE rectifiers, such as, Voltage-Oriented Control (VOC), Direct Power Control (DPC) and predictive control [81–83] have been proposed in the literature. Direct power control technique for three-level and multi-level converters have been discussed in [84], [85]. In [85], individual DC link capacitor voltage of each of the H bridges is controlled by selecting suitable space vectors such that power sharing among different H bridges happen in proportion to their rating. The advent of many fast and powerful microprocessors and digital signal processors have enabled the development of many new control techniques for modern power converters such as model adaptive reference controller (MARC) and predictive controllers [86–88]. Predicting the future behaviour of a system is the main characteristic of a MPC algorithm. At lower switching frequencies, if torque and current pulsations have to be reduced in an IMD, it is essential to use advanced control techniques like FMCC and model predictive direct current control (MPDCC). A comparison between FMCC and MPDCC is carried out in [89]. A combination of a PI controller and predictive dead-beat controller is employed in [90], in order to achieve fast torque and flux responses, when sufficient voltage reserve is available. Predictive optimal switching sequence direct power control of a two level converter is presented in [91], which is computationally intensive al-

though the output response is excellent. There have been research on the predictive direct power control (PDPC) schemes for DC/AC converters [92]- [93], where the well-known predictive control is combined with DPC for selecting the voltage vectors sequence. In contrast to all direct model predictive controllers present until today, that precalculates the behaviour of the system for only next sampling time, the new optimising control technique predicts the behaviour even for a longer duration as discussed in [94]- [95].

2.3.5 Power Quality Improvement

Extensive use of power converters in several applications has adverse effect PQ which results in unfavorable attention from the utilities, simultaneously affecting the customers economically as well. PQ problems include harmonics in voltage/current at load and supply sides, unbalance in voltages/currents, neutral current in a 3-phase 4 wire configuration and deviation of power factor from unity. Power converters connected to the utility are expected to maintain a power factor close to unity [96]. A review of single-phase and three-phase improved PQ converters presented in the literature [97]- [98] outline different converter configuration that could be employed to mitigate PQ issues. Several power factor correction (PFC) methods [99]- [100] are available for PQ improvement at the PCC, in both DC-DC and AC-DC converters. In general, passive (multiphase transformer based), active (switch based topologies) and hybrid (combination of passive and active) wave-shaping techniques are employed for PFC at the front end [101]- [102]. In addition to this, current injection technique is applied to AC-DC converters for mitigating of harmonics and also to improve PQ indices [103]- [104]. But, it requires accurate current control. A third harmonic current injection circuit using a zig-zag transformer is applied to front end AC-DC converter in order to enhance PQ improvement in [105]. To mitigate problems related to voltage sag and swell, dynamic voltage restorer (DVR) is commonly used as a remedial device [106].

2.4 Objectives of the Research work

Based on the literature review carried out on converters and control techniques for IMDs, it is found that ample work has been done on the MLI fed IMDs; however, reduced switch MLIs have not been analyzed sufficiently. This thesis work takes up analyzing reduced switch MLI thoroughly. To reduce switching losses in the MLI, it is essential to follow optimal switching sequence while transitioning from one switching state to another. The work carried out in this thesis strives to minimize the number of switchings that takes place during the operation of the DTC based IMD. Predictive torque control for an IMD has been implemented with reduced switch MLI combining that with optimizing the sequence of

switching of the devices in the MLI. The entire scheme is implemented on FPGA based control platform. Employing an active front-end converter (AFEC) for a DTC fed IMD has been explored to improve input power quality while direct power control (DPC) is adopted for the AFEC and predictive torque control is used for the inverter feeding the motor drive.

2.5 Conclusions

There has been a lot of research work in the area of ASDs operating at medium and high voltage levels. Due to the inherent advantages of IMDs, the focus, naturally, has been on the three-phase squirrel cage induction motors. Most of the high performance drive applications require fast transient response. This chapter discussed various control strategies available in the literature for torque, flux and speed control of an IMD which results good steady state behavior and dynamic response under different load conditions. This chapter also throws some light on power quality issues related to IMDs and different strategies adopted for mitigating PQ issues. Finally, based on the literature review and identified research gaps, the objectives of this research work have been spelt out. The next chapter will describe the configuration of the system adopted in this research work.

Chapter 3

System Configuration

3.1 Introduction

Adjustable speed drives (ASDs) controlled by different power converters are used in various applications ranging from low power residential, medium power level commercial to high capacity industrial applications [107]- [108]. The purpose of using a power converter in drives is to improve the time of response, accuracy and efficiency of the system. On the whole, every application requires suitable topology and appropriate control scheme for accurate performance of the ASD system. Fig. 3.1 represents the general configuration of the ASD system, where active front end (AFE) and machine side converter (MSC) are of suitable power converter topologies chosen based on the application. Gate signals are generated from the constituted control scheme and fed to the respective converter devices. Ultimately, the output voltage of the MSC controls the ASD and AFE converter is fired in such a manner to maintain the input power quality within acceptable standards.

3.2 Control methodology and implementation

There are different types of control schemes that can be used for controlling the speed and torque of an IMD, namely, scalar control, field-oriented control, direct torque control and predictive torque control. Salient features of some of these control schemes are presented in the following sections along with modeling equations.

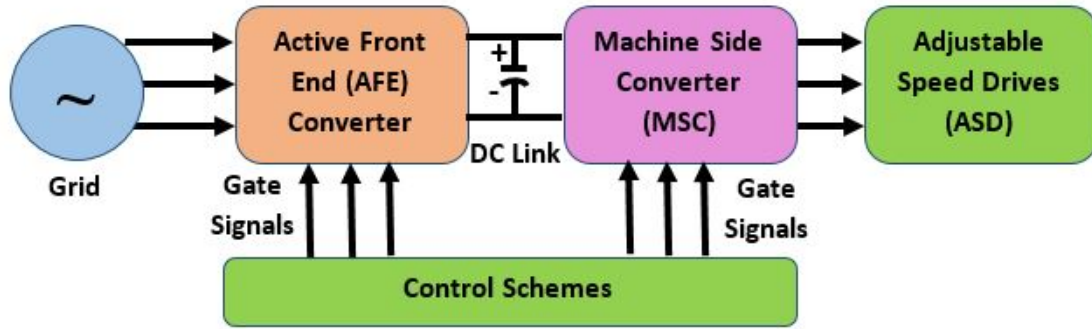


Figure 3.1 General configuration of an Adjustable Speed Drive System

3.2.1 Direct Torque Control (DTC)

DTC technique was introduced by Takahashi and Noguchi [6]. In field-oriented control (FOC), the stator current of an induction motor is resolved into flux and torque producing components of current i_{ds} and i_{qs} where the d-axis is chosen along the magnetizing flux linkage vector position. So, FOC requires exact position of the flux vector and also computation of currents along d and q-axes. On the other hand, DTC requires the sector position of the flux vector and it deals with the voltages applied from the VSI directly, as the applied voltage instigates the rate of change of flux linkages.

DTC is simpler as it deals with flux linkages and torque directly rather than dealing with currents as is the case with FOC. DTC does not require coordinate transformation and it is not necessary to determine the exact position of the flux linkage space vector. Because of these advantages, DTC is becoming popular with three-phase IMDs [107]. But, one of the major drawbacks of any DTC drive is the pulsations in its torque [108]. The pulsations are caused by the overshoot and undershoot in the magnitude and position of the flux linkage space phasor. There are only six non-zero voltage vectors available in a two-level voltage source inverter (VSI) out of which two voltage vectors have to be chosen to nullify the flux and torque errors obtained from the DTC algorithm. Due to the constraints imposed by the power converter devices and processor used, the minimum sampling time is restricted to a certain value. So, any voltage vector applied to the stator in a DTC drive, is sustained for a duration of that sampling interval. This causes overshoots and undershoots in the torque and flux values. If there had been more choices of voltage vectors, this situation could have been avoided [109], [12]. One has more choices in voltage vectors by using a multilevel inverter. Such an inverter, say, a 3-level inverter will have various switching combinations of the devices involved. In a 3 level inverter, 360° space is divided into 12 sectors and one can utilize twelve non-zero vectors out of 27 possible voltage vectors to control the position and magnitude of the flux.

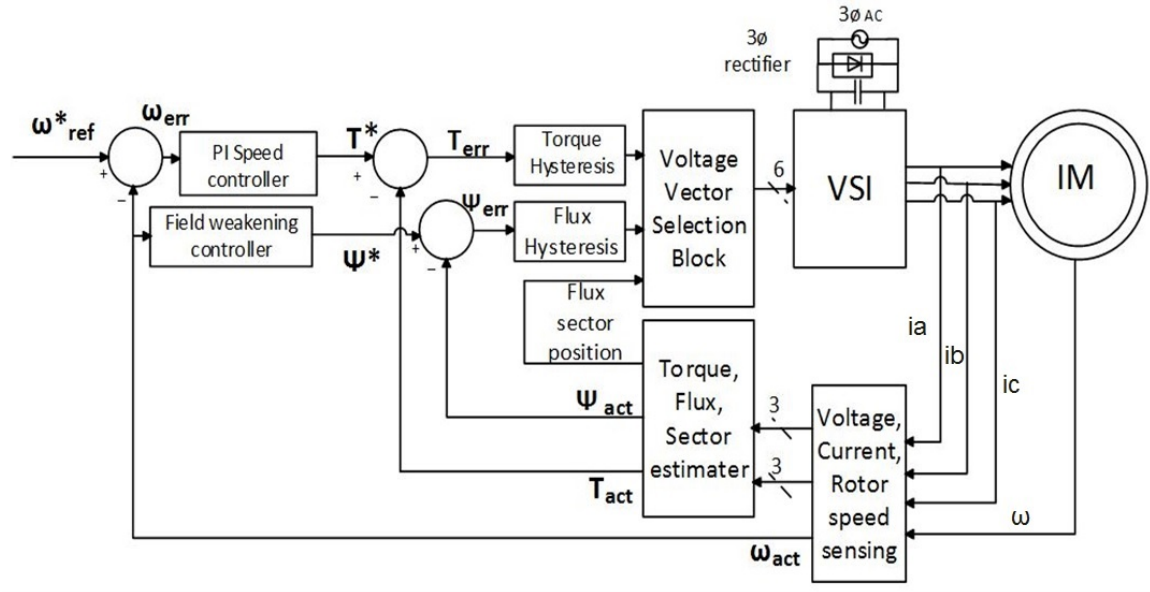


Figure 3.2 DTC Scheme for an induction motor drive(IMD)

Fig. 3.2 shows the DTC scheme for an IMD. The main building blocks are speed PI controller, torque, flux and field angle calculator, torque and flux hysteresis comparators, optimum voltage vector selection table and the inverter feeding the motor. The idea of DTC is to control stator flux and torque by regulating switching states of inverter. Optimum switching state is selected based on the present sector position of the flux and on output of the flux and torque hysteresis controllers, so as to keep them within the specified limits. Flux and torque are estimated from stator voltages and currents by flux & torque estimators. Rotor speed is compared with reference speed to yield the speed error, which is used to calculate the torque reference using a PI controller. Flux reference is calculated from field weakening controller for above rated speeds. Estimated and reference values are compared and error values are given to hysteresis controllers. Optimum voltage vector is selected from switching table based on output signals from the flux and torque hysteresis controllers and sector position of flux. Various blocks in Fig. 3.2 are explained as follows:

A. PI speed controller and Field weakening controller

The PI speed controller processes the speed error with proportional and integral constants and gives electromagnetic torque reference as output.

$$\tau_e = \left(k_p + \int k_i \right) \times \text{Speed error} \quad (3.1)$$

$$\Psi_{ref} = L_m \times I_m = \frac{V_{ph}}{2\pi f} \quad (3.2)$$

where ψ_{ref} is reference flux linkage,

V_{ph} is phase voltage,

L_m is the per-phase magnetizing inductance,

I_m is the per-phase magnetizing current.

For speeds below rated speed,

$$\psi = \psi_{ref} \quad (3.3)$$

But for speeds above rated speed, field weakening happens and

$$\psi = \psi_{ref} \times \frac{\text{ratedspeed}}{\text{newspeed}} \quad (3.4)$$

B. Torque and flux estimator

d-q transformation for stationary reference frame is applied to ABC (three-phase) voltages and currents.

Direct and quadrature axes components of currents and voltages are:

$$v_{qs} = \frac{2}{3} (v_a - 0.5v_b - 0.5v_c) \quad (3.5)$$

$$v_{ds} = \frac{1}{\sqrt{3}} (v_c - v_b) \quad (3.6)$$

$$i_{qs} = \frac{2}{3} (i_a - 0.5i_b - 0.5i_c) \quad (3.7)$$

$$i_{ds} = \frac{1}{\sqrt{3}} (i_c - i_b) \quad (3.8)$$

where v_a, v_b, v_c are stator phase voltages and i_a, i_b, i_c are stator phase currents. Stator flux, torque and angle of flux are estimated using these d and q values. Direct and quadrature axes components of flux are:

$$\psi_{ds} = \int (v_{ds} - i_{ds} \times R) dt \quad (3.9)$$

$$\psi_{qs} = \int (v_{qs} - i_{qs} \times R) dt \quad (3.10)$$

$$\psi_{actual} = \psi_{ds} + j\psi_{qs} \quad (3.11)$$

where R is the stator winding (per-phase) resistance. Estimated flux magnitude and position are given by:

$$|\psi| = \sqrt{\psi_{ds}^2 + \psi_{qs}^2} \quad (3.12)$$

and flux position $\alpha = \tan^{-1} \left(\frac{\psi_{qs}}{\psi_{ds}} \right)$

Electromagnetic torque developed by induction motor is obtained as:

$$\tau_e = \frac{3p}{2} (\psi_{ds} i_{qs} - \psi_{qs} i_{ds}) \quad (3.13)$$

where, p is the number of poles

C. PI speed controller

This block processes the error between the reference speed and actual speed and arrives at the reference torque so that appropriate rate of change of speed is arrived at. This torque will nullify the speed error eventually. k_p and k_i values have been chosen by trial and error.

D. Hysteresis Controller

Actual flux and torque values computed by the flux & torque estimators are compared with their reference values set by the field weakening controller and PI speed controller output respectively. These errors are fed to the respective hysteresis controllers. Flux controller is of two level type and torque controller is of three-levels. Flux and torque errors are given by:

$$\psi_{err} = \psi_{ref} - \psi_{estimated} \quad (3.14)$$

$$\tau_{err} = \tau_{ref} - \tau_{estimated} \quad (3.15)$$

The output of the flux hysteresis controller is,

$$\text{For } \psi_{err} > \frac{f_{HBW}}{2}; H_\psi = 1 \quad (3.16)$$

$$\text{For } \psi_{err} < -\frac{f_{HBW}}{2}; H_\psi = -1 \quad (3.17)$$

where, f_{HBW} is flux hysteresis band width and H_ψ is the flux hysteresis controller output. The output of the torque hysteresis controller is,

$$\text{For } \tau_{err} > \frac{\tau_{HBW}}{2}; H_\tau = 1 \quad (3.18)$$

$$\text{For } \tau_{err} < -\frac{\tau_{HBW}}{2}; H_\tau = -1 \quad (3.19)$$

$$\text{For } -\frac{\tau_{HBW}}{2} < \tau_{err} < \frac{\tau_{HBW}}{2}; H_\tau = 0 \quad (3.20)$$

where τ_{HBW} and H_τ are torque hysteresis band width and the controller output respectively.

E. Voltage Vector Selection

From the outputs of the flux and torque hysteresis controllers and the sector position of the flux vector, a specific voltage vector is chosen such that both flux and torque errors will be nullified. The voltage vector selection table is a look-up table for the selection of an appropriate voltage vector depending upon the torque & flux hysteresis controller outputs and the sector position of the flux linkage vector. If zero voltage is to be applied (as the errors are zero), V_0 and V_7 may be used as the switching vectors.

3.2.2 Predictive Torque Control (PTC)

The same procedure adopted for DTC is followed in PTC [110] except that the prediction of the future behaviour of the system is considered, which means future (predicted) values of stator flux and torque are calculated. Predictions are made for every exciting function possible (due to different switching combinations in the inverter) and the reference tracking is improved by selecting the switching vector for which the error is minimum. Block diagram of PTC is shown in Fig. 3.3.

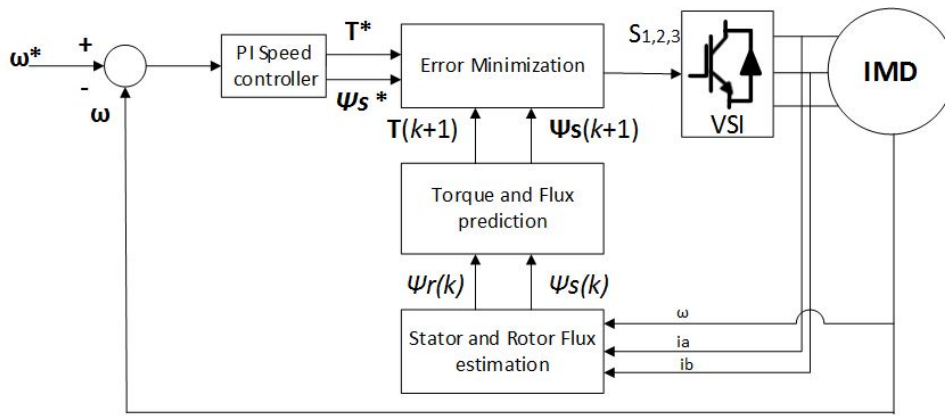


Figure 3.3 Block diagram of PTC scheme

The stator currents (i_a, i_b, i_c) of an IMD defined in three-phase coordinates are as follows:

$$i_a = I \cdot \sin(\omega_0 t) \quad (3.21)$$

$$i_b = I \cdot \sin\left(\omega_0 t + \frac{2\pi}{3}\right) \quad (3.22)$$

$$i_c = I \cdot \sin\left(\omega_0 t + \frac{4\pi}{3}\right) \quad (3.23)$$

where ω_0 is the angular frequency, “I” is the peak of the input current of the IMD. The transformation of the stator currents from three phase to two phase are described as:

$$i_s = \frac{2}{3} (i_a + \mathbf{a}i_b + \mathbf{a}^2i_c) \quad (3.24)$$

where “ i_s ” is stator current space phasor, $\mathbf{a} = e^{j\frac{2\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$, $\mathbf{a}^2 = e^{j\frac{4\pi}{3}} = -\frac{1}{2} - j\frac{\sqrt{3}}{2}$

The *estimation* block calculates the present values of space phasor variables that cannot be measured such as rotor flux (ψ_r), stator flux (ψ_s) and stator current (i_s), using the sensed values of a- and b-phase stator currents (i_a, i_b). The estimation of stator flux depends on the stator voltage (v_s) equation.

$$v_s = R_s i_s + \frac{d\psi_s}{dt} \quad (3.25)$$

After discretization of eq. 3.25 using Euler’s formula, estimated value of stator flux at k^{th} instant for a sampling time of T_s is obtained as:

$$\hat{\psi}_s(k) = \hat{\psi}_s(k-1) + T_s V_s(k) - R_s T_s i_s(k) \quad (3.26)$$

Similarly, the rotor flux estimation can be derived from the rotor flux linkage equations as:

$$\psi_r = i_s L_m + i_r L_r \quad (3.27)$$

From eq. 3.27,

$$i_r = \frac{\psi_r - i_s L_m}{L_r} \quad (3.28)$$

The stator flux linkage equation is:

$$\psi_s = i_s L_s + i_r L_m \quad (3.29)$$

Substituting eq. 3.28 in eq. 3.29, the rotor flux can be re-written as:

$$\hat{\psi}_r = \frac{L_r}{L_m} \hat{\psi}_s + i_s \left(L_m - \frac{L_r L_s}{L_m} \right) \quad (3.30)$$

Thus, by discretizing eq. 3.30, the rotor flux can be estimated based on the present value of the stator flux ($\hat{\psi}_s(k)$) as:

$$\hat{\psi}_r(k) = \frac{L_r}{L_m} \hat{\psi}_s(k) + i_s(k) \left(L_m - \frac{L_r L_s}{L_m} \right) \quad (3.31)$$

The *estimation stage* is completed by estimating stator and rotor flux at k^{th} instant using eq. 3.26 and eq. 3.31. In PTC, during second stage, the *predictions* for the controlled variables i.e. electromagnetic torque (T) and stator flux (ψ_s) are computed for the next sampling i.e., $(k+1)^{th}$ instant. Prediction for stator flux ($\psi_s^p(k+1)$) and Torque ($T^p(k+1)$) are obtained as:

$$\psi_s^p(k+1) = \widehat{\psi}_s(k) + T_s V_s(k) - R_s T_s i_s(k) \quad (3.32)$$

$$T^p(k+1) = \frac{3p}{2} \mathcal{I}m \left\{ \overline{\psi}_s^p(k+1) i_s^p(k+1) \right\} \quad (3.33)$$

The torque prediction totally depends on the predicted stator current and flux. According to [111] and [112], the equations of the rotor and stator dynamics of an IMD (squirrel-cage type) are:

$$i_s + \tau_\sigma \frac{di_s}{dt} = -j\omega_k \tau_\sigma i_s + \frac{k_r}{R_\sigma} \left(\frac{1}{\tau_r} - j\omega \right) \psi_r + \frac{V_s}{R_\sigma} \quad (3.34)$$

where $k_r = \frac{L_m}{L_r}$, $R_\sigma = R_s + R_r k_r^2$, $\tau_\sigma = \left(1 - \frac{L_m^2}{L_s L_r}\right) \frac{L_s}{R_\sigma}$ and $\tau_r = \frac{L_r}{R_r}$ (whose values are mentioned in the A.2)).

After discretization of eq. 3.34 based on Euler's approximation, the obtained value of predicted stator current ($i_s^p(k+1)$) is:

$$i_s^p(k+1) = \left(1 + \frac{T_s}{\tau_\sigma}\right) i_s(k) + \frac{T_s}{\tau_\sigma + T_s} \left\{ \frac{1}{R_\sigma} \left[\left(\frac{k_r}{\tau_r} - k_r j\omega \right) \widehat{\psi}_r(k) + V_s(k) \right] \right\} \quad (3.35)$$

Prediction of stator flux (eq. 3.32) and stator current (eq. 3.35) are used to calculate the torque prediction (eq. 3.33). Both the stator flux and torque prediction are written in terms of inverter voltage ($V_s(k)$).

The *error minimization* is the third and last stage. The error (ϵ_h) is the difference between the predicted and reference values of controlled variables. Basically, the predictions of the controlled variables (stator flux, torque and stator current) are obtained for every possible value of ($V_s(k)$) at $(k+1)^{th}$ instant. Also, the error function is evaluated for every prediction and finally, that switching state is selected for which the error is minimum. Based on this process, the firing pulses are generated and applied to inverter.

$$\epsilon_h = |T^* - T^p(k+1)_h| + \lambda_\psi |\psi_s^* - \psi_s^p(k+1)_h| \quad (3.36)$$

where $h \in [0, 1, \dots, 6]$ in case of two level and $[0, 1, \dots, 18]$ in case of three level. Weighting factor (λ_ψ) is chosen as the ratio of nominal torque to nominal stator flux.

3.2.3 Power quality improvement and DPC

A block diagram of the proposed technique is represented in Fig. 3.4. First the three-phase balanced voltages and line currents are converted into two-phase form by making use of Clarke's transformation [113].

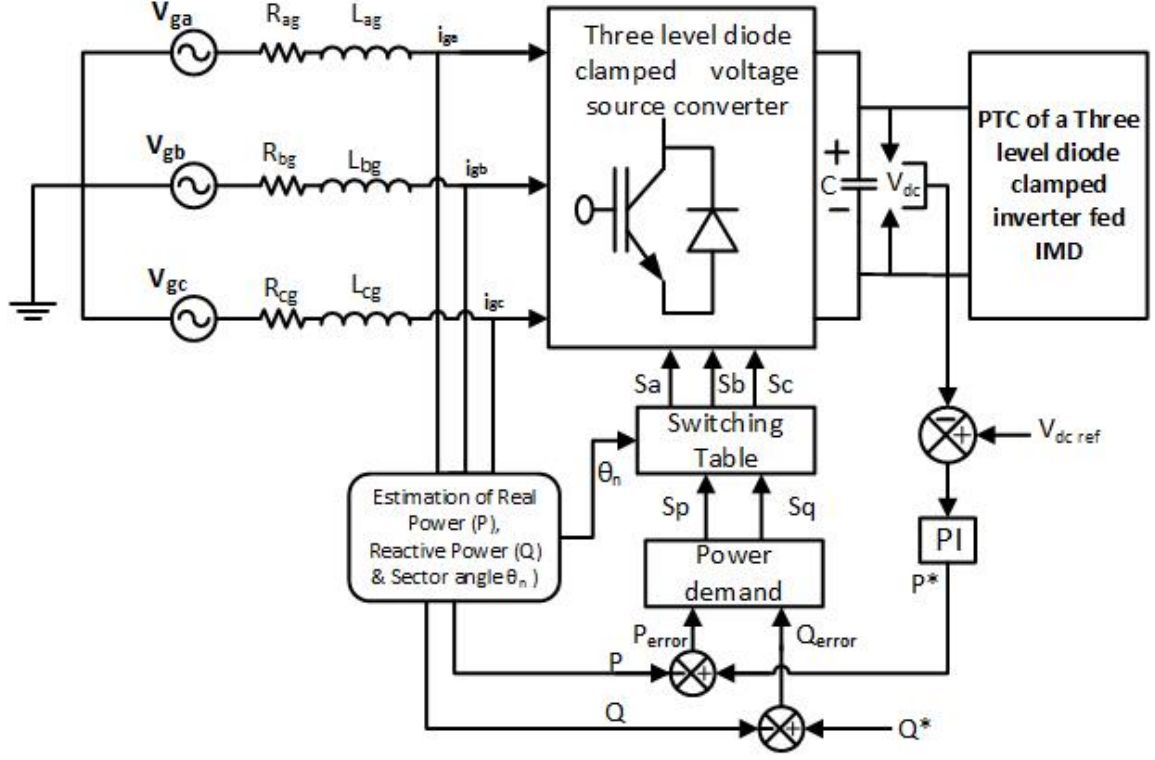


Figure 3.4 Block diagram of Modelling of the proposed DPC for a back-to-back connected multilevel converter fed IMD

$$\begin{bmatrix} \hat{V}_a \\ \hat{V}_b \\ \hat{V}_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \hat{v}_\alpha \\ \hat{v}_\beta \end{bmatrix} \quad (3.37)$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \mathbf{i}_a \\ \mathbf{i}_b \\ \mathbf{i}_c \end{bmatrix} \quad (3.38)$$

where V_a, V_b, V_c are three phase power source voltages and $\mathbf{i}_a, \mathbf{i}_b, \mathbf{i}_c$ are three phase line currents. The instantaneous real power and reactive power can be calculated from these transformed voltages and currents as [114]:

$$p = v_\alpha i_\alpha + v_\beta i_\beta \quad (3.39)$$

and

$$q = v_\alpha i_\beta - v_\beta i_\alpha \quad (3.40)$$

The real power and reactive power thus calculated could be compared with the reference values of real power and reactive power obtained from the error in the DC link capacitor voltage and the set value

of Q respectively, in a hysteresis comparator [115] whose rules are given below:

$$S_p = \begin{cases} 1 & \Delta p \in (h_p, +\infty) \\ 0 & \Delta p \in (-\infty, -h_p) \end{cases} \quad (3.41)$$

$$S_q = \begin{cases} 1 & \Delta q \in (h_q, +\infty) \\ 0 & \Delta q \in (-\infty, -h_q) \end{cases} \quad (3.42)$$

The virtual flux vector position of the source voltages is calculated as follows: Neglecting resistances of all the components involved, flux vector along alpha axis and beta axis are given by:

$$\psi_\alpha = \int v_\alpha dt \quad (3.43)$$

$$\psi_\beta = \int v_\beta dt \quad (3.44)$$

Angular position and magnitude of the flux space vector is given by:

$$\theta = \tan^{-1}\left(\frac{\psi_\beta}{\psi_\alpha}\right) \quad (3.45)$$

$$\psi = \sqrt{\psi_\alpha^2 + \psi_\beta^2} \quad (3.46)$$

3.2.4 FPGA based implementation

This section discusses the implementation of this IMD in hardware. Field programmable gate array (FPGA) has been used as an interfacing device between the software/drive controllers and the hardware. A three-level diode clamped inverter fed 5hp IMD has been setup as a laboratory prototype. A novel PTC algorithm with optimal voltage vector selection is realized on a single FPGA chip (from Xilinx Inc.) to generate controlling gate pulses for the multilevel inverter devices. The details of the experimental set-up are explained in *Chapter 6*.

3.3 Conclusions

In this chapter, the configuration of the system taken up for analysis in this dissertation has been presented in detail. Initially, each of the components in the drive system is explained. After that, the concept of classical DTC for an IMD has been elucidated with the corresponding mathematical equations and the issues related to DTC have been described. This naturally leads to another emancipated control

methodology known as PTC. The concept of PTC has been explained for both 2-level and three-level inverter cases. Subsequently, direct power control for improving the input power quality of the inverter fed IMD has been taken up. Finally, FPGA based implementation has been touched upon which would be described in detail in *Chapter 6*. The next chapter will be presenting the modeling and simulation aspects of the inverter fed IMDs.

Chapter 4

Modelling and Simulation

4.1 Introduction

The modelling and simulation is an important stage, where the performance of a system is evaluated without actually building the system. In this Chapter, simulation aspects of the proposed drive system are presented. Multilevel inverter fed IMD is modelled and simulated in MATLAB/SIMULINK environment using various control strategies. The proposed DTC, PTC and DPC algorithms are implemented for three level diode clamped converter fed IMD. These novel control algorithms have been analyzed for different load conditions, transient and steady state operations.

4.2 Modelling of Classical DTC with Two-level Inverter

A two-level inverter is shown in Fig. 4.1 where three switches conduct at a time. No two switches on the same leg are closed concurrently. When a device connected to the positive terminal of the DC supply is closed, that phase is designated to have a '1' state, when the device connected to the negative terminal of the DC source is closed, it has a '0' state. For example, consider switching state '110' where Q1, Q3 and Q6 conduct resulting in a resultant voltage space vector V_2 . The next switching state of Q2, Q3 and Q6 being ON, results in a voltage vector shifted by 60° , i.e., V_3 . Every switch combination results in a distinct voltage space phasor as shown in Fig. 4.2 as specified in voltage vector selection table (Table 4.1). The 360° space is divided into 6 sectors, each subtending a 60° angle as depicted in Fig. 4.2.

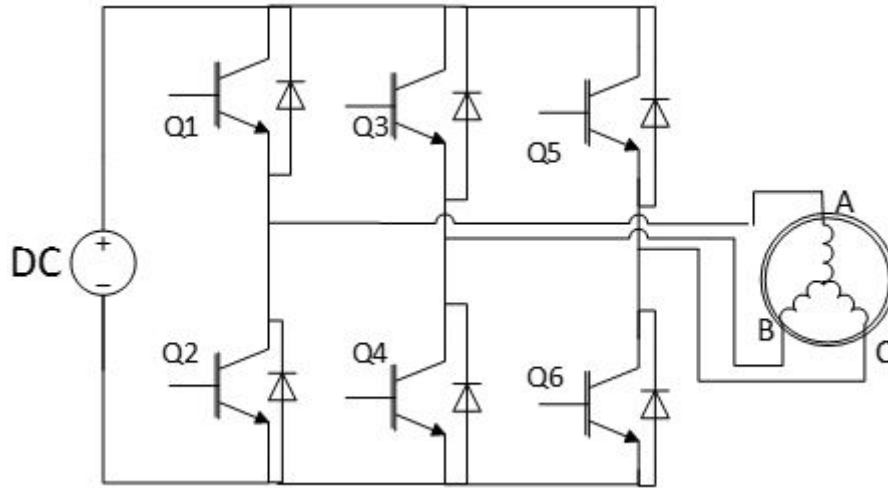


Figure 4.1 Two level inverter circuit

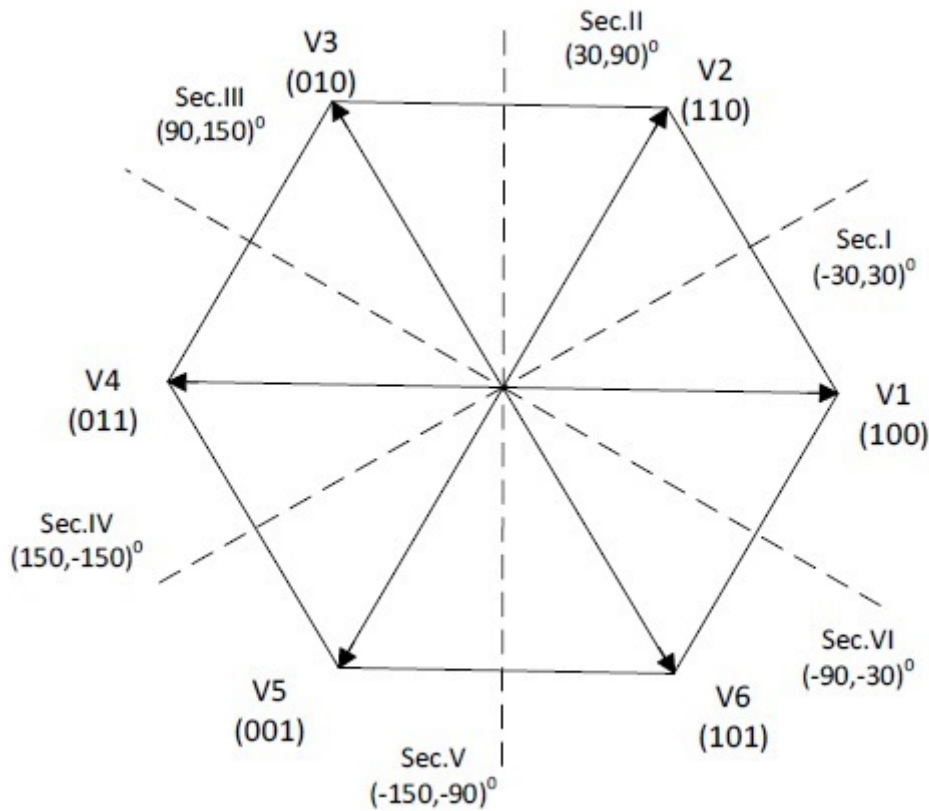


Figure 4.2 Voltage vectors for two level inverter

4.3 Modelling of Classical DTC with Three level Inverter

A. Inverter Operation

A three-level diode clamped inverter circuit is shown in Fig. 4.3 which consists of 12 switches (four per

Table 4.1 Switching table for Two level inverter

ψ_{hys}	\mathbf{T}_{hys}	Sector	Sector	Sector	Sector	Sector	Sector
		I	II	III	IV	V	VI
1	1	V_2 (110)	V_3 (010)	V_4 (011)	V_5 (001)	V_6 (101)	V_1 (100)
	0	V_7 (111)	V_0 (000)	V_7 (111)	V_0 (000)	V_7 (111)	V_0 (000)
	-1	V_6 (101)	V_1 (100)	V_2 (110)	V_3 (010)	V_4 (011)	V_5 (001)
-1	1	V_3 (010)	V_4 (011)	V_5 (001)	V_6 (101)	V_1 (100)	V_2 (110)
	0	V_0 (000)	V_7 (111)	V_0 (000)	V_7 (111)	V_0 (000)	V_7 (111)
	-1	V_5 (001)	V_6 (101)	V_1 (100)	V_2 (110)	V_3 (010)	V_4 (011)

leg). In a two level inverter, the voltage space phasor that can be applied to the stator of the induction motor can only be V_0 to V_7 . This is because any particular line voltage can have values of $+V$ or $-V$. In case of three-level inverters, phase voltages can be $+V$, 0 or $-V$. So 12 non-zero vectors are present for the operation of DTC. For the same case of torque and flux errors, with a three-level inverter, more options (to be precise-two options) are available whereas with the two-level inverter has a very limited choice. To decide between the two options in the three-level inverter, number of specified ranges in torque hysteresis controller is increased to 5, namely, $\tau_e > \tau_{HBW}$, $\tau_{HBW} > \tau_e > \frac{\tau_{HBW}}{2}$, $\frac{\tau_{HBW}}{2} > \tau_e > \frac{-\tau_{HBW}}{2}$, $\frac{-\tau_{HBW}}{2} > \tau_e > -\tau_{HBW}$ and $\tau_e < -\tau_{HBW}$; but, the number of bands in the flux hysteresis controller is kept the same.

B. Hysteresis controller

The working of the hysteresis controller is same as that of the two level DTC case. Flux hysteresis controller remains the same, but the number of levels of torque hysteresis controller has changed due to increased number of vectors. Output of torque hysteresis controller is:

$$\text{For } \tau_e > \frac{\tau_{HBW}}{2}; \quad H_\tau = 2 \quad (4.1)$$

$$\text{For } \frac{\tau_{HBW}}{2} < \tau_e < \frac{\tau_{HBW}}{2}; \quad H_\tau = 1 \quad (4.2)$$

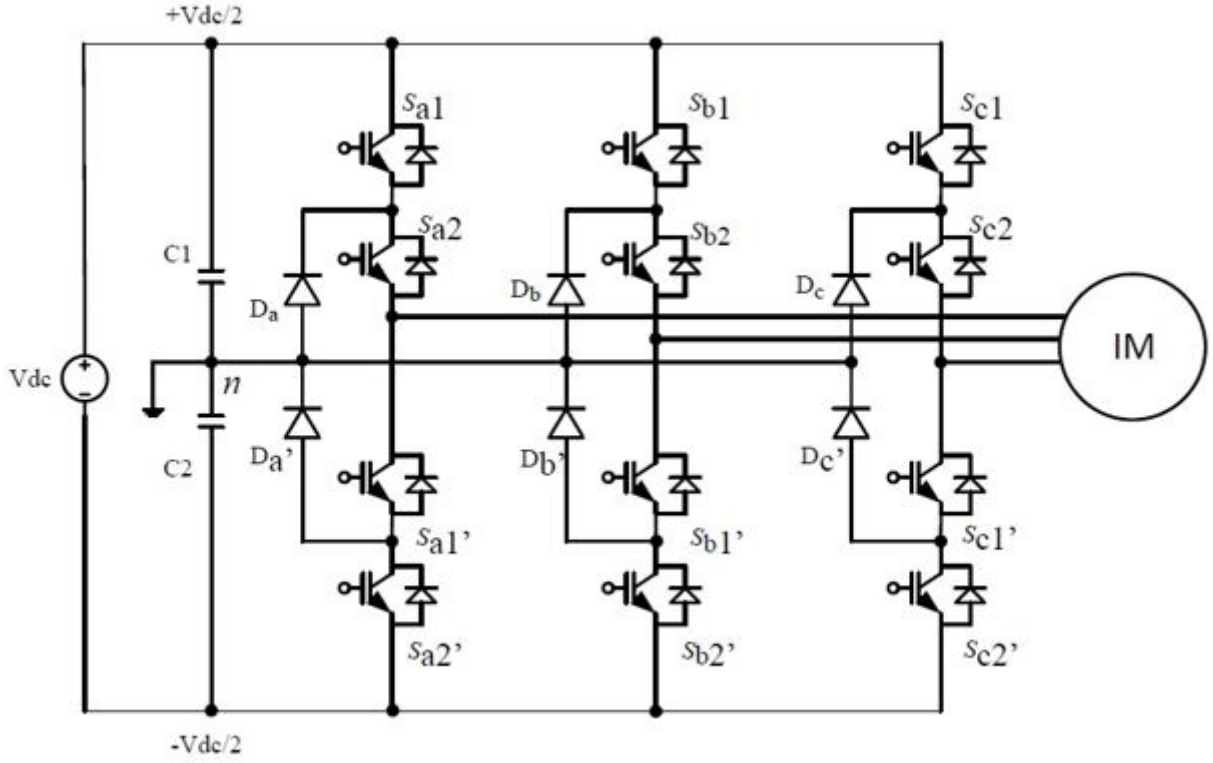


Figure 4.3 Three level diode clamped inverter circuit

$$\text{For } -\frac{\tau_{HBW}}{2} < \tau_e < \frac{\tau_{HBW}}{2}; \quad H_\tau = 0 \quad (4.3)$$

$$\text{For } -\tau_{HBW} < \tau_e < -\frac{\tau_{HBW}}{2}; \quad H_\tau = -1 \quad (4.4)$$

$$\text{For } \tau_e < \frac{-\tau_{HBW}}{2}; \quad H_\tau = -2 \quad (4.5)$$

C. Switching Table

The operation of the switching table in the three-level case is similar to that of the two level DTC except that there are a total of 12 vectors. The 360° space into 12 sectors each of 30° span. Six longer voltage vectors are the diagonals of the hexagon; the bisector of these angles between two adjacent diagonals are the other smaller voltage vectors as shown in Fig. 4.4. The optimum vector is selected depending on the output of the 2-level flux hysteresis controller and the 5-level torque hysteresis controller. Suppose the flux is in i^{th} sector currently, then voltage vectors $V_{(i+1)}$, V_{i+2} , V_{i+4} , V_{i+5} are capable of increasing the torque; but former two voltage vectors increase the flux, while latter two decrease the flux. V_{i-1} , V_{i-2} , V_{i-4} , V_{i-5} decrease torque; among these, the first two increase the flux, while latter two decrease the flux. Table for voltage vector selection, when the flux lying in any ' i^{th} ' sector (' i ' varying from 1 to 12) is tabulated in Table 4.2.

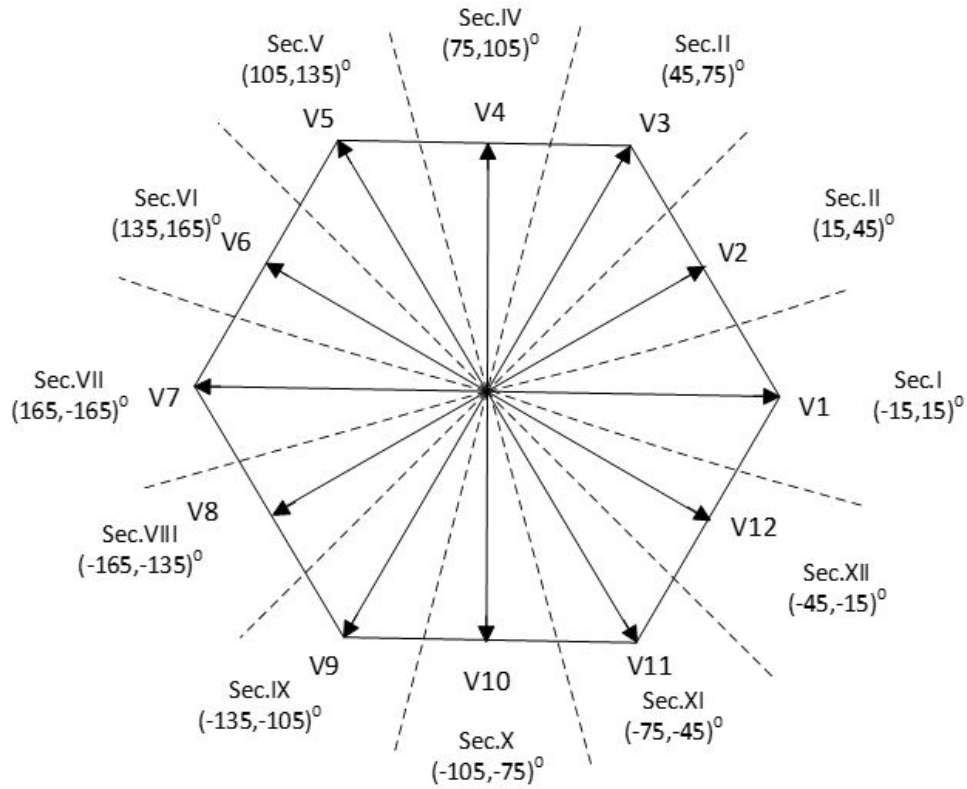


Figure 4.4 Voltage vectors for three level inverter

4.4 DTC with reduced switch Three-level inverter

A. Inverter operation

A three-phase three-level nine switch VSI [10] as shown in Fig. 4.5 is modelled for simulation. This topology consists of three bidirectional switches inserted between the source and the full-bridge power switches of the classical three-phase VSI. The 12 phasors which are the outputs of the three-level VSI are implemented by various switch combinations. They are as shown in Table 4.3. For example, one can obtain V_4 by having a switching combination of S1, Q3 and Q6 in ON state. The circuit configuration pertaining to V_4 is shown in Fig. 4.6. The effect of applying V_4 when the flux linkage is in sector 1, is represented in Fig. 4.7.

Table 4.2 Switching table for Three level Diode Clamped Inverter

S E C T O R	ψ_{hys} (Flux Hysteresis)									
	1					-1				
	T_{hys} (Torque Hysteresis)									
	2	1	0	-1	-2	2	1	0	-1	-2
1	V_3	V_2	V_0	V_{12}	V_{11}	V_5	V_6	V_0	V_8	V_9
2	V_4	V_3	V_0	V_1	V_{12}	V_6	V_7	V_0	V_9	V_{10}
3	V_5	V_4	V_0	V_2	V_1	V_7	V_8	V_0	V_{10}	V_{11}
4	V_6	V_5	V_0	V_3	V_2	V_8	V_9	V_0	V_{11}	V_{12}
5	V_7	V_6	V_0	V_4	V_3	V_9	V_{10}	V_0	V_{12}	V_1
6	V_8	V_7	V_0	V_5	V_4	V_{10}	V_{11}	V_0	V_1	V_2
7	V_9	V_8	V_0	V_6	V_5	V_{11}	V_{12}	V_0	V_2	V_3
8	V_{10}	V_9	V_0	V_7	V_6	V_{12}	V_1	V_0	V_3	V_4
9	V_{11}	V_{10}	V_0	V_8	V_7	V_1	V_2	V_0	V_4	V_5
10	V_{12}	V_{11}	V_0	V_9	V_8	V_2	V_3	V_0	V_5	V_6
11	V_1	V_{12}	V_0	V_{10}	V_9	V_3	V_4	V_0	V_6	V_7
12	V_2	V_1	V_0	V_{11}	V_{10}	V_4	V_5	V_0	V_7	V_8

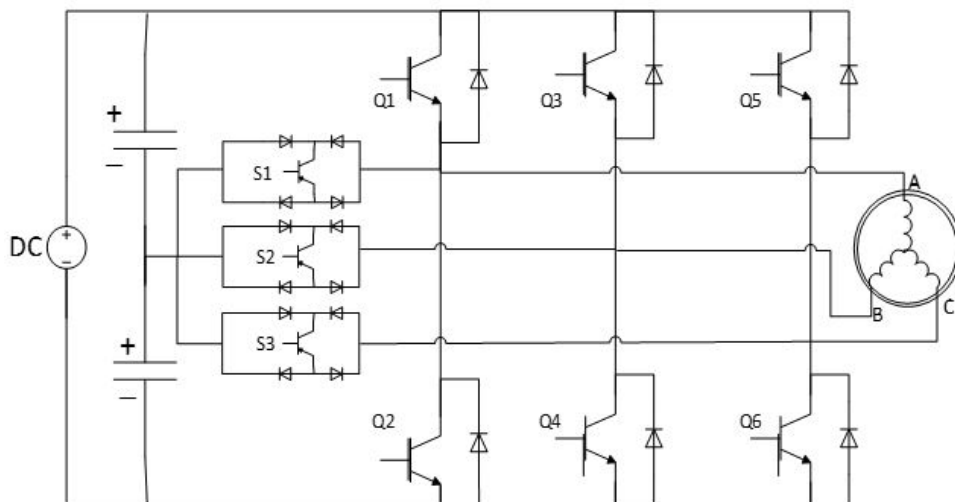


Figure 4.5 Implementation of Three level reduced switch diode clamped inverter circuit

Table 4.3 Gate Signals for different Voltage Vectors for the Three level Reduced Switch Diode Clamped Inverter

States	Switches								
	Q1	Q2	Q3	Q4	Q5	Q6	S1	S2	S3
V_0	1	0	1	0	1	0	0	0	0
V_1	1	0	0	1	0	1	0	0	0
V_2	1	0	0	0	0	1	0	1	0
V_3	1	0	1	0	0	1	0	0	0
V_4	0	0	1	0	0	1	1	0	0
V_5	0	1	1	0	0	1	0	0	0
V_6	0	1	1	0	0	0	0	0	1
V_7	0	1	1	0	1	0	0	0	0
V_8	0	1	0	0	1	0	0	1	0
V_9	0	1	0	1	1	0	0	0	0
V_{10}	0	0	0	1	1	0	1	0	0
V_{11}	1	0	0	1	1	0	0	0	0
V_{12}	1	0	0	1	0	0	0	0	1

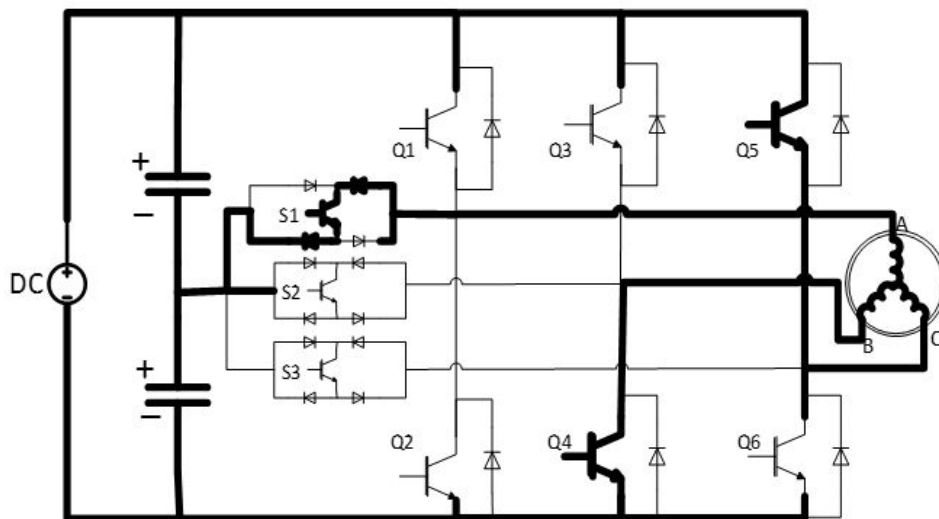


Figure 4.6 Circuit diagram for voltage vector V_4

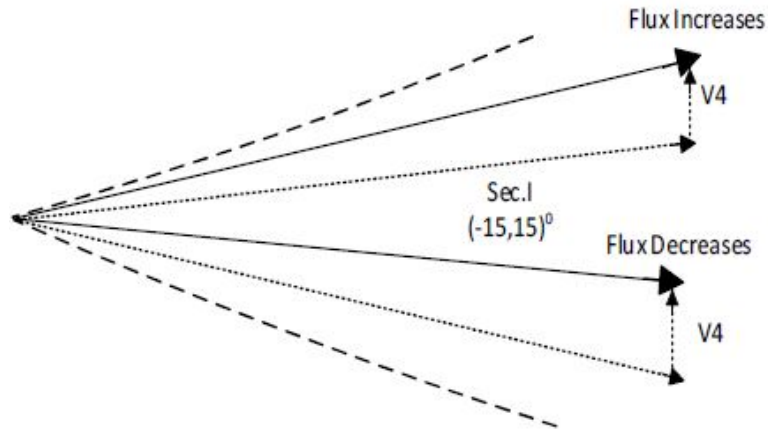


Figure 4.7 Operation of vector V_4 for flux in sector 1

4.5 PTC

The main feature of PTC is to predict the future values of torque and stator flux and compare them with the existing conditions, thus controlling the future behavior of the system [110]. Predictions are calculated for every possible switching combination of the inverter. The reference tracking is improved by the voltage vector selected using error minimization function. The block diagram of PTC is shown in Fig. 3.3 which involves three main stages: *estimation* of variables, *prediction* of future values of the controlled variables and *optimization* of present output depending on future error.

Eight switching states and seven voltage vectors are possible for a two level inverter (Fig. 4.1) as shown in Table 4.4, in which two vectors V_0 and V_7 give the same zero voltage output. The predicted values of flux, current and torque are calculated for every possible inverter voltage (V_s).

Table 4.4 Switching States and Voltage Vectors for Two level Inverter

Switching States	Voltage Vectors
000	V_0
100	V_1
110	V_2
010	V_3
011	V_4
001	V_5
101	V_6
111	V_7

Seven predictions for flux, current and torque are obtained i.e. $(i_s^p(k+1), \psi_s^p(k+1), T^p(k+1))_h$, $h \in [0, 1, \dots, 6]$. The error minimization function (eq. 3.36) is evaluated for every prediction and the one that produces the minimum error is selected as the switching state. It must be highlighted that there are two ways of applying a zero vector (either 111 or 000). Therefore, if the zero vector combination nearest to the previous switching combination is applied, the number of switchings can be reduced. This logic is shown in Table 4.5 where it can be observed that the vector V_0 is selected if the previous vector is close to it (i.e., V_0, V_1, V_3 , and V_5) and V_7 is selected otherwise. On the other hand, vector V_7 is selected if the previous vector is close to vectors V_2, V_4, V_6 , and V_7) and V_0 is selected otherwise. Hence, whenever a zero vector has to be applied, the algorithm selects either V_0 or V_7 whichever is attainable with minimum change of states of the switches, thus minimizing the switching losses. Finally, the selected switching states are given out to the inverter devices for successful operation.

Table 4.5 Proposed Zero Vector Selection logic table for Two level Inverter

Present Zero Vector to be applied	Previous Voltage Vector
V_0	V_0, V_1, V_3, V_5
V_7	V_2, V_4, V_6, V_7

In a three-level inverter case, there are three ways of applying zero vector (switch combinations: 000, 111 and 222) in the proposed PTC algorithm. Redundant states are observed for some other non-zero voltage vectors as well (example V_{14} and V_{22} , V_{13} and V_{21} etc.) as observed in space vector diagram of a three level inverter (Fig. 4.8) and switching states in Table 4.6. The three zero vector options namely are V_0, V_{19} and V_{20} . Table 4.7 presents the logic where it can be observed that, at $(k+1)^{th}$ instant zero vector V_0 is selected if the previous vector is one of $(V_0, V_1, V_5, V_9, V_{13}, V_{15}, V_{17})$ as this will require the transition of only one of the three-phases. Similarly in the case of non-zero voltage vector with redundant states, (i.e. $V_{13} - V_{21}$, $V_{14} - V_{22}$, $V_{15} - V_{23}$, $V_{16} - V_{24}$, $V_{17} - V_{25}$, $V_{18} - V_{26}$), the voltage vector with least number of switching transition is selected. For example, voltage vector V_{21} is selected while considering the redundant vector pair of V_{13} & V_{21} , if the previous vector is one of $(V_2, V_{12}, V_{16}, V_{19}, V_{21}, V_{22}, V_{26})$, as this will require the transition of only one phase switches. The number of switchings during any transition will be reduced, if the voltage vector (especially where there is redundancy) nearest to the previous vector is chosen as per the switching states shown in Table 4.7.

The flowcharts for selecting the efficient voltage vector with minimum switching transitions when zero vector is to be chosen and non-zero vector with redundancy is to be chosen are shown in Figs. 4.9, 4.10 and 4.11, respectively.

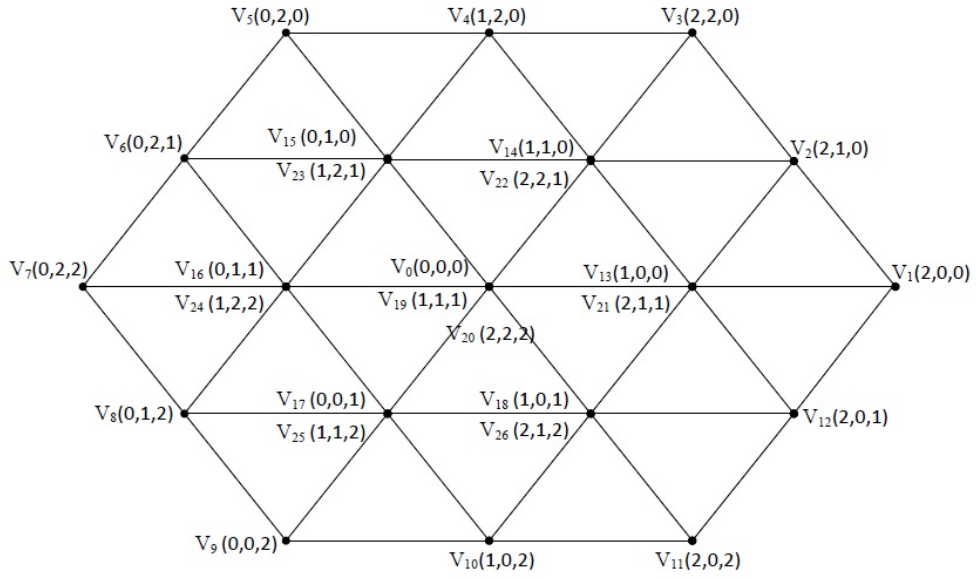


Figure 4.8 Space vector diagram of a Three level inverter

Table 4.6 Switching States and Voltage Vectors for Three level Inverter

Voltage Vector = Switching State		
$V_0 = 000$	$V_{10} = 102$	$V_{20} = 222$
$V_1 = 200$	$V_{11} = 202$	$V_{21} = 211$
$V_2 = 210$	$V_{12} = 201$	$V_{23} = 221$
$V_3 = 220$	$V_{13} = 100$	$V_{24} = 121$
$V_4 = 120$	$V_{14} = 110$	$V_{25} = 122$
$V_5 = 020$	$V_{15} = 010$	$V_{26} = 112$
$V_6 = 021$	$V_{16} = 011$	$V_{27} = 212$
$V_7 = 022$	$V_{17} = 001$	
$V_8 = 012$	$V_{18} = 101$	
$V_9 = 002$	$V_{19} = 111$	

Table 4.7 Proposed $(k + 1)^{th}$ Optimal Voltage Vector selection logic for Three level Diode Clamped Inverter

$(k + 1)^{th}$ vector to be applied	Previous Voltage Vector
V_0	$V_0, V_1, V_5, V_9, V_{13}, V_{15}, V_{17}$
V_{20}	V_3, V_7, V_{11}, V_{20}
V_{19}	$V_{14}, V_{16}, V_{18}, V_{19}$
V_{13}	$V_0, V_1, V_4, V_{10}, V_{13}, V_{14}, V_{18}$
V_{21}	$V_2, V_{12}, V_{16}, V_{19}, V_{21}, V_{22}, V_{26}$
V_{14}	$V_2, V_4, V_{13}, V_{14}, V_{15}, V_{19}, V_{25}$
V_{22}	$V_3, V_6, V_{12}, V_{20}, V_{21}, V_{22}, V_{23}$
V_{15}	$V_0, V_2, V_5, V_8, V_{14}, V_{15}, V_{16}$
V_{23}	$V_4, V_6, V_{18}, V_{19}, V_{22}, V_{23}, V_{24}$
V_{16}	$V_6, V_8, V_{15}, V_{16}, V_{17}, V_{19}, V_{21}$
V_{24}	$V_4, V_7, V_{10}, V_{20}, V_{23}, V_{24}, V_{25}$
V_{17}	$V_0, V_6, V_9, V_{12}, V_{16}, V_{17}, V_{18}$
V_{25}	$V_8, V_{10}, V_{14}, V_{19}, V_{24}, V_{25}, V_{26}$
V_{18}	$V_{10}, V_{12}, V_{13}, V_{17}, V_{18}, V_{19}, V_{23}$
V_{26}	$V_2, V_8, V_{11}, V_{20}, V_{21}, V_{25}, V_{26}$

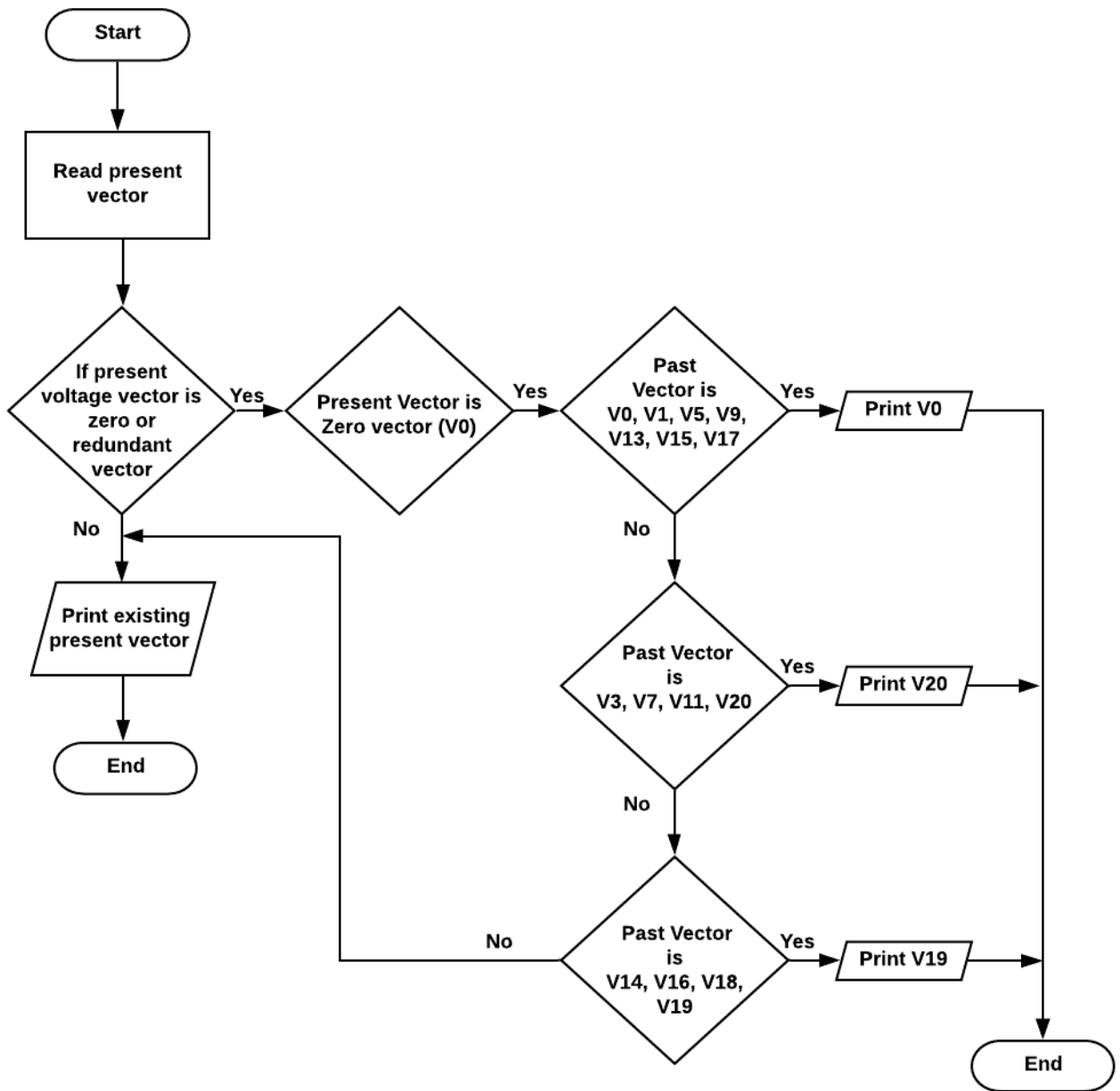


Figure 4.9 Flowchart for selecting the efficient voltage vector with minimum switching when zero vector occurs

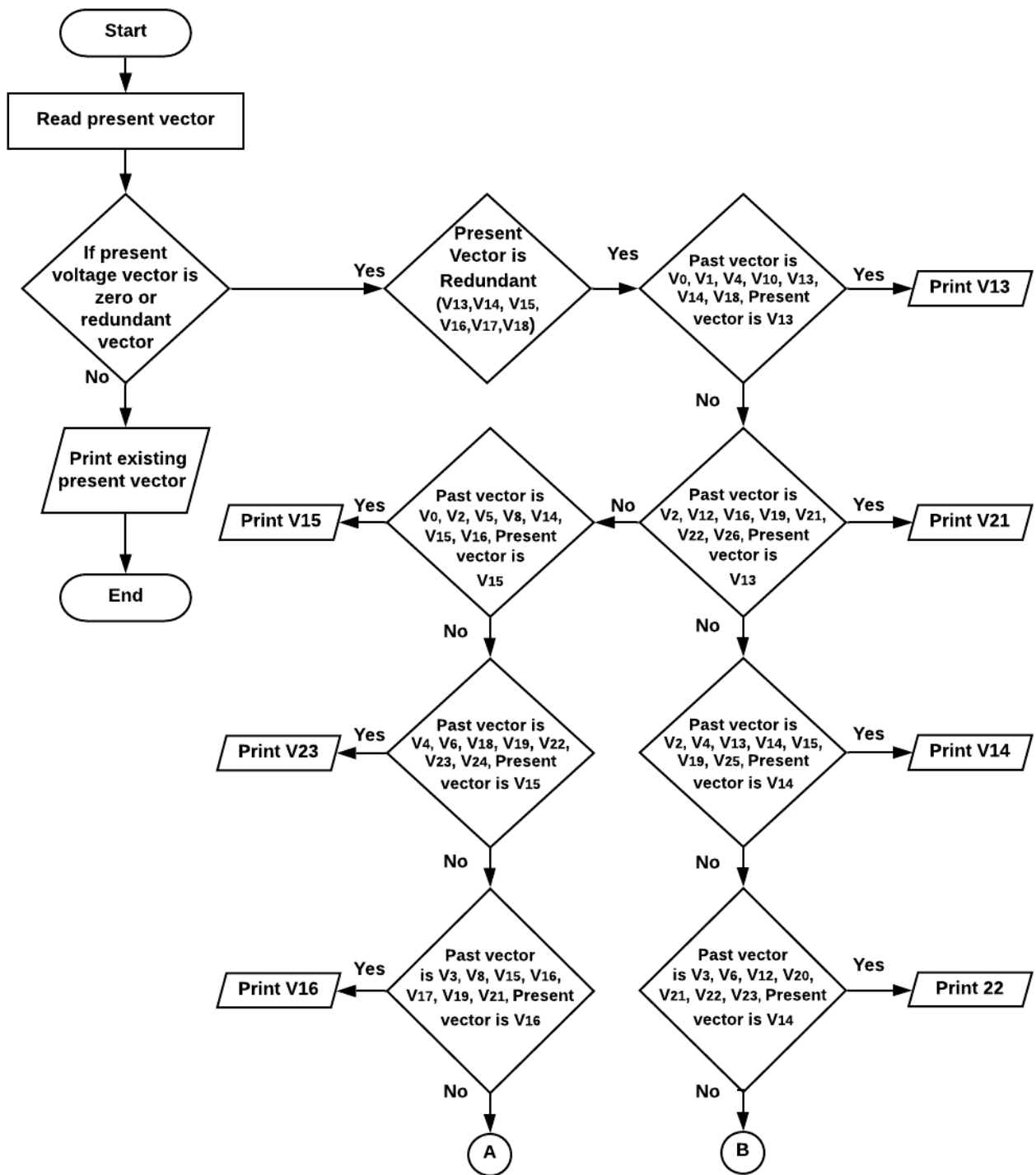


Figure 4.10 Flowchart for selecting the efficient voltage vector with minimum switching when redundant vector occurs-I

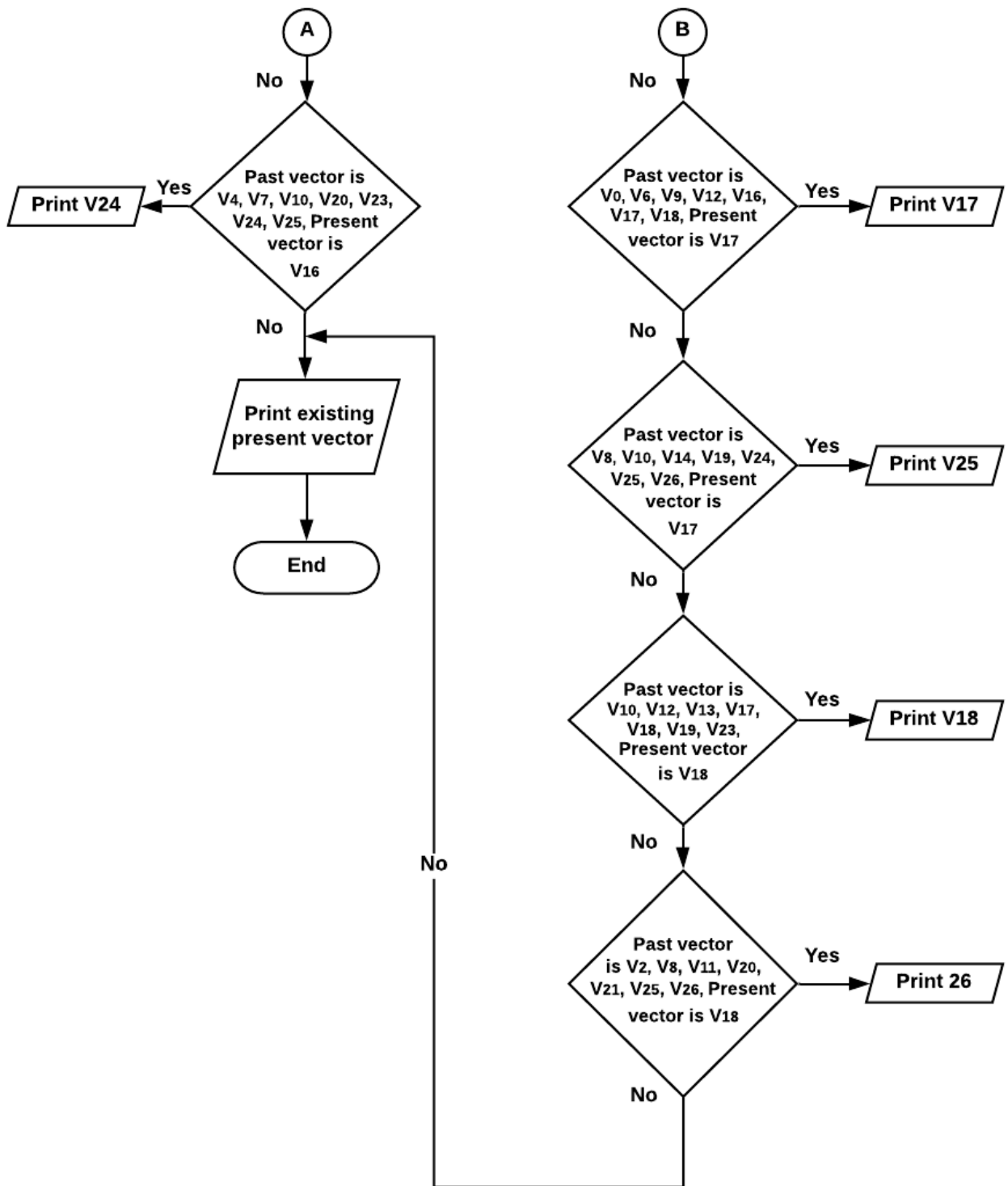


Figure 4.11 Flowchart for selecting the efficient voltage vector with minimum switching when redundant vector occurs-II

4.6 DPC

The proposed DPC technique is applied to a back-to-back connected three level diode clamped converter fed IMD as shown in Fig. 3.4. The converter acts as a rectifier at the front end and as an inverter at the load side. The proposed DPC technique is implemented on the AFE rectifier and PTC is employed for the three level diode clamped inverter feeding the IMD. The estimation of real power (P), reactive power (Q), and sector angle (θ) has been carried out using equations eq. 3.39, 3.40 and 3.45. It is assumed that the values of resistances of the grid i.e. R_{ag} , R_{bg} , R_{cg} are negligibly small and have no voltage drops. The reference active power command (P^*) is provided from the DC bus voltage (V_{dc}) error, while the reactive power command (Q^*) is chosen as per the power factor requirement. In this controller, active power flow governs the DC bus voltage and unity power factor (UPF) is ensured by setting (Q^*) to be zero. The process of error minimization between the reference and actual commands of active and reactive powers is performed in power demand block. For different values of errors in P and Q, and the virtual flux vector position of the source voltages, the switching table for the AFE- VSC is depicted in Table 4.8 (sector positions are specified in Fig. 4.12). If θ calculated from eq. 3.45 is lying within a particular range then, it is supposed to be specified as Sector1, Sector 2 and so on as given by eq. 4.6.

Table 4.8 Switching table for Direct Instantaneous Power Control

Sp	Sq	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
0	0	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}	V_{11}	V_{12}
0	1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}	V_{11}	V_{12}	V_1
1	0	V_{13}	V_{21}	V_{14}	V_{22}	V_{15}	V_{23}	V_{16}	V_{24}	V_{17}	V_{25}	V_{18}	V_{26}
1	1	V_{14}	V_{22}	V_{15}	V_{23}	V_{16}	V_{24}	V_{17}	V_{25}	V_{18}	V_{26}	V_{13}	V_{21}

$$(n - 2)\frac{\pi}{6} \leq \theta_n < (n - 1)\frac{\pi}{6} \quad (4.6)$$

where $n = 1, 2, \dots, 12$. Table 4.8 yields the switching positions of various devices in the AFE rectifier which would make sure that P^* and Q^* values are adhered to within an error margin tolerated by the hysteresis controller. S_a, S_b, S_c are the switching states generated by switching table and further fed to the VSC (as per Table 4.6).

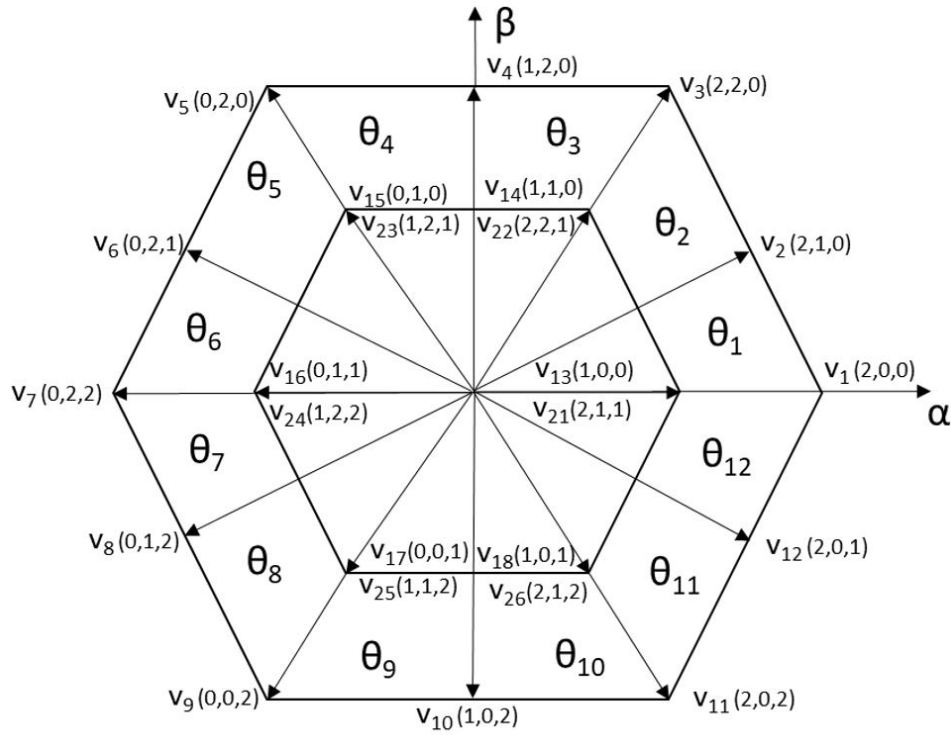


Figure 4.12 Twelve sectors on Stationary reference frame to specify the flux vector position

4.7 Simulation Models

The simulink model representation of DTC two level inverter fed IMD is shown in Fig. 4.13. The two level inverter in the SIMULINK/MATLAB model is designed as per the circuit diagram shown in Fig. 4.1. The error between actual and reference speeds are carried out in the speed controller block which in further produces the reference torque and flux. The control method of direct torque is implemented in DTC block, furtherly the required gates are fed to the two level inverter. In case of three level reduced switch inverter, a nine switched inverter is designed and fed to the IM as shown in Fig. 4.14. The switches block in the sim model represents the design of reduced switches as shown in Fig. 4.15.

The simulink model representation of PTC for inverter fed IMD is shown in Fig. 4.16. The algorithm for zero vector selection/optimal voltage vector selection using PTC in both cases i.e two level and three level inverters are implemented in predictive controller block. Similarly, DPC simulink model representation for AFE rectifier and PTC employed for three level diode clamped inverter fed IMD is shown in Fig. 4.17.

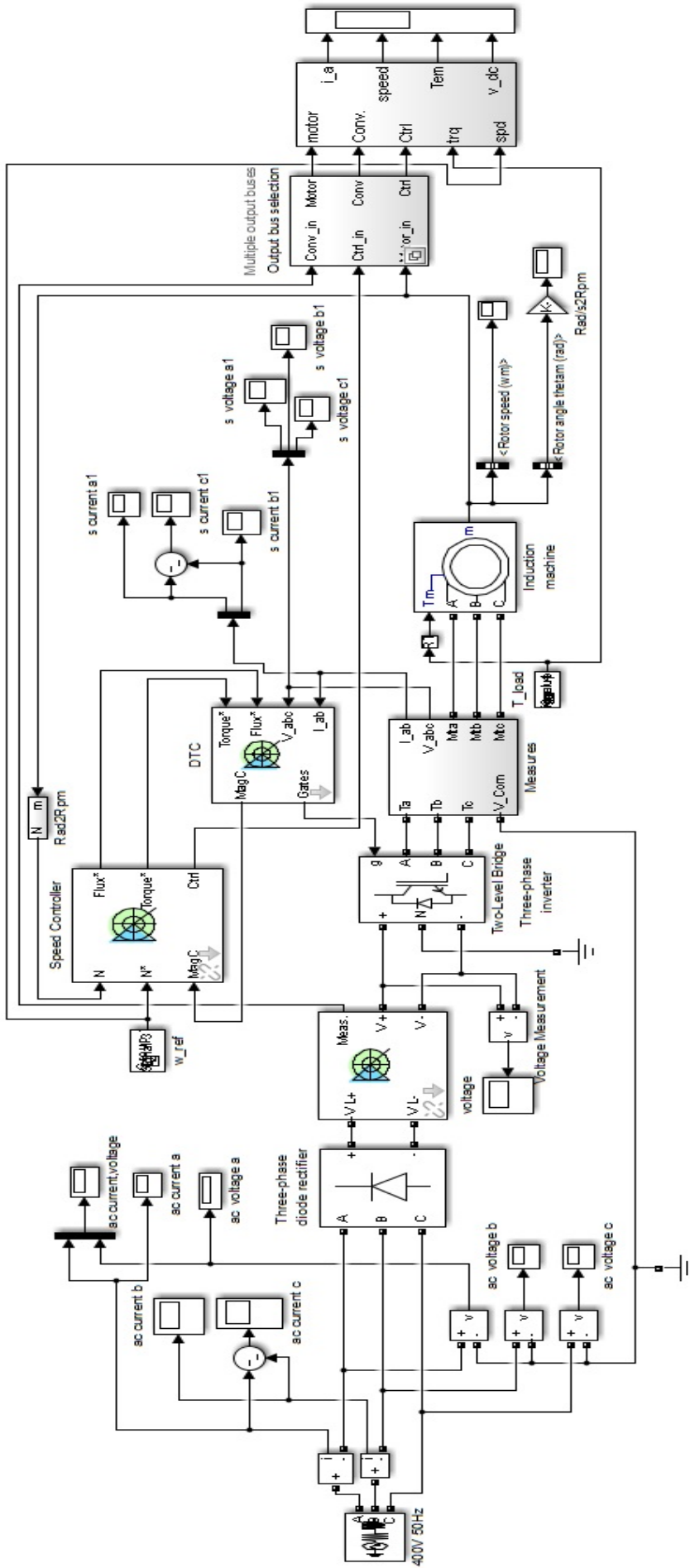


Figure 4.13 Simulink model representation of DTC for two level inverter fed IM

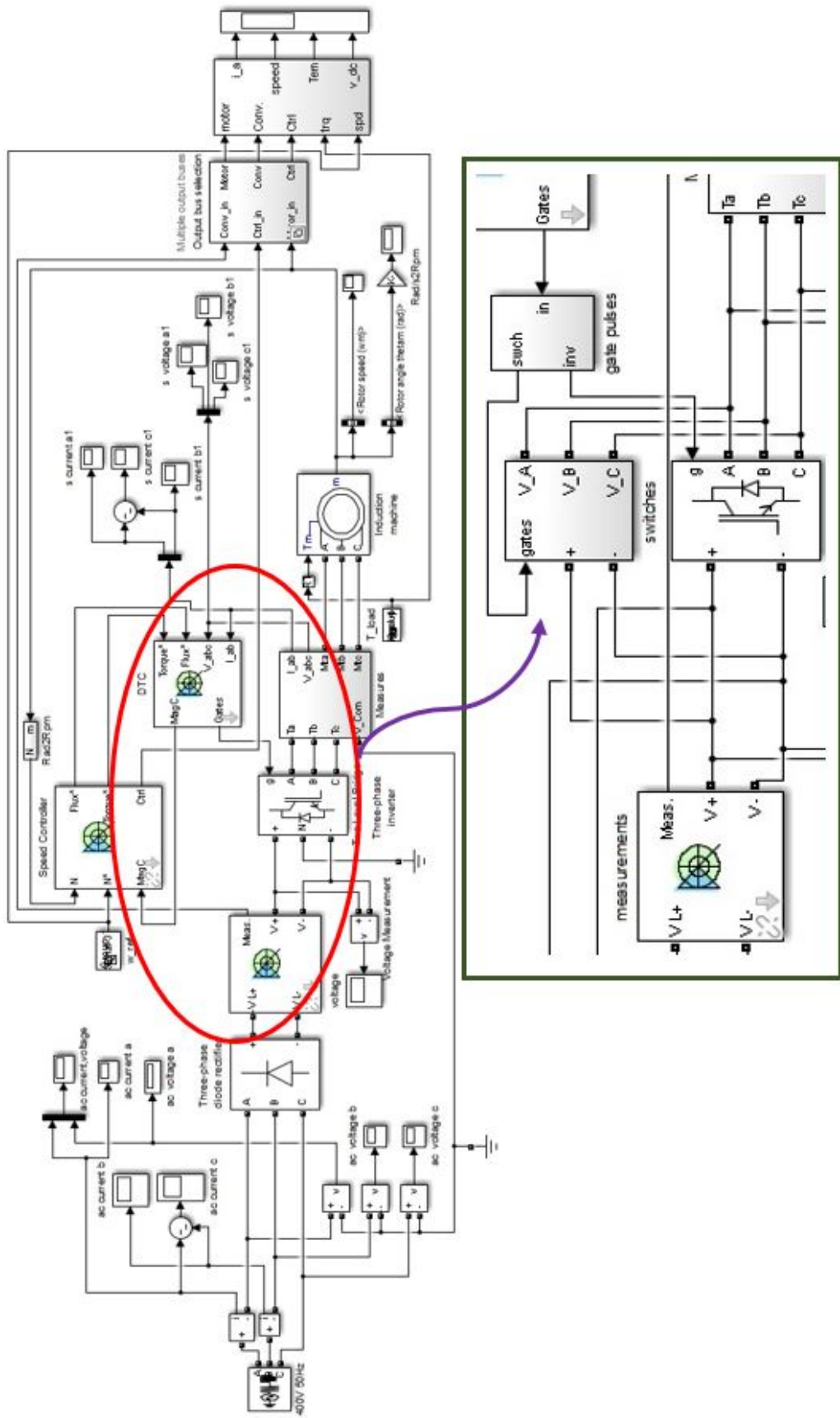


Figure 4.14 Simulink model representation of DTC for three level reduced switch inverter fed IM

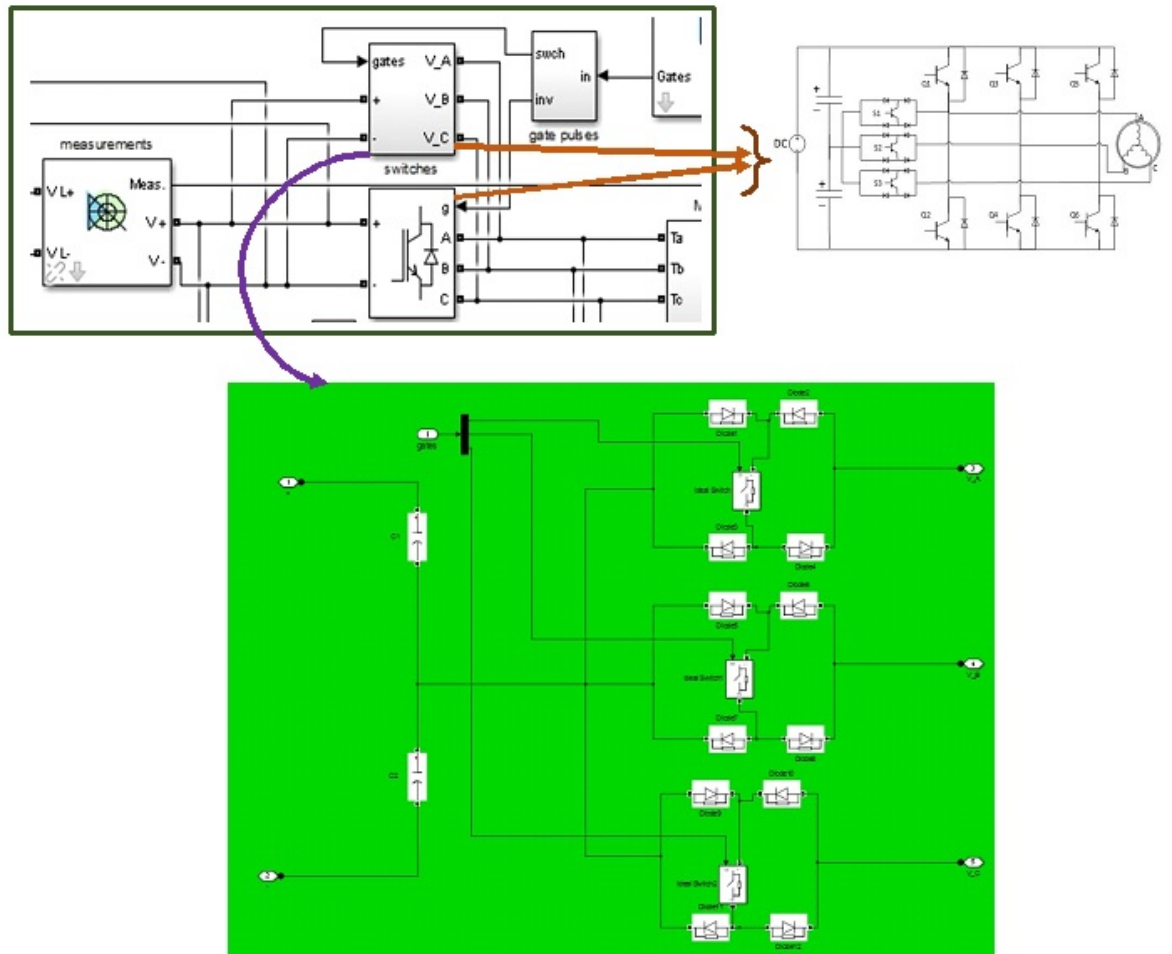


Figure 4.15 Simulink model representation of switch block of three level reduced switch inverter fed IM using DTC technique

Discrete,
Ts = 2.5e-05 s.
powergui

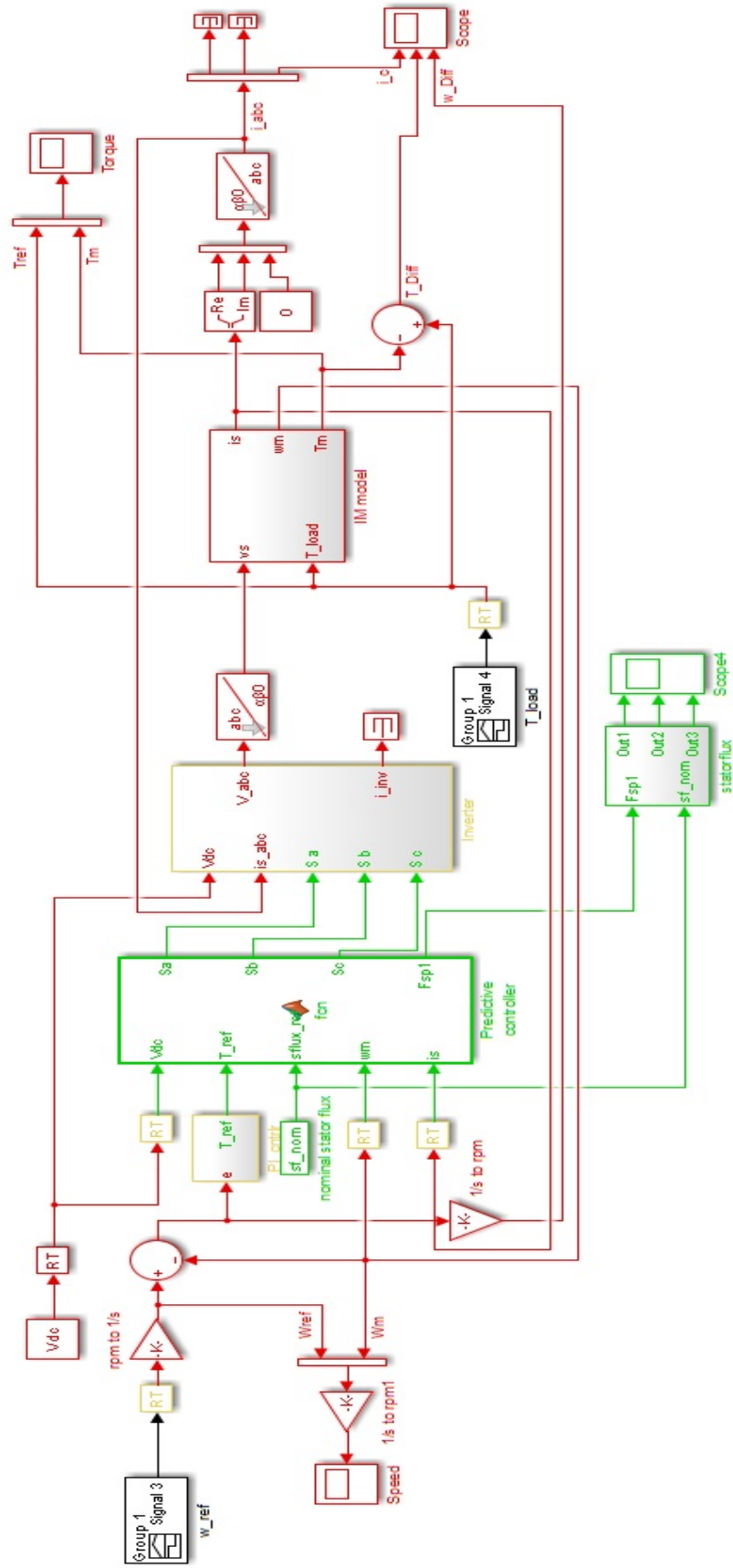


Figure 4.16 Simulink model representation of PTC for three level inverter fed IMD

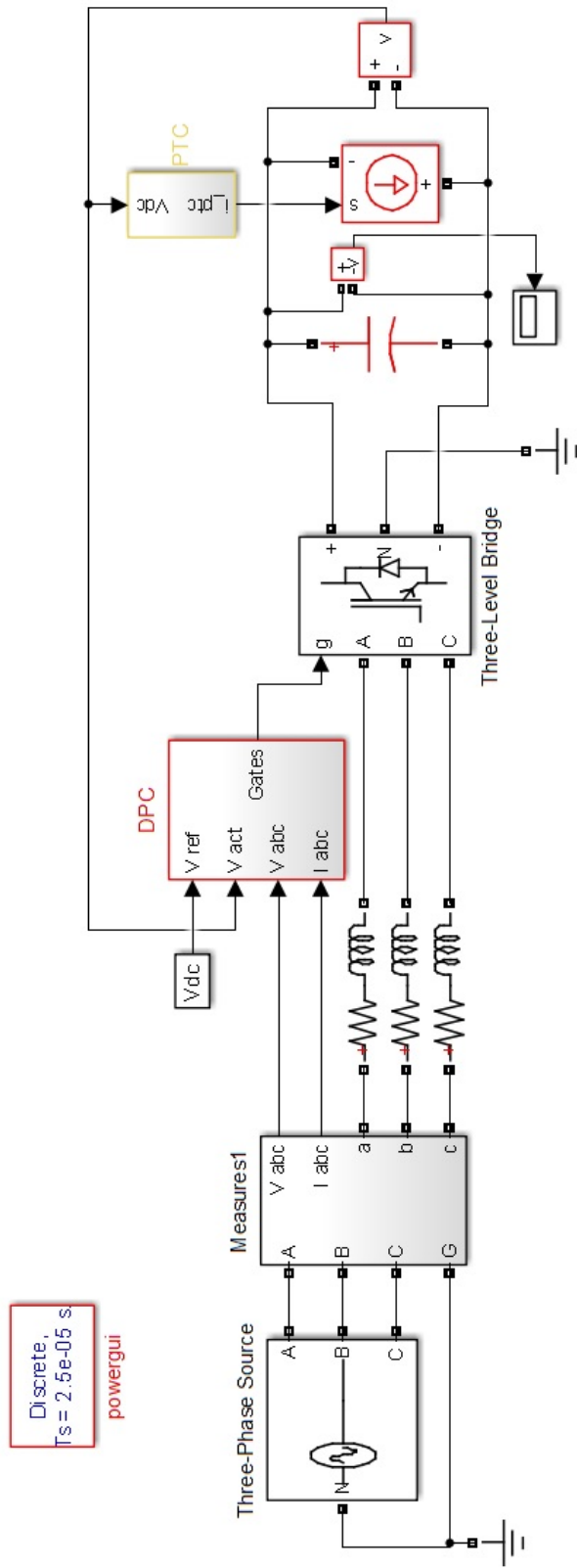


Figure 4.17 Simulink model representation of DPC for back-to-back connected three level diode clamped converter fed IMD

4.8 Conclusions

This chapter presented a modified direct torque control strategy incorporating a predictive control algorithm for a three level reduced switch (nine switches) VSI fed IMD. This inverter topology will be less costly as compared to a regular three level NPC inverter due to the use of only one additional device per leg while being compared with a normal two-level VSI. The future behaviour of the system in terms of flux, current, and torque are predicted using mathematical model equations. The voltage vector that will reduce future error is deduced and applied to the IMD. The complete system will be studied for different speed and load conditions using Matlab/Simulink. Simultaneously, the torque and current ripples, settling times and overshoot, THD etc. will also be analysed and compared with classical DTC method. Further, novel PTC which reduces number of switchings by optimal voltage vector selection has been explained for the same diode clamped inverter fed IMD. Moreover, DPC of three phase AFE rectifier is proposed with optimal voltage vector selection based on the estimation of grid virtual flux. This enables the control strategy to calculate instantaneous active and reactive powers. The simulation results are presented and discussed in detail, in *Chapter 5*.

Chapter 5

Simulation Results and Discussions

5.1 Introduction

IMDs are well known for their rugged and maintenance-free nature apart from being versatile. They are employed in various industrial set-up with state-of-the-art control schemes to enhance their dynamic behaviour. As discussed in the previous chapters, to improve the dynamic response of the IMD system and to reduce the torque and current ripples, a modified DTC algorithm and also a PTC algorithm have been employed. Also, a DPC algorithm based AFE converter has been tried out for implementing reactive power control at the grid side (at the point of common coupling). Since simulations can predict the performance of the drive quite accurately without actually implementing the drive in actual hardware, the proposed control algorithms are tested in Simulink/MATLAB platform by first modelling the complete drive system in the software tool. The analysis of the proposed control algorithms are carried out in MATLAB/Simulink environment for various dynamic operating conditions in all four quadrants of the drive operation.

5.2 Two-level inverter fed IMD

Simulation of DTC for a 3-phase 5 hp induction motor fed by a two-level VSI is carried out in MATLAB/ SIMULINK after modeling the entire drive system. The parameters of IMD used in simulation are listed in Appendix A.1. Switching frequency is limited to 20 kHz by making use of a zero order hold with a suitable sampling time.

5.2.1 Steady State response

Fig. 5.1 shows the responses of the motor operating in steady state at no-load initially and subsequently with a load perturbation, when fed by a two-level VSI. Initially the motor is running at 1400rpm and at 1s a load torque of 25 N-m is applied. Although there is a dip in the speed momentarily, it gets back to the original value within a matter of 0.1s duration. The stator current rises to 8.5 A (rms) from the original no-load current of 0.7 A (rms), with a ripple content of 2.2A whereas the speed ripple is about 3 rpm. The torque ripple is of the order of about 8 N-m (33%). The speed drops to 1315 rpm during the load change and torque overshoots to 31 N-m. During starting, it can be observed that the speed overshoots to 1410 rpm before settling to the steady state speed of 1400 rpm in about 0.75 s.

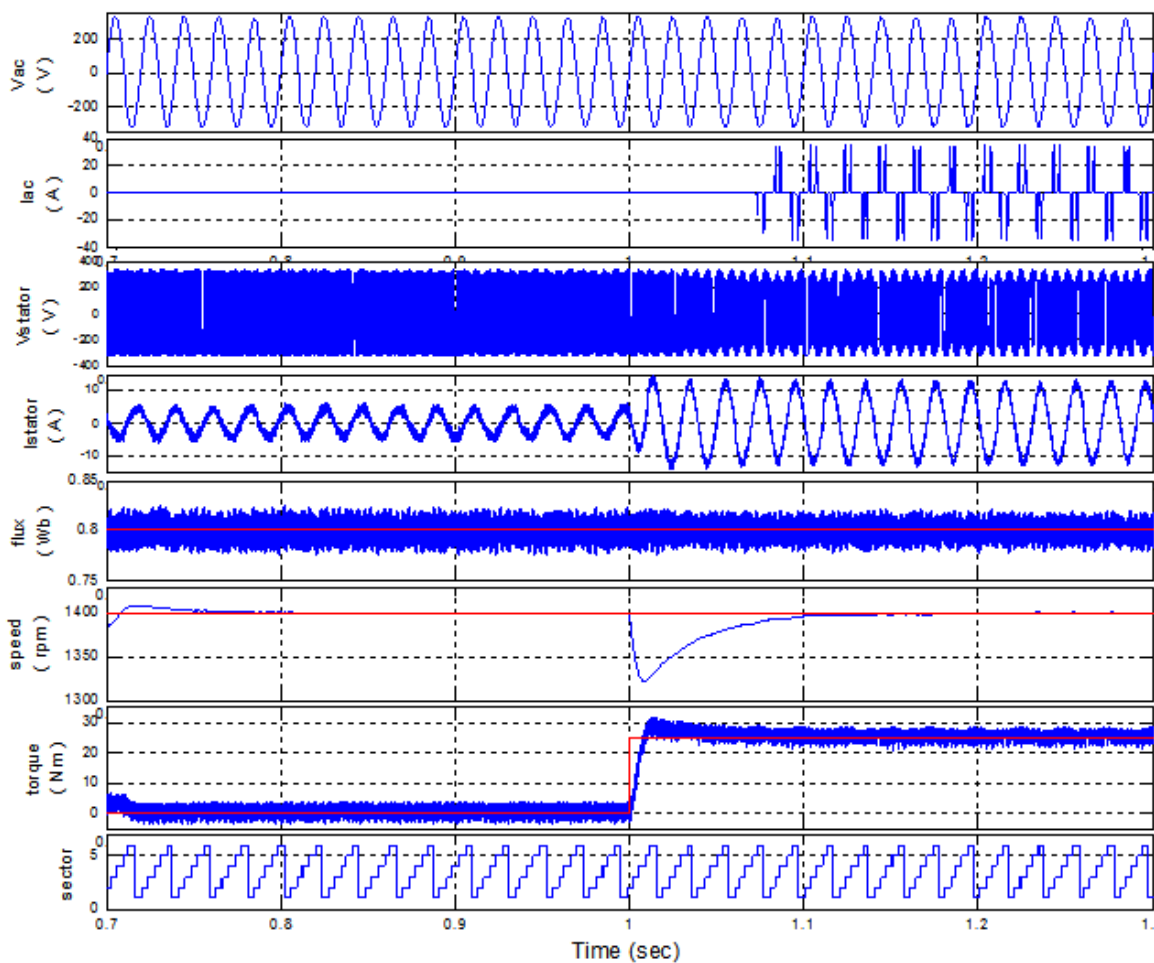


Figure 5.1 Steady state response of the IMD fed by a two level VSI- supply voltage and current, stator voltage, current (i_a : 8.5 A rms) and flux (0.8 Wb), reference and actual speeds (1400 rpm) , reference and actual torque values (0 to 25 N-m), sector position of the flux

5.2.2 Response to load perturbation

Fig. 5.2 shows the transient response of the DTC drive for load disturbance. Initially the motor is running on no-load with the load torque being increased to 10 N-m and 25 N-m at 1s and 1.4 s respectively. For 10 N-m load, stator current rises to 4.24 A rms with a current ripple of 3A. Speed reduces to 1368 rpm and settles back to the reference value at 1.2s with a ripple of 2.2 rpm. Torque overshoots to 14.4 N-m and finally settles with ripple of 7.7 N-m. For 25 N-m load, current rises to 12 A (8.5 A rms) with a ripple of 2.3 A. Speed dips to 1352 rpm and settles back at 1.6 s with a ripple of 2.6 rpm. Torque overshoots to 30 N-m and settles with a torque ripple of 8 N-m.

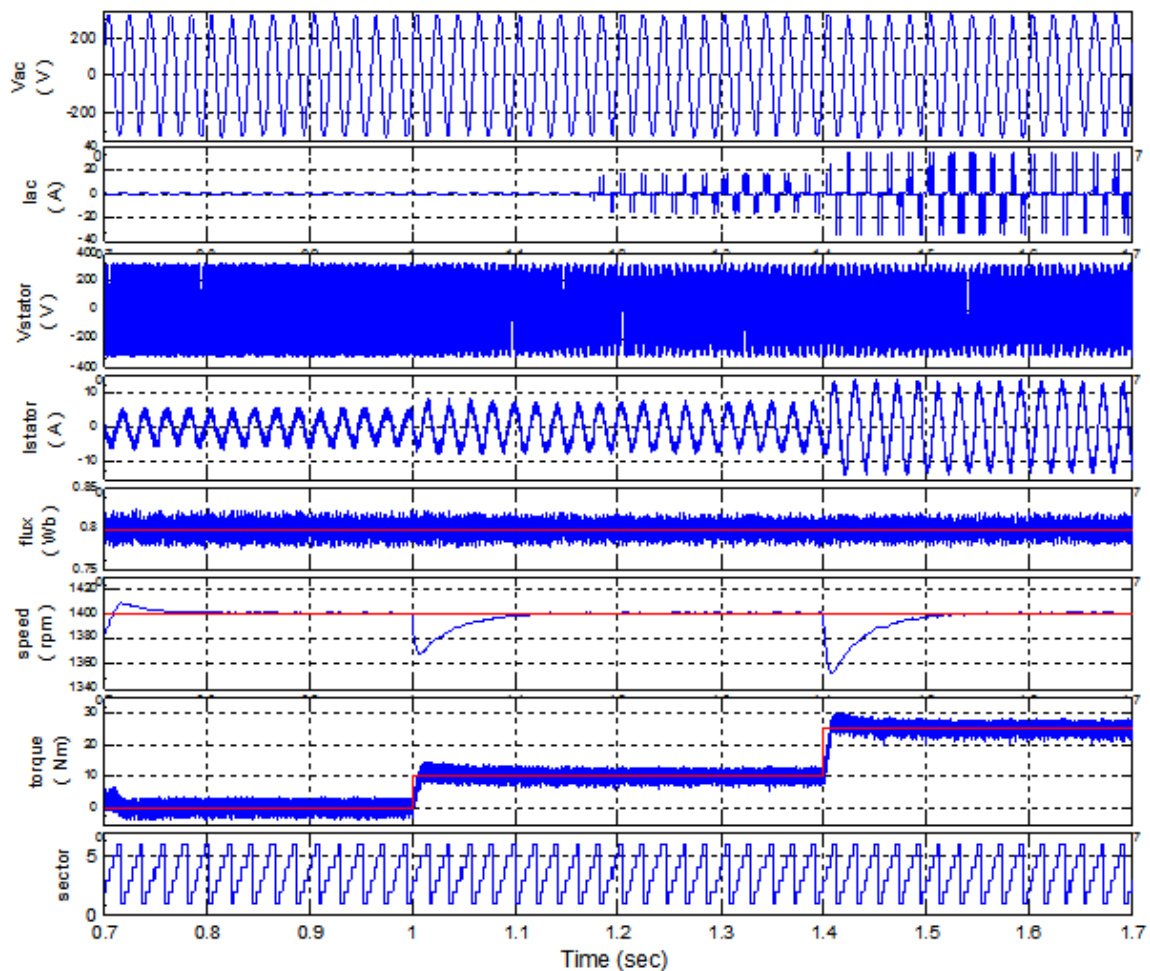


Figure 5.2 Load perturbation in a DTC drive with two level VSI- supply voltage and current, stator voltage, current (i_a : 4.24 A to 8.5 A rms) and flux (0.8 Wb), reference and actual speeds (1400 rpm), reference and actual torque values (10 N-m to 25 N-m), sector position of the flux

The response of the DTC drive fed by a two-level inverter when the reference speed setting changed, is shown in Fig. 5.3. Initially the motor is running at 1400 rpm and the speed setting is changed to 500 rpm at 1.5s. At this speed setting, with 25 N-m load torque, current magnitude remains at 12 A and has

ripple of 2.6 A. Speed overshoot is about 9 rpm after which the speed settles to 500 rpm at 2.1s with a speed ripple of 2 rpm and a torque ripple of 6 N-m.

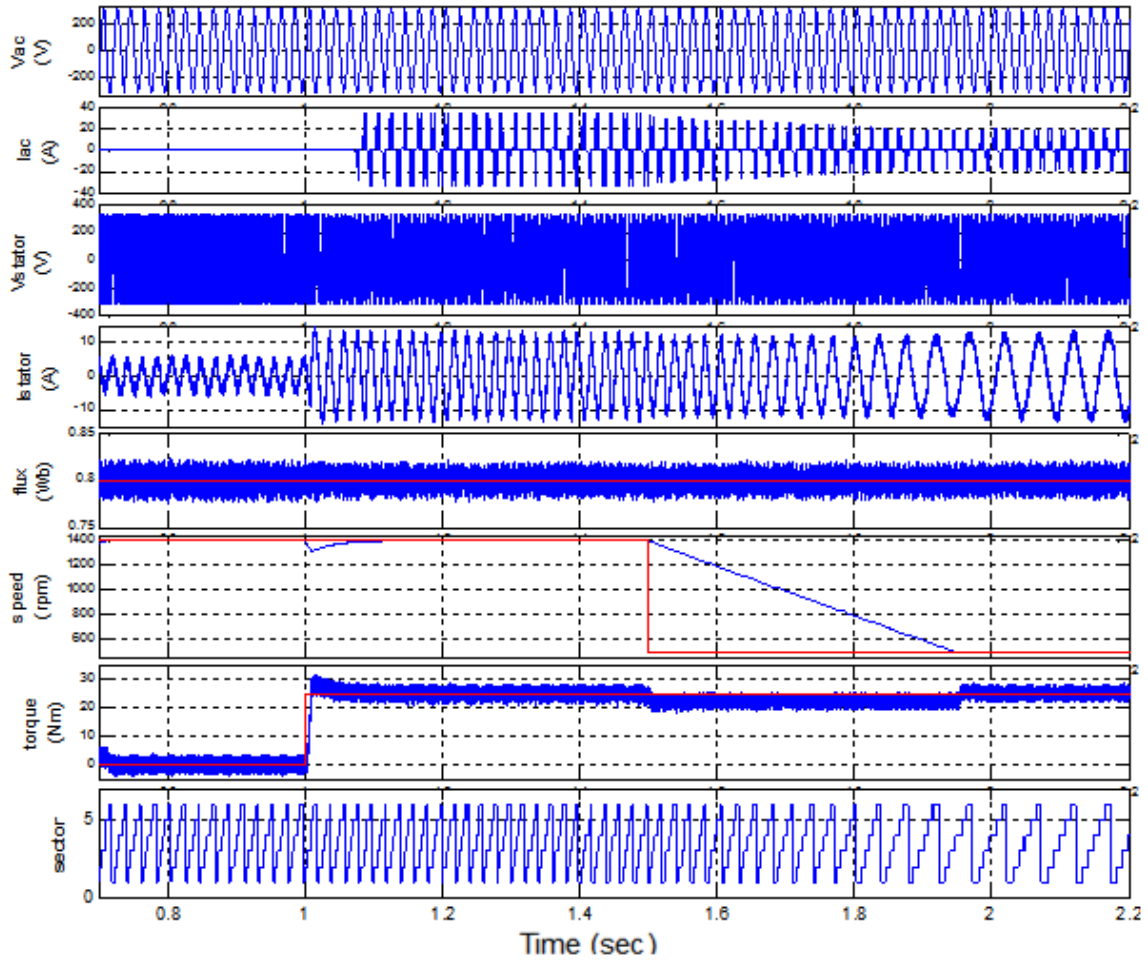


Figure 5.3 Response to reference speed change in two level VSI fed DTC drive- supply voltage and current, stator voltage, current (i_a : 8.5 A rms) and flux (0.8 Wb), reference and actual speeds (1400 rpm to 500 rpm), reference and actual torque values (25 N-m), sector position of the flux

The response of the two-level VSI fed DTC drive during speed reversal is observed in Fig. 5.4. At 1.5s, speed reversal command is given so that the drive changes its speed to -1400 rpm. Current rises to 12.02A rms to generate a braking torque and there is a reversal of rotation. The flux linkage sector position shown in the last plot of Fig. 5.4 depicts reversal clearly. Due to reversed speed command at 1.5s, speed overshoots to 1547 rpm which is greater than rated speed value, so flux weakening occurs. Flux gets back to the rated value after speed reaches below rated speed after which speed overshoots to -1410 rpm and finally settles to -1400 rpm at 3.1s with speed and torque ripples of 2.5 rpm and 8 N-m, respectively.

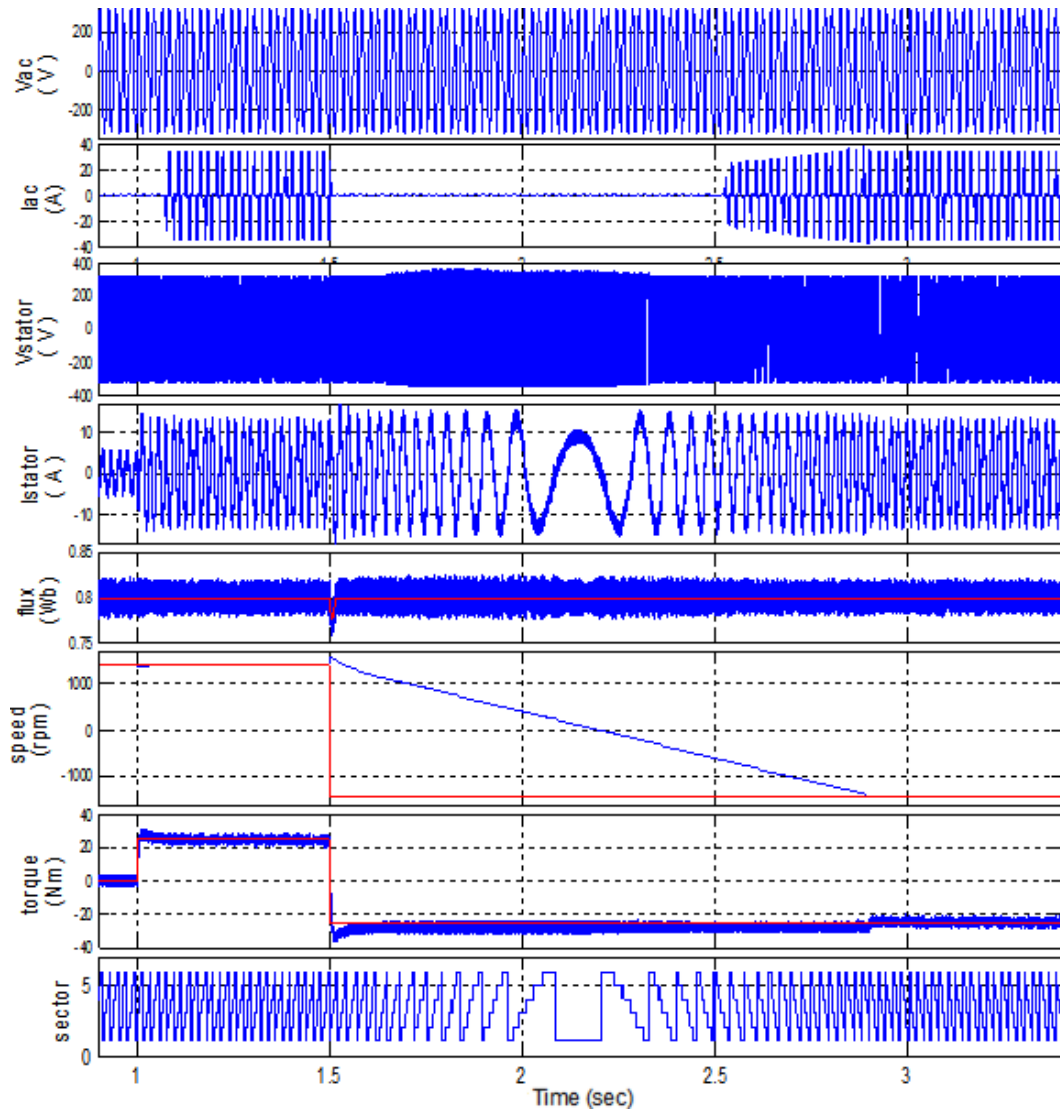


Figure 5.4 Response of the DTC drive for speed reversal-two level VSI case- supply voltage and current, stator voltage, current (i_a : 8.5 A rms) and flux (0.8 Wb), reference and actual speeds (1400 rpm to -1400 rpm), reference and actual torque values (25 N-m to -25 N-m), sector position of the flux

5.3 Multilevel inverter fed IMD with classical DTC

The three level reduced switch VSI fed 5 hp IMD is simulated in MATLAB/SIMULINK environment. The fundamental difference in the voltage waveforms in 3-level and 2-level cases is that in three-level case, voltage stays put at zero level for a finite duration of time. But, in two-level case the line voltage excursion is between $+V_{dc}$ and $-V_{dc}$. The response of the motor drive under different dynamic operating conditions is discussed in the following sections.

5.3.1 Steady State response

The steady state operation for 3-level VSI fed IMD is shown Fig. 5.5. In the 3-level case, current and torque ripples are 1.5 A and 5 N-m (20%) respectively, which are considerably reduced as compared to the 2-level case. The speed dip and torque overshoot during the load change are also considerably reduced in the three level case which are at 1322 rpm and 29.5 N-m respectively.

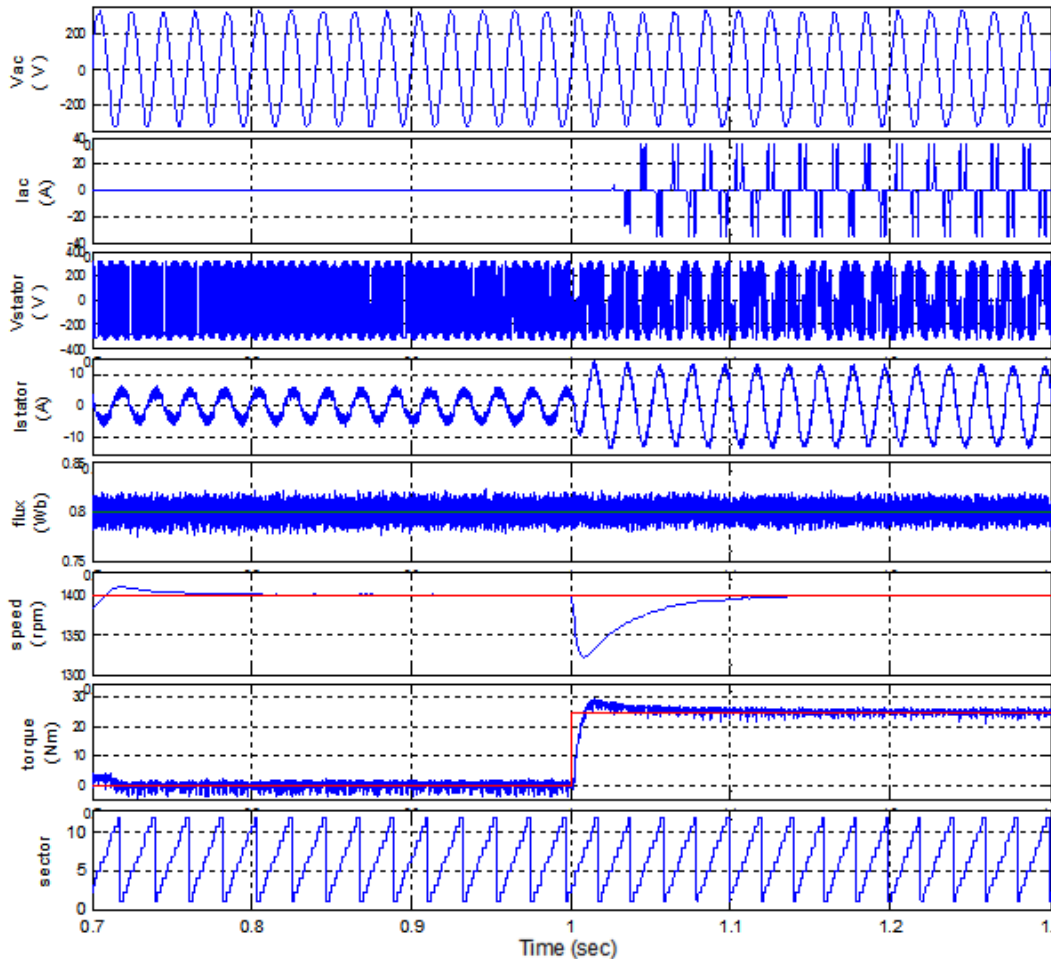


Figure 5.5 Steady state operation with three level inverter- supply voltage and current, stator voltage, current (i_a : 8.5 A rms) and flux (0.8 Wb), reference and actual speeds (1400 rpm), reference and actual torque values (0 to 25 N-m), sector position of the flux

5.3.2 Response during load disturbance

In the three level inverter case shown in Fig. 5.6, when the load torque is increased from no-load condition to 10 N-m, stator current rises to 6A with a ripple of 2.3A; speed reduces to 1370 rpm and finally settles to the reference speed at 1.2s with speed ripple of 1.5 rpm. The overshoot in torque is only 12.7 N-m when it settles down and its ripple is 4.7 N-m. For a load torque of 25 N-m, stator current rises

to 8.5A with ripple of 2A; speed reduces to 1352 rpm and finally settles to the reference speed within 5 cycles with speed ripple of 2 rpm. The overshoot in torque is 28.5 N-m; after reaching the steady state value of 25 N-m, the ripple in torque is 5.1 N-m.

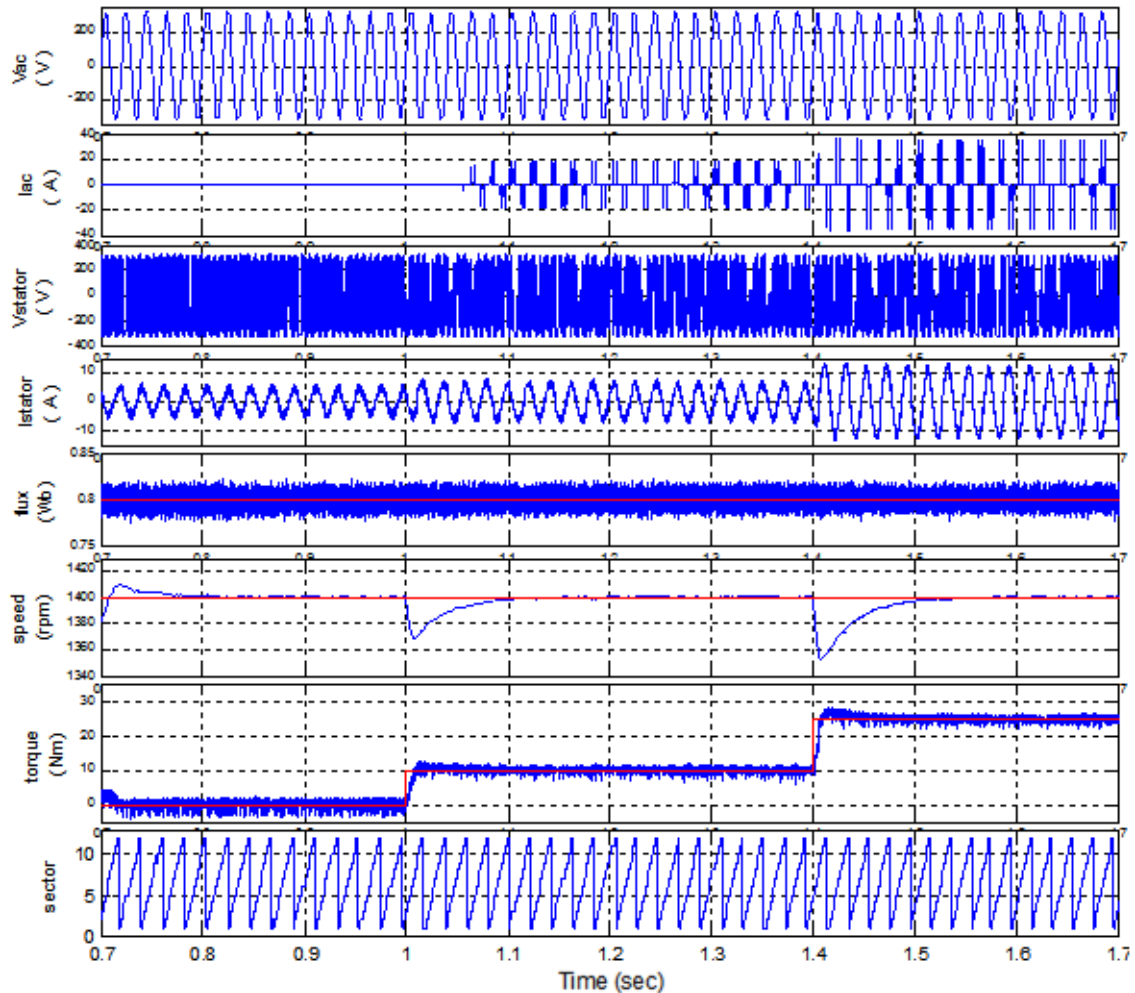


Figure 5.6 Load perturbation in a DTC drive fed by a three level VSI - supply voltage and current, stator voltage, current (i_a : 4.24 A to 8.5 A rms) and flux (0.8 Wb), reference and actual speeds (1400 rpm), reference and actual torque values (10 N-m to 25 N-m), sector position of the flux

In the case of reference speed change (as shown in Fig. 5.7), current remains at 12 A for 25 N-m load torque with a ripple of 2 A. Speed undershoot is almost the same as the two-level VSI case; speed ripple is about 1 rpm and the torque ripple is 5.4 N-m.

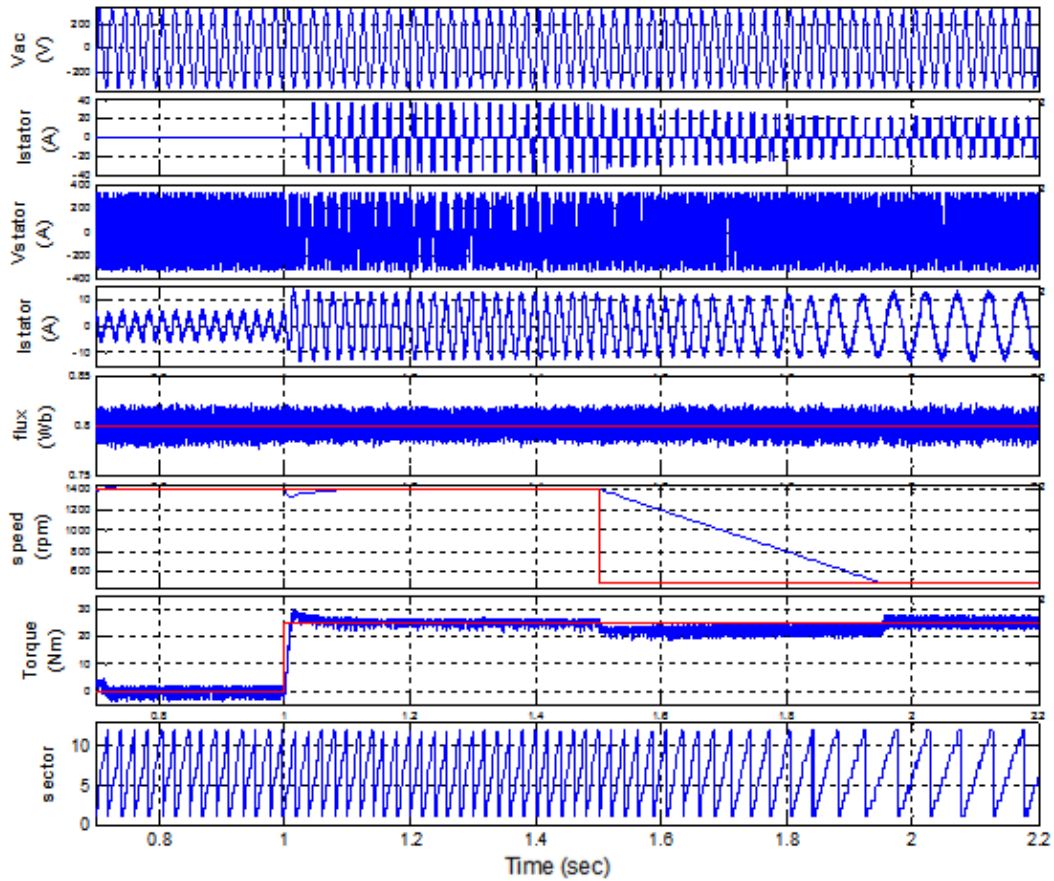


Figure 5.7 Response to reference speed change in three level VSI fed DTC drive- supply voltage and current, stator voltage, current (i_a : 8.5 A rms) and flux (0.8 Wb), reference and actual speeds (1400 rpm to 500 rpm), reference and actual torque values (25 N-m), sector position of the flux

Speed reversal condition of the three level inverter case is observed in Fig. 5.8. Current increases to 16.5 A (11.6A rms) initially, during the beginning of speed reversal. Speed shoots up to 1544 rpm and eventually it settles to -1400 rpm at 1.6s with a speed ripple of 2 rpm and a torque ripple of 5 N-m.

5.4 Predictive Torque Control (PTC)

The proposed PTC algorithm is applied to both two level VSI and three level diode clamped inverter fed IMD and the results are discussed in this section. The performance of the algorithm is analyzed in terms of current and torque ripples in steady-state, over shoot and settling time during transients (for a sudden change in speed or load torque) and also THD of the output currents.

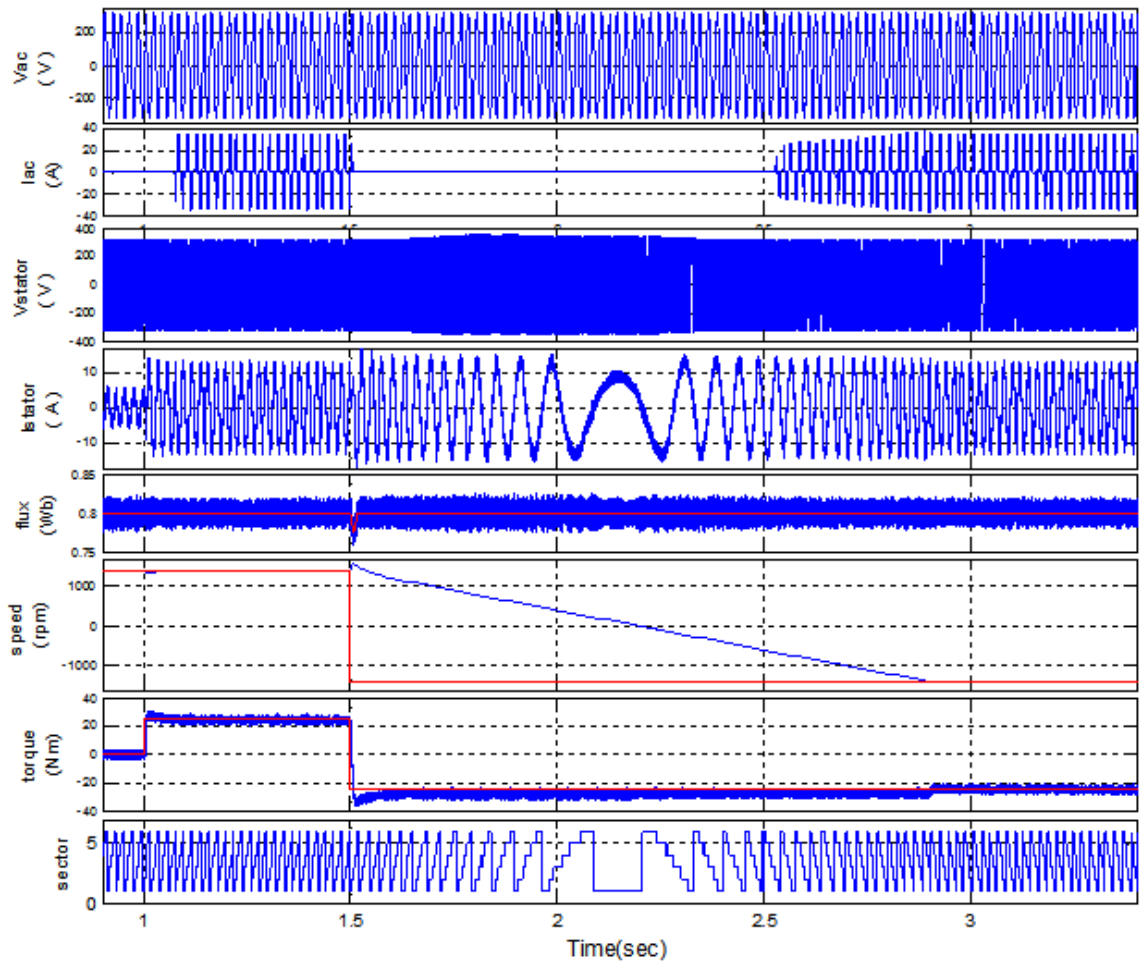
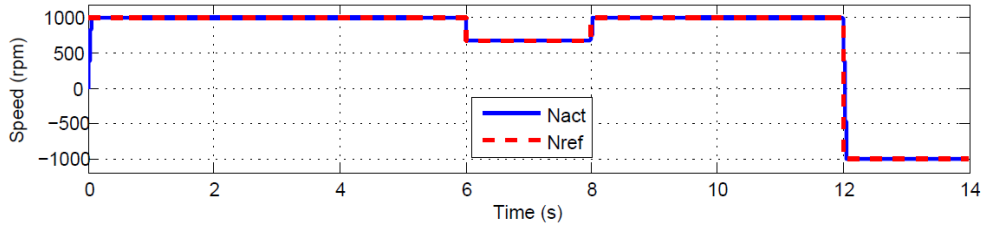


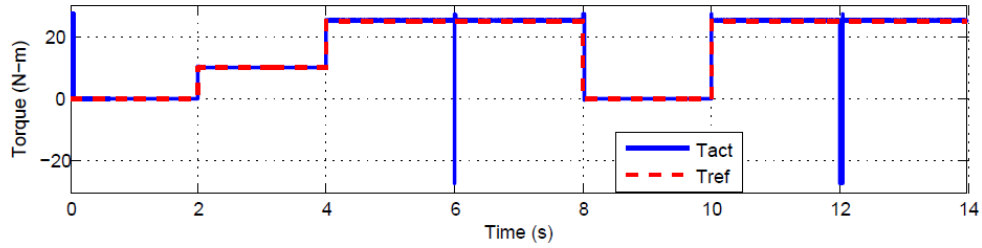
Figure 5.8 Response of the DTC drive for speed reversal-three level VSI case- supply voltage and current, stator voltage, current (i_a : 8.5 A rms) and flux (0.8 Wb), reference and actual speeds (1400 to -1400 rpm), reference and actual torque values (25 N-m to -25 N-m), sector position of the flux

5.4.1 Steady state response of two level inverter fed IMD

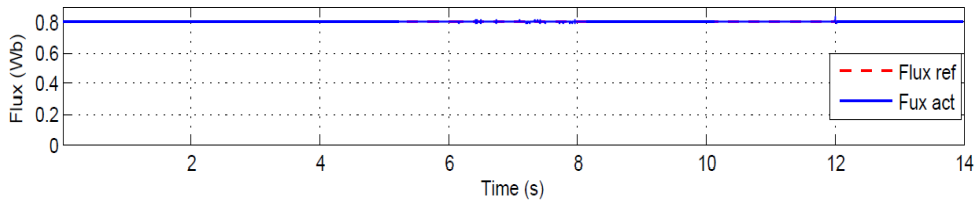
Fig. 5.9 shows the steady-state performance of the drive at various operating conditions of speed and load torque. The plots shown are of speed (both reference and actual values), torque and flux of 0.8 Wb. The magnified view of torque is shown in Fig. 5.9d from which it can be seen that the torque ripple is hardly 0.1 N-m while the load torque delivered is 25 Nm. The steady-state torque ripple is found to be 0.6%.



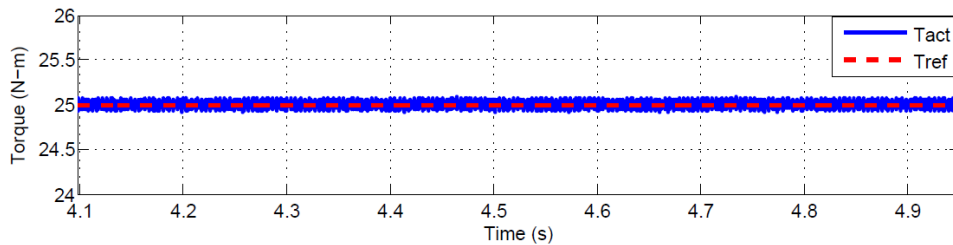
(a)



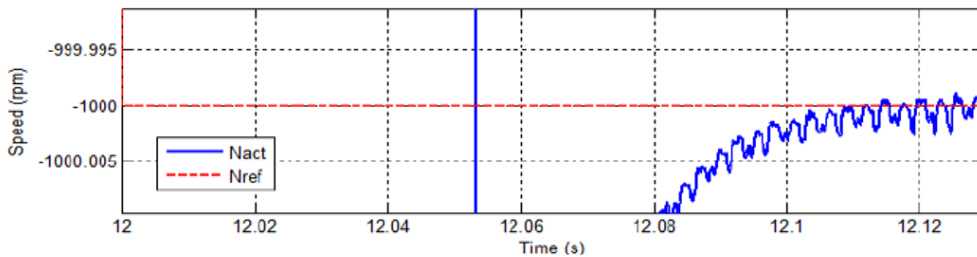
(b)



(c)



(d)



(e)

Figure 5.9 Steady state response of the two-level inverter fed IMD with proposed PTC algorithm (a) Reference (Nref) and Actual (Nact) speeds, (b) Reference (Tref) and Actual (Tact) Torques at different speed and load conditions (c) Reference and Actual Flux (0.8 Wb) (d) Torque ripple at 25 N-m, (e) Expanded portion of speed tracking during speed reversal (-1000 rpm)

5.4.2 Transient response of two level inverter fed IMD

To understand the transient behavior of the IMD working with this algorithm, a sudden change in load torque from 10 N-m to 25 N-m is applied at 4s as shown in Fig. 5.10a. This portion is expanded and shown in Fig. 5.10b where the torque overshoot is about 0.31 N-m and settling time is 0.02 s. The rotor speed during this load change is shown in Fig. 5.10c where the speed dips from 1000 to 997.27 rpm. The a-phase stator current in this case is illustrated in Fig. 5.10d.

Similarly, the algorithm is also tested for a sudden change in the reference speed from 1000 to 680 rpm at 6s as shown in Fig. 5.11. As seen in Fig. 5.11a, the speed overshoot is 8 rpm and settling time is 0.014 s. During this speed change, the torque and stator current can be observed in Figs. 5.11b and 5.11c respectively. The THD of the stator current is observed to be 0.91% in Fig. 5.11d.

Motor speed reversal can be observed from Fig. 5.9a itself where the machine took around 0.11 s for reversal with an overshoot of 0.49 rpm as depicted in Fig. 5.9e. Efficient zero vector selection for two level inverter fed IMD is illustrated in Fig. 5.12 where, 0-7 represent the voltage vectors V_0-V_7 respectively. As shown, if a zero vector has to be applied, the nearest zero vector obtained from Table 4.5 is selected so that number of switch transitions required is reduced.

5.4.3 Steady state response of three level inverter fed IMD

At steady-state, various operating conditions of the drive in terms of speed and load torque are shown in Fig. 5.13 for a three-level inverter case with PTC algorithm with optimal vector placement. The applied speed reference (N_{ref}) and the actual (N_{act}) speed coincide with each other as depicted in Fig. 5.13a. The electromagnetic torque generated from the IM and the load torque reference obtained from speed loop error are shown in Fig. 5.13b. In Fig. 5.13c, reference and actual values of stator flux are of 0.8 Wb magnitude which are maintained throughout. The torque ripple calculated at 25 N-m load in Fig. 5.13d is found to be 0.4% of the reference value.

5.4.4 Dynamic response of three level inverter fed IMD

Fig. 5.14 illustrates a load change from 10 to 25 Nm when rotor speed is maintained constant at 1000 rpm. The actual torque generated by the machine tracks the load torque as shown in Fig. 5.14a where the overshoot and settling time are 0.29 N-m and 0.9 ms respectively. At the instant of load change the rotor speed dip of around 3 rpm is observed in Fig. 5.14b. After that, speed controller restores the rotor speed to the reference value. During load change, the variation of a-phase stator current is shown

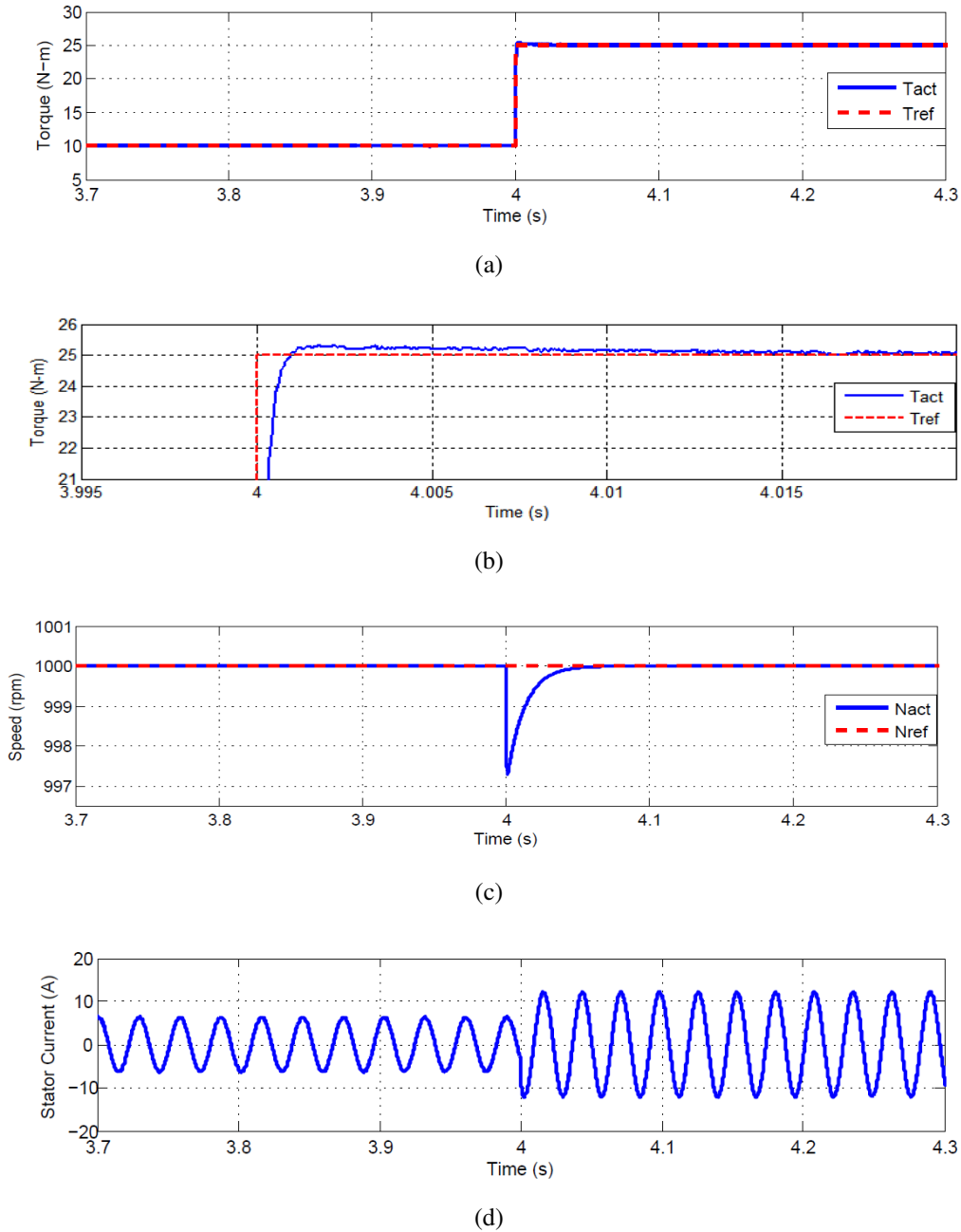
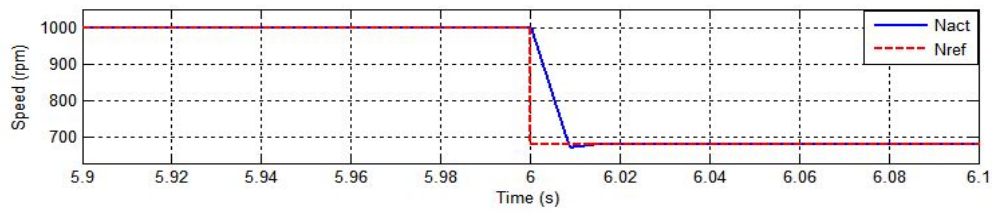


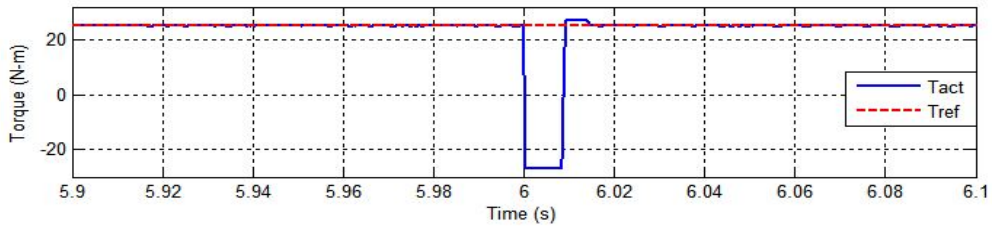
Figure 5.10 Dynamic response of two level inverter fed IMD when Load Torque changes with speed maintaining constant (a) Torque (10 N-m to 25 N-m) (b) Magnified portion of load change (at 25 N-m) with speed constant (c) Speed (1000 rpm) (d) Stator current (i_a : 3.5 A - 7 A rms) with the proposed PTC algorithm

in Fig. 5.14c.

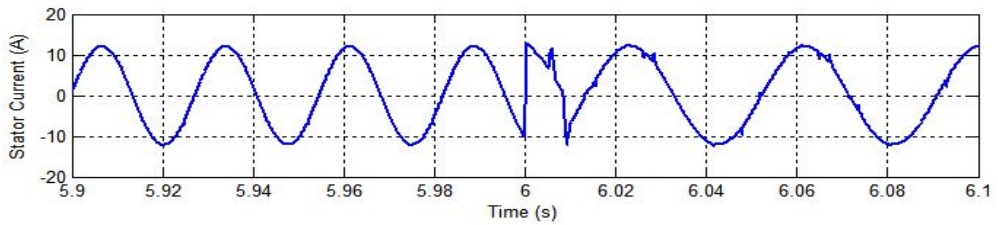
A sudden speed change from 1000 to 680 rpm in Fig. 5.15 is demonstrated by keeping load torque constant at 25 N-m. The reference speed command tracks the machine speed with an overshoot of approximately 7 rpm and settling time of 8 ms as shown in Fig. 5.15a. The torque dips to -27 N-m as could be observed in Fig. 5.15b, in order to facilitate fast response during speed change. The a-phase



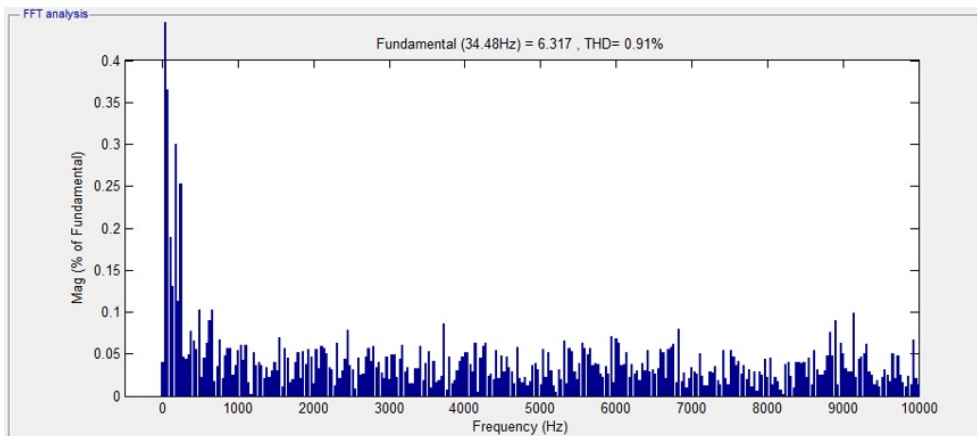
(a)



(b)



(c)



(d)

Figure 5.11 Response when speed changes with constant load torque for two level inverter (a) Speed (1000 rpm to 680 rpm) (b) Torque (25 N-m) (c) Stator current (i_a : 7 A rms) with the proposed PTC algorithm (d) THD (0.91%) analysis with the proposed PTC algorithm.

stator current is shown in Fig. 5.15c, whose THD in predictive torque control strategy for three level inverter fed IMD is observed to be 0.34% (Fig. 5.15d).

The optimal voltage vector/efficient zero vector selection for three level inverter fed IMD for few vectors is illustrated in Fig. 5.16. As shown, if a optimal voltage vector has to be applied, the nearest

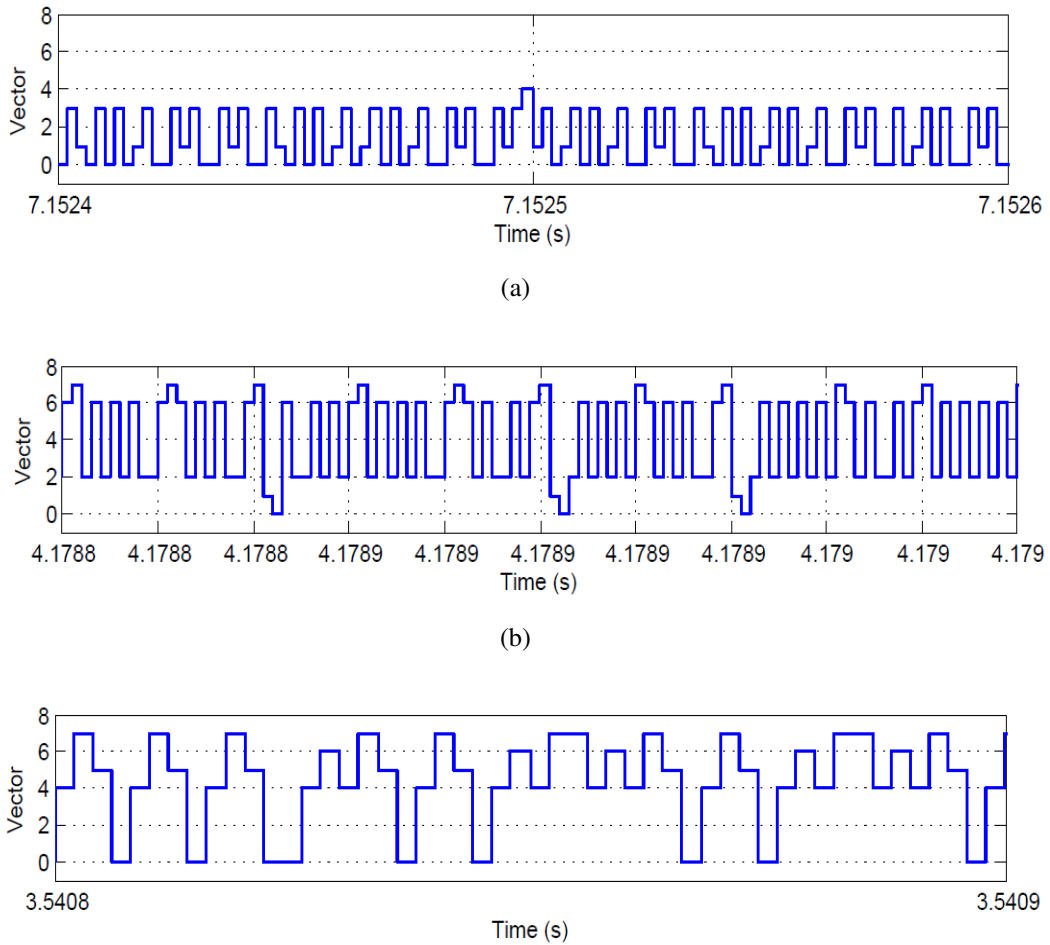
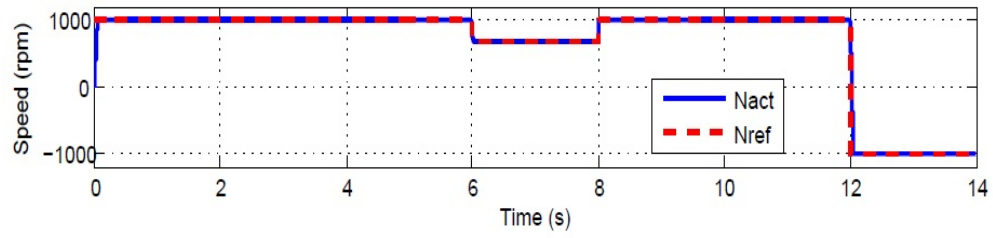


Figure 5.12 Response of efficient zero vector selection for two level VSI fed IMD (a) V_0 and V_3 changing to zero vector V_0 (b) V_2 and V_6 changing over to V_7 and V_1 changing to V_0 (c) V_4 and V_7 switched to zero vector V_7 and V_5 switched to V_0 .

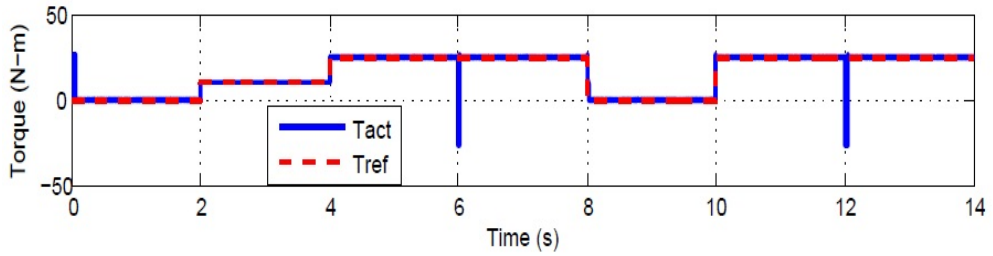
zero/redundant vector obtained from Table 4.7 is selected so that number of switch transitions required is reduced. Table 5.1 illustrates the reduction in the total number of switching transitions caused by this proposed optimal voltage vector selection algorithm.

5.5 DPC with active front end converter

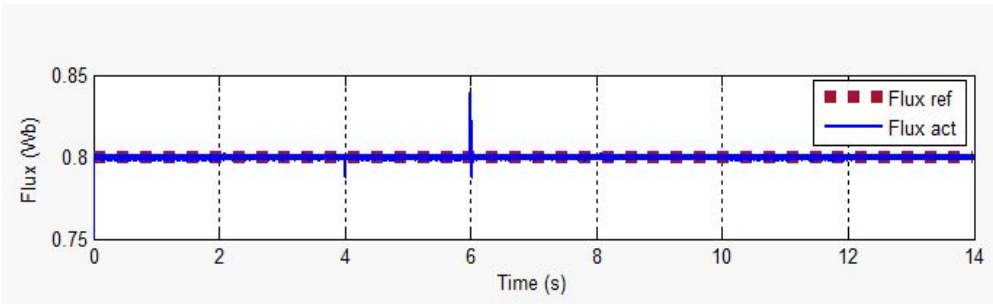
The proposed algorithm is applied to both three level diode clamped rectifier (on the grid side) and multi-level inverter feeding the IMD. The performance of the drive with the proposed algorithm is analyzed for all the four quadrants of motor operation.



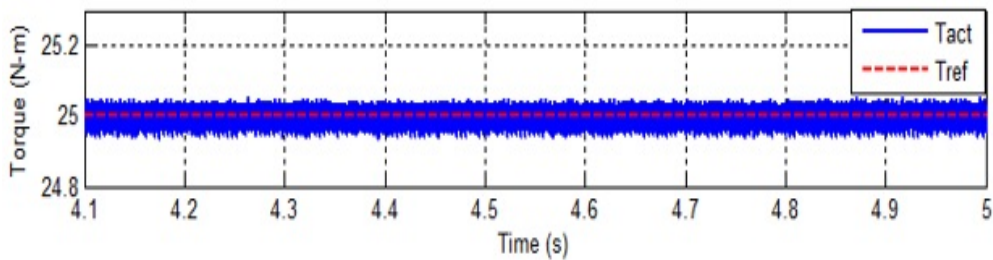
(a)



(b)



(c)

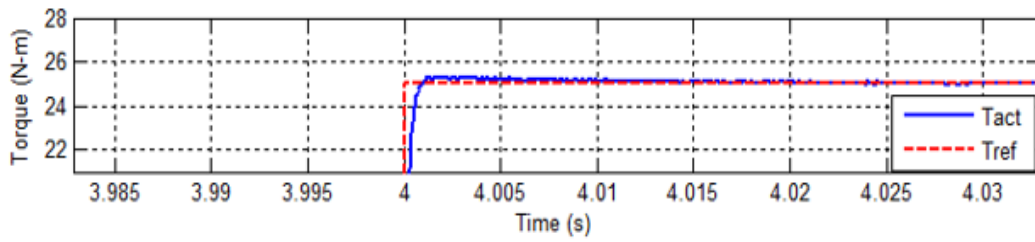


(d)

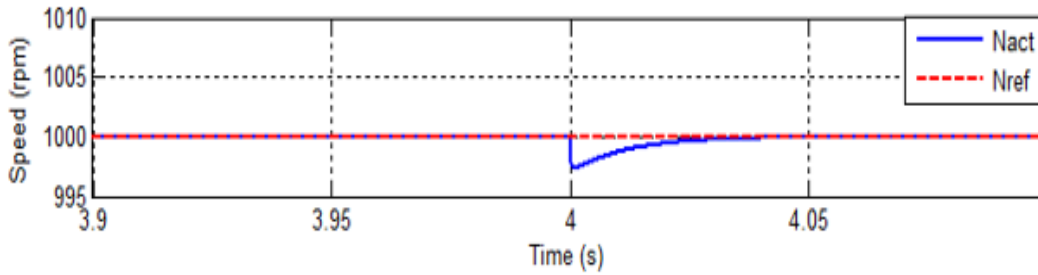
Figure 5.13 Steady state response of the proposed PTC based Three level Inverter fed IMD. (a) Reference (Nref) and Actual (Nact) speeds (b) Reference (Tref) and Actual (Tact) Torque at different speed and load conditions (c) Reference and Actual Flux (0.8 Wb) (d) Torque ripple at 25 N-m.

5.5.1 Power Quality Performance at PCC during steady state

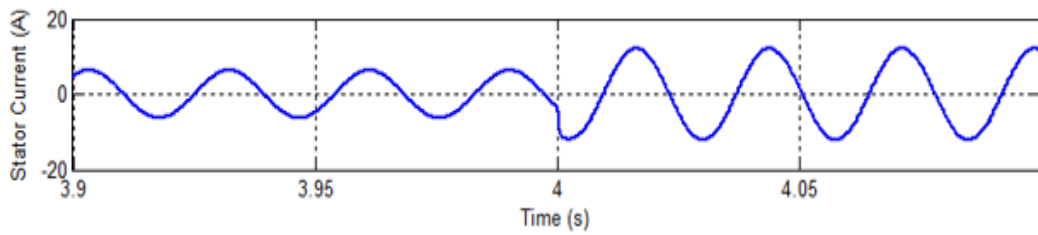
The settling time, overshoot and undershoot are observed during different steady state conditions both at grid side and load side as shown in Fig. 5.17. Both actual and reference values of real power,



(a)



(b)



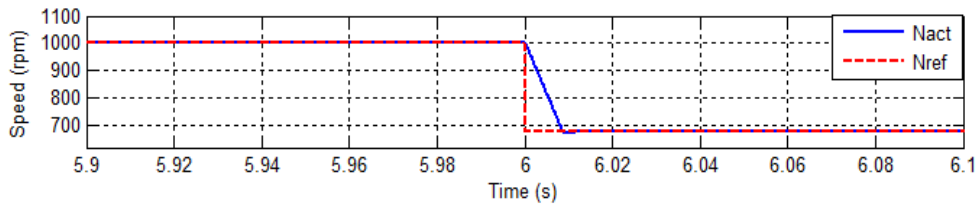
(c)

Figure 5.14 Dynamic response when Load Torque changes and speed maintaining constant (a) Torque (10 N-m to 25 N-m) (b) Speed (1000 rpm) (c) Stator current (i_a : 3.5 A - 7 A rms) in PTC based IMD fed by a Three-Level VSI.

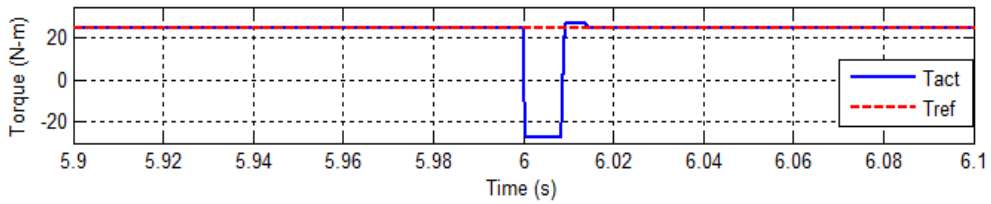
Table 5.1 No. of Switchings for a duration of 14 secs, with a switching frequency of 20 kHz with and without efficient choice of voltage vector in $(k + 1)^{th}$ instant.

Level of the Inverter	No. of Switching Transitions without Efficient choice of voltage vector	No. of Switching Transitions with Efficient choice of voltage vector
Two Level Inverter	0.3684 million	0.3664 million (0.54% less switching)
Three Level Inverter	0.3749 million	0.3559 million (5.07% less switching)

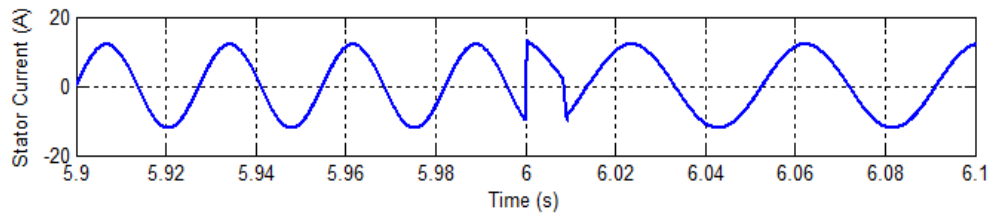
reactive power (maintained at -500 VAR), DC voltage of 600 V and supply side current (I_a) are plotted in Fig. 5.17a, 5.17b, 5.17c and 5.17d respectively.



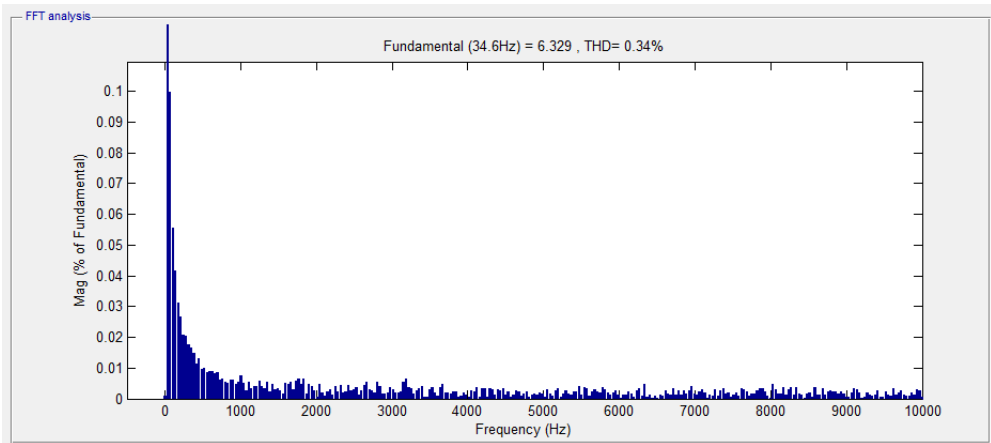
(a)



(b)



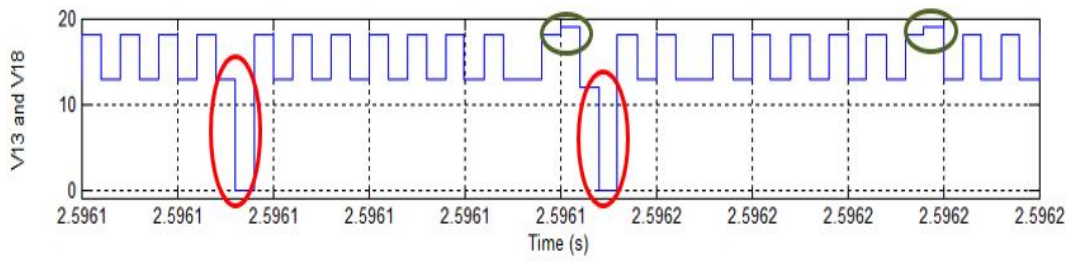
(c)



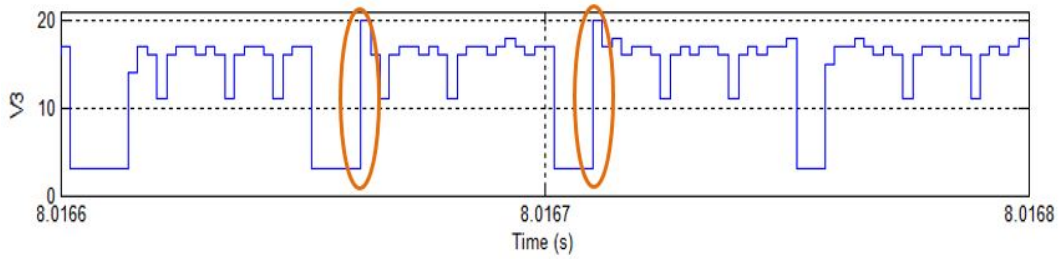
(d)

Figure 5.15 Response when speed changes maintaining load torque constant (a) Speed (1000 rpm to 680 rpm) (b) Torque (25 N-m) (c) Stator current (i_a : 7 A rms) (d) THD (0.34%) analysis in IMD fed by a Three-Level VSI.

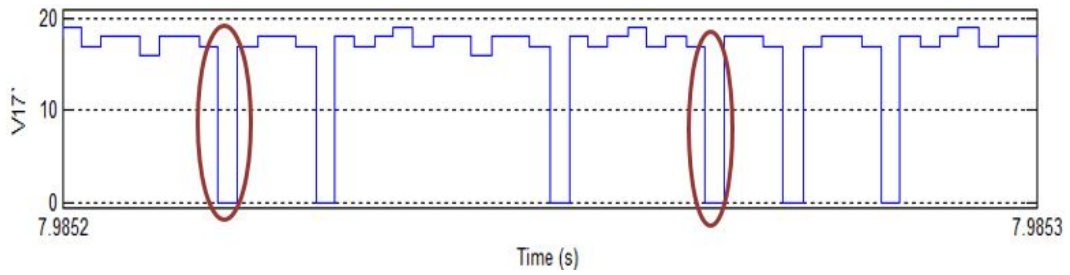
Fig. 5.18 shows the performance at load side i.e., three level diode clamped inverter fed IMD using PTC. Speed (Fig. 5.18a) and Flux of 1.53 Wb magnitude (Fig. 5.18b) at different load conditions is shown. The load torque (Fig. 5.18c) and a- phase stator current (Fig. 5.18d) ripples at 2 s are observed to be 3% and 4.7%, respectively.



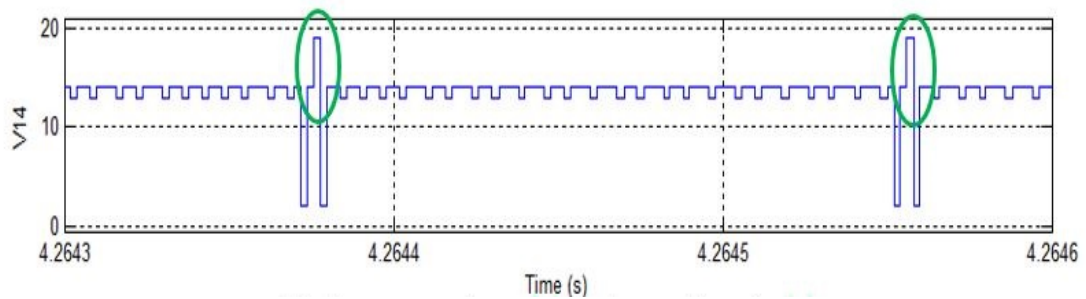
(a)



(b)

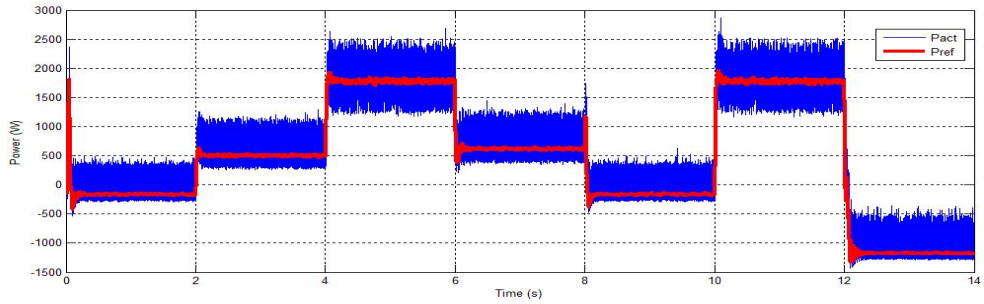


(c)

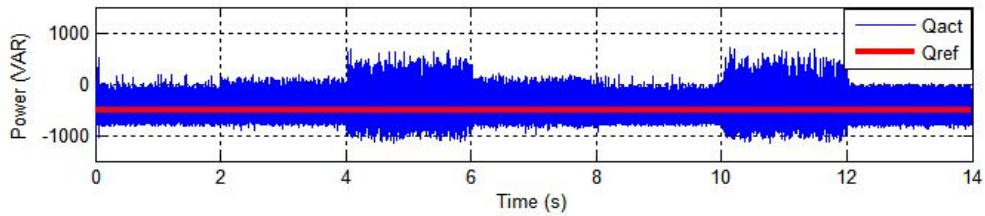


(d)

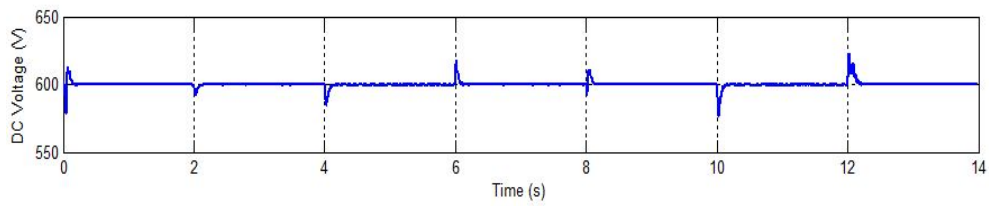
Figure 5.16 Illustration of Optimal Voltage vector selection for Three level diode clamped inverter fed IMD (a) Voltage Vectors V_{13} and V_{18} changing to zero vectors V_0 and V_{19} (b) V_3 changing over to V_{20} (c) V_{17} switched to zero vector V_0 (d) V_{14} changing over to V_{19} .



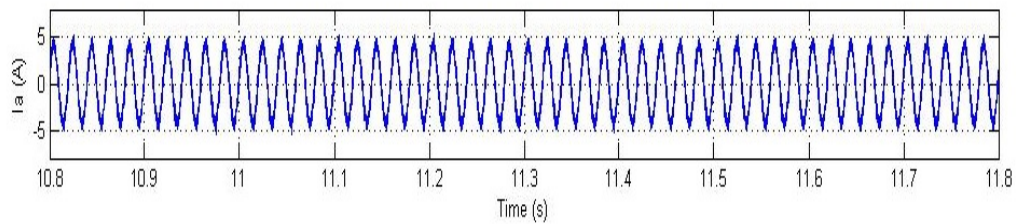
(a)



(b)

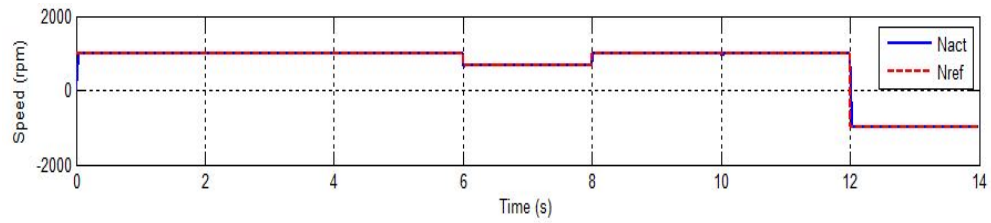


(c)

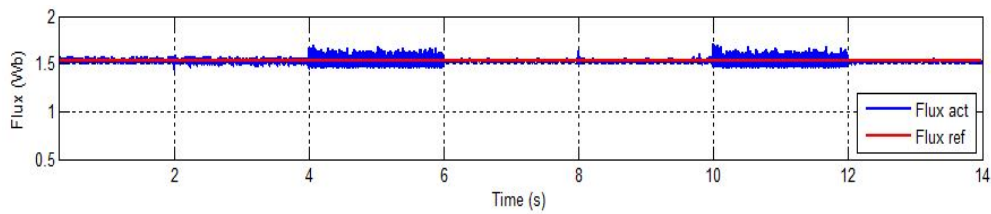


(d)

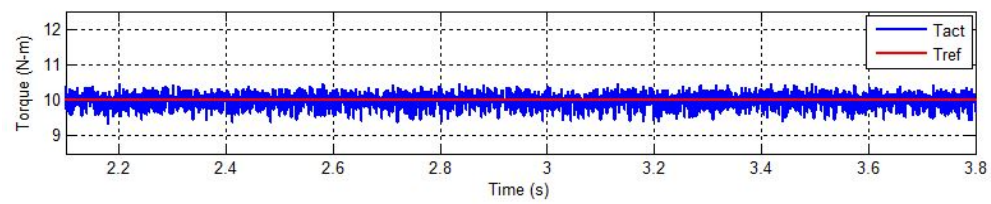
Figure 5.17 Response of (a) Active power (b) Reactive power (-500 VAR) (c) DC Voltage (600 V) (d) Supply side current waveform (I_a : 2.8 A rms) at different steady and transient state conditions.



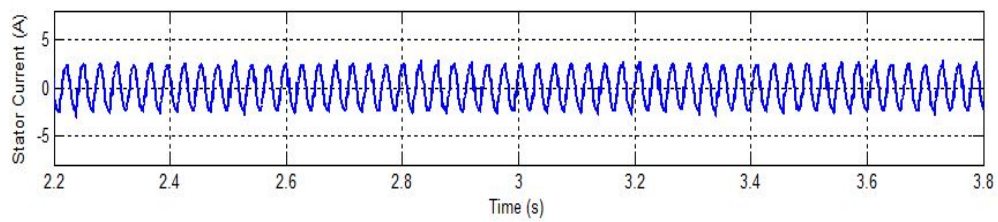
(a)



(b)



(c)

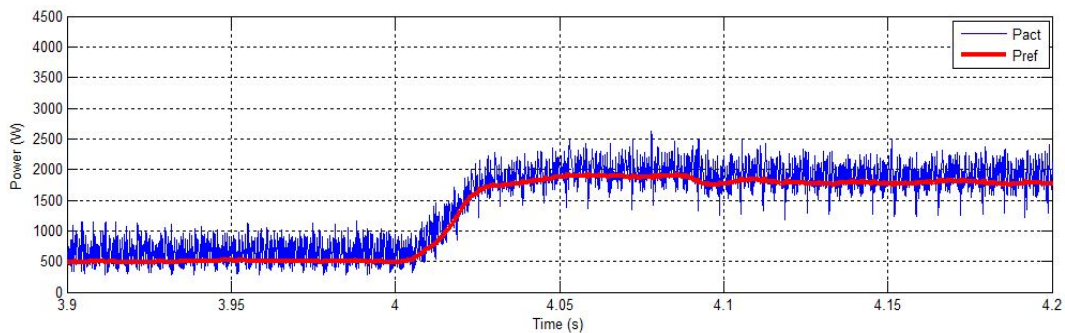


(d)

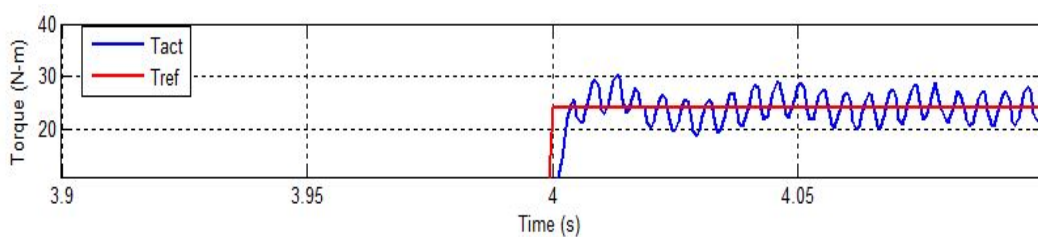
Figure 5.18 Response of the IMD during reference speed change and reversal: (a) Speed (1000- 680- 1000- -1000 rpm) (b) Flux (1.53 Wb) (c) Torque (10 N-m) (d) Stator Current (i_a : 2.12 A rms).

5.5.2 Power Quality Performance during transient operating conditions

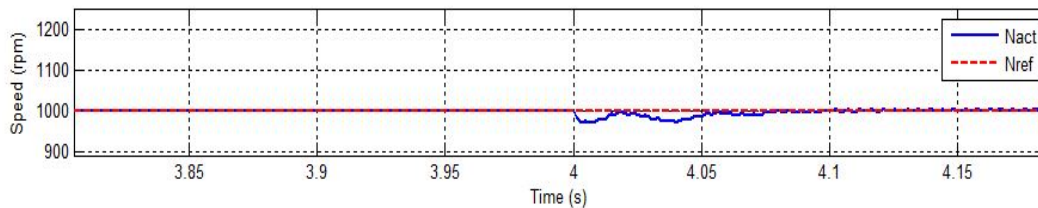
The performance of the system for a step change in the load i.e, from 10 N-m to 25 N-m is illustrated in Fig. 5.19. In this case, the active power at grid side overshoots (Fig. 5.19a) to 2226 W and it settles within 0.06s, from the time the torque disturbance is created. The peak overshoot in load torque is 20.79% and settling time is about 0.06 s as shown in Fig. 5.19b while the speed is maintained constant at 1000 rpm. However, speed dips to 969 rpm for a short-while during increase in load which bounces back to the original value within 3 cycles.



(a)



(b)

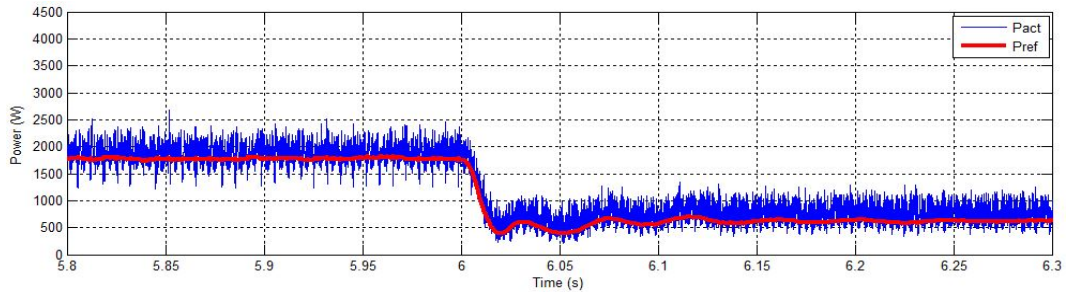


(c)

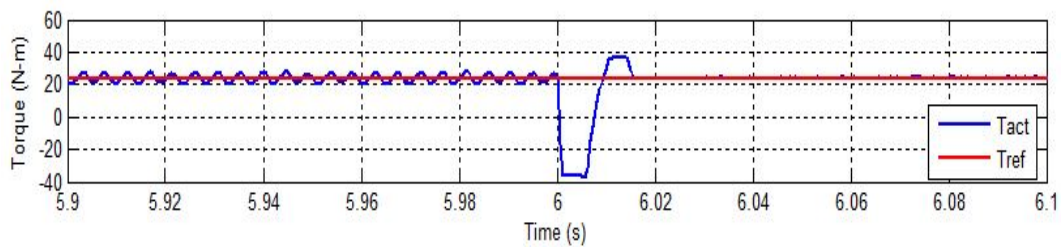
Figure 5.19 Response of (a) Power (500 W to 1700 W) (b) Torque (10 N-m to 25 N-m) (c) Speed (1000 rpm) when Torque changes with speed remaining constant.

The transient behavior for a sudden change in the reference speed i.e., from 1000 rpm to 680 rpm at 6s while maintaining constant load torque (25 N-m) and repercussion on the grid side are illustrated in Fig. 5.20. Active power at grid side in Fig. 5.20a dips to 280 W and settles within 0.22 s. At the

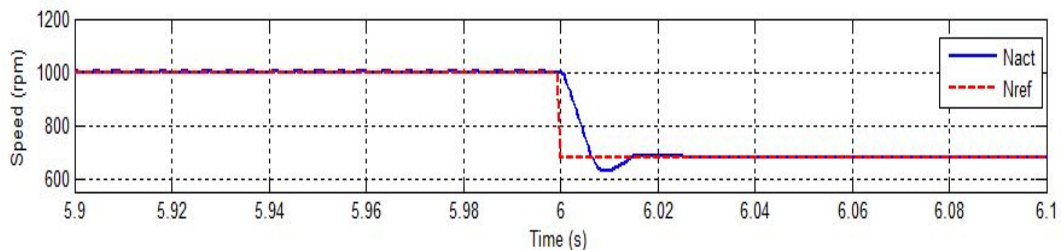
same time, to achieve a fast response, the torque dips to -36.7 N-m in Fig. 5.20b. Fig. 5.20c shows an undershoot in speed which corresponds to 626.7 rpm. However, the speed settles to the reference value within three cycles.



(a)



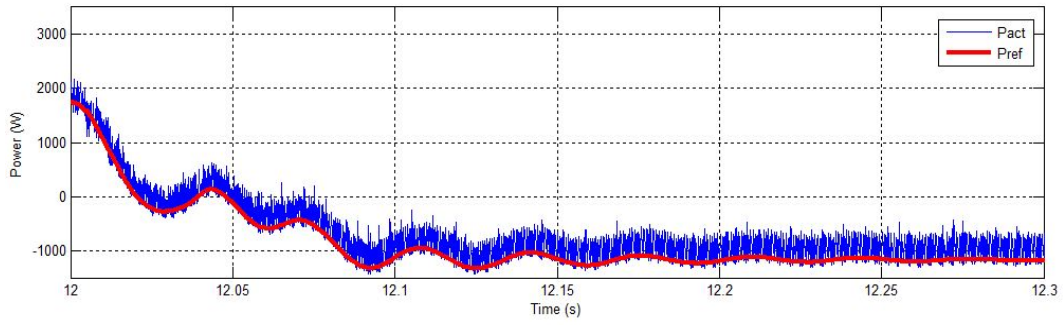
(b)



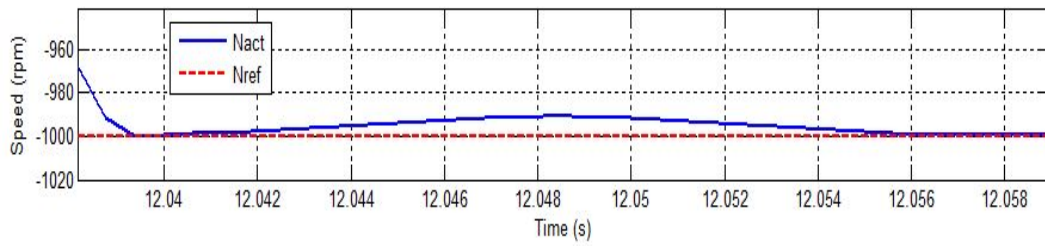
(c)

Figure 5.20 Response of (a) Power (1700 W) (b) Torque (25 N-m) (c) Speed (1000 rpm to 680 rpm) when speed changes with load torque remaining constant.

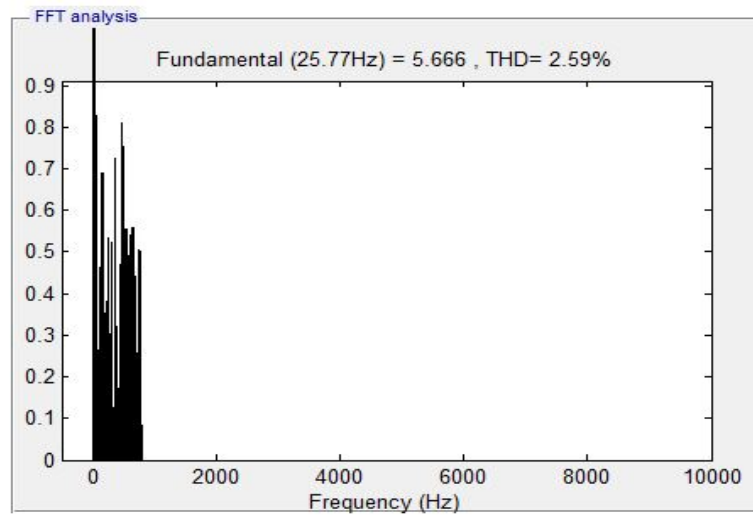
Fig. 5.21 shows power and speed responses of the drive when speed reversal takes place. The drive takes about 0.06 s for reversal. During this time, the grid side power dips to -1347 W and settles within 0.25 s. The proposed optimal voltage vector selection algorithm is implemented both on three level diode clamped rectifier (grid side) and inverter (load side). During the application of voltage vectors which have redundancies, efficient voltage vector logic is applied to these converters. The THD analysis in Fig. 5.21c is carried out for the stator current of the IMD, which is found to be 2.59%. Table 5.2 shows the number of switchings with and without optimal choice of voltage vectors at $(k + 1)^{th}$ instant of time.



(a)



(b)



(c)

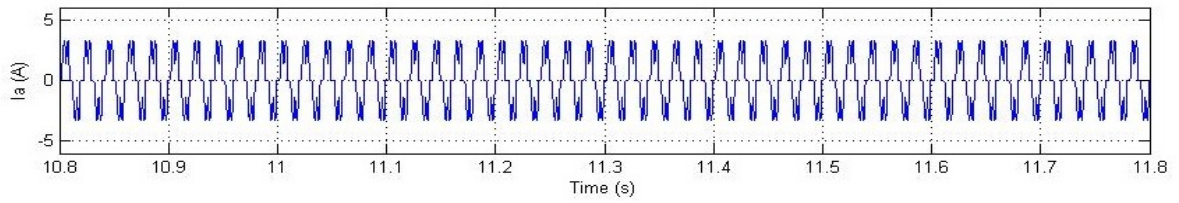
Figure 5.21 Response of IMD during machine reversal (a) Power (-1000 W) (b) Speed (1000 rpm to -1000 rpm) (c) THD (2.59 %) analysis for stator current (i_a) in three level inverter fed IMD using PTC.

Table 5.2 Number of switchings during optimal voltage vector logic algorithm applied to both three level neutral point clamped rectifier (grid side) and inverter (load side) at $(k + 1)^{th}$ instant.

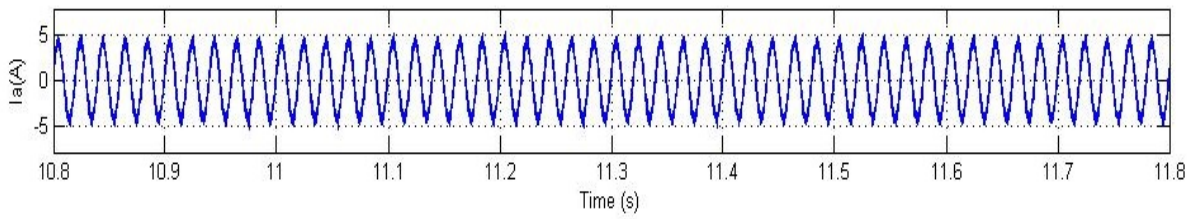
Type of converter	No. of switchings without optimal voltage vector logic at $(k + 1)^{th}$ instant (in million)	No. of switchings with optimal voltage vector logic at $(k + 1)^{th}$ instant (in million)
Three level rectifier (for DPC)	3.666	0.3647 (90.05% less switching)
Three level inverter (for PTC)	0.5528	0.5282 (4.45% less switching)

The magnitude and THD value of supply current with and without AFEC are shown in Fig. 5.22. Fig. 5.22a shows the current waveform (which is highly non-sinusoidal) with DBR in the front end where the THD is 50.25% (Fig. 5.22c), whereas with direct power control algorithm applied to the three-level diode clamped converter acting as the AFEC, the phase current is fairly sinusoidal (Fig. 5.22b) and the corresponding THD value is reduced drastically to 3.67% (Fig. 5.22d). This clearly shows that DPC algorithm works very well improving the power quality at the PCC significantly.

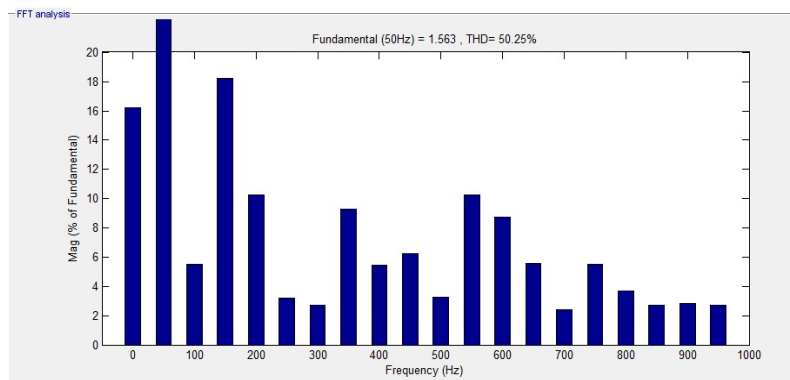
Thus, the simulation of two-level and three-level VSI fed IMD with AFE rectifier with classical DTC and PTC both have been carried out along with DPC at the front end.



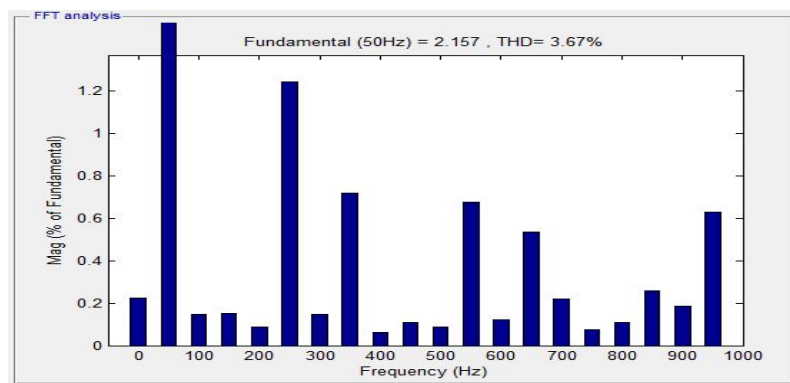
(a)



(b)



(c)



(d)

Figure 5.22 Response of Supply current ($I_a : 2.8 \text{ A rms}$)(a & b) : (c) THD=50.25% without AFEC and only diode bridge rectifier (DBR) (d) THD=3.67% when DPC applied to the AFEC.

5.6 Conclusion

It is very clear that the three level VSI has less torque and current pulsations as compared to a two level VSI fed DTC IMD. The proposed PTC algorithm with optimal voltage vector selection, thus, not only reduces the switching losses but also improves the performance in terms of torque and current pulsations and THD of stator current. Novel control strategy for an IMD with AFE rectifier controlled by DPC at the front end and multilevel inverter controlled by PTC at the load end also shows a better performance for the motor drive in terms of less torque and current pulsations. Simultaneously, AFE rectifier shows better performance in terms of active and reactive power consumption during different load conditions. The THD of the supply current at the PCC with AFEC working on the proposed DPC algorithm is found to be 3.67%, whereas when the front end converter is a DBR, the THD at the PCC was 50.25%. This shows the effectiveness of using an AFEC with a suitable control configuration.

Chapter 6

Hardware Setup for the PTC based adjustable speed Induction Motor Drive implementation using FPGA

6.1 Introduction

The proposed novel predictive torque control (PTC) approach for multilevel inverter (MLI) fed IMD is presented in the previous chapters and subsequently modeled and simulated in MATLAB/SIMULINK environment. The results were presented in the previous chapter. Further, this algorithm is implemented using field programmable gate arrays (FPGA), as an interfacing device between the software and the inverter fed induction motor (hardware), the details of which are presented in this chapter. The hardware implementation could be carried out very well even with involved computations of the PTC algorithm because of the fast processing speed of FPGA. Here, the FPGA implementation is carried out on Xilinx ZynqTM – 7000 All Programmable SoC (AP SoC).

6.2 System description

The Zed (ZynqTM Evaluation and Development) Board [116] is an advanced and decision-making board, the heart of which is Xilinx ZynqTM – 7000, an “All Programmable SoC” (AP SoC). A laboratory prototype for the VSI fed IMD is developed using this Xilinx® XC7Z020-1CLG484C Zynq-7000 AP SoC based controller board incorporating Hardware-in-loop method in order to validate the simulation results. The block diagram of the complete hardware setup is shown in Fig. 6.1 and its photograph is

depicted in Fig. 6.2.

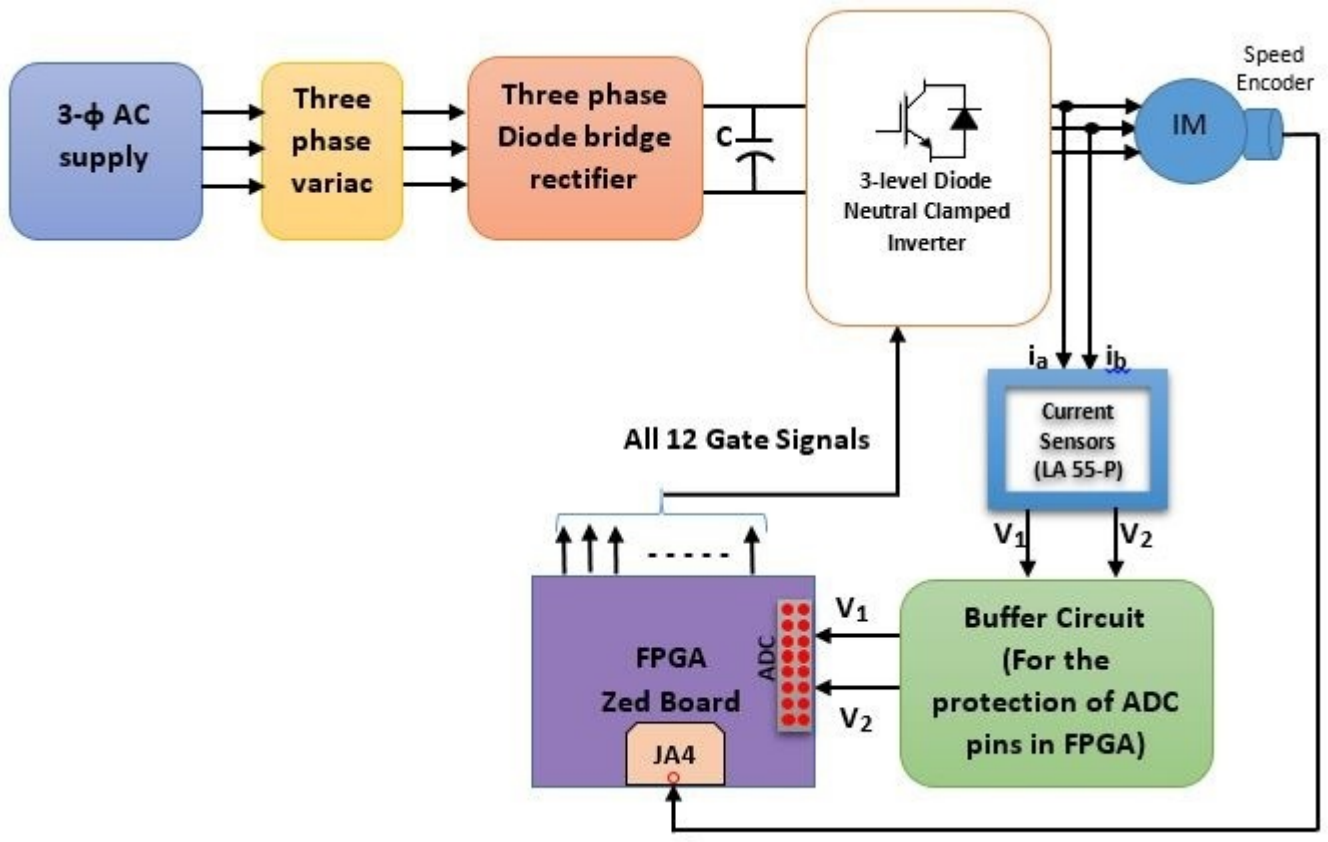


Figure 6.1 Block diagram of the hardware setup for the three-level neutral point clamped (NPC) inverter fed induction motor

The induction motor [117] (whose parameters are mentioned in the A.1)) is coupled with a separately excited DC machine to enable it to be loaded. During the loading conditions of the induction motor at different speeds and regenerative modes, the DC machine armature is controlled appropriately to realize four quadrant operation of the IMD.

A 3- ϕ 415V50 Hz AC supply is fed to the 3- ϕ Semikron Diode Bridge Rectifier [118] (SKD 2516 Module) through a three phase variac. A 2500 μ F DC link capacitor is used to filter out the voltage ripples before being fed to the three-level inverter whose output energizes the induction machine. The speed of the motor is sensed through an encoder (EN-901) [119]. The proposed algorithm requires motor currents and speed as inputs to generate the gate pulses for the inverter devices from the FPGA which are isolated and amplified before being connected to the gates of the power devices.

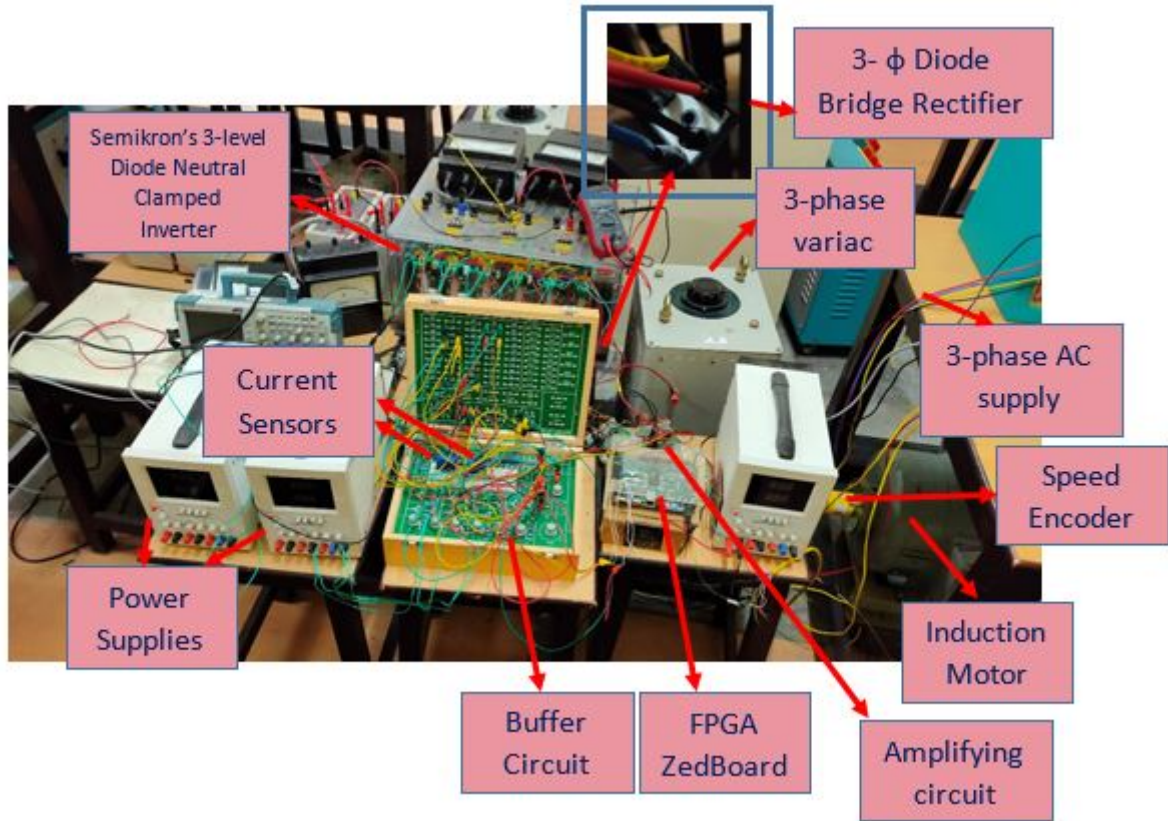


Figure 6.2 PTC-based IMD laboratory prototype controlled by FPGA

6.3 Control configuration

The FPGA board consists of IO ports, ADC and DAC pins. Two inputs, namely, speed and motor currents are provided to the board. Speed of the motor is obtained from the encoder in the form of pulses. The encoder generates 400 PPR (Pulses Per Revolution). Further, these pulses are fed to the JA4 (Signal Name)-AA9 (Zynq pin) through a voltage divider circuit (as shown in Fig. 6.3) that reduces the voltage level of the pulses generated at 4.4V (from the encoder) to 3.3V. The resistance values taken are: $R_1 = 50\Omega$, $R_2 = 150\Omega$.

Current Sensors LA 55-P [120] are used to sense the motor currents as shown in Fig. 6.2. Besides, the “Analog header port” (AHP) provides analog connectivity for analog reference signals. Since the required maximum voltage is 1V peak-to-peak, a buffer circuit with Op-amps LM 741 is used in between the current sensors and AHP. Auxiliary analog input channels 0 & 8 (VAUX0P: XADC-AD0P-R: F16 /VAUX0N: XADC-AD0N-R: E16 & VAUX8P: XADC-AD8P-R: D16 /VAUX8N: XADC-AD8N-R: D17) are the dedicated channels needed for simultaneous sampling applications. Analog header port is shown in Fig. 6.4.

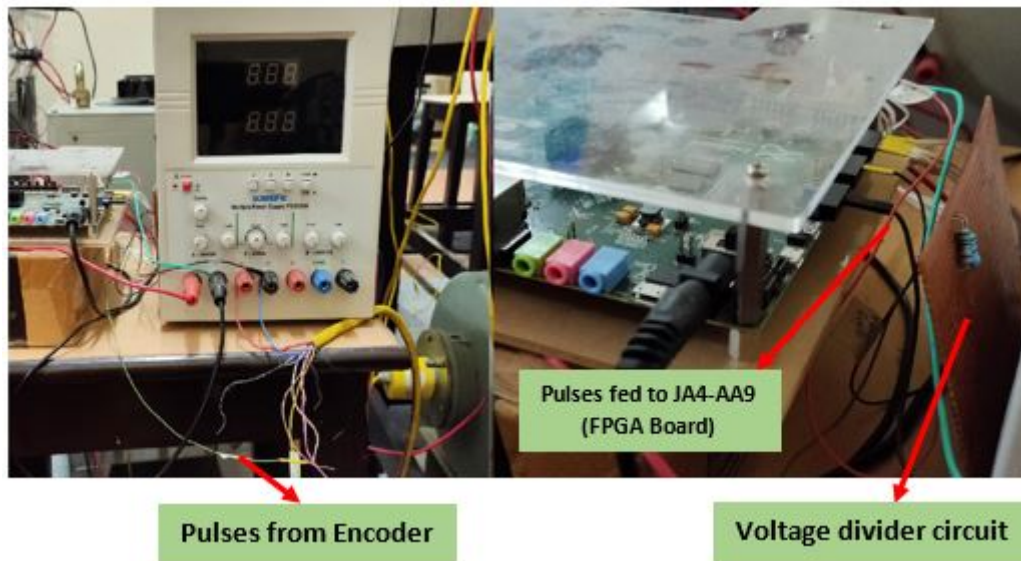


Figure 6.3 Pulses shifting from encoder to FPGA

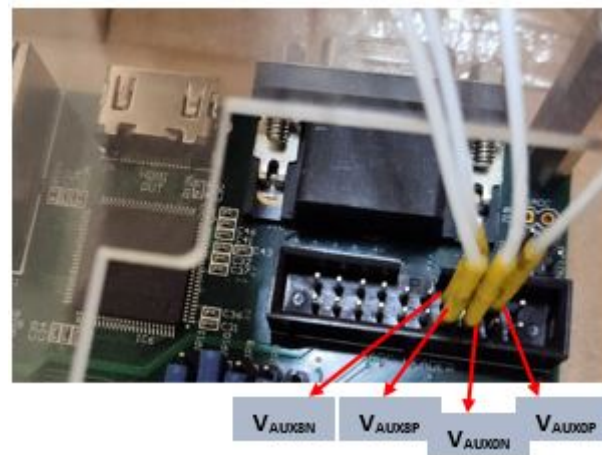


Figure 6.4 Analog Header Port

6.4 Signal processing and amplification

The 12 PWM pulses generated from FPGA board are fed to the three-level NPC [121] inverter through an amplifying circuit that shifts the voltage level of 3.3V from the board to 15V. These pulses are assigned to specific pins as shown in Table 6.1. Further, the outputs from these pins are fed to gate drivers of the inverter through an amplifying circuit as represented in Fig. 6.5. The amplifying circuit consists of LM 339 Quad Op-amps, observed in Fig. 6.6. The switching and sampling frequencies along with gains of the PI controller are mentioned in the Appendix A.2.

Table 6.1 Signal and Zynq pins from which respective PWM pulses are fed to the gate drivers of the inverter.

PWM Pulse	Signal Name	Zynq pin
1	JB1	W12
2	JB2	W11
3	JB3	V10
4	JB4	W8
5	JB7	V12
6	JB8	W10
7	JB9	V9
8	JB10	V8
9	JC1_N	AB6
10	JC1_P	AB7
11	JC2_N	AA4
12	JC2_P	Y4

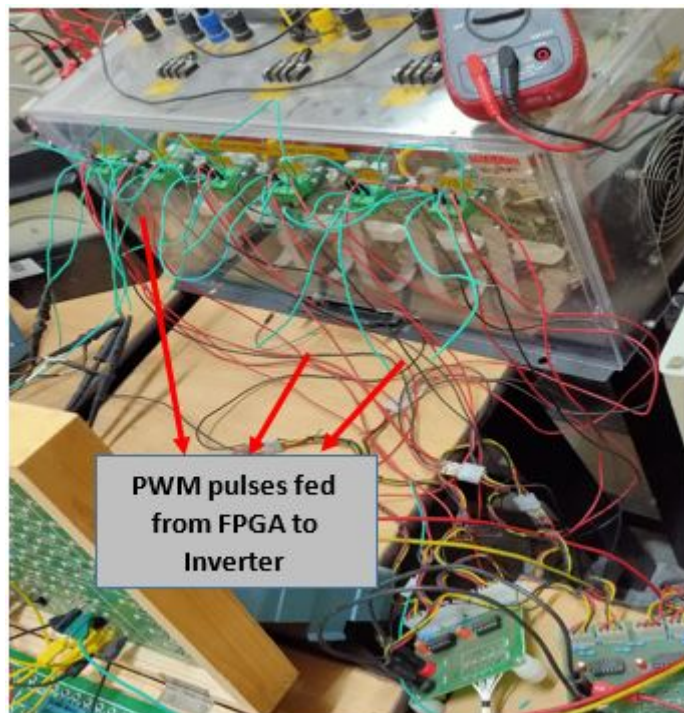


Figure 6.5 Amplifying circuits through which PWM pulses from FPGA board are fed to the gates of the devices in the inverter.

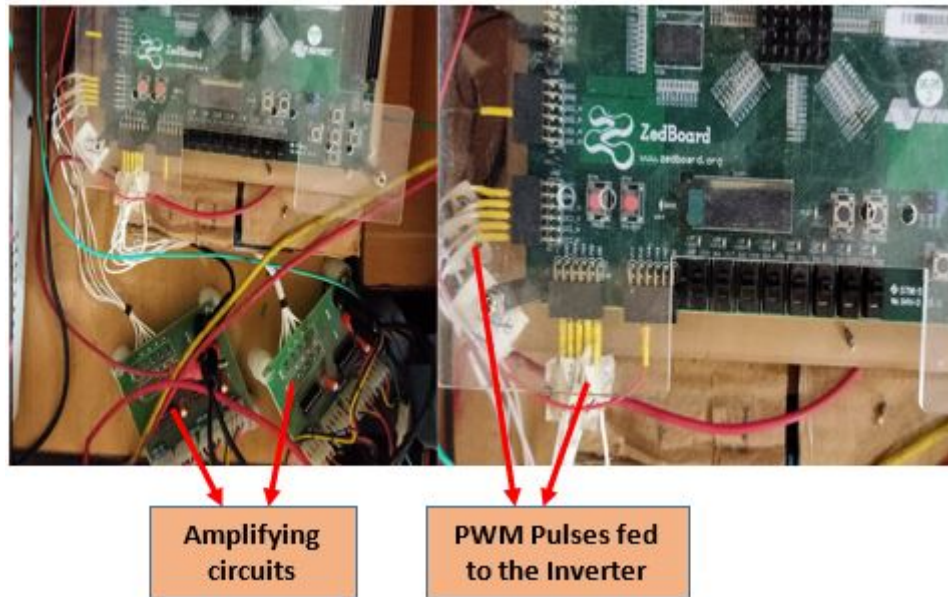


Figure 6.6 Amplifying circuits and PWM output pins of the FPGA board.

6.5 Conclusion

This chapter presented the details of the hardware implementation of the three-level VSI fed IMD using FPGA controller. Various parts of this controller have been explained clearly with block diagrams and photographs. The control algorithm implementation using the FPGA works really fast because of parallel processing. The next chapter shows the software developed and the results obtained using PTC implementation in FPGA platform.

Chapter 7

Experimental Results

7.1 Introduction

The hardware implementation of proposed novel predictive torque control algorithm has been carried out for three level diode clamped inverter fed IMD. A laboratory prototype has been developed (as discussed in Chapter 6) for multilevel inverter fed IM using PTC. The novelty involved is in selecting the optimal voltage vectors for impressing a reference voltage space vector to the stator of a three-phase induction motor deduced by making use of PTC. The parameters of the induction motor are mentioned in Appendix A.1. The steady state and dynamic responses obtained from the experimental set up are detailed in the following sections.

7.2 Steady State responses

Block diagram of the experimental setup for the implementation of PTC algorithm for a three phase three level diode clamped inverter feeding an induction motor, is shown in Fig. 7.1.

A 3- ϕ , 50 Hz, 415V supply is connected to a three phase diode bridge rectifier whose output is fed to the diode clamped 3-level inverter which is energizing the induction motor at the required voltage magnitude and frequency. FPGA board generates the firing pulses for the inverter devices as per the PTC algorithm.

The PTC algorithm requires two inputs i.e., stator current (i_s) and speed (ω). The current is sensed by current sensor(s) and fed to the FPGA board through an ADC. The speed obtained from the encoder (in the form of a digital signal) is passed through a DAC before being displayed in a digital storage

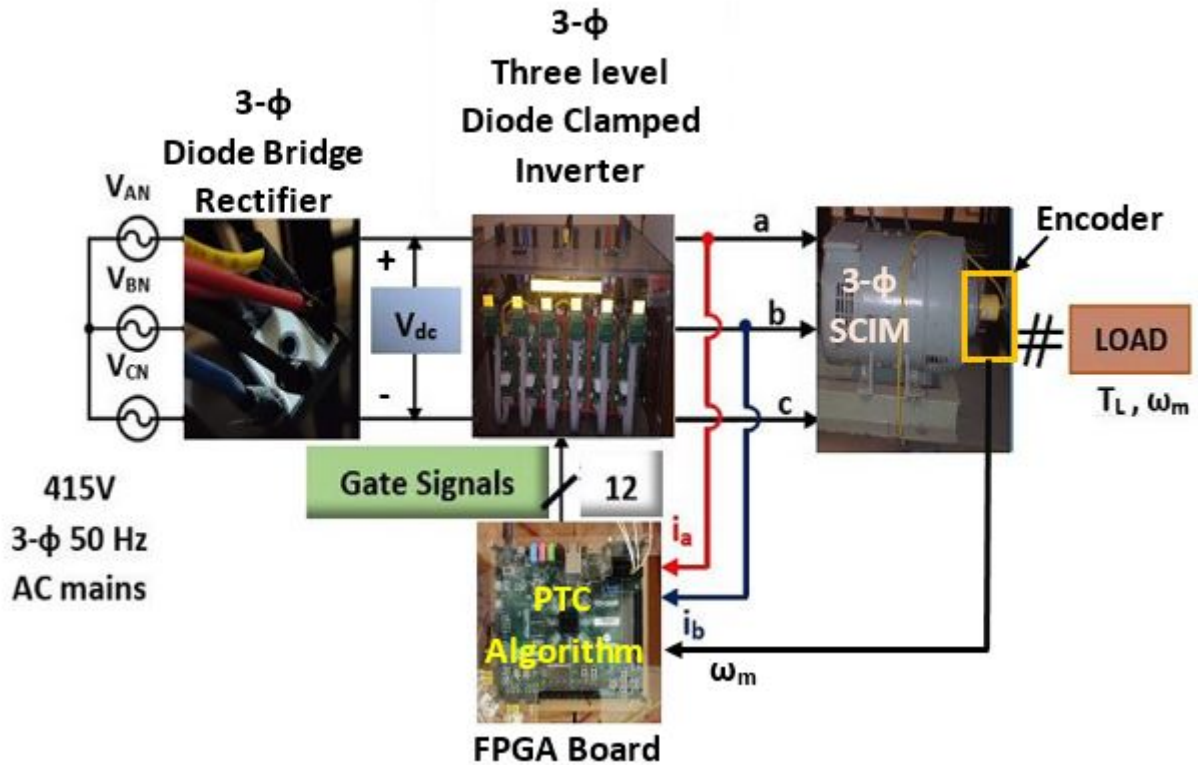


Figure 7.1 Block diagram of hardware implementation of PTC algorithm of three phase three level diode clamped inverter fed 3- ϕ Squirrel Cage Induction Motor (SCIM)

oscilloscope (DSO). The steady state response of the motor drive, in terms of stator currents (i_a & i_b) and speed at no-load condition, while the motor is running at 1425 rpm are shown in Figs 7.2 and 7.3, respectively. The X-Y axis scale observed in CRO for Fig 7.2 is: X scale: 20 msec/div; Y scale: 5 A/div.

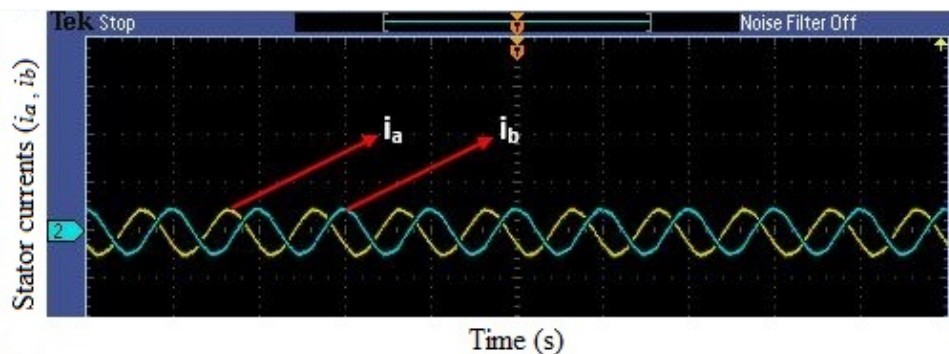


Figure 7.2 Steady state response of stator currents (i_a, i_b) of 2 Amps; Scale X: 20 msec/div, Y: 5A/div

The generated gate pulses for all 12 switches are depicted in Fig. 7.4 (for g_1, g_2), Fig. 7.5 (for g_3, g_4), Fig. 7.6 (for g_5, g_6), Fig. 7.7 (for g_7, g_8), Fig. 7.8 (for g_9, g_{10}) and in Fig. 7.9 (for g_{11}, g_{12}). The X-Y axis scale observed in CRO for all the gate pulses is: X scale: 20 msec/div; Y scale: 2 V/div. The optimal voltage vector selection was already presented in Table 4.7 which has been made use to generate these gate pulses.

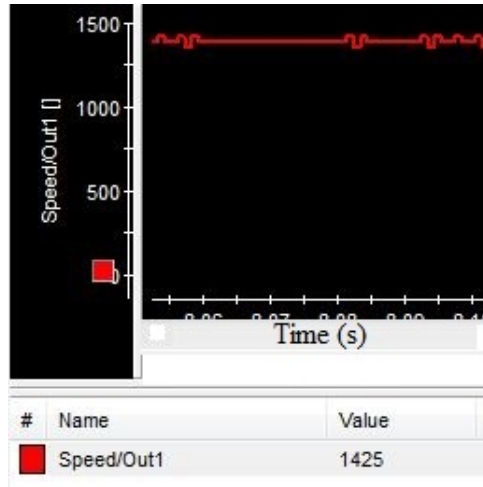


Figure 7.3 Steady state response of speed at 1425 rpm; Scale X: 20 msec/div, Y: 250 rpm/div

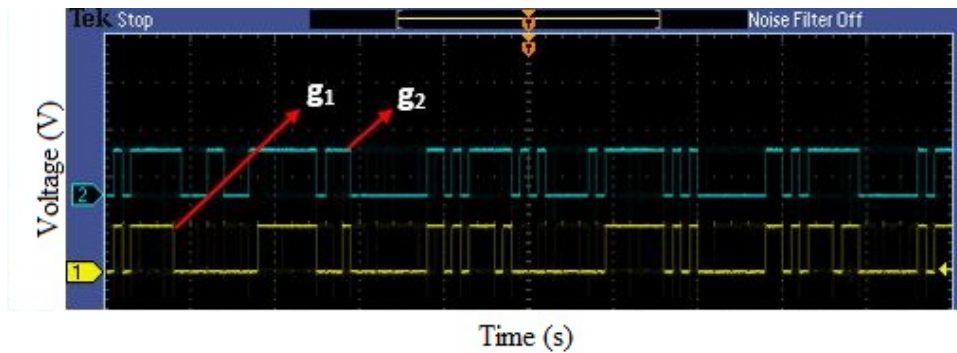


Figure 7.4 Generated pulses for Gates g1, g2; Scale X: 20 msec/div, Y: 2V/div

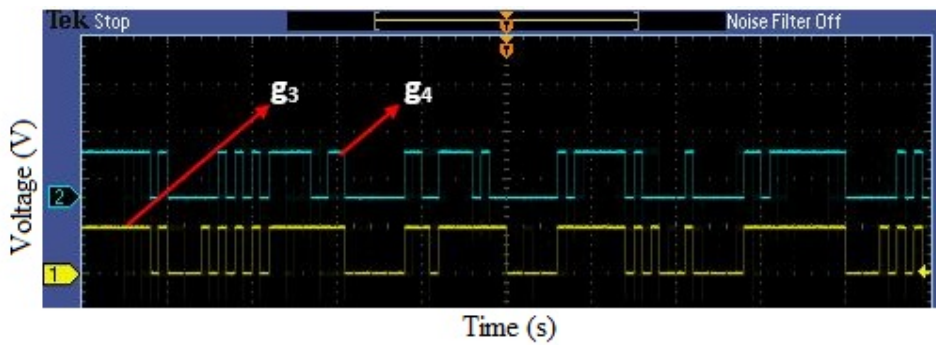


Figure 7.5 Generated pulses for Gates g3, g4; Scale X: 20 msec/div, Y: 2V/div

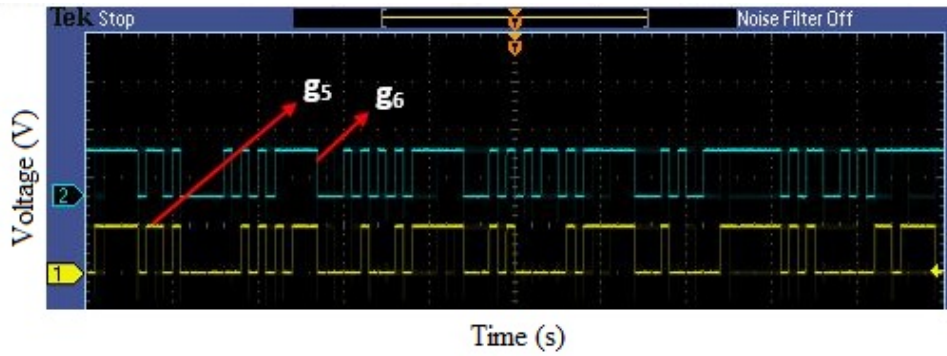


Figure 7.6 Generated pulses for Gates g5, g6; Scale X: 20 msec/div, Y: 2V/div

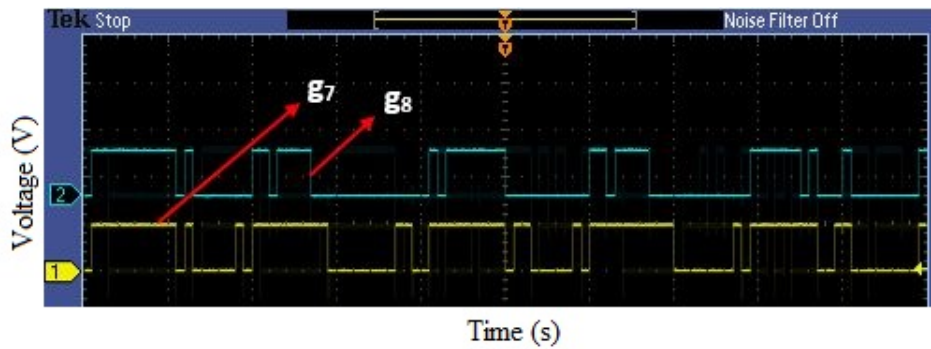


Figure 7.7 Generated pulses for Gates g7, g8; Scale X: 20 msec/div, Y: 2V/div

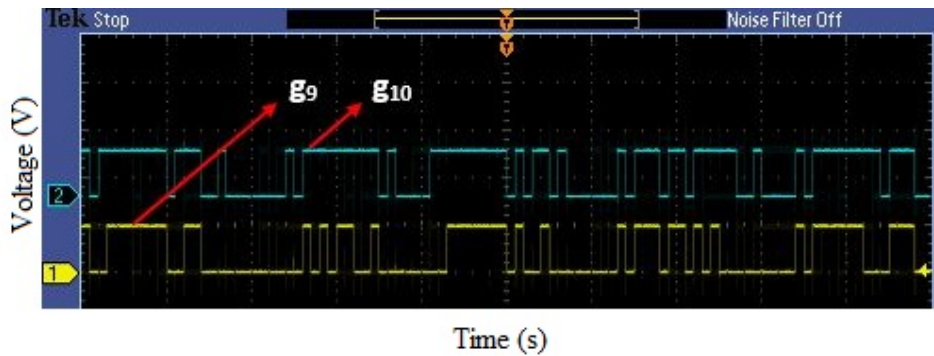


Figure 7.8 Generated pulses for Gates g9, g10; Scale X: 20 msec/div, Y: 2V/div

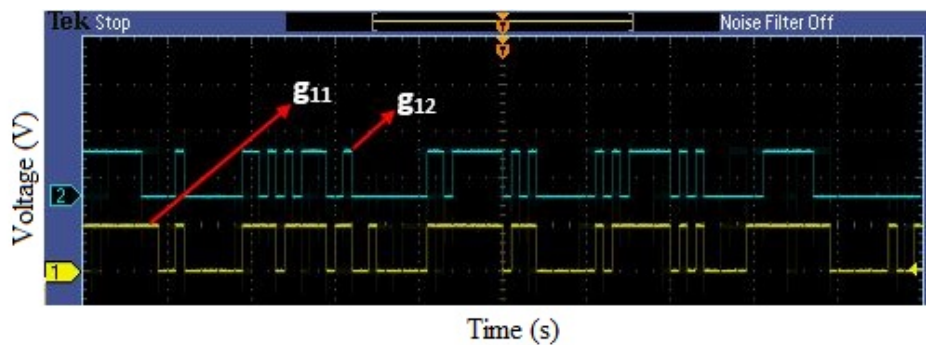


Figure 7.9 Generated pulses for Gates g11, g12; Scale X: 20 msec/div, Y: 2V/div

With a DC output of 160V from the rectifier, the AC voltage generated was about 110V (line-to-line rms). The sampling frequency used was 1 kHz. Under this condition, the line voltage (V_{ab}) at the output of the inverter depicted in Fig. 7.10 and the X-Y axis scale observed in CRO is X scale: 20 msec/div; Y scale: 50 V/div.

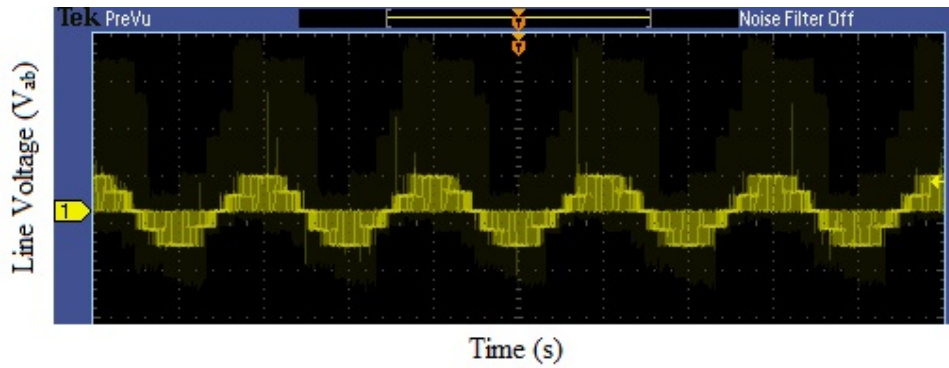


Figure 7.10 Response of line voltage (V_{ab} : 110 V) at the Output of the inverter; Scale X: 20 msec/div, Y: 50V/div

7.3 Dynamic Responses

During dynamic conditions, the capability of the IMD to take on load was observed. Also, its ability to track the variations in reference speed was also observed. These responses were tested at a reduced voltage of about 30V (line to line rms) with the motor loaded upto 2 Amp even at this reduced voltage. The line voltage being 29 V in all the three lines is depicted in Fig. 7.11. The line currents (in 2 of the 3 lines) are shown in Fig. 7.12 and its X-Y axis scale observed in CRO is X scale: 20 msec/div; Y scale: 5 A/div.

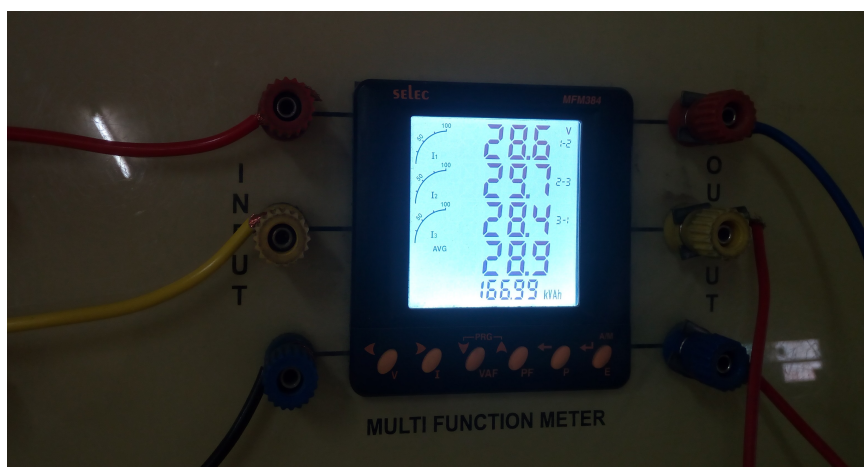


Figure 7.11 Response of the rms line voltage of 28.9 V observed at the input of the motor

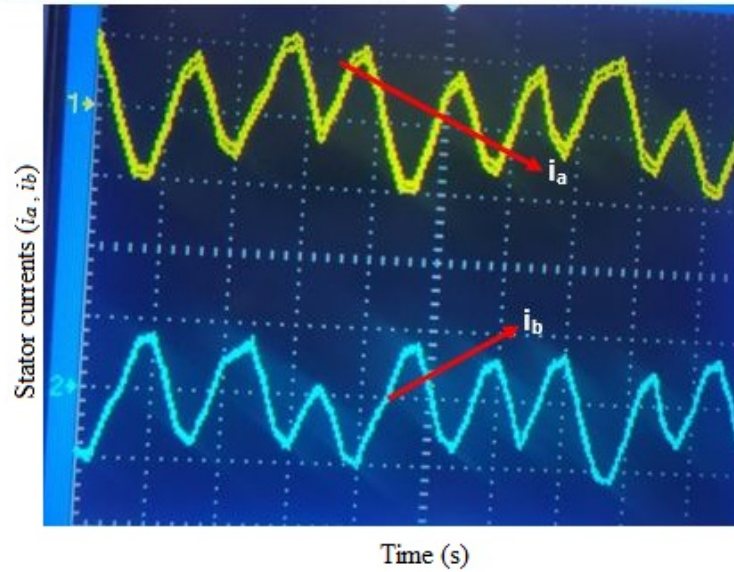


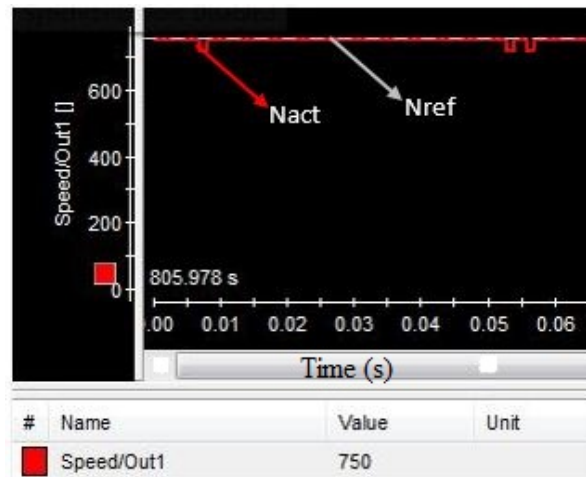
Figure 7.12 Response of the stator currents i_a and i_c (2 A) of the motor; Scale X: 20 msec/div, Y: 5A/div

Two cases were studied to know the response while tracking the ω_{ref} . In first case, ω_{ref} is set to 1015 rpm and the ω_{act} is changed from 1050 rpm to 1015 rpm. The motor was found to track the speed effectively in a matter of a few cycles. In the second case, ω_{ref} in the algorithm is set to three different speeds i.e. 750 rpm, 825 rpm and 900 rpm and the load applied at the respective speeds is shown in Table 7.1. The stator current of the motor at different ω_{act} speeds are shown in Figs 7.13 (4 A pk-pk), 7.14 (4.3 A pk-pk) and 7.15 (4.7 A pk-pk) respectively. It is clear that the frequencies of the stator currents are changing correspondingly. Respective X-Y axis scale observed in CRO is X scale: 20 msec/div; Y scale: 5 A/div, 100& 250 rpm/div.

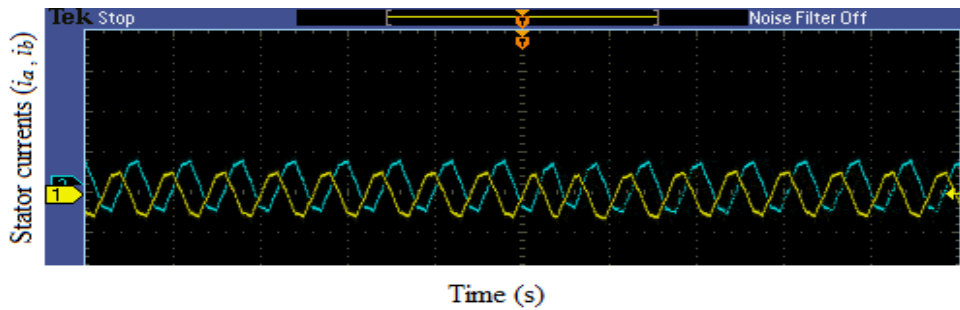
During load conditions, the response of the load torque has been observed in the following Table 7.1. Neglecting the efficiency of the DC machine, load voltage and current were taken into account as the DC generator output, in the estimation of load torque.

Table 7.1 Response of Load torque during dynamic condition of hardware implementation.

N(rpm)	V_L (Volts)	I_L (Amps)	T_L (N-m)
Speed	Load Voltage	Load Current	Load Torque
900	215	5	11.4
862	211	4	9.3
825	200	3	6.9
787	195	5	11.8
750	190	6	4.5

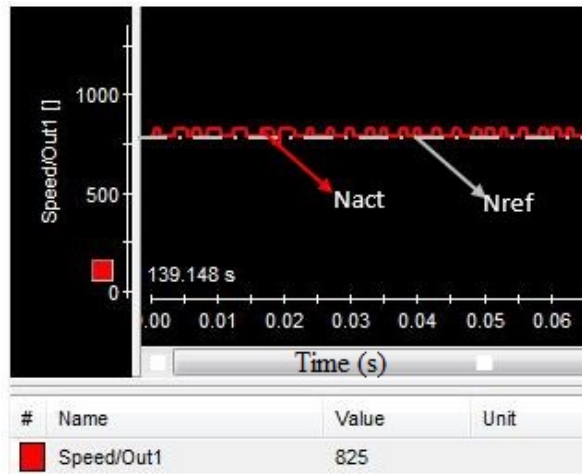


(a)

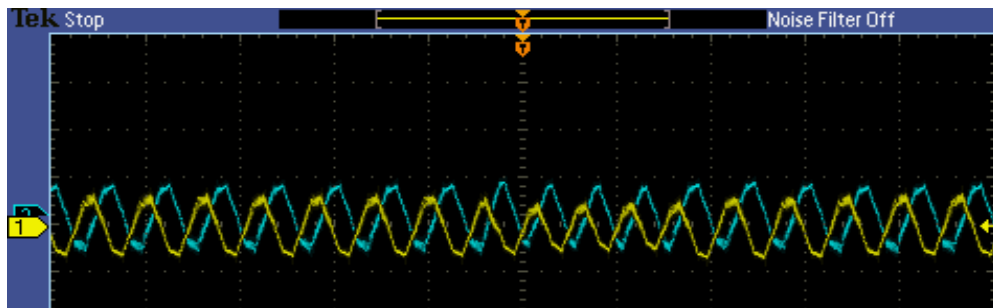


(b)

Figure 7.13 Response of (a) ω_{act} at 750 rpm, (b) stator phase currents (i_a & i_b) of 4 A pk-pk; Scale X: 20 msec/div, Y: 5A/div, 100 rpm/div

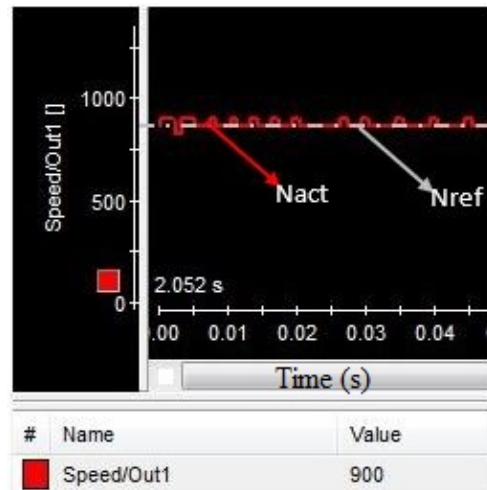


(a)

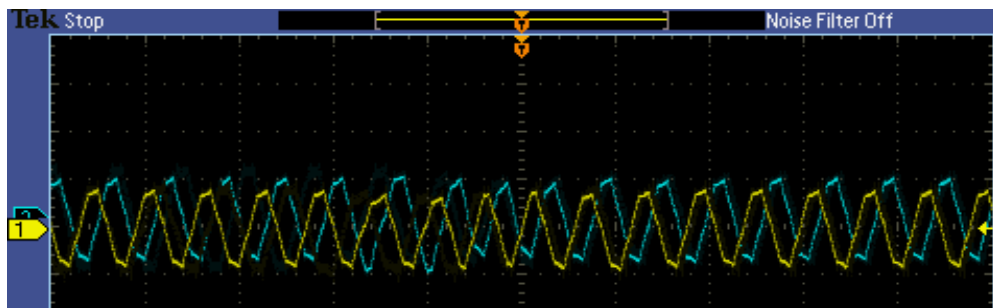


(b)

Figure 7.14 Response of (a) ω_{act} at 825 rpm, (b) stator phase currents (i_a & i_b) of 4.3 A pk-pk; Scale X: 20 msec/div, Y: 5A/div, 250 rpm/div



(a)



(b)

Figure 7.15 Response of (a) ω_{act} at 900 rpm, (b) stator phase currents (i_a & i_b) of 4.7 A pk-pk; Scale X: 20 msec/div, Y: 5A/div, 250 rpm/div

7.4 Conclusion

This Chapter presented the results of hardware implementation of the 3-level inverter fed three-phase cage IMD using FPGA. PTC algorithm has been implemented in FPGA board and corresponding phase currents and speed responses of the drive has been shown for different operating conditions. The stator currents are also depicted along with gate pulses to the inverter devices. The waveforms show the proper working of the three-level inverter and the control algorithm.

Chapter 8

Conclusion and Future Work

8.1 Introduction

The objectives of this research work are to design, analyze, model, simulate and implement in hardware a novel predictive torque control scheme for a 3-phase IMD fed by an SVM based three-level inverter. The modified space vector modulation technique put forth in this work reduces the number switchings per cycle by selecting an optimal sequence of voltage vectors during every sampling interval. Later, the front end diode rectifier has been replaced by a converter with self-commutating devices to achieve direct power control. The conclusions drawn from this thesis work and the scope for future work are elaborated in this chapter.

8.2 Main Conclusions

This work presents the performance of a three-phase induction motor controlled by DTC technique. Initially, a two-level inverter fed SVM based DTC IMD has been analyzed. Then, reduced switch three-level inverter and an NPC three-level inverter both have been explored for implementing classical DTC as well as PTC. An objective comparison between a three-level VSI and a two-level VSI fed DTC drives has been brought out under steady state operation and also during load perturbations and speed disturbances.

The two-level and three-level VSI fed IMDs have been modelled in MATLAB/SIMULINK environment and are simulated under various operating conditions such as steady state operation, load perturbation, reference speed change and speed reversal. It is found that the three-level VSI fed DTC drive always out-performs the two-level VSI DTC drive in terms of response time, speed and torque overshoots and

undershoots, torque and current ripples. If a high response application demands lower values of speed and torque ripples then, from the obtained results, it can be concluded that the three-level VSI fed DTC drive is the obvious choice. However, complexity of the circuit and computations in the switching logic are more in the 3-level case; so, judicious choice needs to be made on the basis of performance expectations and the cost and complexity involved.

A model predictive control algorithm with efficient zero vector placement is proposed and implemented for the VSI fed DTC drive wherein the inverter devices are fired by the novel SVM technique. The algorithm is not only simple to implement but also it could reduce torque and current ripples. DTC and PTC have been investigated on a reduced switch three level inverter fed IM drive. It is observed that the predictive torque control algorithm has superior performance in terms of output current THD (0.34% in PTC and 15.77% in DTC), torque ripple (0.4% in PTC and 21.2% in DTC), settling time (0.9 ms in PTC and 8 ms in DTC) etc. as compared to the classical DTC. The proposed algorithm improves the dynamic response and reduces the losses incurred as the number of switchings decrease. The algorithm is modeled and simulated with the help of Matlab/Simulink software tool for analyzing its transient and steady-state operations. The obtained current and torque ripples, overshoots, settling times, THD values are reported. The results show a tangible improvement in the performance of a PTC based drive as compared to a classical DTC drive.

The PTC algorithm has been applied to both two level and three level inverter fed IM drive. It is observed that the PTC algorithm for a three level inverter yields a better performance in terms of output current THD, torque ripple and current ripple, as compared to a two level inverter fed IMD. The proposed PTC algorithm is simple to implement and also improves the efficiency due to the reduction in the number of switchings. While 0.54% is the reduction in the number of switching transitions during the switching process in the proposed PTC algorithm for two level inverter fed IMD, the reduction in the three-level case is 5.07%. Thus, the proposed PTC algorithm is recommended for torque/speed control applications that require faster and ripple-free performance.

Finally, the experimental investigations have been carried out to corroborate the simulation results. The results obtained from a PTC based three-level inverter fed three-phase IMD controlled by an FPGA show that the drive performs extremely well under various dynamic and steady state operating conditions.

The direct power control strategy on the front end converter and predictive torque control on the motor side converter are implemented for a multi-level inverter fed IMD by modelling these converters in Simulink environment. Three level NPC converters are used at the front end as well as at the load end. The simulated results shows the performance of the active and reactive power control of the AFEC working effectively. Similarly, torque, speed and stator current variations under different load conditions have been observed for the multi-level inverter fed IMD which is controlled by PTC on the motor side. During the switching condition, the choice of selection of optimal voltage vector is done in such a manner (wherever redundancy exists) that the number of switching transitions are reduced. Because of this, a considerable reduction in switchings of the AFE rectifier and multi- level inverter at the motor end, could be attained. The THD of the output current at the motor side is observed to be 2.59% which is less when compared with the classical DTC method presented in the literature. Also, the THD of the supply current at the PCC with proposed DPC algorithm applied to the three-level diode clamped converter which functions as the AFEC, has been improved to 3.67% as compared to the DBR case (where the THD at the PCC was 50.27%). The complete behavior of the system in all the four quadrants not only yields better performance of the drive, but also brings down the losses, since the number of switchings are reduced due to optimal voltage vector selection logic.

In all, this work has presented two-level and three-level VSI feeding a DTC and PTC based three-phase IMDs wherein simulations have been carried out for various steady state and dynamic operating conditions to find that improved performance and reduced losses have been achieved. Further, experimental prototype has been implemented in the laboratory using FPGA.

8.3 Scope for Future work

- The novel PTC algorithm with efficient vector placement can be tested on Five-level and seven-level inverters.
- Active front end converter can be implemented in hardware for the inverter fed IMD.
- Reduced-switch three-level inverter can be implemented in hardware for PTC based IMD.
- The scheme with AFEC on the grid side and VSI on the motor side can easily be used for induction machine based wind energy conversion system to achieve maximum power for a given wind velocity and also to improve the power quality at the point of common coupling.

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Appendix A

A.1 Induction Machine Rating and Parameters

Parameter	Symbol	Nominal Value
Rated Shaft Power	-	3.7 kW (5 hp)
Line to Line Voltage	-	415 V
Rated Speed	-	1425 rpm
Pole pair	p	2
Stator Self-Inductance	L_s	1.56 H/ph
Rotor Self-Inductance	L_r	1.56 H/ph
Magnetizing Inductance	L_m	1.54 H/ph
Stator Resistance	R_s	4.92 Ω /ph
Rotor Resistance	R_r	6.54 Ω /ph
Machine Inertia	J	0.01061 kg- m^2

A.2 The equivalent circuit parameters of the stator and rotor of the squirrel cage induction machine:

$$\tau_s = \frac{L_s}{R_s} = 0.317 \text{ H}/\Omega$$

$$\tau_r = \frac{L_r}{R_r} = 0.239 \text{ H}/\Omega$$

$$\sigma = 1 - \left[\frac{L_m^2}{L_s L_r} \right] = 0.024$$

$$k_r = \frac{L_m}{L_r} = 0.98786$$

$$k_s = \frac{L_m}{L_s} = 0.98786$$

$$R_\sigma = R_s + R_r k_r^2 = 11.302$$

$$\tau_\sigma = \frac{\sigma L_s}{R_\sigma} = 3.28 \text{ m}$$

The inverter switching frequency : 20 kHz and Sampling frequency : 1 kHz

A.3 Name plate details of the three-phase squirrel cage induction motor (Load)

Parameter	Symbol	Nominal Value
Rated Shaft Power	-	3.7 kW (5 hp)
Line to Line Voltage	-	415 V
Rated Speed	-	1440 rpm
Pole pair	p	2

List of Publications

1. Goutham, V., **T. Himabindu**, V. Vikas, and G. Bhuvanewari and Bhim Singh, "Performance improvement using a multi-level converter in a DTC based induction motor drive", in *Proc. of the 2015 IEEE IAS Joint Industrial and Commercial Power Systems/Petroleum and Chemical Industry Conference (ICPSPCIC)*, pp. 52-59. IEEE, 2015.
2. **Himabindu, T.**, A.V Ravi Teja, G. Bhuvanewari, and Bhim Singh, "Simplified predictive torque control of an IM drive with efficient zero vector placement", in *Proc. of the 2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, pp. 362-367. IEEE, 2017 (Recipient IEEE IES SPTA Award).
3. **Himabindu, T.**, A.V Ravi Teja, G. Bhuvanewari, and Bhim Singh, "Predictive torque control of a three-level reduced switch inverter fed induction motor drive", in *Proc. of the 2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, pp. 348-353. IEEE, 2017.
4. **Himabindu, T.**, A.V Ravi Teja, G. Bhuvanewari, and Bhim Singh, "Performance enhancement in a multilevel inverter fed PTC induction motor drive by optimal voltage vector selection", *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 10, no. 2, pp. 801-812, June 2019.
5. **Himabindu, T.**, G. Bhuvanewari, and Bhim Singh, "Direct Power Control for a Multilevel Inverter fed Induction Motor Drive using Predictive Torque Control", *GRENZE International Journal of Engineering and Technology (GIJET)*, vol. 6, no. 2, pp. 266-274, 2020. (Scopus)
6. **Himabindu, T.**, G. Bhuvanewari, and Bhim Singh, "Reduction of switching transitions in a Three level Diode Clamped inverter fed PTC based Induction Motor drive by optimal voltage vector selection using FPGA", (*In Communication*).

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Biography of the Co-Supervisor

Prof. G. Bhuvaneshwari received the B.E. degree in Electrical and Electronics Engineering from College of Engineering, Guindy, Anna University, Madras in 1985. She received M.Tech and Ph.D from IIT Madras in 1987 and 1992 respectively.

She worked as Sr. Project officer Gr II from 1988 to 1992 after which she was with College of Engineering, Guindy, Anna University for a period of one and a half years. Then she worked with the Electric Utility Company ComEd Chicago for 3 years. Subsequently, she joined as a faculty member in the Department of EE, IIT Delhi in August 1997 where she is still working as a Professor. She was working as a visiting professor in BITS, Pilani Hyderabad Campus from July 2014 to July 2016. Her areas of interest are all application areas of power electronics like motor drives, power quality, power conditioning, HVDC transmission, renewable energy, electric vehicles and battery charging. She has over 200 publications in National and International peer-reviewed journals and conferences. She is a fellow of INAE, IE (I), IETE, IEEE-USA, IET-UK and she is a life member of ISTE. She has 4 patents; and graduated 9 PhD students; 6 more are currently working under her supervision towards PhD degree. She has also guided 79 Master's theses and 40 Bachelor's theses.

Further info on: <http://ee.iitd.ac.in/people/gbhuv.html>

Biography of the Co-Supervisor

Prof. Bhim Singh has received his B.E. (Electrical) from the University of Roorkee, India, in 1977 and his M.Tech. (Power Apparatus & Systems) and Ph.D. from the Indian Institute of Technology Delhi, India, in 1979 and 1983, respectively.

His areas of interest include solar PV grid interface systems, microgrids, power quality monitoring and mitigation, solar PV water pumping systems, improved power quality AC-DC converters, power electronics, electrical machines, drives, flexible alternating transmission systems, and high voltage direct current systems.

In 1983, he joined the Department of Electrical Engineering, University of Roorkee (Now IIT Roorkee), as a Lecturer. He became a Reader there in 1988. In December 1990, he joined the Department of Electrical Engineering, IIT Delhi, India, as an Assistant Professor, where he has become an Associate Professor in 1994 and a Professor in 1997. He had been ABB Chair Professor from 2007 to 2012. After that, he occupied CEA Chair and currently, he continues in that Chair position. He had been the Head of the Dept. of Electrical Engineering, IIT Delhi from July 2014 to August 2016. He was the Dean Academics from August 2016 to July 2019. He has been awarded J C Bose fellowship by DST, Govt. of India since 2015. He has over 1000 publications in national and international journals and conferences and several patents to his credit. He is a Fellow of INAE, IE (I), IETE, IEEE-USA, IET-UK, TWAS, NASI, IASc and INSA. He has been Head of the Department of Electrical Engineering at IIT Delhi from July 2014 to August 2016. Since, August 2016, he is the Dean, Academics at IIT Delhi. Currently he is working as a professor in the Dept. of Electrical Engineering and Dean (Academics) at IIT Delhi, Delhi, India.

Further info on: <http://web.iitd.ac.in/~bsingh/>