Superior Analog, Digital, and Ternary Circuit Designs Using Advanced Nano-electronic Gate Overlap Tunnel FET Devices for Ultra-Low Power Applications

Thesis

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Abstract

Energy efficiency limit has become the main obstacle for power-constrained applications using the conventional silicon complementary metal-oxide-semiconductor (CMOS) technology. In particular, the supply voltage scaling has slowed down in the past few technology generations due to the 60 mV/decade fundamental limit for on-off switching in MOSFETs, which prevents the reduction of the energy per operation in today's circuits and systems. To mitigate this challenge, Tunnel FETs or TFETs are envisioned as a viable alternative to achieve the steep on-off switching (SS<60 mV/dec) at low supply voltages and fabrication process, which is compatible with CMOS technology. Gate-controlled BtB tunneling phenomena enable the switching in TFETs at the source channel p-n junction.Tunnel FETs, which are gated PIN diodes whose on current I_{on} arises from band-to-band tunneling, are desirable for ultra-low power applications due to their low off current I_{off} and reduced inverse Sub-threshold Slope SS. Furthermore, a fundamental disadvantage of TFETs is that their ON-state current is significantly lower than that of MOSFETs.

This thesis proposes different types of TFETs for digital, analog, and ternary logic applications. The first DGLTFET device has been optimized such that device characteristics are superior to equally sized 45 nm MOSFETs for analog applications. TFETs show excellent current saturation characteristics and negligible channel length modulation effect, which is detrimental in MOSFETs, especially at lower technology nodes. As a result, output resistance r_o in the saturation region is a high order of 10^6 Ohms. In the proposed TFETs, vertical BtB tunneling has been used compared to point tunneling in conventional TFETs given a more BtB generation rate, which improves I_{on} as well as g_m. DGLTFET has thrice the on currents I_{on}, at least one order lower off currents I_{off}, twice the transconductance g_m, at least two orders higher output resistance r_o, and at least two orders higher overall intrinsic gain $g_m r_o$ than the equivalent metal oxide- semiconductor field-effect transistor (MOSFET) having the same width at the same technology node. Device optimization has been carried out by studying the impact of various device parameters and dimensions on performance. In this work, we have optimized the DGLTFET device by changing critical parameters like the epi-layer thickness t_{ep} and its doping concentration n_{ep}, which seriously influence the line-tunneling behavior. Optimizing the critical parameters for enhanced line-tunneling leads to improved analog performance parameters like g_m , r_o, and, finally, superior analog circuits.

We have compared the performance of the proposed devices with the TFETs reported earlier in the literature and the standard 45 nm MOSFETs. TFET characteristics were simulated using synopsys® TCAD tools, while circuit performance was benchmarked with the standard 45 nm CMOS library using cadence® EDA tools. The performance of the DGLTFET was benchmarked with the equivalent MOSFET in fundamental analog VLSI circuits, namely, Common Source CS amplifier (resistive and cascade loads), current mirror (single-stage and cascode configurations),

and a two-stage op-amp. The AC gain of cascode CS amplifier based DGLTFET devices is observed to be 30 dB higher gain compared with MOSFETs. DGLTFET CS amplifier has a gain-BW product or unity-gain BW f_T of 15 GHz, while the MOSFET CS amplifier with the same bias current is 10 GHz. The DGLTFET current mirror has at least three orders of magnitude higher output resistance R_{out} than the corresponding MOSFET current mirror. Similarly, the common-mode rejection ratio (CMRR) of the DGLTFET op-amp is 57 dB compared to the CMRR of 33.5 dB of the equivalent design in the standard 45-nm complementary metal-oxide semiconductor(CMOS) technology.

Vertically grown TFETs are preferred as they allow the integration of more TFETs on a single chip, increasing device density. This thesis work presents a Vertical Line-Tunneling FET (VLTFET) optimized for superior performance in analog applications. The saturation mechanism, DC, and small-signal behaviors are physically explained with the help of energy band diagrams, electron density, and tunneling width parameters. VLTFET has higher output resistance r_o owing to the independence of the drain bias on the band-to-band (BtB) generation. Increasing the source-gate overlap length L_{ov} from 0.1 μm to 0.5 μm triples the transconductance g_m, maintaining r_o constant, resulting in thrice the intrinsic gain A_{vo}. In analog circuits using conventional MOSFETs, g_m increases and r_o decreases with increasing width W. On the other hand, in analog circuits using VLTFETs, A_{vo} can be enhanced by increasing L_{ov} which increases g_m without affecting r_o. Unity-gain BW f_T (or the GBW product) is dominated by the relative change in the overall gate capacitance C_{GG} and g_m due to change in L_{ov}, since both g_m and C_{GG} are proportional to L_{ov}. However, in analog circuits with realistic capacitive loads, f_T rapidly increases with L_{ov}. VLTFET-based cascode CS amplifiers provide a 10 dB increment in its gain as L_{ov} is increased from 30 nm to 100 nm. Similarly, a VLTFET-based cascode current mirror shows a theoretical output resistance R_{out} in the order of 10^{11} Ω, behaving as an ideal current mirror/source.

In this thesis, we have proposed GOTFETs for prospective digital applications . Its on-state currents I_{on} at least twice ($I_{on,GOT} \geq 2I_{on,MOS}$) with off-state currents I_{off} remaining at least an order of magnitude lower ($I_{off,GOT} \leq 0.1 I_{off,MOS}$), than the corresponding equally-sized MOSFETs at the same 45 nm technology node. The proposed GOTFET designs are targeted for higher I_{on} leading to high-speed operation and lower I_{off} to minimize static leakage in ultra-low-power digital applications. This work further modified the GOTFETs for low and high threshold transistors (LVT & HVT) for ternary logic applications. These devices are designed in such a way that the low and high threshold voltages (V_{tn} & V_{th}) are $V_{DD}/3$ and $2V_{DD}/3$ respectively, with the ranges {0 to $V_{DD}/3$}, {$V_{DD}/3$ to $2V_{DD}/3$} & {$2V_{DD}/3$ to V_{DD}} representing the three logic states 0, 1 & 2 respectively. Proposed LVT & HVT TFETs have on currents (I_{on}) roughly twice and off currents (I_{off}) at least an order of magnitude lower than the corresponding MOSFETs. Dual threshold GOTFETs proposed in this work use single devices by altering their terminal connections.

Along with analog circuits, this thesis shows the performance of GOTFETs-based digital circuits. Proposed GOTFETs outperform similar CMOS designs in both aspects of the speed of operation and power consumption. This work proposes the GOTFET-based basic building blocks of digital circuits like an improved double tail comparator, ultra-low-power dynamic adder, an ultra-low voltage Schmitt trigger, and ultra-low-power ternary flash ADC circuits. The proposed circuit-level modifications in this Complementary GOTFET (CGOT) circuits have not only resulted in significantly lower static power due to TFET technology but also helped achieve faster circuit operation (lower delays) than the corresponding CMOS circuits. The overall Power Delay Product (PDP) in the proposed improved GOTFET-based circuits is only 1-5% of the PDP of the corresponding conventional CMOS-based circuits.

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Abbreviations

ADC	**A**nalog **t**o **D**igital **C**onverter
BtB	**B**and-**t**o-**B**and
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CGOT	**C**omplementary **G**ate-**O**verlap **T**FET
DGTFET	**D**ouble **G**ate **T**unnel **F**ield **E**ffect **T**ransistors
DMDG	**D**ual **M**etal **D**ouble **G**ate
DP-DGTFET	**D**rain-**P**ocket **D**ouble **G**ate **T**FT
DIBL	**D**rain **I**nduced **B**arrier **L**owering
DFA	**D**ynamic **F**ull **A**dder
ETL	**E**pitaxial **L**ayer
GOTFET	**G**ate-**O**verlap **T**unnel **F**ield **E**ffect **T**ransistors
GAA	**G**ate **A**ll **A**round
HVT	**H**igh **V**$_T$ **T**ransistors
HDB	**H**eterodielectric **B**OX
LGOTFETs	**L**ine-**T**unneling **G**ate-**O**verlap **T**unnel **F**ield **E**ffect **T**ransistors
FA	**F**ull **A**dder
LVT	**L**ow **V**$_T$ **T**ransistors
LUT	**L**ook-**U**p **T**able
MOSFETs	**M**etal-Oxide **S**emiconductor **F**ield **E**ffect **T**ransistors
NTI	**N**egative **T**ernary **I**nverter
PTI	**P**ositive **T**ernary **I**nverter
PDP	**P**ower **D**elay **P**roduct
PTL	**P**ass **T**ransistor **L**ogic
STI	**S**tandard **T**ernary **I**nverter
SS	Inverse **S**ubthreshold **S**lope

SOI	**S**ilicon **o**n **I**nsulator
TMDG	**T**riple **M**etal **D**ouble **G**ate
VLSI	**V**ery **L**arge **S**cale **I**ntegrated **C**ircuit
DGLTFET	**D**ouble **G**ate **L**ine **T**unneling **F**ield **E**ffect **T**ransistor
CMRR	**C**ommon **M**ode **R**ejection **R**atio
AVD	**A**tomic **V**apor **D**eposition
ALD	**A**tomic **L**ayer **D**eposition
FIQC	**F**ield **I**nduced **Q**unatum **C**onfinement
SRH	**S**hockly **Read** **H**all
VLTFET	**V**ertical **L**ine **T**unneling **F**ield **E**ffect **T**ransistor
TCAD	**T**echnology **C**omputer **A**ided **D**esign

Chapter 1

Introduction

1.1 Motivation and Related Work

The overall power consumption has increased over the past decade with continuous scaling and an increasing number of transistors per unit area. In power-constrained applications, in order to minimize the dynamic power P_{dyn}, consumption, we need to scale the supply voltage, V_{DD}, and correspondingly, the threshold voltage, V_t, to maintain the same on-state current, I_{on}, for the same performance [1, 2, 3]. However, in CMOS technology, static power consumption increases with the scaling of V_t due to increasing leaking currents. Reduction of static power consumption is a prominent challenge in modern computing systems, from mobile System on Chip (SOC) to data center applications. In order to maintain the same performance as required I_{on} current and power consumption, V_{DD} has been scaling down in the latest technology generations. In order to address the static power consumption problem, researchers worldwide have been exploring new transistors in the recent past. New devices such as carbon nanotube FETs (CNFETs), graphene FETs (GFETs), and tunnel FETs (TFETs) are designed by changing the structure and material properties of conventional MOS devices. Among these devices, TFETs are considered the most promising "beyond-CMOS" technology due to their compatibility with standard CMOS technology and superior inverse sub-threshold slope, SS characteristics of lower than 60 mV/dec at room temperature (T=300 K), which is the theoretical minimum SS for CMOS technology. Having lower SS than similar MOSFETs, TFETs can switch between the on and off states consuming lower P_{dyn} than equivalent MOSFETs, while lower I_{off} ensures lower leakage power than equally-sized MOSFET counterparts at the same technology nodes [4, 5]. The TFET technology replaces conventional diffusion-based minority carrier injection

in the case of MOSFETs with *Band-to-Band* (BtB) tunneling-based minority carrier injection into the channel [6, 7]. TFET's basic structure is the gated PIN diode whose I_{on} arises from BtB generation [8]. This significantly improves SS and power consumption characteristics far beyond the standard CMOS technology [9, 10]. SOI-based structures [11, 12] have been reported to overcome short-channel effects, lower SS, improve soft-error immunity, and improve electrostatics. If we want to replace the current MOSFETs in VLSI circuits with TFETs as viable switches [13, 14, 15], the TFET-based circuits must be as fast as the MOSFETs should have the same fan-out in the same circuit. However, the major limitation of traditional TFETs is that I_{on} is significantly lower than that of MOSFETs, and their inherent, am bipolar behavior. Inhomogeneous materials I_{on}:I_{off} ratio is poor, so it is difficult to get simultaneously high I_{on} and low I_{off} . In order to obtain high I_{on} currents, E_g should be low. However, I_{off} also increases due to Shockley Read Hall, SRH, generation-recombination mechanism. Heterojunction materials [16] are employed simultaneously to improve I_{on} currents and lower the I_{off} currents. To further improve I_{on}, properties of the gate stack, such as the gate materials, gate oxide thickness t_{ox}, and the oxide dielectric constants $\varepsilon_{\mathrm{ox}}$, etc., have been engineered for optimal characteristics. Multiple gate structures like double-gate [17], gate-all-round [18], etc., improved gate control over the channel potentials improving the I_{on} current. Researchers are actively investigating alternative materials to Silicon, like Germanium [19, 20], III-V semiconductors [21, 22, 23], Nanowires [24], 2D transition metal dichalcogenides [25], etc., have been employed to boost I_{on} by reducing tunneling distances. Spacer engineering [26], asymmetric gate structure [27], and strain Engineering [28] improve the I_{on} in TFETs. Along with gate on source overlap [29, 30, 31]and source pocket [32, 33] structures were explored to improve I_{on} further.

Several researchers have analyzed the competitive benefits of TFET inverters vs. MOSFET-based CMOS inverters [34, 35, 36]. It indicates that TFET inverters are faster and more energy-efficient energy-efficient at lower supply voltages. At a low supply voltage, V_{DD} = 0.25 V, TFET inverters perform ten times faster than FinFET inverters for the same static power dissipation [37]. At V_{DD}=0.6 V, the authors have demonstrated an improvement in the energy consumption, and latency of the Manchester carry chain adder dynamic logic circuit utilizing the TFET compared to the FinFET [38]. A 4T TFET SRAM cell is 100 times faster than a low static power (LSP) 6T CMOS SRAM cell and uses three times less standby power than a high-performance (HP) 6T CMOS SRAM cell. In [39], the authors explained the possibility of Mixed TFET MOSFET 8T SRAM cells. The combination of TFET and MOSFET cells is more stable and efficient than the MOSFET and TFET cells alone. In addition to SRAMs, additional intriguing applications using

TFETs and flip-flops are also being studied [40, 41, 42].

TFETs have been investigated predominantly for digital applications and as a replacement for conventional MOSFETs for logic applications due to their superior sub-60 mV/dec SS characteristics and their higher $I_{on} : I_{off}$ ratios [3]. At low supply voltages, TFET-based digital circuits have better energy efficiency compared to conventional CMOS. However, researchers have recently evaluated the merits of TFETs in different analog circuits. DC characteristics such as SS, I_{off} , threshold voltage, V_t, transconductance, g_m, output resistance, r_o, intrinsic gain,$g_m r_o$, unity gain cut-off frequency, f_T are important analog parameters for bench-marking the TFETs with CMOS. The current saturation mechanism in the output characteristics of the TFET is quite different from the saturation mechanism of conventional MOSFET. As the channel becomes free from carriers, the currents in TFETs saturate, and the impact of drain potential on the source channel tunnel junction becomes negligible. Therefore, TFETs exhibit excellent current saturation and do not show channel length modulation. As a result, r_o of the TFETs are very high compared to MOSFETs. Due to high r_o, the intrinsic gain A_{vo} of the TFETs is higher than MOSFETs [43].

In earlier papers [44, 45], CS amplifier with active load had been designed using $g_m : I_D$ ratio method, AC gain is improved in heterojunction TFETs, HTFETs, and compared with FinFET with 14 nm technology. In [43], authors compared the performance of InAs homojunction and GaSb-InAs heterojunction TFET with Si TFET and applied to analog building blocks. The performance of analog circuits such as operational transconductance amplifier, OTA, using $g_m : I_D$ in the sub-threshold region was studied for low-frequency operations. TFETs and HTFETs give higher DC gains than CMOS due to their higher output resistance. In [46, 47], authors showed improved performance of TFETs in cascode current mirror circuits due to their higher output resistance r_o.

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1.2 Objectives, Research Gaps, and Scope of this Work

Based on the literature review, the following are the research gaps and issues in TFET devices that are investigated, and the best possible LTFET structures have been proposed as part of the PhD thesis.

The first aim of this research is to optimize the design of the TFET device, which will be used for designing novel analog and digital circuits with significant improvement in the performance parameters of the circuits for ultra-low power applications. Following are the proposed deliverable of this research problem, which is going to be investigated, and the optimal solutions will be addressed as part of this Ph.D. thesis

1. Most of the TFETs reported in the literature have low r_o and g_m, which affects their analog performance. There is a severe need to modify the design of conventional TFETs, resulting in higher r_o and g_m, which subsequently improve the analog performance.
2. In the literature, TFETs shown the device performance parameters improvement, but they didn't discuss the circuit performance.
3. Most TFETs in the literature explain how affecting the gate overlap on source length (L_{ov}) improves digital circuit performance; they didn't discuss the analog performance of their circuits.
4. Most of the TFETs in the literature have very low I_{on} compared to MOSFETs. There is a substantial need to design a TFETs resulting in higher I_{on}, lower I_{off}, and lower SS.
5. L_{ov} places a significant role in LTFET devices. This thesis demonstrates the effect of L_{ov} on analog performance parameters and the circuits.
6. The Ternary logic design has received considerable attention from researchers worldwide because of its many advantages compared to digital logic. Hence there is a need to design the multi-threshold TFETs for ternary logic applications.

1.3 Operating Principle of the Tunnel Field Effect Transistor

In MOSFETs, carrier injection is controlled by an electrostatic potential barrier at the source-channel pn junction. Minority carriers are injected from the source to the channel through diffusion transport. Only those injected minority carriers with energies exceeding the energy barrier can form the inverted channel and contribute to the I_{on}. On the other hand, TFETs are reverse-biased gated p-i-n tunnel diodes. These devices have asymmetric source and drain doping. Switching in TFETs is enabled by gate-controlled Band-to-band, BtB, tunneling phenomena at the source-channel junction [5]. Figure 1.1 shows the energy band diagram of an nTFET in

different switching states. In its on state, band bending occurs at the source-channel junction hence the electrons from the valence band tunnel directly into the conduction band of the channel region. TFET is in its off state when the conduction band of the channel lies above the valence band of the source, preventing BtB tunneling, as depicted in Fig 1.1.

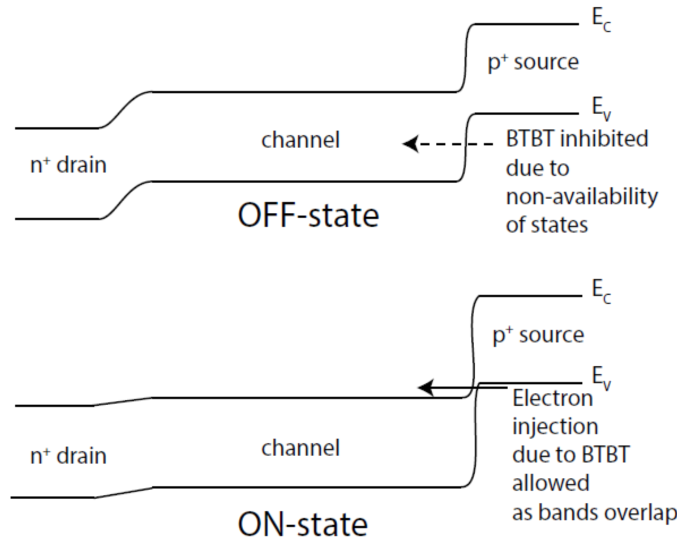

FIGURE 1.1: Energy band diagram of an nTFET [5]

1.4 Contributions

This thesis proposes many innovative Tunnel FET devices for ultra-low-power digital, ternary, and analog circuits. The proposed TFET performance has been compared with industry-standard MOSFET at a 45 nm technology node. TFETs are considered the most promising "beyond-CMOS" technology due to their compatibility with standard CMOS technology and superior inverse SS characteristics of lower than 60 mV/dec at room temperature (T=300 K), the theoretical minimum SS for CMOS technology. In addition, TFETs exhibit excellent current saturation and do not show channel length modulation; as a result, r_o of the TFETs are very high compared to MOSFETs from an analog perspective. Due to higher r_o, the intrinsic gain A_{vo} of the TFETs is much higher than MOSFETs [43]. In double-gate TFET (DGLTFET), structure has been modified to get the double transconductance g_m, and two order higher output resistance r_o than the MOSFETs. Therefore, two orders higher overall intrinsic gain $g_m r_o$ were observed with proposed TFETs than the MOSFETs at the same technology node. Due to its several benefits over digital logic, the ternary logic design has attracted substantial interest from researchers throughout the globe. Therefore, we have built TFETs with low V_T and high V_T for

ternary logic applications. The most exciting aspect of the proposed TFET is that, in the same device structure, we may get the optimum performance of low and high threshold (LVT & HVT) devices simply by adjusting the device's material and doping parameters.

The primary contributions of this thesis are as follows:

1. Double-gate line-tunneling field-effect transistor (DGLTFET) device optimized for superior analog performance.
2. Design of DGLTFET-based analog building blocks like CS amplifier, Current mirror circuits, and op-amp. Its performance has been compared with MOSFET at the same technology node.
3. Design of VLTFET devices at 20 nm technology node and the effect of L_{ov} on analog performance. In addition, we shown the CS amplifier and current mirror circuit performance with L_{ov} changes.
4. Design of innovative Multi-Threshold GOTFETs for superior ultra-low-power ternary circuits at 45 nm technology node.
5. Design of GOTFET-based VLSI circuits and its performance parameters like speed and power compared with MOSFET at 45 nm technology node.

1.5 Thesis Outline

This thesis is organized as follows:

Chapter 2 examines the optimization of the double gate LTFET structure for twice the transconductance g_m, at least two orders higher output resistance r_o, and at least two orders higher overall intrinsic gain $g_m r_o$ compared to an equivalent MOSFET with the same width and technology node. In these devices, the epi-layer plays a crucial role for BtB tunneling. This chapter discusses the impact of epi-layer doping n_{ep} and thickness t_{ep} on the analog performance of these devices. The performance of a device has been optimized by analyzing the effect of various device parameters and dimensions on analog performance.

Chapter 3 discusses the circuit performance of the DGLTFET devices and its performance bench-marked with the equivalent MOSFET in fundamental analog VLSI circuits, viz., CS amplifier (both resistive and cascode loads), current mirror (both single stage and cascode configurations), and a two-stage op-amp. This chapter explains the compact SPICE simulation methodology for circuit simulation. AC and DC analysis of CS amplifier using DGLTFET devices has been analyzed in this chapter. This chapter shows the impact of output resistance R_{out} in the current mirror using these devices. The influence of CMRR on op-amp with DGLTFET device aspects is investigated in this chapter.

Chapter 4 discusses the effect of the gate on source overlap length L_{ov} in VLTFET devices on analog performance parameters. In addition, this chapter explains the impact of L_{ov} on AC gain in CS amplifiers and the effect of output resistance R_{out} on current mirror circuits.

Chapter 5 discusses the GOTFET devices for digital and ternary ultra-low power circuit applications, and its performance has been bench-marked with MOSFET at a 45 nm technology node. The proposed device designs are targeted for higher I_{on} leading to high-speed operation, lower I_{off} to minimize the static leakage and SS for ultra-low power digital applications. Also, introduce low and high V_t GOTFET devices for ternary logic applications. These devices are designed so that the low and high threshold voltages are $V_{DD}/3$ and $2V_{DD}/3$ respectively. This chapter also presents dual-threshold GOTFETs that exhibit both LVT & HVT characteristics by simply altering their terminal connections in the same device instead of the dedicated devices.

Chapter 6, Ultra-low-power digital circuits based on suggested GOTFETs were compared against the identical circuit based on 45 nm CMOS industry-standard devices. The typical digital gates, double tail comparator, dynamic full adder, schmitt trigger, and ternary flash ADC circuits are evaluated in this chapter. Digital circuits built on GOTFETs outperform equivalent CMOS systems in terms of both operating speeds and power consumption.

Finally, Chapter 7 summarizes this thesis's contributions and proposes recommendations for future work.

Chapter 2

Double-Gate Line-Tunneling FET (DGLTFET) Devices for Superior Analog Performance

2.1 Introduction

Due to their superior saturation characteristics, line tunneling-based Si TFETs were recently explored for analog applications [48, 49]. Authors [29, 50] explained the influence of epi-layer thickness t_{ep} and doping n_{ep} on the device performance parameters like I_{on}, I_{off} & SS. This chapter optimizes the LTFET structure for superior analog performance parameters like g_m, r_o, R_{out}, A_d, A_{CM} & f_T, and applies it to different analog building blocks. To improve the intrinsic gain, DGLTFET yields twice the g_m and two orders higher r_o owing to the epi-layer sandwiched between the gate and the source, resulting in excellent saturation characteristics. The performance of DGLTFET analog circuits was benchmarked with MOSFET circuits at the 45 nm technology node.

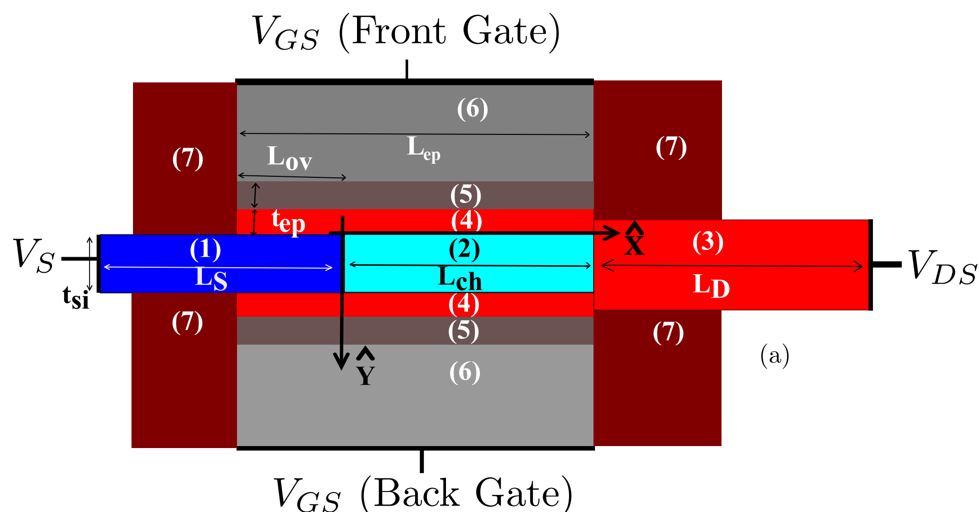

FIGURE 2.1: (a) Schematic cross-sectional view of the proposed DGLTFET device. (1) p^+ $Si_{0.5}Ge_{0.5}$ source (2) p^- Si channel (3) n^+ Si drain (4) n^+ Si epitaxial layer (5) HfO_2 gate oxide (6) Al metal gate (7) SiO_2 spacer oxide.

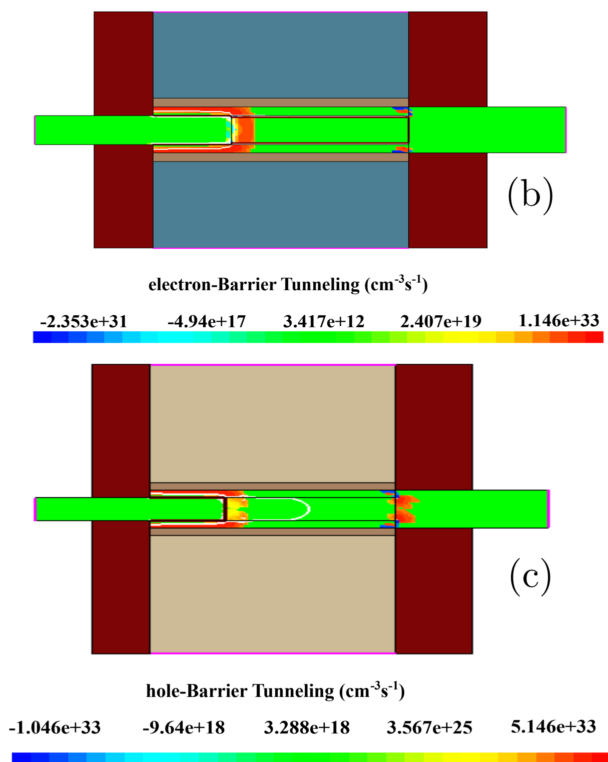

FIGURE 2.2: (a) Electron and (b) hole BtB tunneling rate in nDGLTFET & pDGLTFET respectively.

2.2 Proposed DGLTFET device structure and its characteristics

2.2.1 DGLTFET device structure

Fig. 2.1 shows the schematic and Fig. 2.2 BtB tunneling of the nDGLTFET and pDGLTFET. t_{ep} and n_{ep} are the major critical parameters for analog performance, which are appropriately optimized for superior performance. To benchmark the performance of DGLTFET analog circuits with the industry-standard CMOS circuits, we have used an effective channel length of 45 nm in the device and simulated the device-level characteristics using the industry-standard synopsys® TCAD tool [51]. In the DGLTFET, SiGe source and Si channel have been used to form a heterojunction, enabling higher I_{on} and lower I_{off} compared to conventional homo junction TFETs. However, analog circuits require a flat saturation region in I_D-V_{DS} characteristics, as shown in Fig 2.8, which implies higher output resistance r_o. Therefore, to maximize r_o, we have sandwiched a 3 nm thick epi-layer between the source overlap and the channel region and used a 3 nm thick high-κ dielectric (HfO_2) as the gate oxide [52]. Aluminum (work-function Φ_m=4.15 eV), Zn polycrystalline (Φ_m=4.9 eV) metals for n-type and p-type DGLTFETs used as the gate material yields lower threshold voltage V_t and higher I_{on}. Table 2.1 lists the device parameters, doping concentrations of all the regions and the work functions of the gate metals for both pDGLTFET & nDGLTFET. The numerical simulations include (i) the Wentzel-Kramer-Brillouin (WKB) approximation along with 2-band dispersion models from TCAD [53] to get more accurate BtB tunneling across all the regions, (ii) fine non-local meshing defined across the tunneling junctions, (iii) the effects of trap-assisted-tunneling (TAT) captured by the Shockley-Read-Hall (SRH) recombination model along with the field-enhanced Schenk TAT model [54, 31], (iv) the Fermi-Dirac statistics, (v) doping-dependent mobility models, as well as (vi) band gap narrowing models.

2.2.2 Calibration of the simulation deck with experiments

The parameters in our simulation deck, primarily the tunneling effective masses m_e, m_h, the SRH recombination time τ_{max}, and the effective phonon energy $\hbar\omega$ have been calibrated with a previously reported experimental work [55]. Fig. 2.4 shows the close agreement of the simulated device characteristics with the experimental data published in [55] using the calibrated parameters used in this work, validating our simulation deck. In order to cross-verify our

TABLE 2.1: Parameters of the generic DGLTFET devices.

Parameter	Units	nDGLTFET		pDGLTFET	
Channel length L_{ch}	nm	45		45	
Source length L_S	nm	50		50	
Drain length L_D	nm	40		40	
Gate/Epitaxial layer length L_{ep} or L_G	nm	65		65	
Gate oxide thickness t_{ox}	nm	3		3	
Channel thickness t_{si}	nm	10		10	
Epi-layer thickness t_{ep}	nm	3		3	
Gate-source overlap length L_{ov}	nm	20		20	
Spacer length L_{sp}	nm	30		30	
Source doping N_S	$/cm^3$	2×10^{20}	p^+SiGe	2×10^{20}	n^+Si
Channel doping N_{ch}	$/cm^3$	10^{16}	pSi	10^{16}	nSi
Drain doping N_D	$/cm^3$	5×10^{19}	n^+Si	5×10^{19}	p^+Si
Epitaxial layer doping N_{ep}	$/cm^3$	2×10^{18}	n^+Si	2×10^{18}	p^+SiGe
Gate work-function Φ_m	eV	4.15	Al	4.9	poly Zn

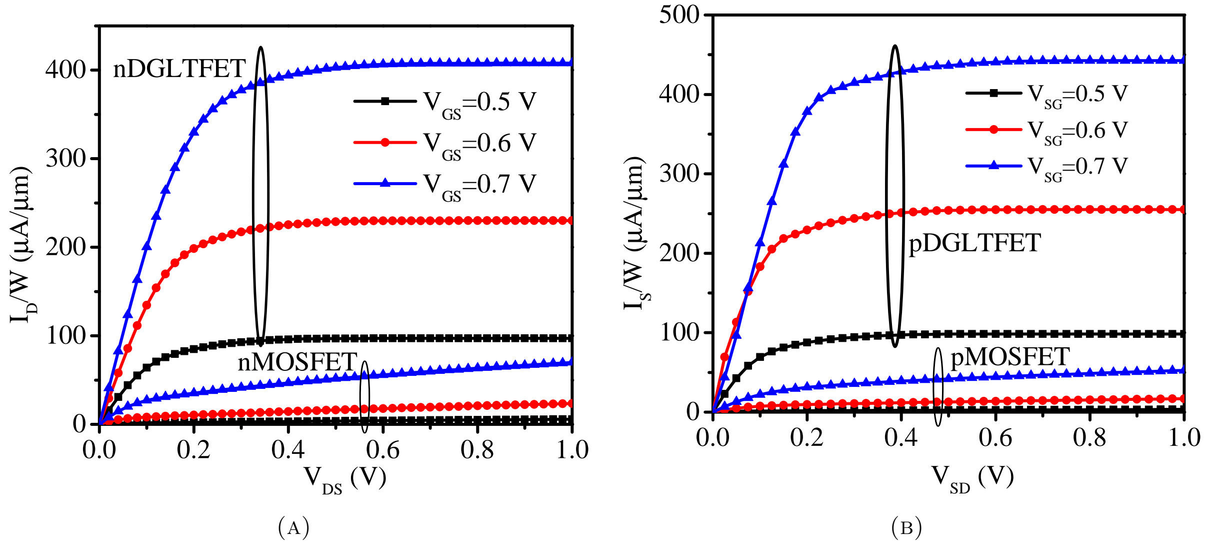

FIGURE 2.3: I_D-V_{DS} characteristics of nDGLTFET & nMOSFET for different values of V_{GS} and (b) I_S-V_{SD} characteristics of pDGLTFET & pMOSFET for different values of V_{SG}.

simulation parameters, our parameters were essentially the same as that used in [53], where the authors calibrated their simulation deck with the results in [55] for their simulation-based work published earlier. It is interesting to note that the simulation results (dotted lines in Fig. 2.4) show much lower I_{off} than the measured data (bold line in Fig. 2.4, reproduced from [55]). This discrepancy can be attributed to the noise currents, which are in the order of pA, which get reflected in the measurements but cannot be captured in the simulations. However, as the circuits reported in this work will operate in the order of $\mu A/\mu m$, currents below 0.01 $\mu A/\mu m$

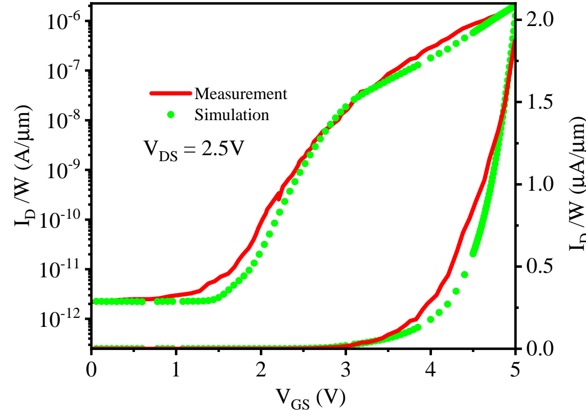

FIGURE 2.4: Calibration of the simulation deck with the I_D-V_{GS} characteristics measured from a prefabricated device at V_{DS}=2.5 V[55]

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may be considered as if the device is practically off or in the sub-threshold regime, as the $V_t \approx 3$ V in the device of [55], evident in Fig. 2.4.

2.2.3 Physical explanation for DGLTFET's superior performance

The proposed DGLTFET works fundamentally on the same physical principle of BtB tunneling but with a different strategy than conventional TFETs. BtB tunneling in a DGLTFET occurs from the p$^+$ source to the n$^+$ epi-layer under the gate-overlapping source, indicated in Fig. 2.1. In a conventional TFET, BtB tunneling is caused by the lateral field $\widehat{x}F_x$, while in a DGLTFET, BtB tunneling occurs due to the vertical field $\widehat{y}F_y$, which is much larger in magnitude than $\widehat{x}F_x$ as the thickness of DGLTFET t_{si}(=10 nm) $\ll$ L_{ch}(=45 nm). When the DGLTFET switches on, the electrons in the valence band of the p$^+$ source's bulk directly tunnel into the conduction band of the n$^+$ epi-layer. Fig. 2.2 depicts the typical BtB tunneling phenomenon occurring in the source region of the DGLTFETs. In a conventional TFET (working on the principle of lateral BtB, due to lateral field from source to intrinsic channel $\widehat{x}F_x$), electrons tunnel from the valence band of the p$^+$ source to the conduction band of the intrinsic channel under the gate. The DGLTFET starts behaving exactly like a typical symmetric double-gate (DG) MOSFET: n$^+$ source (at the epi-layer), near-intrinsic / lightly-doped p$^-$ channel, and n$^+$ drain. Consequently, the I_{on} levels are higher than the MOSFETs, instead of the low I_{on} in the standard TFETs. Hence DGLTFET amalgamates the advantages of the MOSFETs and TFETs into a single device.

Furthermore, the maximum doping in Si possible is in the order of 10^{20} /cm^3, which means that the maximum density of free holes in the valence band we can expect in the p$^+$ source would be around 10^{20} /cm^3, even at elevated temperatures. Even though the principle of operation of the DGLTFET is quite similar to the GOTFETs published earlier [56, 57, 58, 59, 60, 61]. However the epi-layer restricts the maximum carrier density to the order of doping in the epi-layer. This ensures that beyond deep saturation $V_{DS} \geq V_{GS}$, the carrier density in the channel cannot increase any further, leading highly flat saturation characteristics, as evident in Fig. 2.3a. As expected, an extremely flat saturation characteristics will yield the maximum r_o, leading to the maximum possible intrinsic gain $g_m r_o$. Hence the proposed DGLTFETs will achieve better gains than the equivalent MOSFETs at the same technology node.

The 'hump' or 'kink' effect arises due to the different onset voltages initiating point and line-tunneling. The 'hump' effect is negligible in the proposed DGLTFET since we have a double-gated structure leading to a very high vertical field compared to the lateral field. So the hump effect primarily becomes evident when the line tunneling and point-tunneling rates are roughly in the same order of magnitude. In DGLTFET, the line tunneling due to a much higher vertical field dominates over the point tunneling (due to the much lower lateral field) beyond $V_t \approx 0.4$ V, which approximately defines the device's threshold.

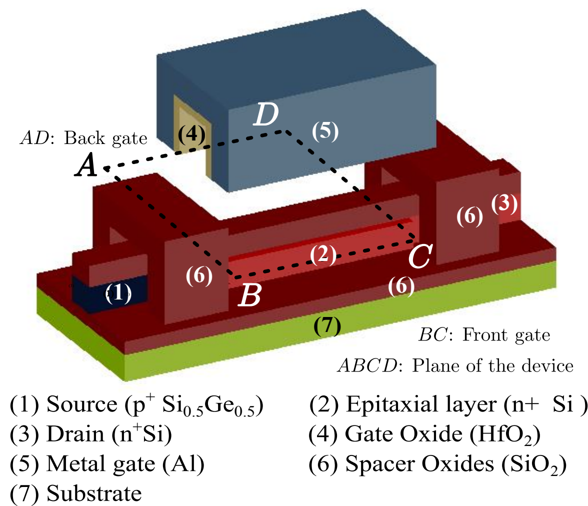

FIGURE 2.5: Section-wise view of the DGLTFET for visualizing the fabrication process. The horizontal plane $ABCD$ represents the device cross-section illustrated in

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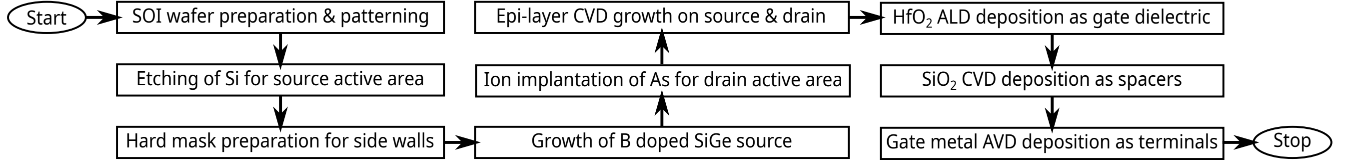
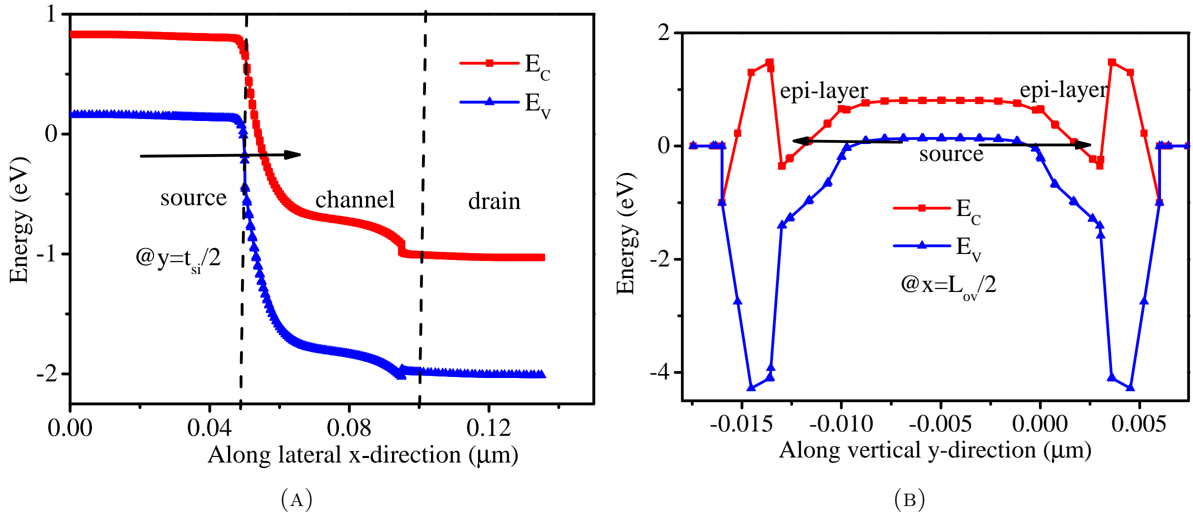


FIGURE 2.6: Process flowchart for the DGLTFET structure. Abbreviations used are SOI: Silicon On Insulator, CVD: Chemical Vapor Deposition, ALD: Atomic Layer Deposition, AVD: Atomic Vapor Deposition.

2.2.4 DGLTFET fabrication process

Fig. 2.5 shows the sectional view of the different layers of the DGLTFET to visualize the fabrication process. One can fabricate the DGLTFET structure using the following steps, as reported in [62, 53, 63, 64, 65, 66, 67, 68, 36], and its flow chart is shown in Fig. 2.6:

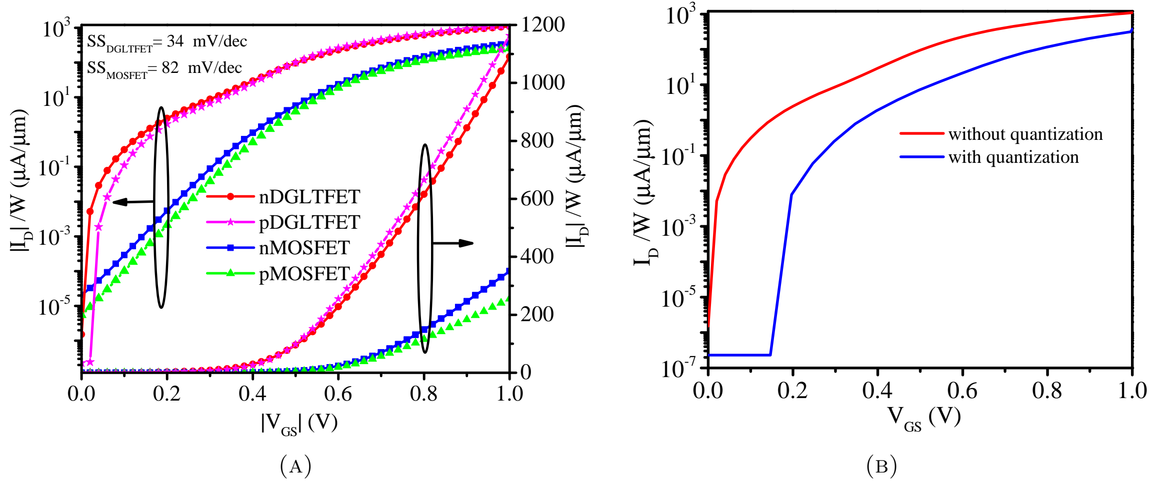


(A) (B)

FIGURE 2.7: Energy bands aiding BtB generation along the (A) lateral & (B) vertical directions in the nDGLTFET for V_{GS}=V_{DS}=1 V.

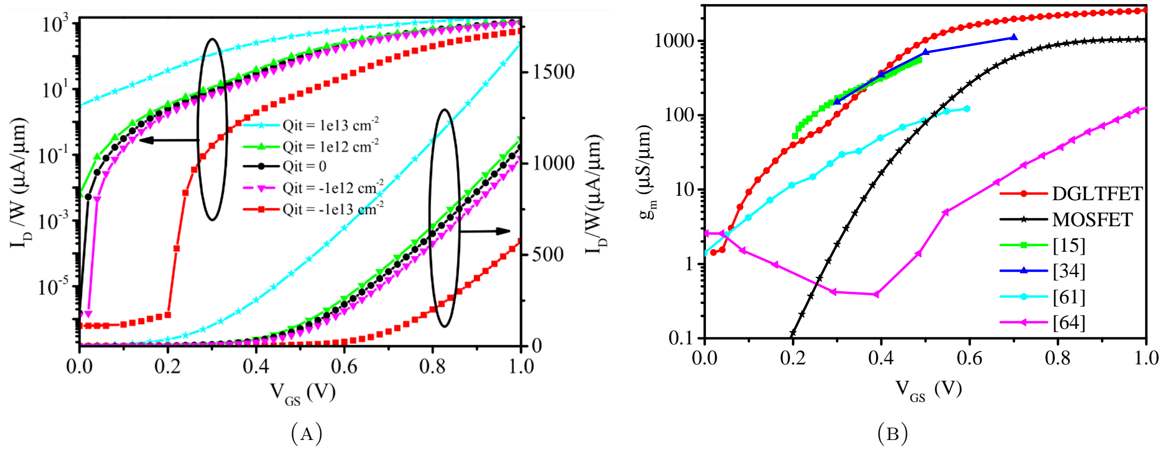
2.2.5 Results and discussions on the nDGLTFET

I_D-V_{GS} characteristics of nDGLTFET obtained using the non-local BtB tunneling model at V_{DS} =1 V are shown in Fig. 2.8a with I_{on}=1090 μA/μm at V_{DS}=1 V, which exceeds thrice the I_{on} of the MOSFET at 45 nm technology node. The impact of quantum effects on the transfer characteristics is shown in Fig. 2.8b. Field-Induced Quantum Confinement (FIQC) effects result in a shift of 150 mV in the onset voltage than without the inclusion of quantum confinement. This leads to a shift in V_t decreasing the I_{on} substantially, as discussed in [69, 70, 31].



(A) (B)

FIGURE 2.8: $|I_D|$-$|V_{GS}|$ characteristics of DGLTFET & MOSFET (both p- and n-channel) for $|V_{DS}|$=1 V plotted on linear and logarithmic scales. The inverse subthreshold slopes SS are calculated as the average of four-decade change in the magnitude of I_D within the subthreshold region. and (b) Impact of Field-Induced Quantum Confinement (FIQC) effects on the I_D-V_{GS} characteristics of DGLTFET.



(A) (B)

FIGURE 2.9: (a) Effect of trap charge density on the I_D-V_{GS} characteristics of DGLTFET. (b) Transconductance g_m of the DGLTFET, compared with equivalent MOSFET and other TFETs reported earlier

Further, the effect of the semiconductor/gate oxide interface trap charges Q_{it} on I_D-V_{GS} characteristics [71, 72, 73, 61], is shown in Fig 2.9a. It is observed that an increase of donor (acceptor) type charges increases (decreases) the I_{off}, I_{on}, decreases (increases) V_t, and degrades the SS. Furthermore, as the DGLTFET V_t≈0.4 V, a Q_{it} of 10^{13} /cm^2 will not even turn off the device, as evident in Fig. 2.9a. The device has higher I_{on} as a consequence of both *point-BtB* as well as *line-BtB* tunneling. At lower voltages, point-BtB dominates, while line-BtB tunneling dominates carrier tunneling at higher voltages . The two simultaneous tunneling events result in higher I_{on} & 2.5 times higher g_m than MOSFETs, as shown in Fig. 2.9b. Increasing the

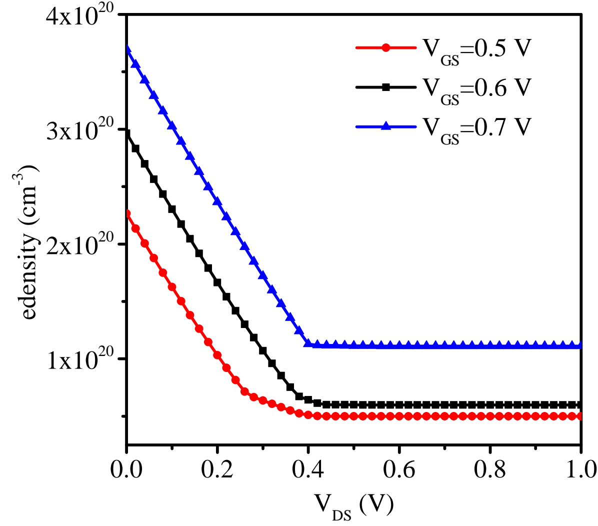


FIGURE 2.10: Variation of the electron density with increasing V_{DS} within the epi-layer under the gate overlap.

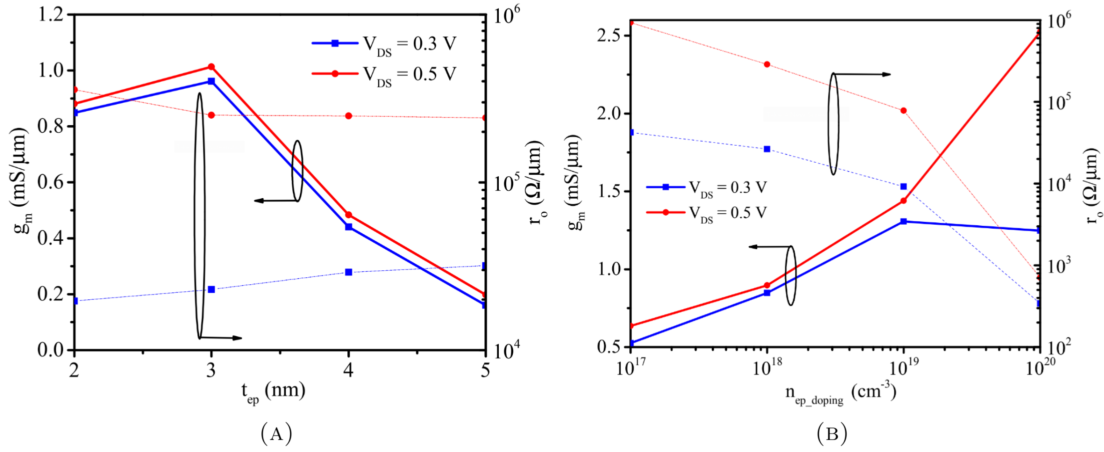


FIGURE 2.11: Variation in transconductance g_m and output resistance r_o with (a) the epi-layer thickness t_{ep} and (b) epi-layer doping n_{ep} in the nDGLTFET.

gate-overlap length increases the vertical BtB tunneling, increasing g_m (advantageous, increases gain) and C_{GS} (disadvantageous, decreases BW). So we need to optimize the desired overlap length depending on the application. The output characteristics for the nDGLTFET device are shown in Fig. 2.3a for different gate biases. For a given value of V_{GS} with increasing V_{DS}, initially, the electron density decreases in the epi-layer over the source region. Beyond a certain V_{DS}, electron density becomes independent of a further increase in V_{DS} as shown in Fig. 2.10. Portion of the I_D-V_{DS} characteristics within the range (V_{GS}-V_t)≤V_{DS}<V_{GS} is the *soft saturation* region, while *deep saturation* occurs for V_t<V_{GS}≤V_{DS}, where V_{DS} (hence, the lateral field $\overrightarrow{F_x}$, along the $\widehat{x}$ direction in Fig. 2.1) loses control over the carrier density, and as a consequence, a constant carrier density in maintained. Epi-layer thickness t_{ep} and doping n_{ep} play significant

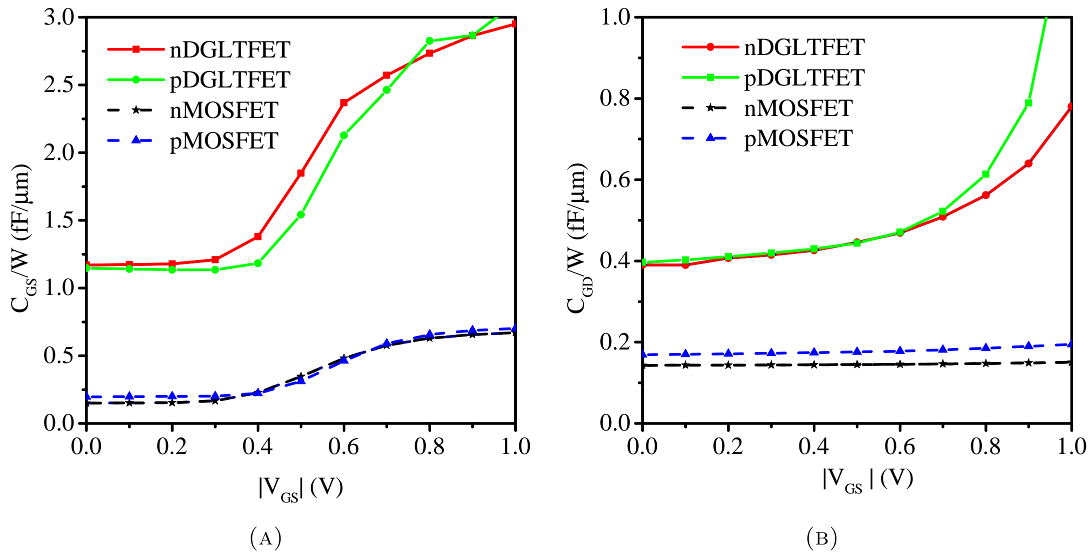


FIGURE 2.12: Comparison of the (A) C_{GS}-$|V_{GS}|$ (B) C_{GD}-$|V_{GS}|$ characteristics of nDGLTFET, pDGLTFET, nMOSFET & pMOSFET at $|V_{DS}|$=1 V.

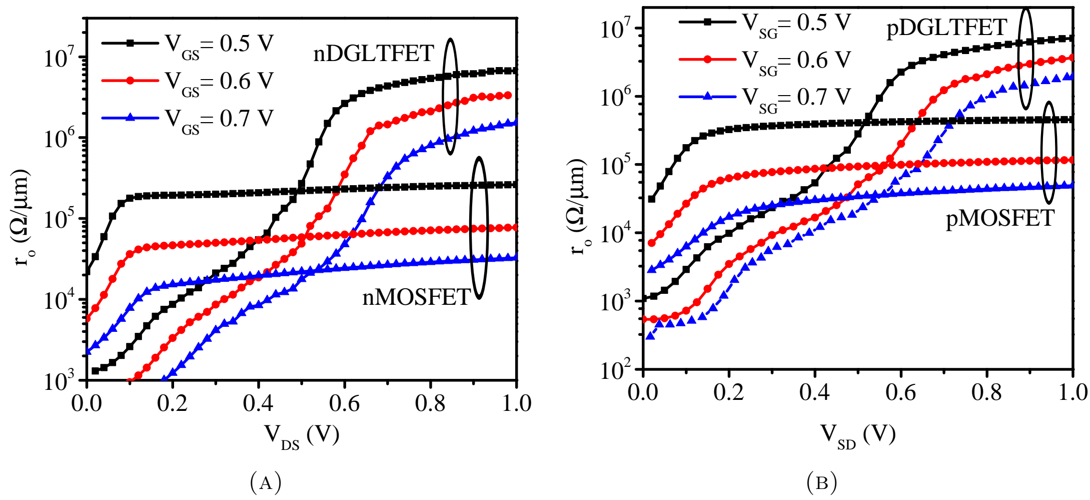


FIGURE 2.13: The output resistance r_o as a function of (A) V_{DS} in nDGLTFET & nMOSFET for different V_{GS}, as well as (B) V_{SD} in pDGLTFET & pMOSFET for different V_{SG}.

roles in analog performance parameters like g_m & r_o. Decreasing t_{ep} reduces the tunneling barrier width between the source valence band and the epi-layer conduction band , improving g_m. The tunneling width between source and epi-layer remains practically independent of the drain potential, maintaining almost a constant r_o with changing t_{ep}, as shown in Fig. 2.11a. As the doping of the epi-layer n_{ep} increases, g_m increases due to a rise in the junction electric field between the source and epi-layer, resultantly more BtB tunneling.Thus, the onset of saturation in I_D occurs at larger V_{DS} for increasing the n_{ep} consequently, reduces the r_o as illustrated in Fig. 2.11b. Gate capacitances C_{GS} and C_{GD} for different values of V_{GS} are shown in Fig. 2.12a

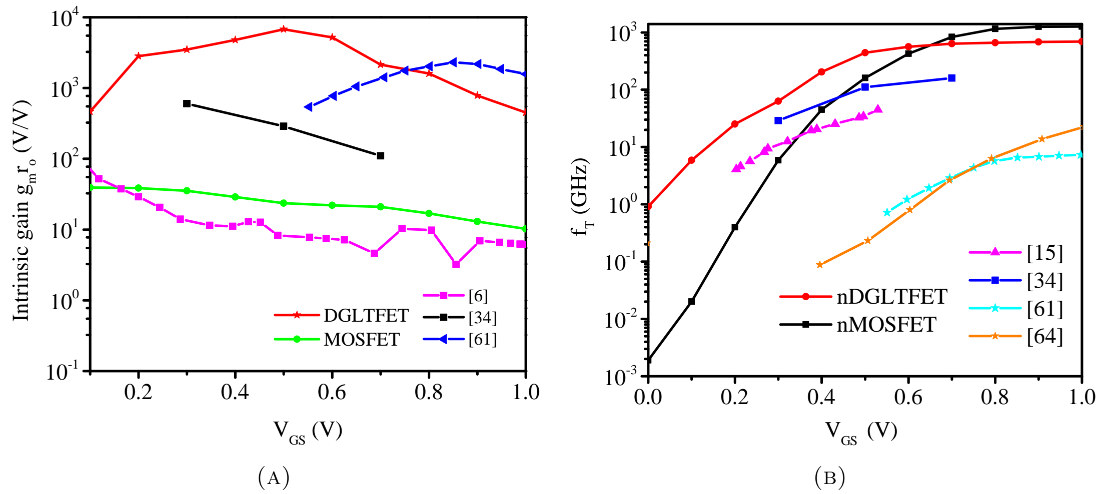


FIGURE 2.14: Comparison of (a) the intrinsic gain $g_m r_o$ and (b) the unity-gain frequency f_T of DGLTFET, the equivalent MOSFET at the same technology node and other TFETs at V_{DS}=1 V.

& 2.12b. The comparison of the output resistances for different V_{GS} values for the DGLTFET vs. MOSFET are shown in Fig. 2.13a. The nDGLTFET has r_o at least two orders of magnitude higher than MOSFET in deep saturation. The intrinsic gain $g_m r_o$ and the unity-gain frequency f_T have been calculated for different values of V_{GS} at V_{DS}=1 V as shown in Fig. 2.14a & 2.14b. Due to the higher g_m coupled with superior saturation characteristics, the intrinsic gain exceeds two orders higher magnitude in DGLTFET device compared to MOSFET. Due to the higher g_m at lower V_{GS}, f_T is higher in DGLTFET, and at higher V_{GS}, gate capacitance dominates. Consequently f_T is lower in DGLTFET compared to MOSFET. DGLTFET has a leakage current I_{off}=1.5 pA/μm at V_{DS}=1 V, which is one order of magnitude lower than the corresponding MOSFETs. The threshold voltage V_{tn} of the optimized DGLTFET is extracted using the third derivative method [74], where $\partial^3 I_D/\partial V_{GS}^3$ for V_{DS}=1 V has its first peak at V_{GS}=0.4 V, denoting V_{tn}≈0.4 V. The AC analyses in TCAD extract the gate capacitances C_{GS} & C_{GD}. The verilog-A behavioral model developed for the proposed DGLTFET includes the *I*-*V* characteristics for $I_D(I_S)$ as functions of $V_{GS}(V_{SG})$ & $V_{DS}(V_{SD})$, the *C*-*V* characteristics for $C_{GS}(C_{SG})$ as well as $C_{GD}(C_{DG})$ as functions of $V_{GS}(V_{SG})$ & $V_{DS}(V_{SD})$. We have carried out the circuit-level simulations using the Verilog-A behavioral model in the industry-standard cadence® EDA tool [75].

2.2.6 Results and discussions on the pDGLTFET

Conventional pTFET devices have lower on currents I_{on} due to poor BtB tunneling. To increase the BtB tunneling, SiGe based p-type epi-layer has been used, which improves the line tunneling from the source to the gate in pDGLTFET device. Increasing the t_{ep}, increases the SRH recombination's current density, increasing I_{off} as well. The impact of doping concentration n_{ep} in the epi-layer has been explained in [50]. Higher doping of the n_{ep} causes short carrier lifetimes, increasing the SRH recombination currents. Thus, I_{off} increases with doping concentration. I_S-V_{SG} characteristics of pDGLTFET obtained using the non-local BtB at V_{SD}=1 are shown in Fig. 2.3b. The I_{on} of the pDGLTFET is 1.1 mA/μm, which is almost thrice as high as pMOSFET, and the I_{off} is 0.2 pA/μm at V_{SD}=1 V, which is one order magnitude lower than equally sized pMOSFET. Proposed pDGLTFET threshold voltage $|V_{tp}|$ =0.36 V extracted using the 3$^{\text{rd}}$ derivative method [74]. It is observed that pDGLTFET has twice the g_m as shown in Fig. 2.9b and two orders of magnitude higher r_o than MOSFET in deep saturation, shown in Fig. 2.13b.

2.3 Comparison of the DGLTFET with the other TFETs reported earlier

Table 2.2 compares SS, I_{on} & I_{on}:I_{off} ratios of the DGLTFET reported in this chapter, and other TFETs published earlier. Fig. 2.15 compares the performance of DGLTFET with the state-of-the-art TFETs: Line-tunneling based TFET [52], Planar area scaled TFET [53], Dual-Metal Double Gate (DMDG) TFET [76], Triple-Metal Double-Gate (TMDG) TFET [77]. The DGLTFET shows superior characteristics to most of the published TFET devices.

2.4 Comparison of the analog performance of DGLTFET with other TFETS reported earlier

Table 2.3 compares analog performance parameters like g_m, r_o, f_T and the SS, I_{on}:I_{off} ratio of the DGLTFET with other TFETs. The DGLTFET structure gives the higher g_m and higher r_o due to its excellent saturation characteristics, which improves the intrinsic gain $g_m r_o$ and unity-gain frequency f_T compared to the other state-of-the-art TFETs.

TABLE 2.2: Comparison of the DGLTFET's device performance with the other TFETs reported earlier. *Denotes unreported data in the publication.

		Simulated TFETs							Fabricated TFETs			DGLTFET
Parameter	Units	[53]	[52]	[76]	[78]	[77]	[79]	[80]	[81]	[82]	[83]	[this work]
Material	–	SiGe	SiGe	SiGe	Si	Si	Si	Si	Si	InGaAs	InGaAs	SiGe
L_{ch}	nm	20	20	50	50	150	1000	1000	100	100	150	45
Max. V_{DS}	V	0.5	1	1	1	1	1.2	0.5	1.1	0.3	0.5	1
Max. V_{GS}	V	0.5	0.7	1	1	2	1.5	0.5	2	1.2	1.5	1
I_{on}	μA/μm	80	280	6.2	22	141	0.068	0.45	1.4	6.4	135	1090
I_{off}	pA/μm	0.1	1	0.00015	0.41	110	0.019	1.7	0.1	62	50	1.5
I_{on}:I_{off}	μA/μA	10^5	10^8	10^{20}	10^8	10^6	10^6	10^5	10^7	10^5	10^4	10^9
SS	mV/dec	40	34	*	62	*	85.4	34	46	77	169	34

TABLE 2.3: Comparison of the DGLTFET's analog performance with the other TFETs reported earlier. *Denotes unreported data in the publication.

Parameter	Units	[53]	[52]	[84]	[85]	[46]	[86]	[87]	[88]	[this work]
I_{on}:I_{off}	μA/μA	10^5	10^8	10^9	10^7	10^7	10^{11}	10^{12}	10^{10}	10^9
SS	mV/dec	40	34	48	*	*	*	12.24	24.4	34
g_m	mS/μm	0.5	0.7	0.4	0.1	0.005	0.025	0.23	0.232	1
r_o	MΩ	0.1	0.1	*	0.1	0.1	*	*	*	0.9
f_T	GHz	45	250	1.19	10	*	13	37.7	2.3	111

2.5 Conclusions

The DGLTFET proposed in this chapter for analog circuit applications has roughly thrice the I_{on} and at least one order of magnitude lower I_{off} than that of an equally-sized standard MOSFET at the same technology node. The intrinsic gain of DGLTFET is far superior to the MOSFETs, and other conventional TFETs due to its higher g_m and r_o. The superior characteristics of the DGLTFET are primarily due to its excellent saturation characteristics on account of the epi-layer-based line-tunneling. Using the characteristics of the DGLTFET devices, the next chapter reports the design of multiple standard analog circuit designs, viz., CS amplifier, current mirror, and an op-amp.

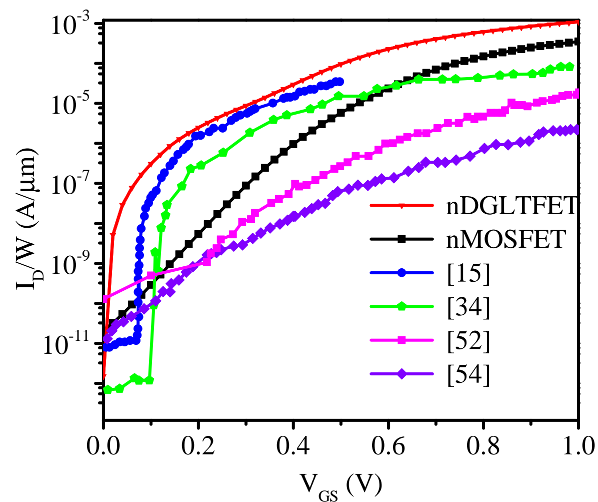


FIGURE 2.15: Comparison of the DGLTFET I_D-V_{GS} characteristics with other TFETs reported earlier.

2.6 Publications Based on This Chapter

Journals

1. **S. Hariprasad**, S. S. Dan, Ramakant Yadav, and Ashutosh Mishra, "Double-Gate Line-Tunneling FET (DGLTFET) Devices for Superior Analog Performance", Wiley International Journal on Circuits Theory and Applications, Apr 2021, DOI:10.1002/cta.3002.

Chapter 3

Analog Circuits using DGLTFET devices

This chapter goes beyond the device level and shows the implementation of analog circuits using the proposed DGLTFETs in the previous chapters. This chapter explains the device circuit methodology for designing the circuits using TFETs. The performance of the DGLTFET was benchmarked with the equivalent MOSFET at 45 nm technology node in fundamental analog VLSI circuits, viz., CS amplifier (both resistive and cascode loads), current mirror (both single-stage and cascode configurations), and a two-stage op-amp. This work shows that the DGLTFET CS amplifier has a gain-BW product or unity-gain BW f_T of 15 GHz, while that of the MOSFET CS amplifier with the same bias current is 10 GHz. The DGLTFET current mirror has at least three orders of magnitude higher r_o than the corresponding MOSFET current mirror. Similarly, the CMRR of the DGLTFET op-amp is 57 dB compared to the CMRR of 33.5 dB of the equivalent design in standard 45 nm CMOS technology.

3.1 Co-simulation Methodology and Benchmarking Criteria

The device & circuit co-simulation methodology is schematically represented in Fig. 3.1. An accurate Look-Up Table (LUT) of device characteristics viz. variation of I_D current, C_{GS} & C_{GD} capacitance obtained for various V_{DS} in the range -1 to 1 V and V_{GS} sweep from -1 to 1 V was compiled using industry-standard synopsys® TCAD tools [51]. As there is no standard SPICE models for the TFET structures in circuit simulators yet [89, 90, 91], a behavioral model

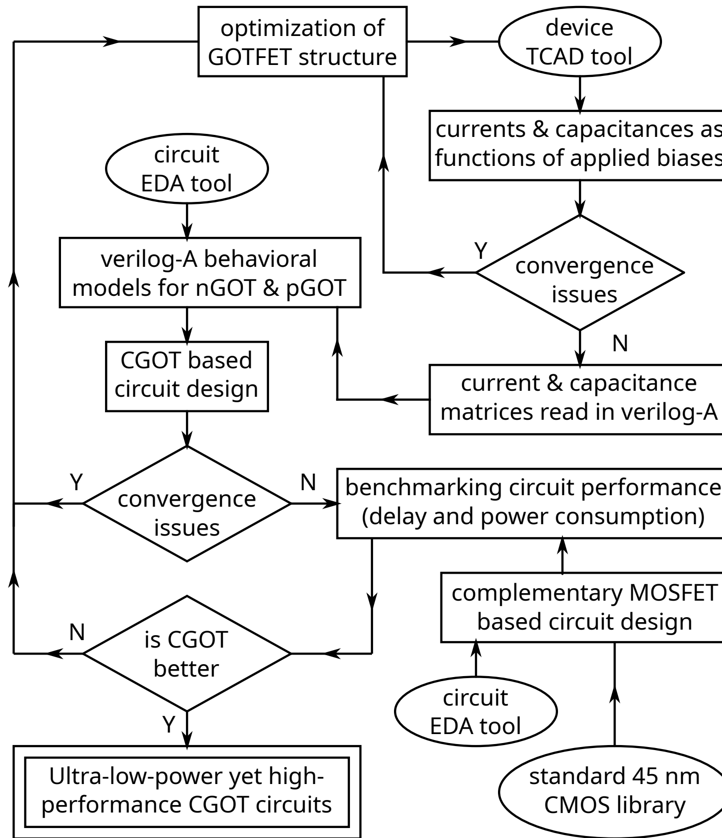


FIGURE 3.1: Flowchart explaining the co-simulation methodology used in this work.

for the proposed GOTFET was coded in verilog-A that automatically interpolates the data in LUT using shape-preserving quadratic spline techniques for accurate prediction of currents corresponding to the applied biases. Circuit performance was then evaluated and analyzed using the industry-standard cadence® EDA tools [92], using the Verilog-A code. At the time of this investigation, 45 nm CMOS generic PDK (GPDK) was distributed for free at Europractice industrial consortium [93] for academic research purposes. Cadence® [94] has customized the GPDK for integrated circuit designs using ARM 45-nm RTL-to-GDSII technology, and it has become the standard for designing all CMOS circuits in industry and academia. The effective channel lengths of the proposed TFETs have been maintained at 45 nm, and the GPDK 45 nm CMOS technology library has been used for co-simulation & benchmarking. The proposed TFET has been designed with a fixed channel length of 45 nm, and the channel width of the TFET has been kept as a design variable for circuit implementation. The device characteristics like oxide thickness, doping concentration, I_{on}, I_{off} & V_t are unique and very specific to the type of devices (TFETs and MOSFETs) because the current conduction mechanisms in TFETs and MOSFETs are entirely different, as explained in chapter 1. To carry out meaningful benchmarking, the channel widths of the corresponding devices, applied input voltages, power supplies, and load

capacitance have been kept identical in the device and circuit benchmarking test setups, and the final figure of merits have been compared.

3.2 Common source (CS) amplifier in resistive load and cascode configurations

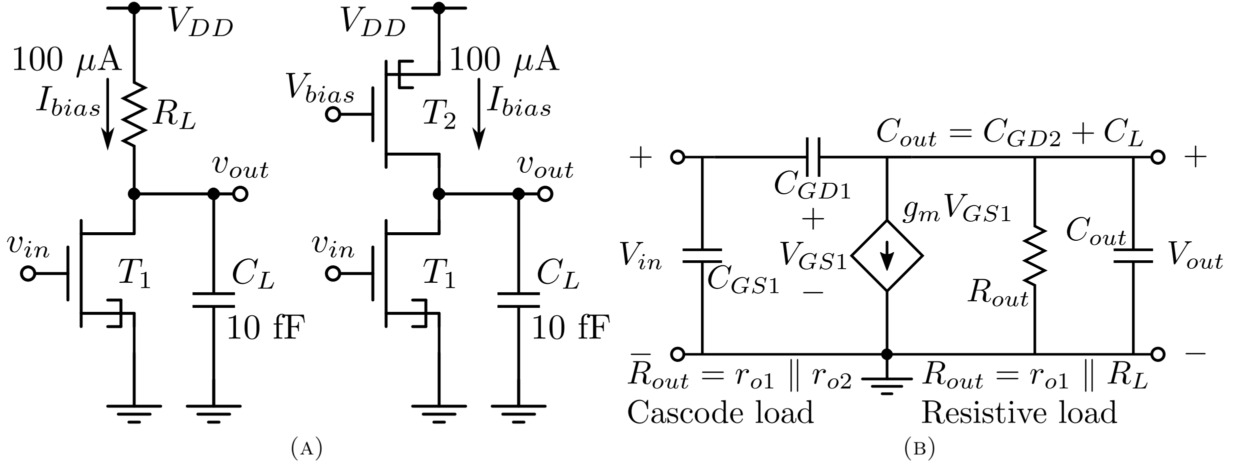
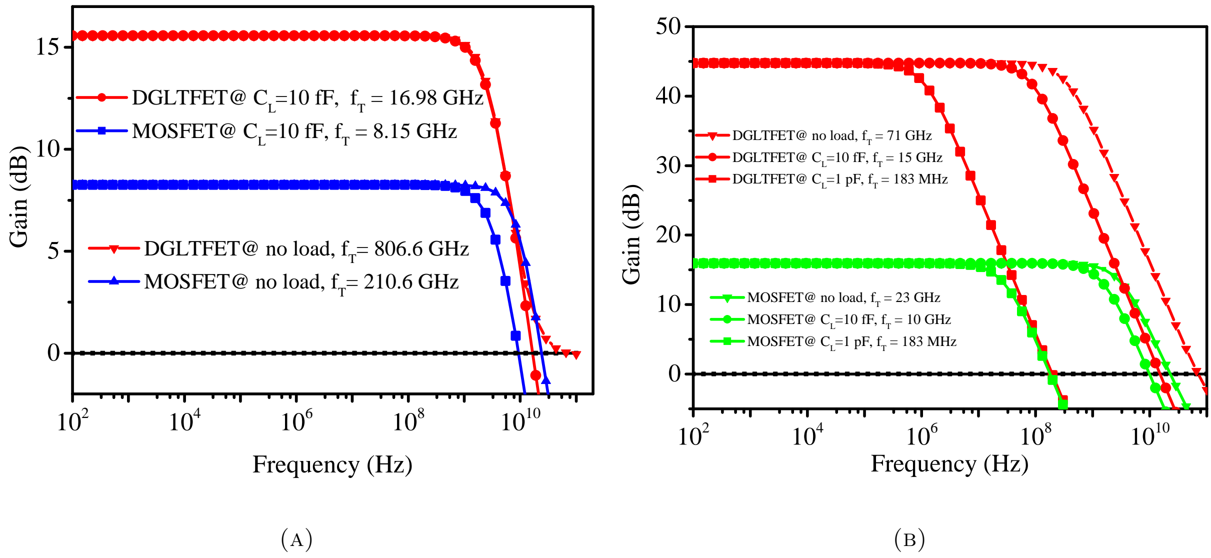


FIGURE 3.2: (a) Circuit schematics and the (b) equivalent circuits of the CS amplifier in resistive-load and cascode configurations.

The schematics of the DGLTFET-based CS amplifier in resistive load and cascode configurations are shown in Fig. 3.2a. Both the circuits operate at a supply V_{DD}=1 V and are designed for the same bias current I_{bias}=100 μA and V_{out}=V_{DD}/2 for obtaining the maximum swing. The resistive load is tuned (R_L=5 kΩ), to sustain the I_{bias}=100 μA in both DGLTFET and MOSFET-based designs. Similarly, the cascode CS stage yields maximum gain for the same bias current I_{bias}=100 μA for a V_{bias}=0.5 V and 0.4 V for DGLTFET and MOSFET-based designs, respectively. Co-simulation of the circuit was done with the same circuit implemented with 45 nm CMOS devices for the same bias currents for meaningful benchmarking. Table 3.1 shows a comparison of the cascode CS amplifier designed using the proposed DGLFET standard 45 nm MOSFET and the other TFETs reported earlier.

TABLE 3.1: Comparison of the DGLTFET cascode CS amplifier with similar other works published earlier.

Parameters	Units	[48]	[52]	[85]	[95]	[96]	MOSFET	DGLTFET
I_D	μA/μm	0.066	80	8	0.2	1.5	100	100
A_v	dB	44	38	39	50.8	23	15.95	44.7
f_T	GHz	0.0015	0.5	2	0.01	2	10	15



(A) (B)

FIGURE 3.3: AC analyses of the CS amplifier with (A) resistive-load under C_L=0 & 10 fF, and (B) cascode configuration under C_L= 0, 10 fF, 1 pF.

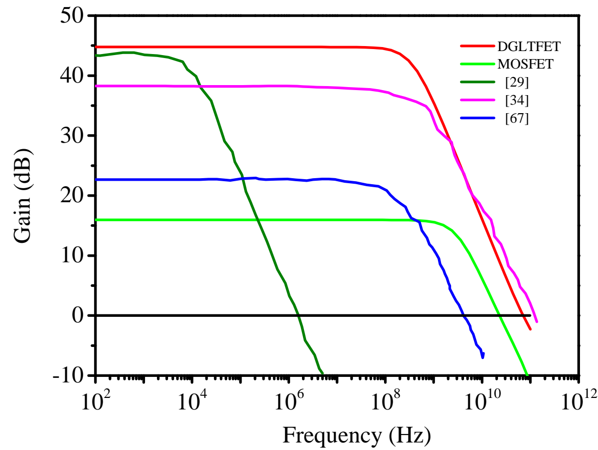


FIGURE 3.4: Mid-band gain of DGLTFET cascode CS amplifier compared with the other reported TFETs in terms of the AC analyses.

The AC gain of CS amplifier-based DGLTFET devices with resistive load is observed 8 dB higher gain compared with MOSFET technology . Similarly, the AC gain of cascode CS amplifier-based DGLTFET devices is observed 30 dB higher gain compared with MOSFETs, as shown in Fig 3.3 . The unity-gain BW [97] of the DGLTFET-based CS amplifier with resistive load is 806 GHz and 16.98 GHz without load and with a capacitive load C_L of 10 fF respectively, as compared to the unity-gain BW of 210.6 GHz (without load) and 8.1 GHz (with load) of MOSFET-based CS amplifier with resistive load. Similarly, the unity-gain BW [97] of the DGLTFET-based CS amplifier with cascode load is 71 GHz and 15 GHz without load and with capacitive load C_L=10 fF, respectively, as compared to the unity-gain BW of 23 GHz (without load) and 10 GHz (with

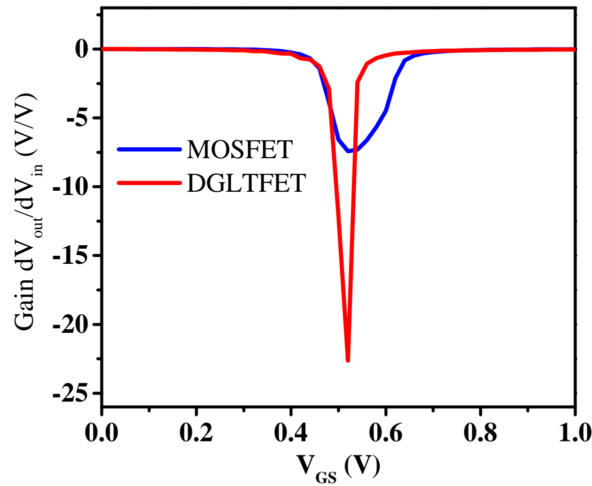


FIGURE 3.5: The gain dV_{out}/dV_{in} as a function of V_{in} of cascode CS amplifier under a V_{bias}=0.5 V.

TABLE 3.2: Comparison of the DGLTFET with the equivalent MOSFET for the resistive-load and cascode CS amplifiers.

Parameter	Units	DGLTFET	MOSFET
Drain current I_{bias}	μA	100	100
Effective channel length L	nm	45	45
Input voltage V_{in}	μV	100	100
Resistive load CS amplifier			
nFET sizes W	μm	1	1
Resistive-load R_L	kΩ	5	5
Output voltage V_{out}	mV	1	0.506
Intrinsic gain A_0	dB	15.56	8.254
Unity gain frequency f_T	GHz	16.98	8.15
Cascode CS amplifier			
pFET sizes W_p	μm	1	8
nFET sizes W_n	μm	1	3.2
Cascode bias V_{bias}	V	0.5	0.4
Output voltage V_{out}	mV	17.5	0.623
Intrinsic gain A_0	dB	44.7	15.95
Unity gain frequency f_T	GHz	15	10

the same 10 fF capacitive load) of MOSFET-based CS amplifier. Fig. 3.5 shows the V_{out} vs. V_{in} or voltage transfer characteristics (VTC) and the differential gain dV_{out}/dV_{in} vs. V_{in} in the same figure. It shows that the transition slope of the DGLTFET-based CS amplifier is much steeper than the transition slope of the CMOS-based CS amplifier. The summary of the benchmarking is shown in Table 3.2.

3.3 Small-signal analysis of the CS amplifier

Fig. 3.2b shows the small-signal equivalent circuit for the CS amplifier of Fig. 3.2a. The net output resistance R_{out}=$r_{o1}\|R_L$ where the load R_L of the resistive load and the cascode configurations are R_L=R_D and R_L=r_{o2}, respectively. Maximizing the gain A_{vo}=$-g_{m1}R_{out}$ necessitates maximizing the R_{out} value. Hence, the cascode configuration is always preferred over the simpler resistive load, since (i) $r_{o2}\gg R_D$ when TFET T_2 is biased in the saturation region (ensured by the V_{bias}) and (ii) transistor fabricating a large enough passive resistive load R_D is very difficult in scaled IC technology. The output capacitance C_{out}=C_{GD1}+C_{DB1}+C_{GD2}+C_{DB2}+C_L and C_{out}=C_{GD1}+C_{DB1}+C_L for cascode and resistive-load configurations, while under no-load condition C_L=0. It is worthy of note that DGLTFET being a symmetric double-gate structure, the gate("front gate") and the body("body gate") terminals are shorted together. Thus, C_{GD1}=C_{DB1} and C_{DB2}=C_{GD2}, making the net C_{GD} capacitance in DGLTFET slightly larger than that of the equivalent MOSFETs, as evident in Fig.2.12b. On the other hand, C_{GS} in DGLTFET is larger than C_{GS} of the equivalent MOSFET since C_{GS} in DGLTFET is dominated by the gate-source overlap capacitance C_{ov}, which is larger than the MOSFET. For the resistive-load DGLTFET CSA, the typical values are C_{GS}=1.78 fF & C_{GD}=1.5 fF; while for the equivalent CMOS resistive-load CSA, the C_{GS}=1.7 fF & C_{GD}=0.148 fF. Similarly, for the cascode-load DGLTFET CSA, the typical values are C_{GS1}=C_{GS2}=1.7 fF & C_{GD1}=C_{GD2}=1.5 fF; while for the equivalent CMOS cascode-load CSA, the C_{GS1}=1.7 fF, C_{GS2}=3.7 fF, C_{GD1}=0.474 fF, C_{GD2}=1.6 fF. We have used the admittance **Y** parameter matrix for the small-signal analysis.

$$I_{in} = s\left(C_{GS1} + C_{GD1}\right)V_{in} - sC_{GD1}V_{out} \qquad \& \qquad I_{out} = \left(g_{m1} - sC_{GD1}\right)V_{in} + \left(\frac{1}{r_{o1}} + sC_{out}\right)V_{out} \tag{3.1}$$

$$\mathbf{Y} \equiv \begin{bmatrix} s\left(C_{GS1} + C_{GD1}\right) & -sC_{GD1} \\ g_{m1} - sC_{GD1} & \frac{1}{r_{o1}} + sC_{out} \end{bmatrix} \tag{3.2}$$

From Fig. 3.2b, V_{out}=$-I_{out}R_L$, which leads to

$$A_v \equiv \frac{V_{out}}{V_{in}} = -\frac{Y_{21}}{Y_{22} + \frac{1}{R_L}} = -\frac{g_{m1} - sC_{GD1}}{\left(\frac{1}{R_L} + \frac{1}{r_{o1}}\right) + sC_{out}} = -g_{m1}R_{out}\left(\frac{1 - s\frac{C_{GD1}}{g_{m1}}}{1 + sC_{out}R_{out}}\right) \tag{3.3}$$

$$A_{vo} = -g_{m1}R_{out} \qquad \& \qquad f_T = \frac{g_{m1}}{2\pi C_{out}} \qquad \& \qquad f_{3dB} = \frac{1}{2\pi R_{out}C_{out}} \tag{3.4}$$

Eqs. (3.4) yield A_{vo}=43 dB & 14.6 dB and under a capacitive load of 10 fF, f_T=12.2 GHz & 13 GHz for DGLTFET & MOSFET based CS amplifier respectively, which are close to the simulation results.

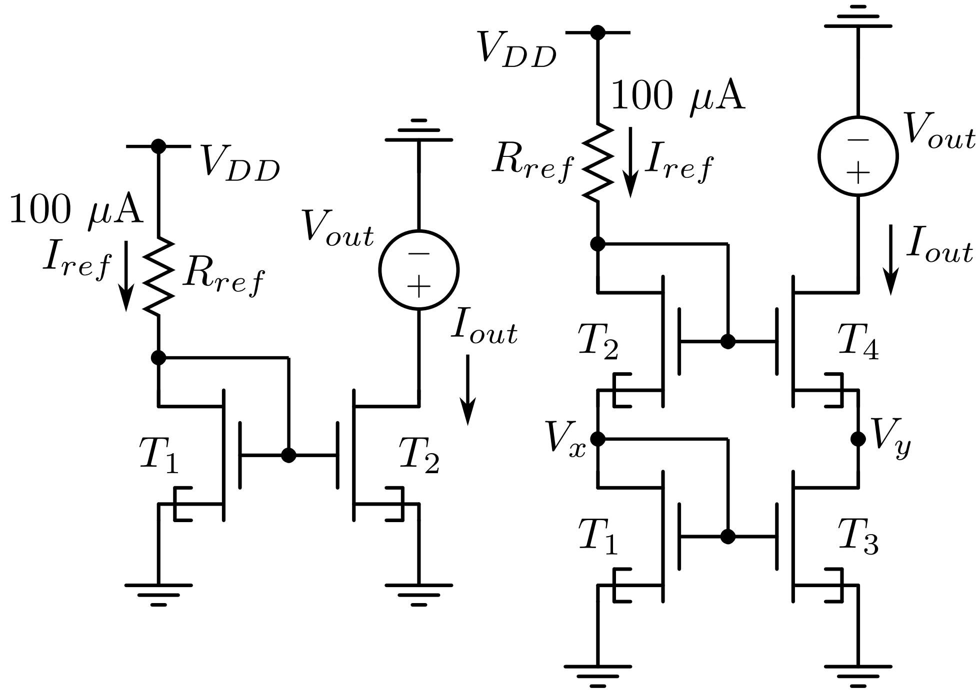


FIGURE 3.6: Circuit schematics of the current mirrors in (a) single-stage and (b) cascode configurations.

3.4 DGLTFET based single stage and cascode current mirrors

The schematic of the DGLTFET-based single stage and cascade current mirrors are shown in Fig. 3.6. Co-simulation of the circuits was carried out with the same circuits implemented with 45 nm CMOS devices. The same reference current I_{ref}=100 μA was used in the DGLTFET and CMOS-based circuits for meaningful benchmarking, leading to an R_{ref}=5 kΩ and 2.4 kΩ for the DGLTFET and MOSFET-based designs, respectively. Following the same strategy for the cascode current mirror, R_{ref}= 8 kΩ and 2 kΩ for the DGLTFET and MOSFET-based designs, respectively, summarized in Table 3.3. In conventional MOSFETs, the effect of channel length modulation is high at lower technology nodes resulting in low R_{out} of the current mirror circuit. In contrast, the DGLTFET-based current mirror has R_{out} more than three orders of magnitude higher than its MOSFET counterpart, as shown in Fig. 3.8a. Low R_{out} of the CMOS current mirror makes the I_{out} more dependent on V_{out}, while the I_{out} of DGLTFET-based current mirror is relatively independent of V_{out}, as shown in Fig. 3.7a.

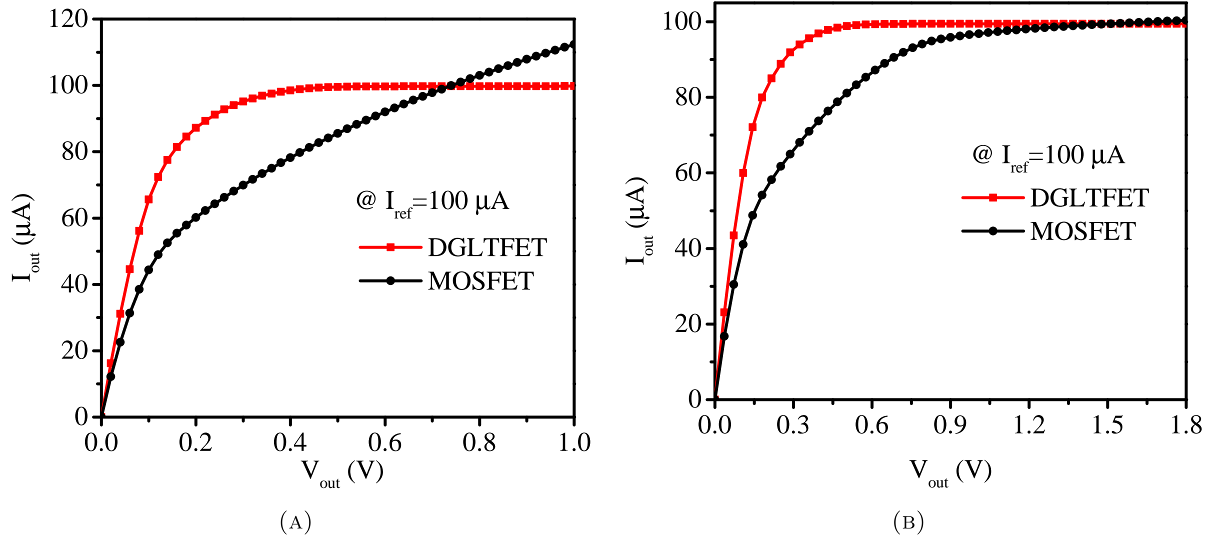


FIGURE 3.7: I_{out} vs. V_{out} in (A) the single-stage current mirror. (B) the cascode current mirror.

TABLE 3.3: Comparison of the DGLTFET with the equivalent MOSFET for the single-stage and cascode current mirrors.

Parameter	Units	DGLTFET	MOSFET
Reference current I_{ref}	μA	100	100
Effective channel length L	nm	45	45
Single stage current mirror			
nFET sizes W	μm	1	1
Reference resistance R_{ref}	kΩ	5	2.4
Output resistance R_{out}	MΩ	64	0.022
Cascode current mirror			
nFET sizes W	μm	1	1
Reference resistance R_{ref}	kΩ	8	2
Output resistance R_{out}	MΩ	4000	3.5

The output resistance R_{out} of the DGLTFET-based cascode mirror is at least two orders of magnitude higher than that of the DGLTFET-based single stage current mirror circuit and five orders higher than the CMOS-based cascode mirror circuit, as observed from Fig. 3.8b and Table 3.3. The minimum value of V_{out} at which the current saturates in DGLTFET-based current mirror circuit is significantly lower than CMOS-based current mirror circuits due to DGLTFET's lower V_t.

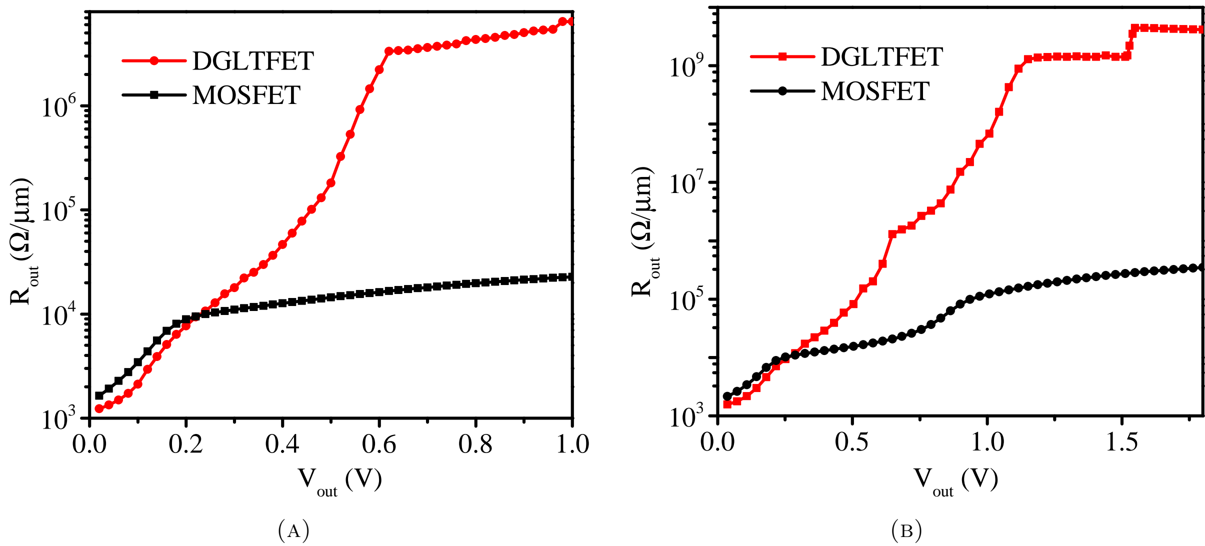


FIGURE 3.8: Output resistance R_{out} of (A) single stage and (B) cascode current mirror.

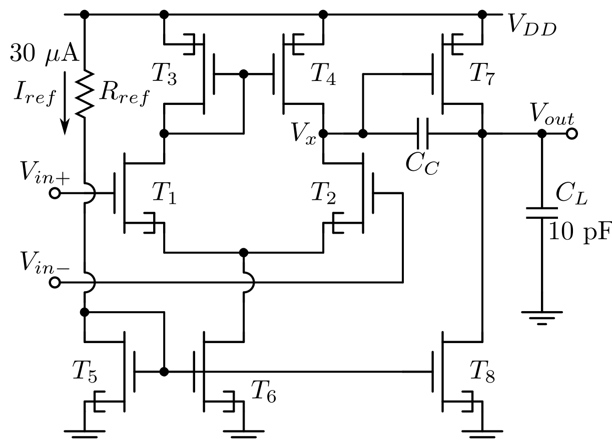


FIGURE 3.9: Schematic of a two-stage complementary DGLTFET op-amp

3.5 Two-stage operational amplifier (op-amp)

The op-amp is one of analog VLSI design's most important fundamental building blocks. Fig. 3.9 shows the schematic of the two-stage op-amp implemented with the DGLTFET, designed for a unity-gain bandwidth f_T=5 MHz at V_{DD}=1 V. The co-simulation of the circuits were carried out with the same circuits implemented with 45 nm CMOS devices whose transistor widths and performance parameters are compared in Table 3.4 & 3.5.

The same bias current I_{bias}=30 μA was used in the DGLTFET and CMOS-based circuits for meaningful benchmarking, leading to a R_{ref}=40 kΩ in the DGLTFET-based design. The nDGLTFETs T_1 & T_2 of the first stage are input transistors for achieving the higher g_m, and

TABLE 3.4: Transistor sizes used in the two-stage op-amp design at the 45 nm technology node.

Transistors	Unit	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8
DGLTFET W	μm	1	1	1	1	0.5	1	10	5
MOSFET W	μm	0.8	0.8	0.8	0.8	0.3	2	3	2

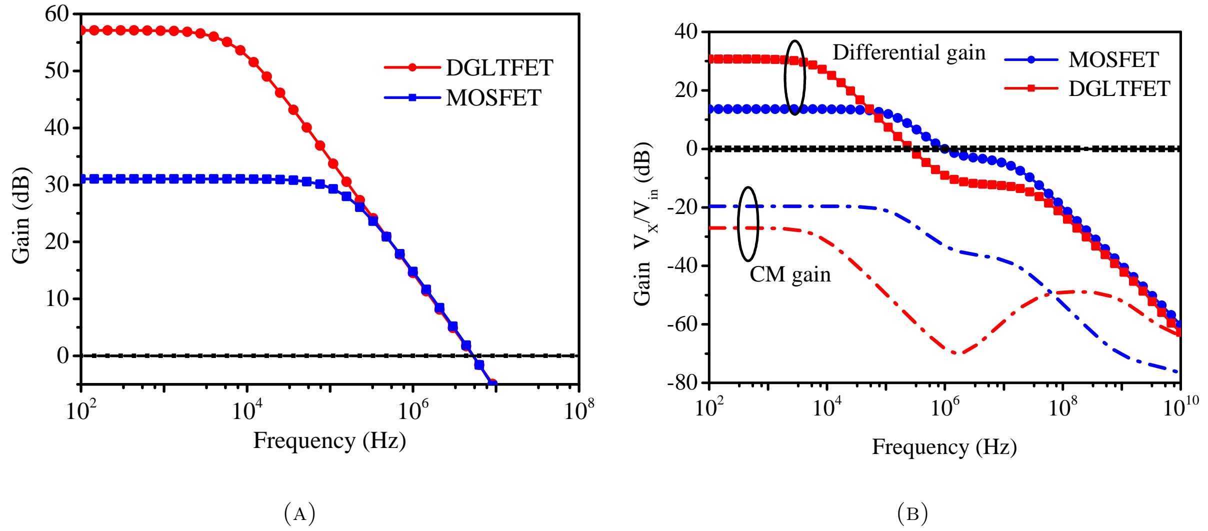
TABLE 3.5: Comparison of two-stage op-amp designed with DGLTFET and the equivalent MOSFET for an f_T=5 MHz.

Parameters	Units	DGLTFET	MOSFET
Bias current I_{ref}	μA	30	30
Effective channel length L	nm	45	45
Load capacitance C_L	pF	10	10
Compensation capacitance C_C	pF	4	4
Unity gain frequency f_T	MHz	5	5
Gain V_{out}/V_d	dB	57	31
Differential gain V_x/V_d	dB	30	13.5
Common-mode gain V_x/V_{cm}	dB	-27	-20
CMRR	dB	51	33.5
Phase margin (PM)	degree	76	62
3-dB band width f_{3dB}	kHz	7.7	120

TABLE 3.6: Comparison of the DGLTFET-based two-stage op-amp with similar other works on TFETs published earlier.

Parameters	Units	[98]	[99]	[100]	[48]	MOSFET	DGLTFET
V_{DD}	V	1	0.5	4.5	2.5	1	1
I_{ref}	μA	0.0036	0.01	0.00375	1.275	30	30
A_v	dB	27.7	39.4	130	110	31	57
f_{3dB}	kHz	3.2	2.1	0.1	0.02	120	7.7

pDGLTFETs T_3 & T_4 are the current mirror loads. DGLTFETs T_7 & T_8 form the second stage CS amplifier. The gains of the first and second stages are $g_{m1}\,(r_{01} \parallel r_{03})$ and $g_{m8}\,(r_{07} \parallel r_{08})$, respectively. For improved stability of the circuit, the phase margin (PM) should be higher than 60 degrees. To achieve at least 60 degrees PM, we have chosen the compensation capacitor C_C=4 pF (>0.22C_L), where C_L=10 pF is the load capacitor. Fig. 3.10a shows that the overall gain of the DGLTFET-based two-stage op-amp is 26 dB higher than the MOSFET op-amp for the same f_T. The differential gain of the DGLTFET op-amp exceeds six times that of the MOSFET op-amp due to the superior saturation region characteristics of the pDGLTFET current mirror load and higher g_m of the input nDGLTFET transistors, as shown in Fig. 3.10b. Furthermore, the common mode gain of DGLTFET is significantly lower (by around 6 dB) compared to the MOSFET due to its higher output resistance of the current mirror-based tail current source. The



(A) (B)

FIGURE 3.10: (a) The overall gains A_v of the two-stage op-amp for an f_T=5 MHz. (b) The differential A_d and common mode (CM) gains A_{cm} of the op-amp differential stage for the overall f_T=5 MHz.

common-mode rejection ratio (CMRR) of the op-amp designed with complementary DGLTFET devices is 23.5 dB (15 times) higher than the CMRR of the equivalent CMOS circuit, primarily due to the former's higher differential gain and lower common-mode gain. Table 3.6 compares the DGLTFET op-amp with the other TFET op-amps reported earlier. Some of the previous works[100, 48] exhibit higher gains than the DGLTFET-based design since they used higher V_{DD} as they did not specifically conform to any industry-standard technology library which strictly adhered to the ITRS roadmaps. With increasing V_{DD}, V_{DS} across every transistor increases, increasing r_o, as seen in Fig. 2.13a , enhancing the gain $g_m r_o$. However, following the ITRS roadmap, the 45 nm technology node limits the maximum V_{DS} that can be applied across the transistors to be 1 V.

3.6 Conclusions

Chapter 2 described the characteristics of DGLTFET devices and their analog performance, and this chapter explained the circuit performance of DGLTFET devices. The AC gain of CS amplifier-based DGLTFET devices with resistive load provides 8 dB higher than MOSFET technology. Similarly, the AC gain of cascode CS amplifier-based DGLTFET devices is 30 dB higher than MOSFETs. The DGLTFET-based current mirror circuits provide superior I_{out} saturation characteristics due to the negligible channel length modulation effect in the DGLTFET than the MOSFETs. Furthermore, the output resistance R_{out} of the DGLTFET is

approximately three orders higher than the MOSFETs. The two-stage op-amp implemented with the DGLTFET yields 23.5 dB higher CMRR compared to the MOSFET-based design. In conclusion, DGLTFETs reported in this chapter are preferable candidates to replace MOSFETs in analog VLSI applications.

3.7 Publications Based on This Chapter

Journals

1. **S. Hariprasad**, S. S. Dan, Ramakant Yadav, and Ashutosh Mishra, "Double-Gate Line-Tunneling FET (DGLTFET) Devices for Superior Analog Performance", Wiley International Journal on Circuits Theory and Applications, Apr 2021, DOI:10.1002/cta.3002.

Chapter 4

Superior Analog Performance due to Source-Gate Overlap in Vertical Line-Tunneling FETs and Their Circuits

4.1 Introduction

Vertically grown TFETs [101, 102, 103] are preferred as they allow the integration of more TFETs on a single chip, increasing device density. In this chapter, the VLTFET device has been optimized for superior analog performance, and the influence of overlap length L_{ov} on the device and circuit performance has been analyzed and successfully explained using physics.

4.2 VLTFET Device Structure and its Characteristics

4.2.1 VLTFET Device Structure

Fig. 4.1 shows the schematic and the BtB generation of the epitaxial (epi-) layer-based nVLTFET structure. A 3 nm thick epitaxial layer of n-type Si is sandwiched between the SiGe layers (source & pocket), doped with P to sharpen the band profile [103, 104]. Considering the device reliability, the source pocket with an intermediate mole fraction, compared to the source and the channel

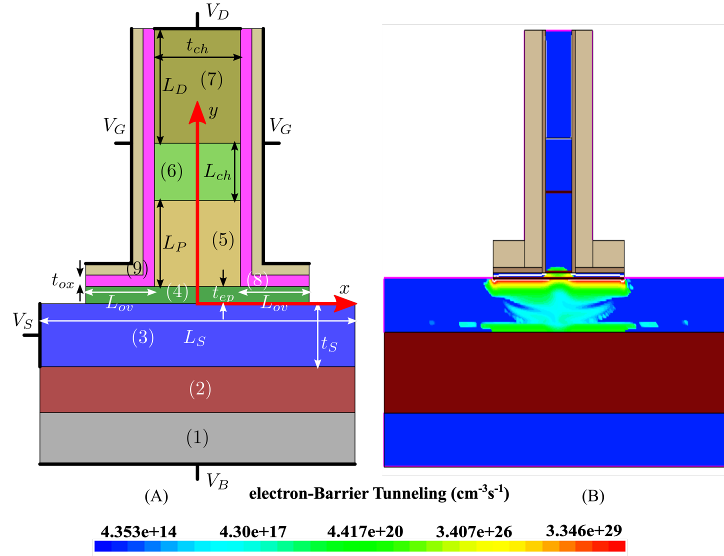


FIGURE 4.1: (a) Schematic cross-sectional view (1) Si substrate (2) SOI (3) p$^+$ SiGe Source (4) n$^+$ Si epitaxial layer (5) i-SiGe Pocket (6) i-Si channel (7) n$^+$ Si drain (8) HfO_2 gate oxide (9) TiN metal gate. (b) Electron BtB tunneling rate of nVLTFET device.

regions, leads to sharpening the band profiles without the risk of junction breakdown. $Si_{0.5}Ge_{0.5}$ is used as the source to improve the device's performance. A 2 nm thick HfO_2 layer is used as the high-κ dielectric layer for better electrostatic control of the gate over the tunneling junction. TiN metal is deposited as the gate terminal material. Table 4.1 lists the device parameters and doping concentrations of all the regions. The 2D numerical simulations of the VLTFET device structure were performed using the dynamic non-local path tunneling model to capture the BtB generation across all the interfaces. The bandgap narrowing model, Fermi-Dirac statistics mobility, doping-dependent mobility, and Shockley-Read-Hall (SRH) generation/recombination models were activated to capture the carrier action in the device.

4.2.2 Physics-Based Modeling Approach

Modeling of the VLTFET structure can be done in two steps. Firstly solve the Poisson equation from the boundary condition to calculate the surface potential $\phi(x, y)$ and electric field $F_y(x, y)$. The second step calculates the tunneling generation rate G_{BtB} and integration over the tunneling volume for the I_D. The continuity of the displacement vector at the source & epitaxial layer and epitaxial layer & oxide interfaces yield

$$\varepsilon_{sg}\left(\frac{\partial\phi}{\partial y}\right)_{y=0,t_{si}} = \varepsilon_{ep}\cdot\frac{\phi_s-\phi_e}{t_{ep}} = \varepsilon_{ox}\left(\frac{\phi_e-V_G'}{t_{ox}}\right) \tag{4.1}$$

TABLE 4.1: Parameters of the nVLTFET and pVLTFET devices.

Parameter	Units	nVLTFET		pVLTFET	
Channel length L_{ch}	nm	20		20	
Source length L_S	nm	1000		1000	
Overlap length L_{ov}	nm	30		30	
Drain length L_D	nm	40		40	
Pocket length L_P	nm	30		30	
Epi-layer length L_{ep}	nm	20		20	
Gate oxide thickness t_{ox}	nm	2		2	
Channel thickness t_{ch}	nm	15		15	
Source thickness t_S	nm	20		20	
Epi-layer thickness t_{ep}	nm	3		3	
Source doping N_S	$/cm^3$	2×10^{20}	p^+ $Si_{0.5}Ge_{0.5}$	2×10^{20}	n^+Si
Pocket doping N_P	$/cm^3$	10^{16}	$iSi_{0.75}Ge_{0.25}$	10^{16}	$iSi_{0.75}Ge_{0.25}$
Channel doping N_{ch}	$/cm^3$	10^{16}	iSi	10^{16}	iSi
Drain doping N_D	$/cm^3$	5×10^{19}	n^+Si	5×10^{19}	p^+Si
Epi-layer doping N_{ep}	$/cm^3$	5×10^{18}	n^+Si	5×10^{18}	p^+ $Si_{0.5}Ge_{0.5}$
Gate work-function Φ_m	eV	4.3	TiN	4.7	Ag

where ε_{sg}, ε_{ep}, & ε_{ox} denote the permittivities of the SiGe source, epi-layer material, & oxide, respectively. Using (4.1) in the solution of the 2D Poisson equation, we obtain the following expression for the 2D potential profile below the gate-source overlap.

$$\phi(x,y) = \phi_s(x) + \frac{y}{\varepsilon_{sg}} \left[\frac{\phi_s(x) - V_G'}{\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{ep}}{\varepsilon_{ep}}} \right] \left(1 - \frac{y}{2t_{si}} \right) \tag{4.2}$$

Differentiating (4.2) along the vertical y axis, we obtain the 2D vertical field profile

$$F_y(x,y) \equiv -\frac{\partial \phi}{\partial y} = \frac{1}{\varepsilon_{sg}} \left[\frac{V_G' - \phi_s(x)}{\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_{ep}}{\varepsilon_{ep}}} \right] \left(1 - \frac{y}{t_{si}} \right) \tag{4.3}$$

The BtB generation rate G_{btb} used in numerical simulation is given by

$$G_{btb} = AF_{yov}^{\gamma} \exp\left(-\frac{B}{F_{yov}} \right) \tag{4.4}$$

where γ=2 & 2.5 for direct and phonon-assisted tunneling process, respectively. F_{yov} & F_{ych} denote the vertical fields $F_y(x,y)$ in the overlap (within L_{ov}) and channel (within t_{ch}) regions, respectively. For direct BtB generation in direct band-gap materials, material-dependent factors

A & B are given by [105]

$$A = \left(\frac{g\pi}{9}\right)\left(\frac{q}{h}\right)^{\gamma}\sqrt{\frac{m_t}{E_g}} \quad \& \quad B = \frac{\pi^2\sqrt{m_t}E_g^{3/2}}{qh} \tag{4.5}$$

g denotes the degeneracy factor of the material used, and h is the Plank's constant. For phonon-assisted BtB generation in indirect band-gap materials, A & B are given by [106]

$$A = \left(\frac{gm_{avg}^{3/2}}{\sqrt{2}}\right)\left(\frac{1+2N_{op}}{\rho\varepsilon_{op}}\right)D_{op}^2\left(\frac{q}{h}\right)^{\gamma}\left(\frac{m_t}{2E_g}\right)^{7/4} \tag{4.6}$$

$$B = \frac{4\pi\sqrt{m_t}(2E_g)^{3/2}}{3qh} \tag{4.7}$$

The tunneling effective mass (also called 'reduced mass') m_t=$(m_c^{-1}$+$m_v^{-1})^{-1}$ and the average mass m_{avg}=$(m_c$+$m_v)/2$ are related as

$$\frac{1}{m_c} = \frac{1}{2m_t} + \frac{1}{m_0} \quad \& \quad \frac{1}{m_v} = \frac{1}{2m_t} - \frac{1}{m_0} \tag{4.8}$$

m_0 is the rest mass of electrons, m_c & m_v are the density of states effective masses in the conduction and valence bands . Line tunneling occurs due to the vertical field $\hat{y}F_{yov}$ (in the vertical $\hat{y}$ direction) so that the total number of free carriers n generated within the source due to BtB and the net drift current is obtained from

$$n = 2W\int_x\int_y G_{btb}dydx \quad \& \quad I_D = qn\mu_nF_{ych} \tag{4.9}$$

where W denotes the width of the device, and a factor of 2 is added as this is a double gate device. Current I_D is modeled using the standard drift transport along the channel due to the field $\hat{y}F_{ych}$ as a result of V_{DS} bias.

4.2.3 Calibration of the Simulation Deck With Experiments

Initially, the device in [103] was simulated using the default parameters in the TCAD simulator. Then the parameters were modified so that the final characteristics matched with experimental data published in [103]. The match between the results of the calibrated simulation deck with the experimental data is shown in Fig. 4.2. The calibrated values of m_c and m_v are $0.328m_o$ and $0.549m_o$ for Si and $0.328m_o$ and $0.421m_o$ for $Si_{0.75}Ge_{0.25}$ materials, which were also used

in [107]. Additionally, the material-dependent parameters A_{indr} and B_{indir} for $Si_{0.5}Ge_{0.5}$ were extracted as 2.27×10^{15} /cm^3/s and 15.5 MV/cm.

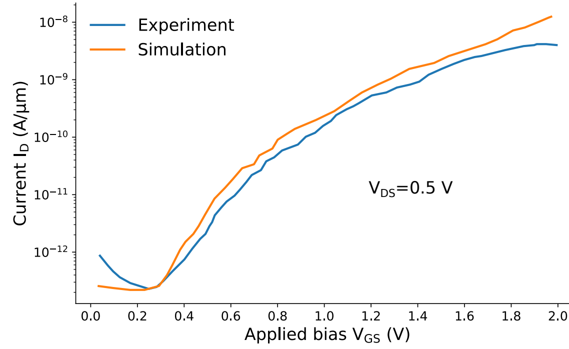


FIGURE 4.2: Calibration of simulation models with the prefabricated device at V_{DS}=0.5 V [103]

4.2.4 VLTFET fabrication process

One can fabricate the VLTFET structure using the following steps, as reported in [62, 102, 103, 63, 64, 65, 66, 67, 68, 36]:

(i) Starting with Si bulk wafer.

(ii) Initial stacks composed of SiGe and Si layers grown by chemical vapor deposition (CVD) technique.

(iii) Si layers patterned like pillar structures by reactive ion etching (RIE).

(iv) $Si_{0.75}Ge_{0.25}$ etch stop layer is removed with selective wet chemistry, leaving a smooth Si surface.

(v) Deposit Si (epi-layer) using oxidation and etched by hydrogen fluoride (HF).

(vi) Gate stack HfO_2/TiN deposited by atomic layer deposition (ALD) to cover the side wall of the pillar continuously.

4.3 Physical Explanation of VLTFET Behavior

Fabrication steps for the VLTFET structure were reported earlier [103, 104, 62, 63, 64, 65, 66, 67, 68, 36]. The transfer characteristics are shown in Fig. 4.3a for L_{ov}=30 nm. I_D obtained

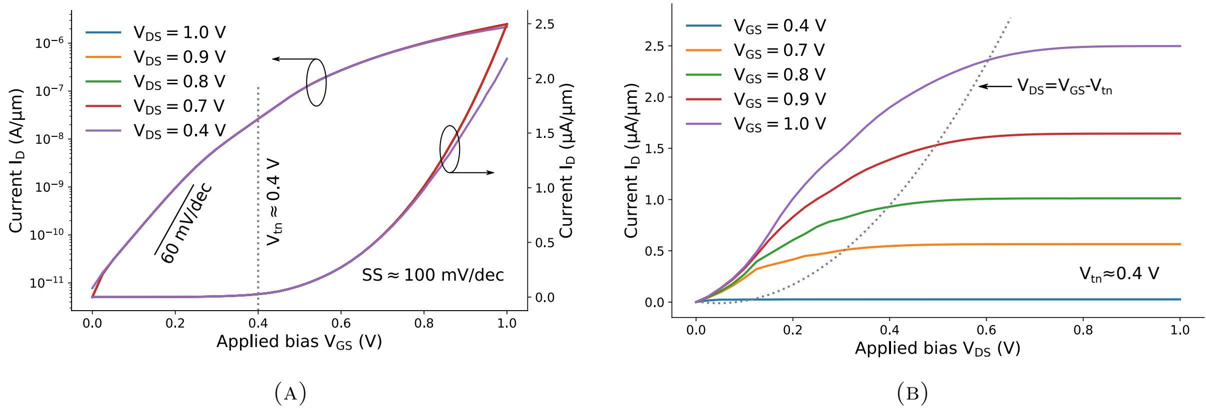


FIGURE 4.3: (a) I_D-V_{GS} characteristics of nVLTFET for different V_{DS} and (b) I_D-V_{DS} characteristics of nVLTFET for different V_{GS}.

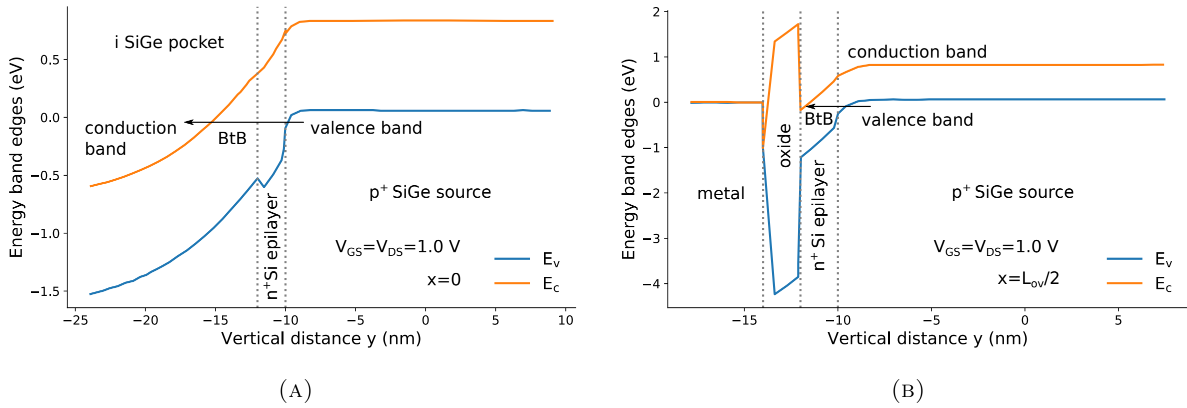


FIGURE 4.4: BtB tunneling profile along the (a) Source & Pocket (@x=0) and (b) Source & Epi-layer (@x=$L_{ov}/2$) in the n-type VLTFET for V_{GS}=V_{DS}=1 V.

due to non-local BtB tunneling is I_{on}=2.4 μA/μm for V_{GS}=1 V and I_{off}=5 pA/μm for V_{GS}=0 V at V_{DS}=1 V. Threshold voltage is extracted using the third derivative method [108] where $\partial^3 I_D/\partial V_{GS}^3$ for V_{DS}=1 V has its first peak, giving $V_{tn}\approx$0.4 V. In conventional TFETs (working on the principle of lateral BtB due to the lateral field from source to intrinsic channel $\widehat{x}F_x$), electrons tunnel from the valence band of the p$^+$ source to the conduction band of the intrinsic (or low-doped) channel under the gate (point tunneling). VLTFET operates fundamentally on the same physical principle of BtB tunneling but with a different strategy than conventional TFETs. When a VLTFET is switched on, BtB tunneling occurs with the electrons from the valence band of the p$^+$ source directly tunneling into the conduction band of the n$^+$ epi-layer under the source-gate overlap (line tunneling) as indicated in Fig. 4.4. In a conventional TFET, BtB tunneling is caused by the lateral field $\widehat{x}F_x$, while in a VLTFET, BtB tunneling occurs due to the vertical field $\widehat{y}F_{yov}$.

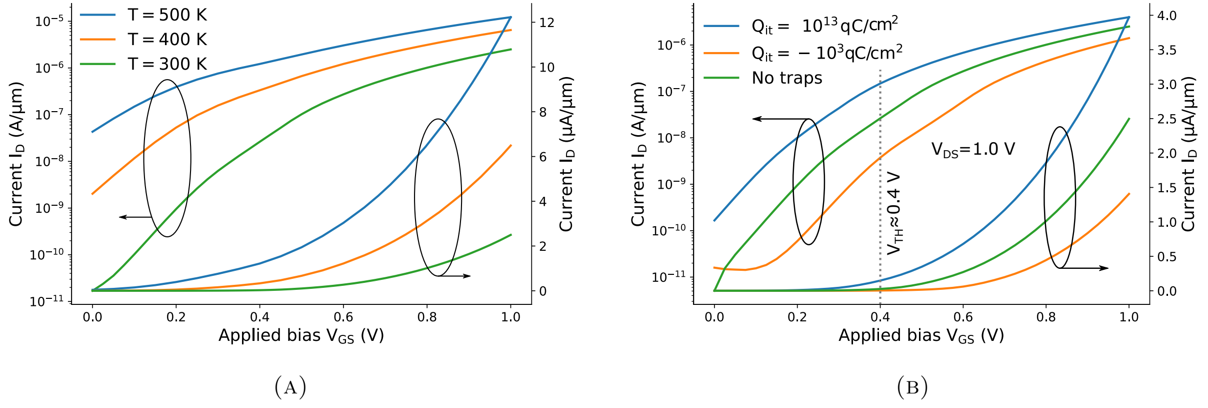


FIGURE 4.5: (a) Influence of temperature on the VLTFET characteristics. (b) Effect of interface trap charges on I_D-V_{GS} characteristics.

The influence of temperature on the VLTFET characteristics is shown in Fig. 4.5a. As expected, increased temperature reduces the bandgap due to the expanding crystal lattice and weakening of interatomic bonds. Reduction in the bandgap increases the tunneling probability; therefore, BtB generation increases, leading to increasing currents. The Field-Induced Quantum Confinement (FIQC) effect leads to a shift in V_t, decreasing the I_{on} substantially [31]. However, the impact of FIQC can be reduced by tuning the work function of gate metal. Furthermore, the influence of the semiconductor/gate oxide interface trap charges Q_{it} on I_D-V_{GS} characteristics [71] is shown in Fig. 4.5b. It was observed that an increase in the donor (acceptor) impurities increase (decrease) the I_{off} & I_{on}, decreasing (increasing) V_t, degrading the SS. The output characteristics for the VLTFET are shown in Fig. 4.3b for different V_{GS}.

The portion of the I_D-V_{DS} characteristics within the range $0<(V_{GS}\text{-}V_t)\leq V_{DS}<V_{GS}$ is the *soft saturation* region, while *deep saturation* occurs for $V_t<V_{GS}\leq V_{DS}$, where V_{DS} loses control over the carrier density, and as a consequence, a constant carrier density is maintained. For a given value of V_{GS} with increasing V_{DS}, initially, the electron density decreases in the epi-layer over the source region. Beyond a certain V_{DS}, electron density becomes independent of any further increase in V_{DS} as shown in Fig. 4.6a. Fig. 4.6b shows that the surface potential near the source region becomes independent of V_{DS} beyond saturation. Inversion charges are formed near the source junction due to vertical BtB tunneling due to the vertical field, flattening the I_D characteristics.

Tunneling width W_{tun} (Fig. 4.8a) remains constant at its minimum after saturation. As V_{DS} has less impact on I_D beyond saturation, r_o is in the order of 100 MΩ/μm, as shown in Fig. 4.7b for different V_{GS} biases. Increasing the L_{ov} increases the vertical BtB tunneling due to the increase

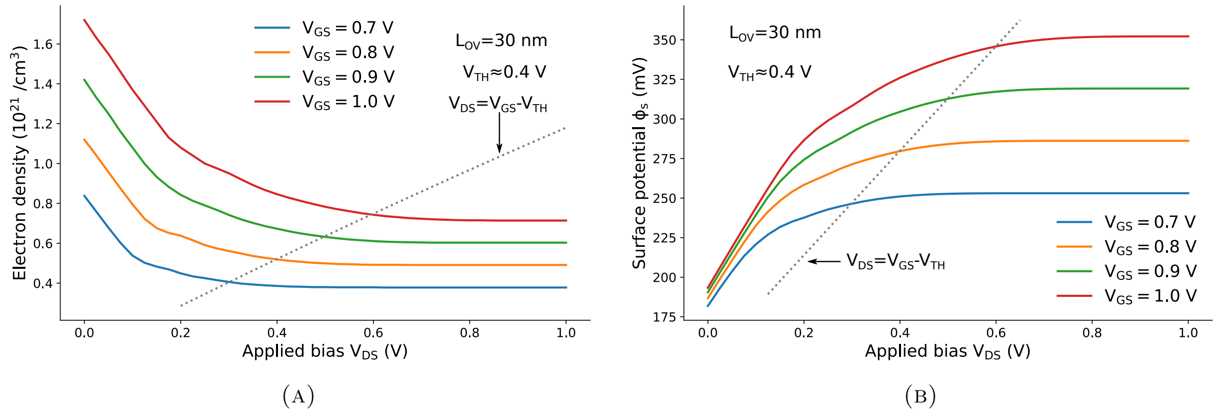


FIGURE 4.6: Effect of (a) eDensity (b) Surface potential at the epi-layer region for different values of V_{DS}

in tunneling cross-section, resulting in an increase in I_{on} as shown in Fig. 4.8b, increasing g_m, without affecting r_o, as depicted in Fig. 4.9. In VLTFET, A_{vo} can be improved with increasing L_{ov} since g_m increases with L_{ov}. In contrast, r_o remains constant, as seen in Fig. 4.10.

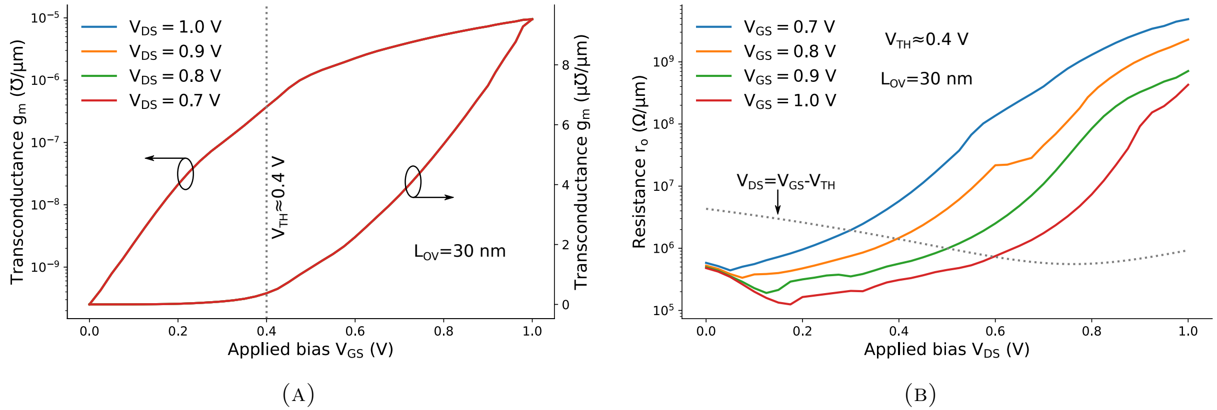


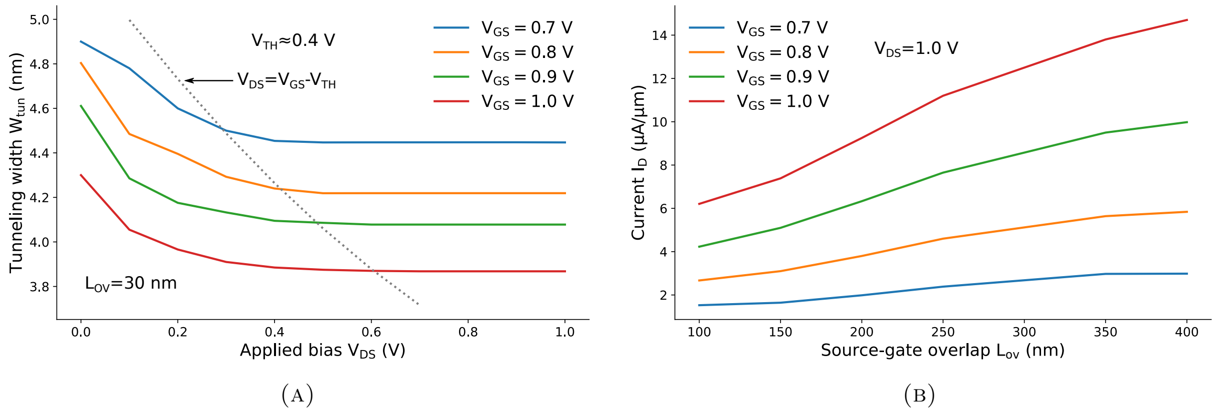
FIGURE 4.7: Variation in (A) transconductance g_m and (B) output resistance r_o in the VLTFET.

Gate capacitances are extracted by computing the rate of change in the charges accumulated on the gate terminal with gate terminal voltages using their fundamental definitions

$$C_{GD} \equiv \left.\frac{\partial Q_G}{\partial V_D}\right|_{V_S,V_G} \quad \& \quad C_{GS} \equiv \left.\frac{\partial Q_G}{\partial V_S}\right|_{V_D,V_G} \tag{4.10}$$

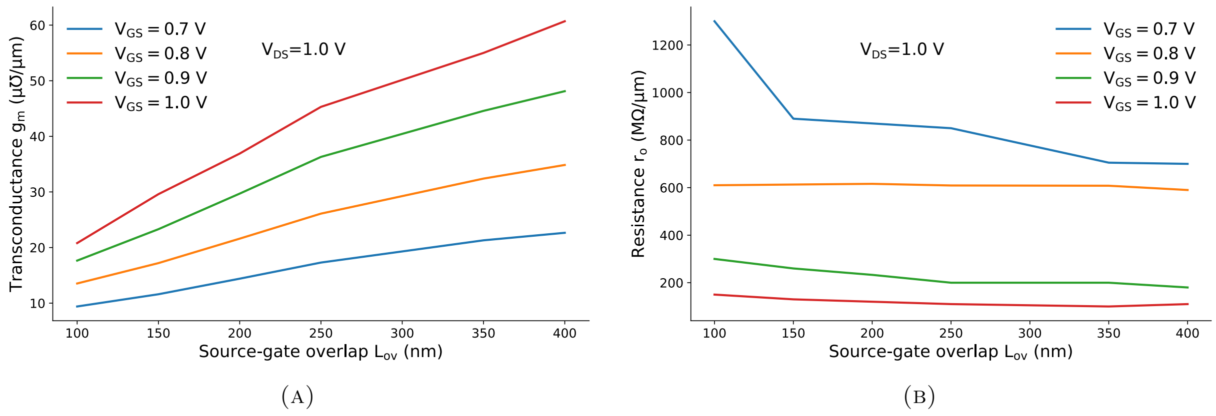
C_{GS} is the sum of gate-source overlap capacitance $C_{GSov} \propto WL_{ov}C_{ox}$, source-side depletion capacitance C_{GSdep}, and outer fringing capacitance C_{of} is given by

$$C_{of} = \frac{2\varepsilon_{ox}\varepsilon_0}{\pi} \ln\left(1 + \frac{t_{gate}}{t_{ox}}\right) \tag{4.11}$$



(A) (B)

FIGURE 4.8: (a) Variation of tunneling width W_{tun} with V_{DS} for different V_{GS} values. (b) I_D variation with L_{ov} for different V_{GS} values at V_{DS}=1 V.



(A) (B)

FIGURE 4.9: Variation in (a) transconductance g_m and (b) output resistance r_o with L_{ov} for different V_{GS} values at V_{DS}=1 V.

where t_{gate} is the gate thickness, ε_{ox} is the permittivity of HfO_2. $C_{GS,dep}$ is formed between the source and epi-layer due to the large electric field between them. $C_{GS,dep} \equiv \partial Q_{Sdep}/\partial V_G$, where $Q_{Sdep}=qN_{src}L_{ov}t_{si}$, N_{src} is the doping in the source region. C_{GS} increases with V_{GS} due to the increase in the depletion width under the source-gate overlap region [109, 110, 111]. C_{GS} increases with increasing L_{ov}, due to the increase in depletion width between the n^+ epi-layer and p^+ source regions, but L_{ov} does not affect C_{GD}, as shown in Fig. 4.11a.

C_{GD} is the sum of inversion capacitance C_{GDinv}, outer fringing capacitance C_{of} (4.11), and drain overlap capacitance $C_{GDov} \propto W L_{ov} C_{ox}$. C_{GD} increases with V_{GS} as shown in Fig. 4.12a, due to the formation of the inversion layer on the drain side, extending toward the source side [112]. The influence of L_{dov} on C_{GG} and C_{GD} are shown in Fig. 4.12. C_{GD} is decreased from 7 fF to 0.59 fF as L_{dov} decreases from 40 nm to 0 due to the decrease in the electric field on the

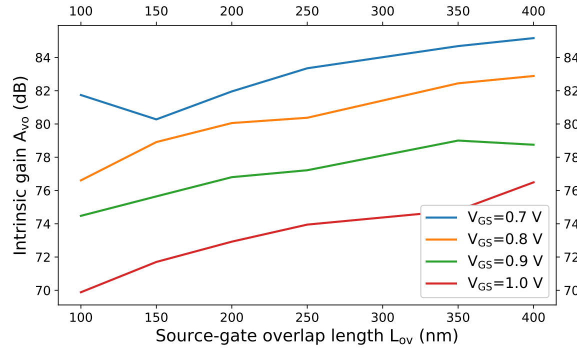
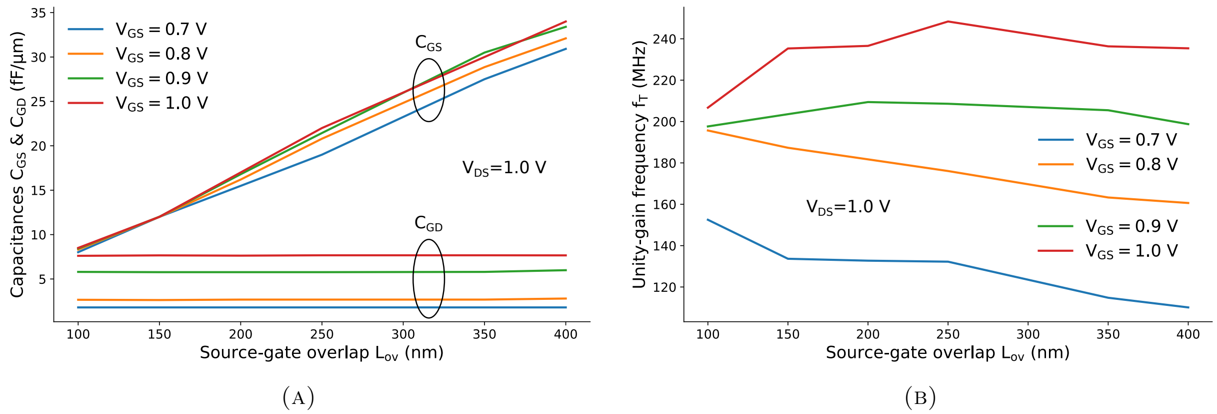


FIGURE 4.10: Intrinsic Gain with L_{ov} for different V_{GS} values at V_{DS}=1 V.



(A) (B)

FIGURE 4.11: Variation of (a) Gate Capacitance (b) f_T with L_{ov} for different V_{GS} values at V_{DS}=1 V.

drain side. With the reduction in C_{GD}, net gate capacitance C_{GG} is reduced from 10 fF to 3 fF but C_{GS} is n't get affected by L_{ov} variation on the drain side [109].

As evident in Fig. 4.11b, the change in unity-gain BW

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{4.12}$$

is dominated by the relative change in C_{GG}=C_{GS}+C_{GD} or g_m, as both g_m and C_{GG} are proportional to L_{ov}. Table 4.2 summarises the influence of L_{ov} on the analog performance parameters in VLTFETs and compares them with those of MOSFETs with gate length L_G. Epi-layer thickness t_{ep} and doping n_{ep} play significant roles in analog performance parameters like g_m & r_o. As expected, decreasing t_{ep} reduces the tunneling barrier width between the source's valence band and the epi-layer's conduction band , improving g_m. Tunneling width between the source and epi-layer remains practically independent of the drain potential, maintaining almost a constant r_o with changing t_{ep}. As the doping of the epi-layer n_{ep} increases, g_m increases due

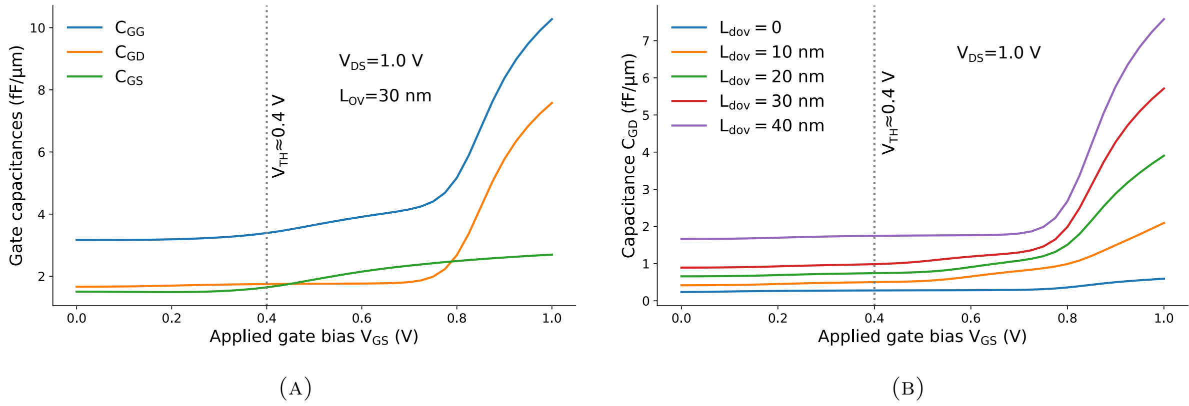


FIGURE 4.12: Variation of (a) gate capacitances with V_{GS} at V_{DS}=1 V and (b) C_{GD} with V_{GS} for different L_{dov} values at V_{DS}=1 V.

TABLE 4.2: Summary of the dependence of MOSFET and VLTFET analog performance on device parameters.

Parameters	MOSFET	VLTFET
Drain current I_D	W/L_G	$W \times L_{ov}$
Transconductance g_m	W/L_G	$W \times L_{ov}$
Output resistance r_o	L_G^2/W	$1/W$
Gain A_{vo}	L_G	L_{ov}
Unity gain frequency f_T	$1/L_G^2$	constant

to a rise in the junction electric field between the source and epi-layer, resulting in higher BtB generation. Unfortunately, this decreases V_t, and as a consequence, the onset of saturation in I_D gets delayed, reducing the r_o [53].

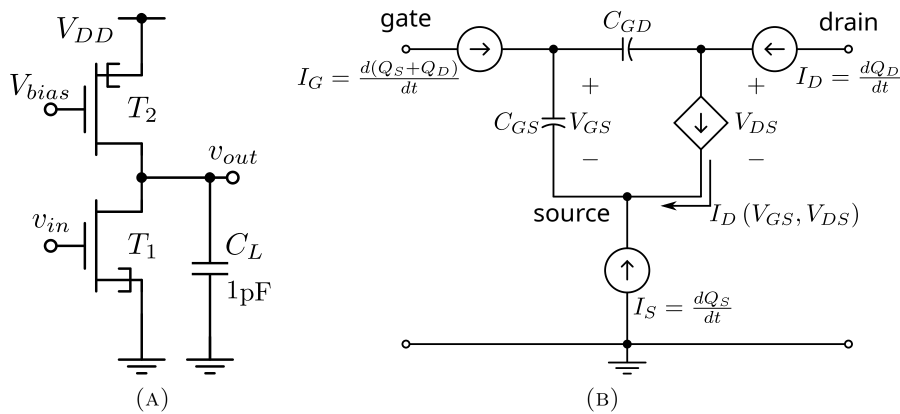
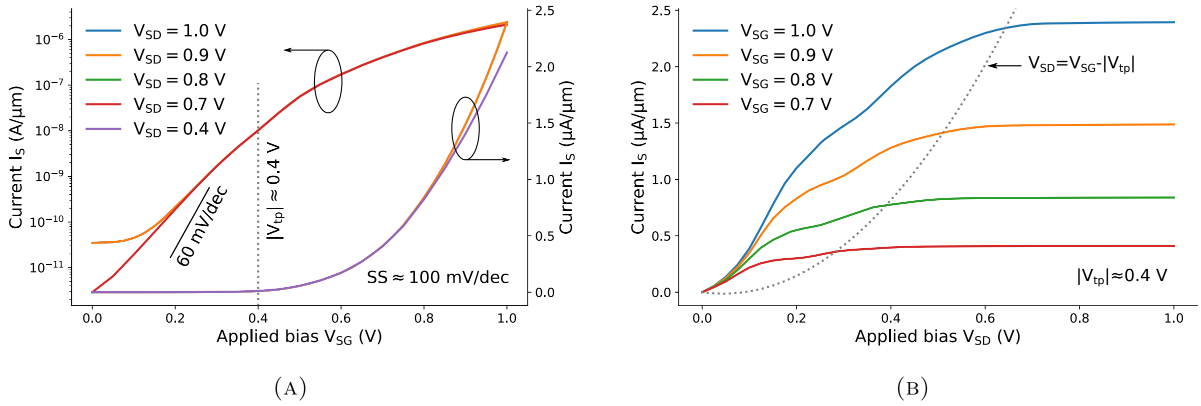


FIGURE 4.13: (a) Schematic and (b) equivalent circuit of the CS amplifier in cascode configurations. The dc biases V_{DD}=1 V, V_{bias}=V_{DD}/2.



(A) (B)

FIGURE 4.14: (a) I_S-V_{SG} characteristics of pVLTFET for different V_{SD} and (b) I_S-V_{SD} characteristics of pVLTFET for different V_{SG}.

4.4 Impact of Gate-Overlap L_{ov} on Analog Circuits

The impact of L_{ov} is studied on the cascode CS amplifier shown in Fig. 4.13. Here, p-channel VLTFET (pVLTFET) is used as a current source load with its gate terminal connected to V_{bias}. The pVLTFET has the opposite and equal doping concentrations with similar dimensions as nVLTFET, except for the materials, as summarised in Table 4.1, and characteristics as shown in Fig. 4.14. First, we design a CS amplifier with L_{ov}=30 nm for nVLTFET & pVLTFET. The DC output voltage (operating voltage) of the CS amplifier is adjusted to be $V_{DD}/2$ for all the analyses. Voltage gain A_v and unity-gain BW f_T of the CS amplifier are measured as 45 dB and 34 MHz, respectively, under no-load conditions. Next, L_{ov} of VLTFET is increased to 100 nm without changing the other parameters. This provides A_v=52 dB and f_T=81 MHz, since g_m increases three times which is observed in Fig 4.15. Like CMOS circuits, the gain of the CS amplifier can also be increased by increasing the width W, increase g_m, and decreasing r_o. In addition to W, in VLTFETs, we can increase the gain with the L_{ov} parameter. The percentage increase in the gain of VLTFET CS amplifier increasing L_{ov} will be very high since increasing L_{ov} increases g_m, without affecting r_o.

Along with the CS amplifier, we designed the cascode current mirror circuit at a reference current I_{ref}=1 μA. In conventional CMOS designs, the channel length modulation effect is more at the lower technology nodes, lowering the R_{out}. In VLTFETs, the source-gate overlap primarily determines I_D, so the channel length modulation effect is negligible. Fig.4.16a shows the I_{out} independent of V_{out}. As a result, R_{out} exceeds several MΩ as shown in Fig. 4.16b and reaches a maximum of 10^{11} Ω, leading to the ideal current mirror/source operation. Furthermore,

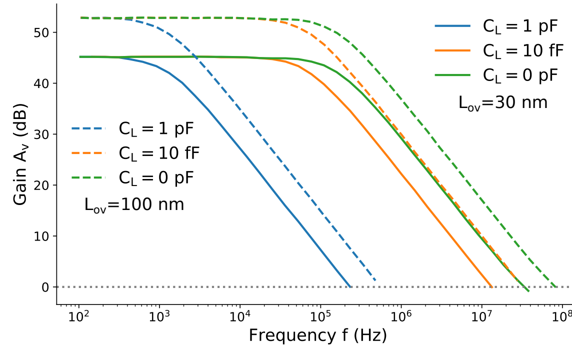


FIGURE 4.15: AC analyses of the CS amplifier with cascode configuration under C_L=no load, 10 fF, 1 pF.

increasing the L_{ov} from 30 nm to 100 nm increases the R_{out} by one order of magnitude under the same V_{out}.

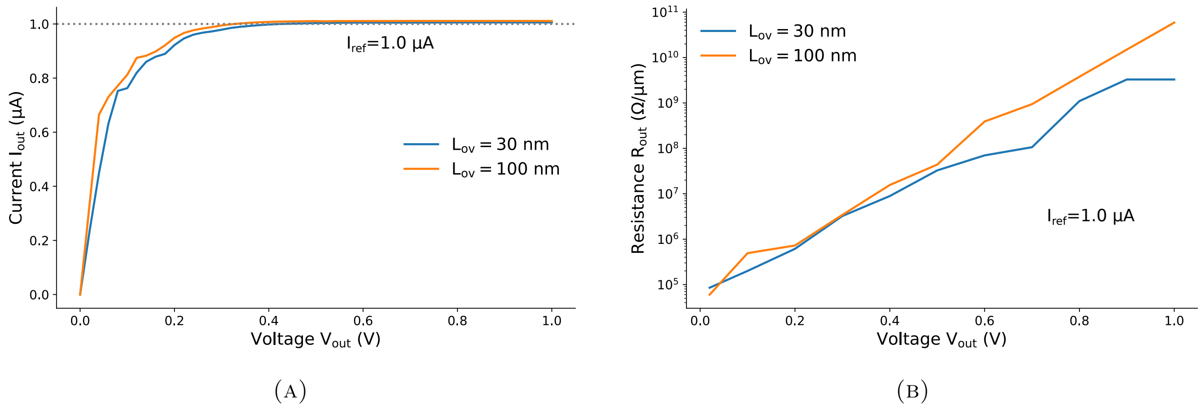


FIGURE 4.16: Variation of (a) I_{out} and (b) R_{out} with increasing V_{out} of cascode current mirror with L_{ov}=30 nm, under a reference current I_{ref}=1 μA.

4.5 Conclusions

In this chapter, we have optimized the VLTFET structure for superior analog performance and analyzed the impact of source-gate overlap length L_{ov} on analog circuit design parameters g_m, r_o, C_{GG}, and f_T. These devices show excellent saturation characteristics due to the independence of drain potential on drain current, resulting in an extremely high r_o. With an L_{ov} of 100 nm, the gain of the cascode CS amplifier is 52 dB with a unity-gain BW of 81 MHz. With an L_{ov} of 30 nm, the cascode current mirror provides a very high R_{out} exceeding 100 MΩ. In essence, L_{ov} is a vital parameter in addition to the width for circuit designers for an effective increase in amplifier performance using VLTFET devices.

4.6 Publications Based on This Chapter

Journals

1. **Simhadri Hariprasad***, Surya Shankar Dan “Superior Analog Performance due to Source-Gate Overlap in Vertical Line-Tunneling FETs and Their Circuits” , Silicon (2022): 1-10 DOI: 10.1007/s12633-022-01954-7

Chapter 5

Novel GOTFET Devices for Digital and Ternary Logic Applications

5.1 Introduction

In this chapter, two different types of Gate-Overlap Tunnel FET (GOTFET) devices are proposed for ultra-low power applications: GOTFETs for (i) digital logic and (ii) Ternary logic applications. These GOTFET structures have been optimized to have their characteristics far superior to equally sized 45 nm MOSFETs. GOTFET characteristics were simulated using industry-standard synopsys® TCAD tools [51] while the benchmarking with an equivalent CMOS technology was carried out using the standard 45 nm CMOS library in the industry-standard cadence® EDA tool [92]. Proposed GOTFETs have on-state currents I_{on} at least twice ($I_{on,GOT} \geq 2I_{on,MOS}$) with off-state currents I_{off} remaining at least an order of magnitude lower ($I_{off,GOT} \leq 0.1 I_{off,MOS}$), than the corresponding equally-sized MOSFETs at the same 45 nm technology node. The proposed GOTFET designs are targeted for higher I_{on} leading to high-speed operation and lower I_{off} to minimize static leakage in ultra-low-power digital applications.

Ambipolar current at high negative gate biases makes the TFET less effective in complementary digital circuit applications. TFET structures reported earlier in the literature [113, 114, 115, 116, 117] try to suppress the ambipolar current I_{amb}; however, most of them are incapable of completely eliminating I_{amb}. All the above techniques reported in the literature to suppress ambipolar behavior in TFETs, result in a considerable reduction in the I_{on}, thereby deteriorating the RF performance. Hence, this chapter investigates a method to suppress the ambipolar current

I_{amb} effectively, enhance the device performance with higher on-current I_{on}, lower off-current I_{off}, lower inverse subthreshold slope SS, and simultaneously improve RF performance. Starting with a conventional double-gate TFET structure, the device optimization reported in this work has led to the gradual improvement in device performance in terms of higher I_{on}, lower I_{off}, higher I_{on}/I_{off} ratio, and lower SS. The RF parameters of the optimized GOTFET, such as the mutual transconductance g_m, gate-to-drain C_{GD}, and gate-to-source C_{GS} capacitances and unity-gain cut-off frequency f_T are analyzed. We have optimized the GOTFET device using the industry-standard synopsys® TCAD tools by studying the impact of various device parameters and dimensions on performance. We demonstrated that at high negative voltages, the proposed nGOTFET would completely suppress the ambipolar behavior of the device without deteriorating the device performance. We have proposed a GOTFET which completely suppresses the ambipolar current at high negative biases without compromising the high I_{on} (1.04 mA/μm) and low I_{off} (0.27 pA/μm) and low SS (32 mV/dec)

Ternary logic has gained considerable popularity in recent years as they yield new functionalities in VLSI applications, which cannot be achieved (or is difficult to achieve) through conventional CMOS-based binary logic. Ternary logic offers several significant advantages, such as reduced interconnects, smaller chip areas, and higher operating speeds over binary logic in the design of digital systems, as reported earlier [118, 119, 120]. The primary requirement of ternary logic is that the devices used to implement them must have two different threshold voltages [121, 122, 123]. For the first time in this work, innovative low and high-threshold GOTFET devices have been reported for ternary logic applications. Based on an iterative algorithm, the DG GOTFET structures have been optimized such that the GOTFET characteristics are better than the MOSFETs with the same width at the standard 45 nm technology node. These devices are designed in such a way that the low and high threshold voltages (LVT & HVT) are $V_{DD}/3$ and $2V_{DD}/3$ respectively, with the ranges $\{0$ to $V_{DD}/3\}$, $\{V_{DD}/3$ to $2V_{DD}/3\}$ & $\{2V_{DD}/3$ to $V_{DD}\}$ representing the three logic states 0, 1 & 2 respectively. Proposed LVT & HVT TFETs have ON currents (I_{on}) roughly twice and OFF currents (I_{off}) at least an order of magnitude lower than the corresponding MOSFETs. This chapter also presents dual-threshold GOTFETs exhibiting both LVT & HVT characteristics by simply altering their terminal connections in the same device instead of the dedicated devices. The threshold voltage (V_T) usually varies with respect to geometry, the channel length, doping concentration, gate material, and the drain bias [74, 124]. In the proposed GOTFETs, gate material type and doping concentration greatly influence on V_t. Considering the influence of various gate material work functions, the device structures

have been optimized to fix the lower & higher V_T at $V_{DD}/3$ and $2V_{DD}/3$, respectively.

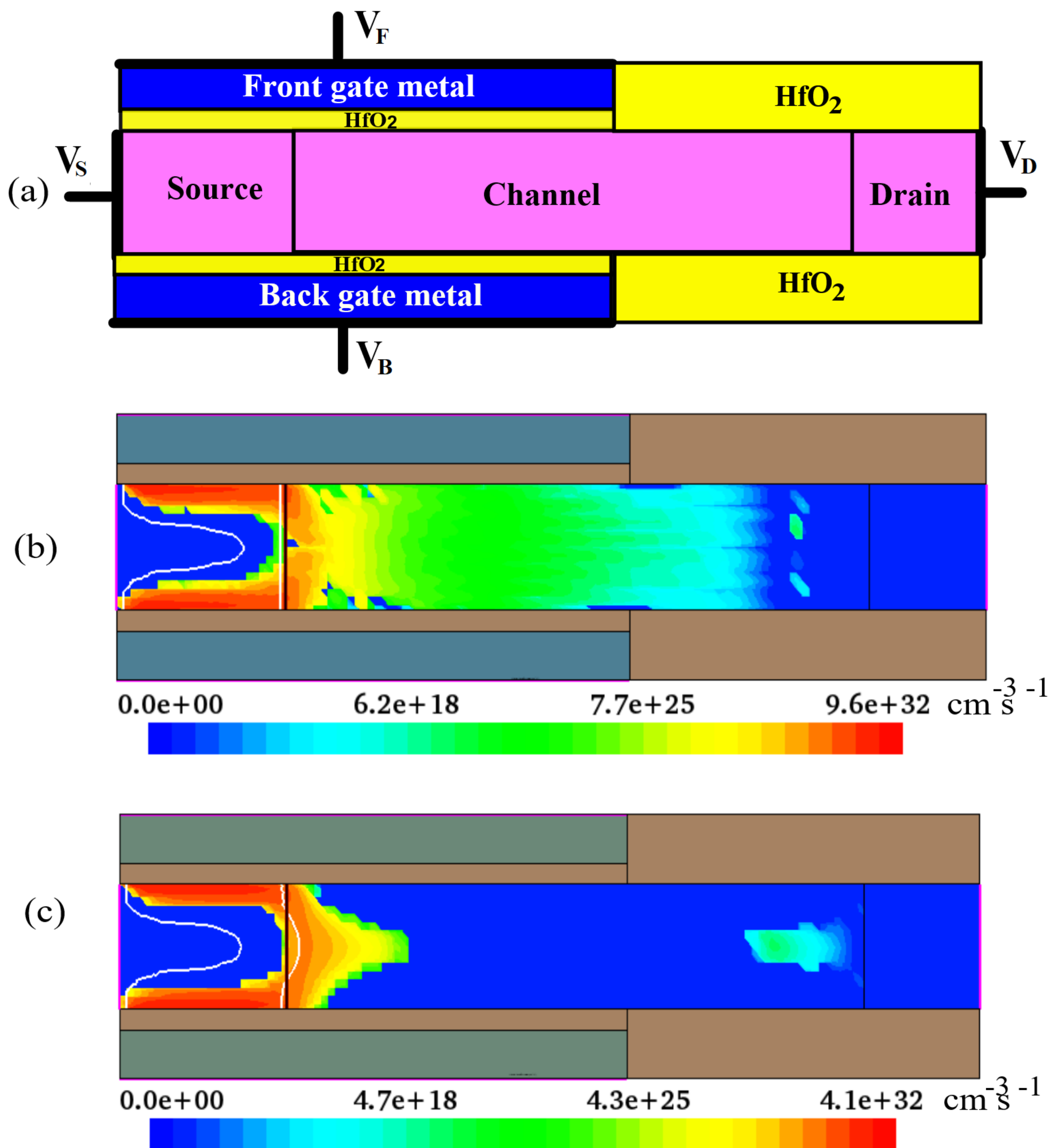


FIGURE 5.1: (a) Schematic of the proposed GOTFET device. (b) Electron & (c) Hole BtB generation in nGOTFET & pGOTFET respectively.

5.2 Proposed GOTFET Devices for Digital Applications

5.2.1 Structure of the Proposed GOTFET

Fig 5.1 shows the schematic and BtB generation of the n & p GOTFET structure. Device optimization can be done by changing the channel thickness, gate overlap length, source length, oxide thickness, metal work function, and the doping concentration of source, channel, and drain regions. The proposed GOTFET structure can be designed in a 45nm technology node using a TCAD simulator. The electrical characteristics of the proposed devices, all with an effective channel length of 45 nm and a thickness of 12 nm, were simulated using the industry-standard synopsys® TCAD tool [51]. The gate metal thickness is 2.5 nm, and the oxide thickness is 1.5 nm.

TABLE 5.1: Parameters of the nGOTFET & pGOTFET devices

	nGOTFET		pGOTFET	
Region	Material	Doping /cm^3	Material	Doping /cm^3
Source	$Si_{.1}Ge_{.9}$	10^{20} p$^+$	$Si_{.2}Ge_{.8}$	10^{20} n$^+$
Channel	Undoped Si	—	$Si_{.2}Ge_{.8}$	5×10^{17} p
Drain	Si	10^{20} n$^+$	$Si_{.2}Ge_{.8}$	5×10^{17} p
Gate	Al	—	Mo	—

To validate this work, model and simulation parameters were extracted from data reported in [125], where authors calibrated the simulation deck with the experimental characterization of fabricated TFET, which is similar to the GOTFET structure. All the simulations reported in this work were carried out using extracted parameters from calibrated data, showing appreciable agreement between experimental and simulation results. Device simulations have been carried out using the dynamic non-local path BtB generation model along with the standard doping-dependent mobility models, high field saturation models, filed-enhanced Schenk TAT model, SRH, and Auger recombination models. Device simulations and analyses were carried out at bias 1 V per the 45 nm technology node limit. Device parameters used for nGOTFET & pGOTFET optimization are listed in Table 5.1. Materials with appropriate work functions used as the gate contacts enhance I_{on}, and V_T can be adjusted accordingly. It has been observed that among all the possible gate materials, Aluminum (Al) & Molybdenum (Mo) provide excellent DC characteristics for nGOTFET & pGOTFET devices, respectively.

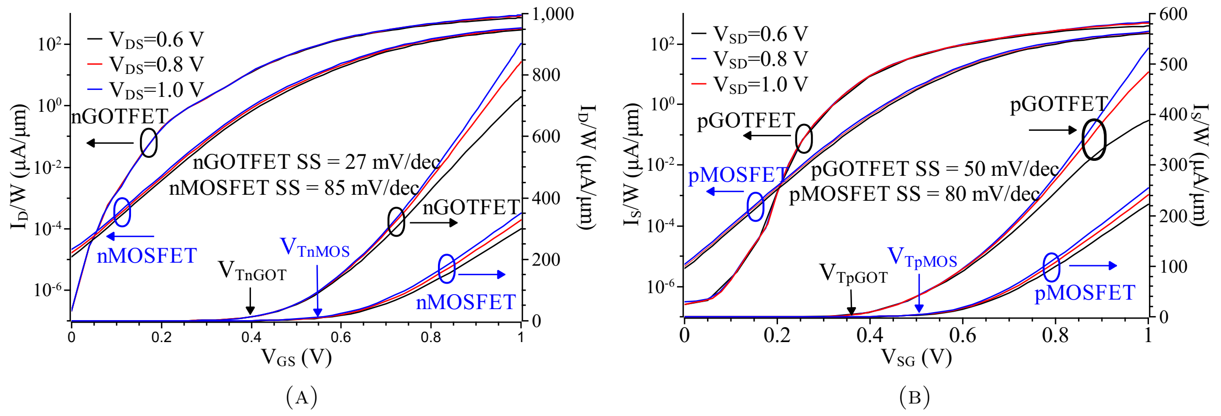


FIGURE 5.2: (a) I_D-V_{GS} characteristics of nGOTFET & nMOSFET for different values of V_{DS}. (b) I_S-V_{SG} characteristics of pGOTFET & pMOSFET for different values of V_{SD}.

I_D-V_{GS} characteristics of nGOTFET obtained using a non-local BtB generation model with increasing V_{DS} are shown in Fig. 5.2a with I_{on}=903 μA/μm at V_{DS}=1 V, which is more than double that of the MOSFET at 45 nm technology node. Leakage current I_{off}=0.3 pA/μm at V_{DS}=1 V is at least one order of magnitude lower than the corresponding equally-sized MOSFET in the same technology node. It has been observed that the I_{on} of GOTFET is nearly independent of the channel and drain doping while it increases with an increase in the source doping. V_{Tn} extracted using the third derivative method [74], where $\partial^3 I_D/\partial V_{GS}^3$ for V_{DS}=1 V has its first peak at V_{GS}=0.4 V, denoting V_{Tn}≈0.4 V for the optimized nGOTFET. Similarly, Fig 5.2b shows pGOTFET I_S-V_{SG} characteristics at V_{SG} = V_{SD} =1 V. The on-current I_{on}=559 μA/μm at V_{SD}=1 V exceeds twice that of an equally-sized MOSFET at the same 45 nm technology node. The leakage current I_{off}=0.1 pA/μm at V_{SD}=1 V is at least one order of magnitude lower than the equally sized MOSFET. $|V_{Tp}|$≈0.36 V obtained from optimized pGOTFET, which is much lower than the equivalent pMOSFET.

5.3 Suppression of Ambipolar Behavior of GOTFET without Compromising I_{on}, I_{off} , and SS

To suppress the ambipolar current at a high gate negative biases, GOTFET is further modified as shown in the schematic Fig. 5.3. In a conventional TFET (without gate-overlap on the source and drain regions), gate biases, and a few other factors influence the BtB generation either at the source-channel interface or drain-channel interface. A high $+V_{GS}$ bias increases the BtB generation at the p$^+$ source-channel junction leading to a considerable drain current

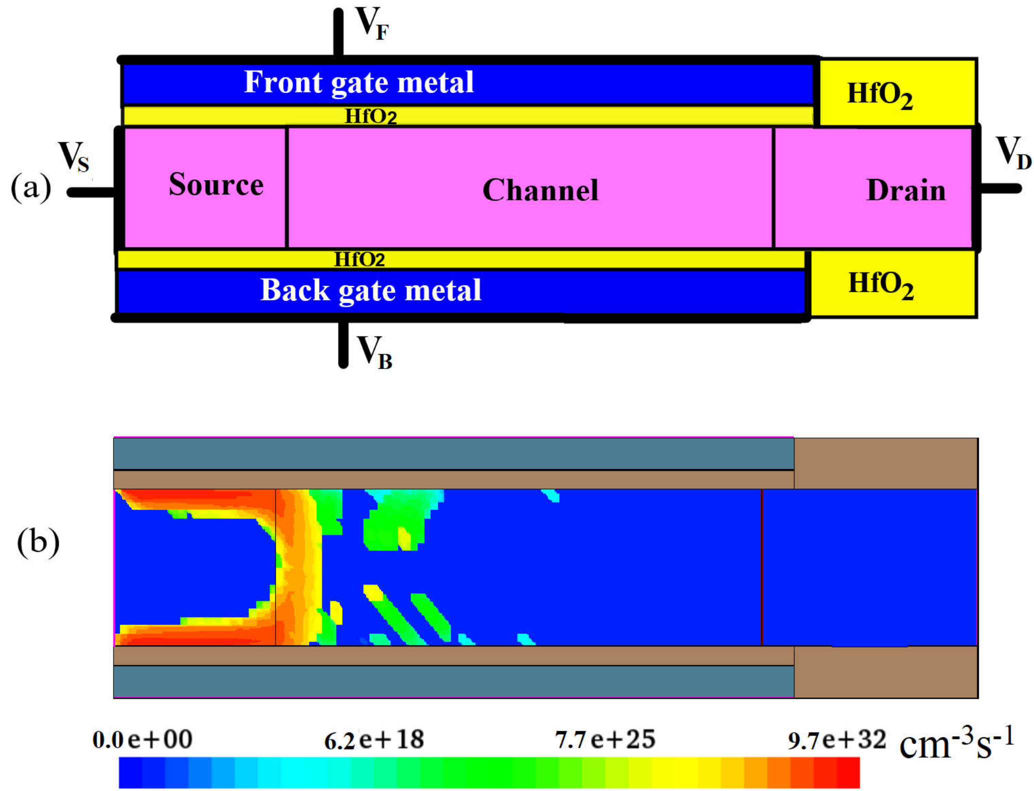
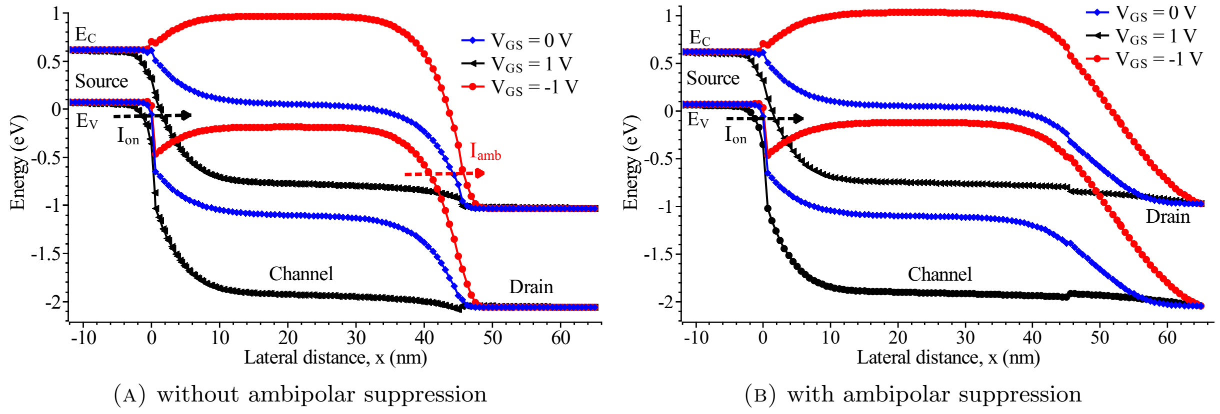


FIGURE 5.3: (a) Schematic of the proposed nGOTFET and (b) its corresponding electron BtB generation..

I_D. Similarly, a high $-V_{GS}$ bias increases the BtB generation at the n$^+$ drain-channel junction leading to the ambipolar current I_{amb}. Such ambipolar behavior of conventional TFETs due to high $-V_{GS}$ makes them generally unsuitable for digital logic design, especially in ultra-low-power applications. To prevent the ambipolar conduction in TFETs, the tunneling width at the n$^+$ drain-channel junction should not be too narrow, as shown in Fig. 5.4b. Higher I_{on} and negligible I_{amb} can be achieved simultaneously if the gate-stack completely overlaps the source and partially overlaps the drain with a drain doping of N_D=10^{19} /cm^3 and a source doping of N_S=10^{20} /cm^3.

As shown in Fig. 5.4a, the GOTFET with gate-overlap only on the source side and drain doping N_D=10^{20} /cm^3 for V_{GS}=1 V, the tunneling barrier width at p$^+$ source-channel interface becomes extremely narrow resulting in a desirable very high I_{on}. However, for V_{GS}=$-$1 V, the tunneling width at n$^+$ drain-channel interface also becomes narrow, resulting in an undesirable I_{amb}, which is detrimental in ultra-low power applications. To suppress I_{amb} due to narrow tunneling width



(A) without ambipolar suppression

(B) with ambipolar suppression

FIGURE 5.4: Energy band diagram of the proposed nGOTFET (a) without gate overlap on the drain side with N_D=N_S=10^{20} /cm^3 and (b) with gate overlap on the drain side with N_D=10^{19} /cm^3 & N_S=10^{20} /cm^3 for V_{GS}=0 V, V_{GS}=1 V, V_{GS}=-1 V and V_{DS}=1 V.

at the drain-channel junction, the gate-overlap on the drain region with a drain doping N_D=10^{19} /cm^3 prevents the narrowing of the tunneling width at the drain-channel interface for high negative gate biases as shown in Fig. 5.4b.

I_D-V_{GS} characteristics of the GOTFET obtained using non-local BtB generation model for different values of V_{DS} are shown in Figs. 5.5a & 5.5b corresponding to without and with gate-drain overlap, respectively. In addition to the lower drain doping compared to the source, gate-overlap of length L_{dov} on the drain determines the drain-channel interface tunneling width. L_{dov}=3 nm and N_D=10^{19} /cm^3 completely suppress the ambipolar component I_{amb} at high $-V_{GS}$ as shown in Fig. 5.5b. In the proposed GOTFET, I_{amb} at V_{GS}=-1 V is six orders of magnitude lower than the I_{amb} of the GOTFET with L_{dov}=0 nm and typical N_D=N_S=10^{20} /cm^3, without reducing the on current (I_{on}=1.046 mA/μm at V_{GS}=V_{DS}=1 V), while restricting the leakage current at I_{off}=0.27 pA/μm at V_{GS}=0 V & V_{DS}=1 V, evident in Fig. 5.5b. SS of the proposed GOTFET is 32 mV/dec, which is much lower than most of the TFETs reported previously in the literature. As seen in Fig. 5.5c, the threshold voltage V_T of the proposed GOTFET extracted using the 3$^{\text{rd}}$ derivative method [74] is 0.38 V. Fig 5.6 shows the impact of drain doping and overlap length for the suppression of ambipolar currents in the GOTFETs. Fig. 5.6a shows an abrupt decrease in ambipolar conduction with the reduction in N_D. The proposed approach effectively suppresses the ambipolar conduction to I_{amb}=74 fA/μm for a drain doping of N_D=10^{19} /cm^3, yielding an on current I_{on}=1.046 mA/μm at V_{DS}=1 V. Fig. 5.6b shows that the gate-drain overlapping effectively suppresses the ambipolar conduction in the GOTFET without compromising I_{on}, I_{off}, and SS.

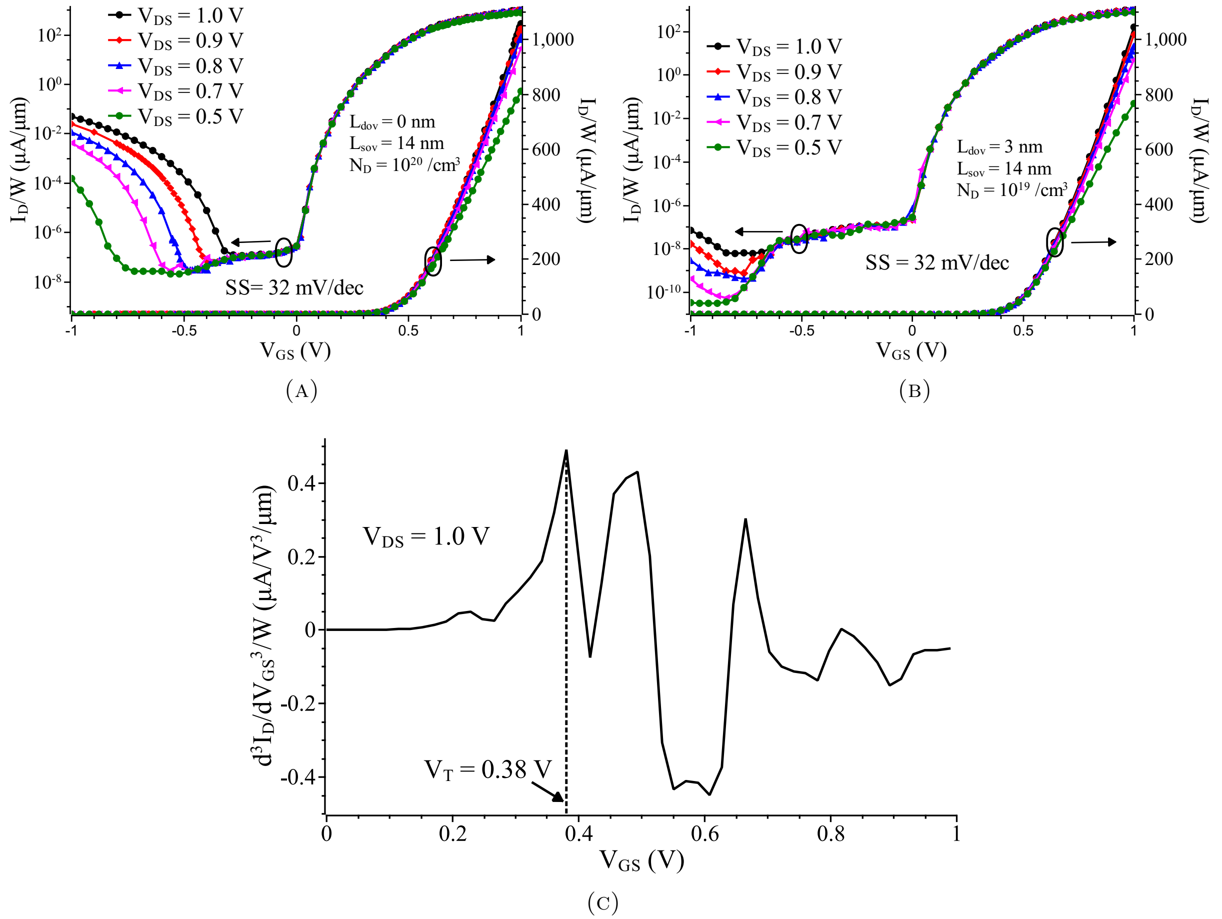


FIGURE 5.5: (a) I_D-V_{GS} characteristics of proposed nGOTFET for different values of V_{DS} with N_D=N_S=10^{20} /cm^3, without gate-drain overlap (b) I_D-V_{GS} characteristics of proposed nGOTFET for different values of V_{DS} with N_D=10^{19} /cm^3 & N_S=10^{20} /cm^3, with gate-drain overlap. (c) Threshold voltage V_T extracted from the characteristics of proposed nGOTFET using the 3rd derivative method [74].

5.4 Proposed LVT & HVT GOTFET Devices for Ternary logic Applications

5.4.1 Proposed LVT & HVT GOTFETs Structure and Parameter Optimization

LVT & HVT GOTFETs structures have been obtained for ternary logic applications by adjusting gate material and doping concentration of the semiconductor material. The length and thickness of the source, channel, and drain regions are similar to as explained in the previous section. Table 5.2 shows LVT & HVT nGOTFETs device materials properties. Fig 5.7 shows transfer characteristics of LVT and HVT nGOTFET acquired using BtB generation in TCAD with increasing V_{DS}. Lower V_{tnl} and higher V_{tnh} threshold voltages were obtained using the third-order

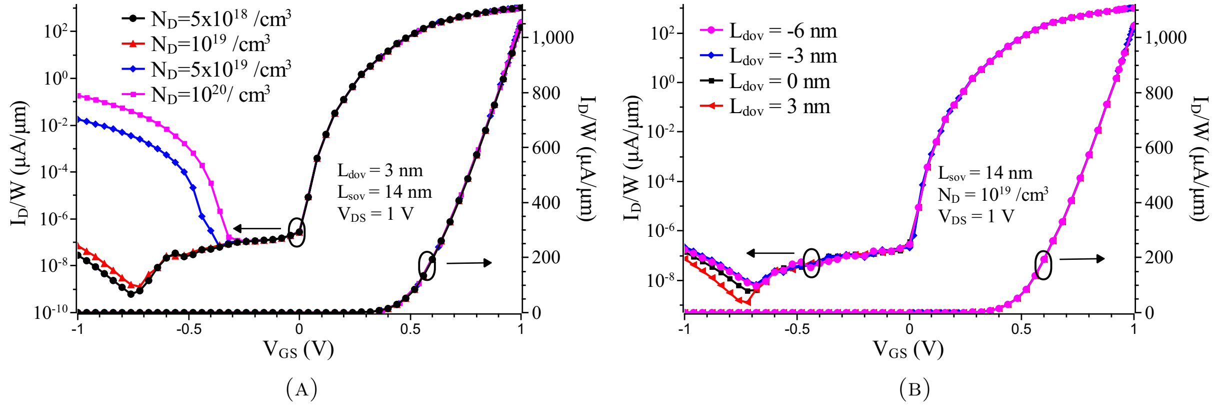


FIGURE 5.6: (a) I_D-V_{GS} characteristics of the proposed nGOTFET showing the influence of drain doping N_D on the ambipolar conduction (b) I_D-V_{GS} characteristics of the proposed nGOTFET showing the influence of gate-drain overlap L_{dov} on ambipolar conduction

TABLE 5.2: Parameters of the Optimized LVT & HVT nGOTFET

	LVT nGOTFET		*HVT nGOTFET*	
Region	*Material*	*Doping* (/cm^3)	*Material*	*Doping* (/cm^3)
Source	$Si_{0.1}Ge_{0.9}$	10^{20} P^+	$Si_{0.15}Ge_{0.85}$	10^{20} P^+
Channel	undoped Si	–	undoped Si	-
Drain	Si	10^{20} N^+	Si	10^{18} N
Gate	Al	–	$TiSi_2$	–

method. It is observed that peak occurs a V_{GS}=0.33 V for LVT and V_{GS}=0.66 V for HVT structure which are considered as V_{tnl}, and V_{tnh}, respectively.

The I_{on} of the proposed LVT nGOTFET is approximately double that of the LVT nMOSFET, while I_{off} remains one order lower magnitude than the LVT nMOSFET as observed from I_D-V_{GS} characteristics as shown in Fig 5.7. Similarly, optimized HVT nGOTFET has I_{on} higher than HVT nMOSFET, while I_{off} remains at least an order magnitude lower than HVT

TABLE 5.3: Parameters of the Optimized LVT & HVT pGOTFET

	LVT pGOTFET		*HVT pGOTFET*	
Region	*Material*	*Doping* (/cm^3)	*Material*	*Doping* (/cm^3)
Source	$Si_{0.26}Ge_{0.74}$	9×10^{19} N	$Si_{0.25}Ge_{0.75}$	10^{20} N^+
Channel	$Si_{0.26}Ge_{0.74}$	5×10^{16} P	$Si_{0.25}Ge_{0.75}$	5×10^{17} P
Drain	$Si_{0.26}Ge_{0.74}$	5×10^{18} P	$Si_{0.25}Ge_{0.75}$	10^{17} P
Gate	TiN	–	$TiSi_2$	–

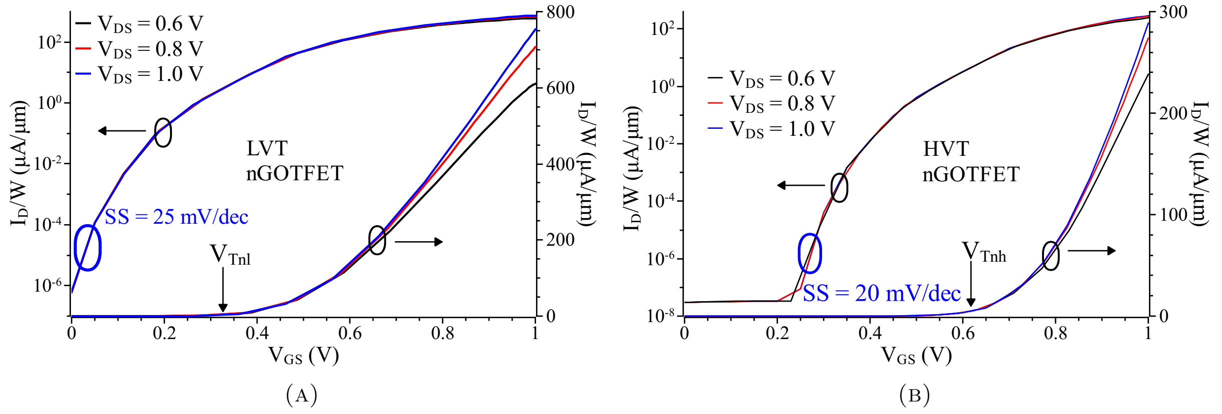


FIGURE 5.7: I_D-V_{GS} characteristics of (A) LVT (B) HVT nGOTFETs for different values of V_{DS}.

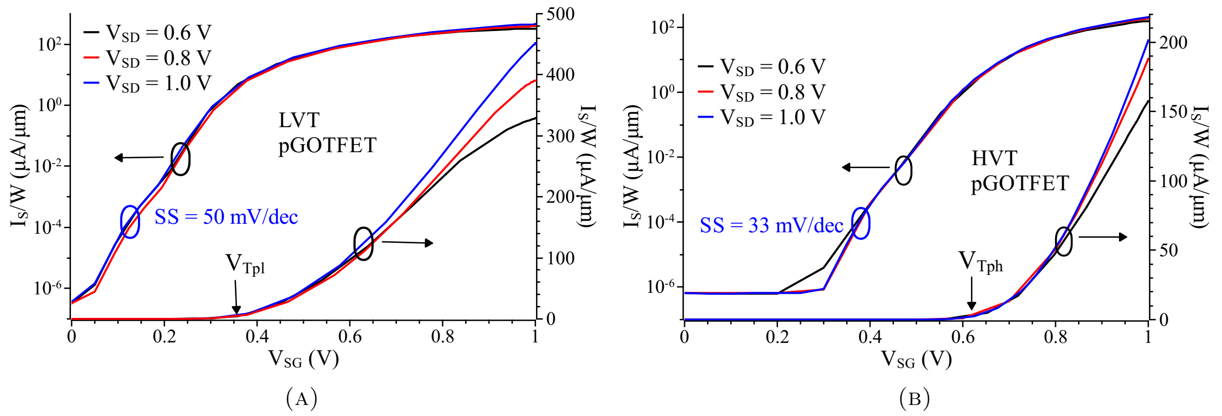


FIGURE 5.8: I_S-V_{SG} characteristics of (A) LVT (B) HVT pGOTFETs for different values of V_{SD}. V_{Tpl} & V_{Tph} denote the Low & High threshold voltages of the LVT & HVT pGOTFETs respectively

nMOSFET as the same technology node. Table 5.3 shows LVT & HVT pGOTFETs device materials properties. Fig 5.8 shows the I_S-V_{SG} characteristics of LVT & HVT pGOFET with corresponding pMOSFETs, for different values of V_{SD}. The I_{on} of the proposed LVT pGOTFET is approximately double that of the LVT pMOSFET, while I_{off} remains at least an order of magnitude lower than the LVT pMOSFET. As well, optimized HVT pGOTFET has I_{on} higher than pMOSFET, while I_{off} remains at least an order of magnitude lower than HVT pMOSFET at the same technology node.

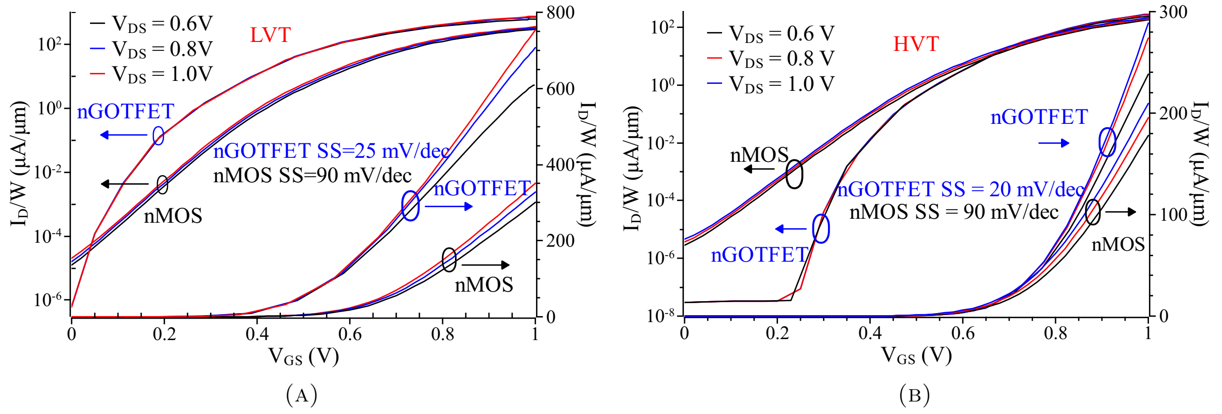


FIGURE 5.9: I_D-V_{GS} characteristics of (A) LVT (B) HVT nGOTFET & nMOSFET for different values of V_{DS}.

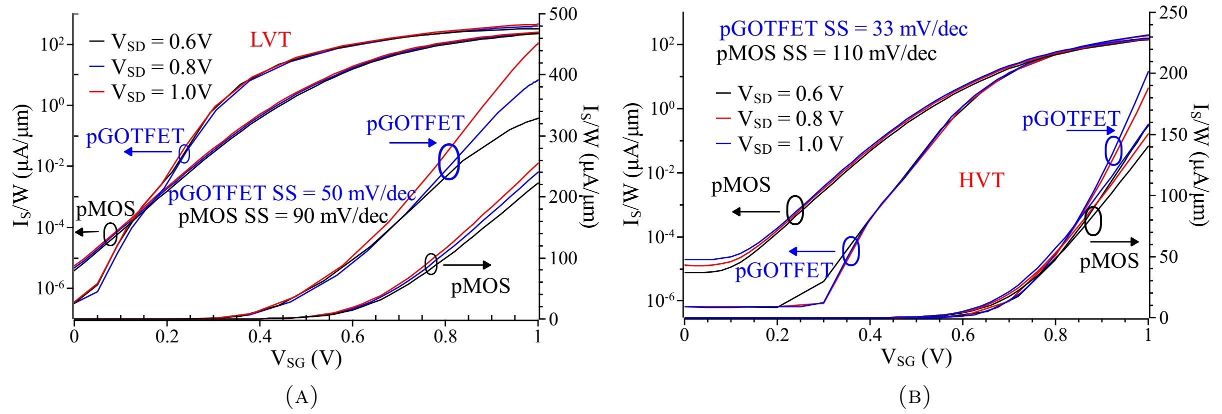


FIGURE 5.10: I_S-V_{SG} characteristics of (A) LVT (B) HVT pGOTFET & pMOSFET for different values of V_{SD}

5.5 NTI, PTI & STI Ternary Logic Cells

Negative Ternary Inverter (NTI), *Positive Ternary Inverter* (PTI), and *Standard Ternary Inverter* (STI) are the basic logic cells in ternary logic applications [121].

TABLE 5.4: Comparison of delay and static power consumption of GOTFET and CMOS based NTI cell.

Circuit parameter	Unit	*GOTFET*	*CMOS*
Power supply V_{DD}	V	1	1
Delay τ_{delay}	ns	**0.09**	0.11
Average static power P_{static}	pW	**0.174**	73.7
PDP ($\times10^{-23}$)	J	**1.57**	810.7
Decrease in PDP		**99.81%**	

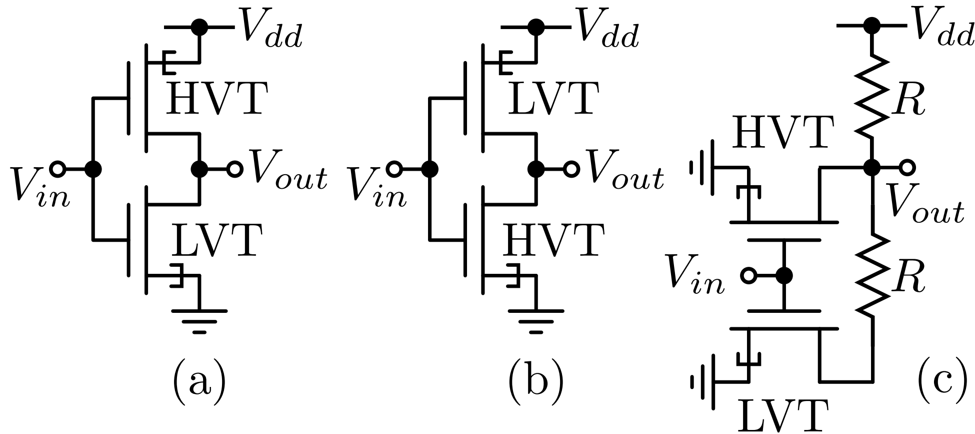


FIGURE 5.11: Schematics of the LVT & HVT CGOT (a) NTI, (b) PTI & (c) STI cells with 100 k$\Omega \leq R \leq$100 MΩ [121].

The following subsections benchmark the characteristics of *Complementary GOTFET (CGOT)* based NTI, PTI & STI cells with CMOS-based cells at 45 nm technology node. The schematics of the NTI, PTI & STI logic cells are shown in Fig. 5.11 for reference. We benchmarked the circuit performance of a CGOT NTI logic cell with a CMOS NTI circuit using the freely distributed 45 nm technology library. Figs. 5.12a, 5.12b & 5.12c show the simulation results of NTI logic cell using the industry-standard cadence EDA tool [92]. The average static power in CGOT NTI is 0.174 pW, which is significantly lower than the CMOS NTI, which consumes 73.7 pW, as highlighted in Table 5.4. The PDP of CGOT NTI is 1.57$\times$10^{-23} J, which is 0.19% of the PDP of standard 45 nm CMOS NTI cells (810.7$\times$10^{-23} J). The overall decrement in PDP owing to the proposed CGOT NTI logic cell is 99.81%. Similar to the NTI cells, Figs. 5.13a, 5.13b & 5.13c show the circuit simulation results, benchmarking the performance of a CGOT vs. CMOS PTI logic cell at the 45 nm technology node. The average static power consumed in CGOT PTI is 0.041 pW, which is significantly lower than the CMOS PTI, which consumes 22.60 pW, highlighted in Table 5.5. The PDP of the CGOT PTI is 0.31$\times$10^{-23} J, which is only 0.11% of the PDP of standard 45 nm CMOS PTI cells (293.8$\times$10^{-23} J). The overall decrement in PDP owing to the proposed CGOT PTI logic cell is 99.89%. The average delay in CGOT STI at the 45 nm technology node is 0.037 ns, which is significantly lower than the CMOS STI cell, which is 0.114 ns, shown in Fig. 5.14 and highlighted in Table 5.6. The PDP of CGOT STI is 9.7$\times$10^{-24} J, which is only 0.00014% of the PDP of standard 45 nm CMOS STI cells (7.15$\times$10^{-18} J). The overall decrement in PDP owing to the proposed CGOT STI logic cell is 99.9999%. It is worthy of note that all the measurements were done under no-load condition (C_L=0), as a consequence, the energy consumed per transition in terms of PDP (J) provides a much better estimate of the power dissipated/consumed rather than the dynamic power, which is dependent on the operating

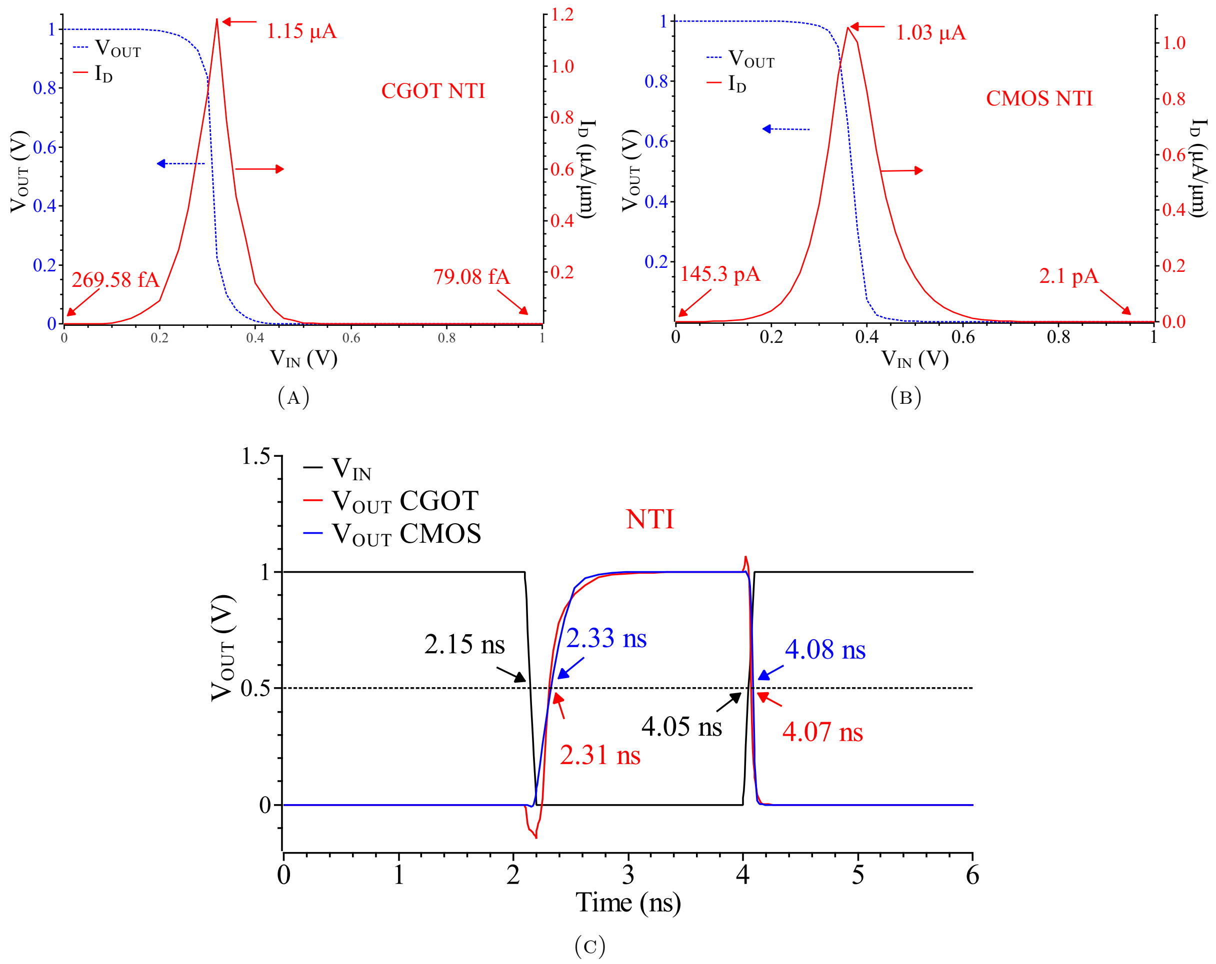


FIGURE 5.12: Static power consumption of (a) CGOT and (b) CMOS NTI cells. (c) Comparison of the delay characteristics of CGOT vs. CMOS NTI cell.

frequency as well as on the capacitive load.

TABLE 5.5: Comparison of delay and static power consumption of GOTFET and CMOS-based PTI cell.

Circuit parameter	Unit	*GOTFET*	*CMOS*
Power supply V_{DD}	V	1	1
Delay τ_{delay}	ns	**0.075**	0.13
Average static power P_{static}	pW	**0.041**	22.6
PDP ($\times 10^{-23}$)	J	**0.31**	293.8
Decrease in PDP		**99.89%**	

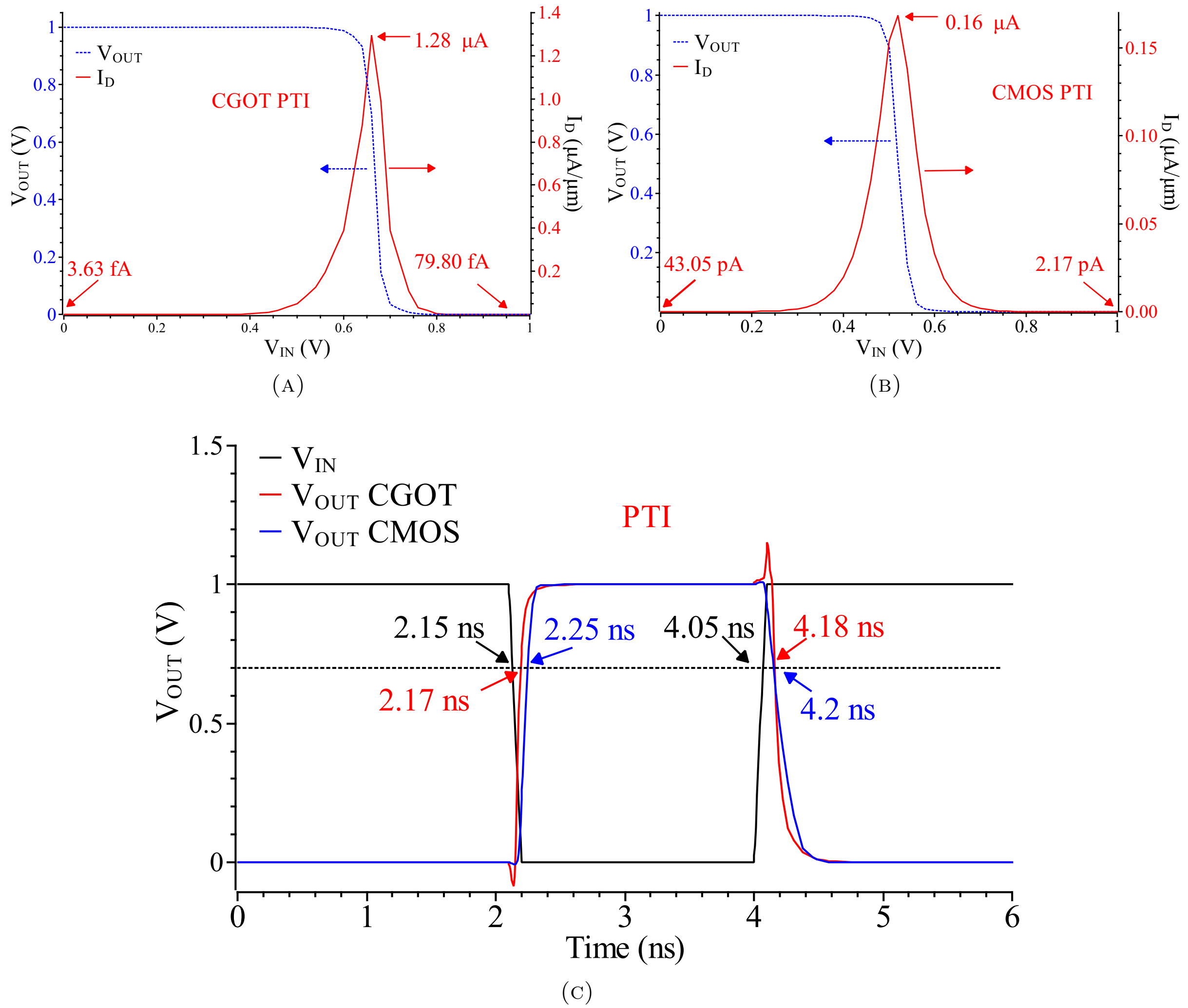


FIGURE 5.13: Static power consumption of (a) CGOT and (b) CMOS PTI cells. (c) Comparison of the delay characteristics of CGOT vs. CMOS PTI cell.

TABLE 5.6: Comparison of delay and static power consumption of GOTFET and CMOS based STI cell.

Circuit parameter	Unit	*GOTFET*	*CMOS*
Power supply V_{DD}	V	1	1
Average Delay τ_{delay}	ns	**0.037**	0.114
Average static power P_{static}	pW	**0.262**	62750
PDP ($\times 10^{-23}$)	J	**0.97**	715350
Decrease in PDP		**99.99%**	

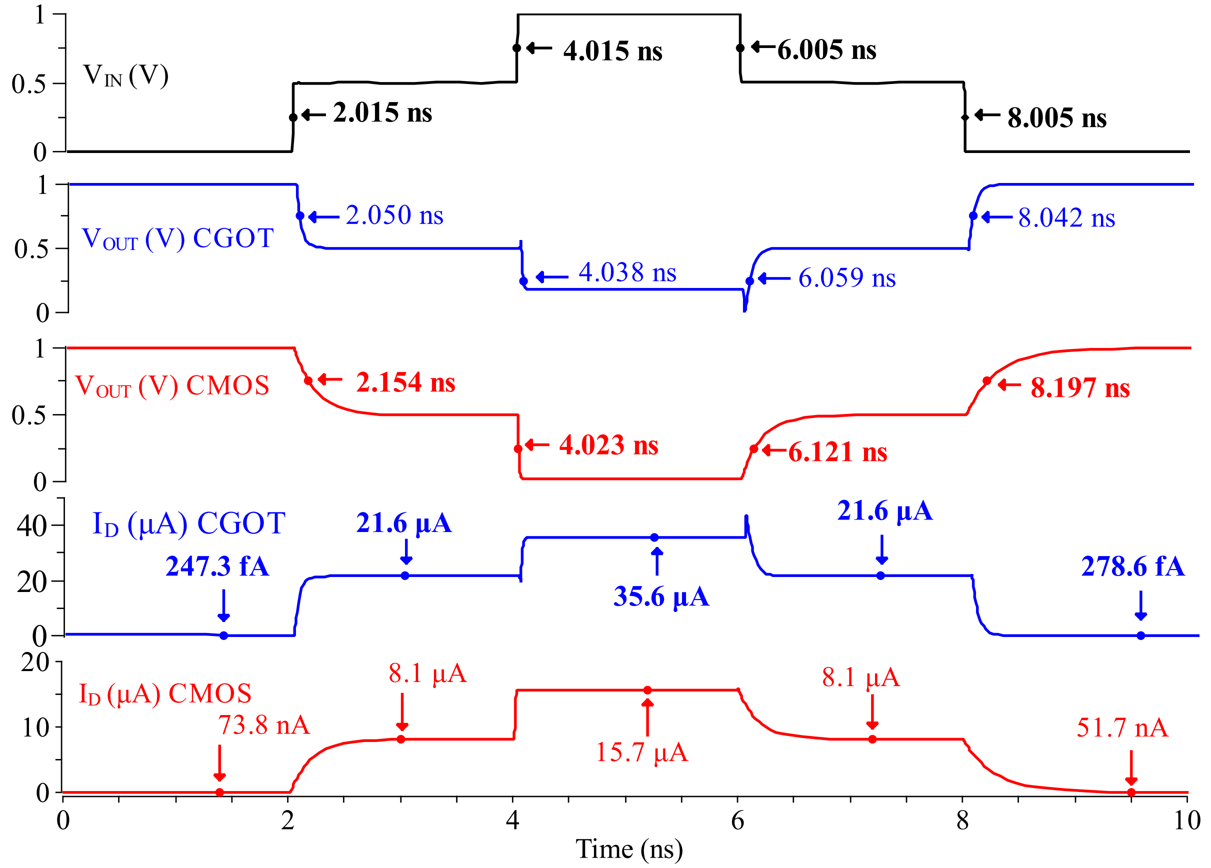


FIGURE 5.14: Comparison of the delay & power characteristics of CGOT vs. CMOS STI cells.

5.5.1 Proposed Dual-Threshold GOTFETs in the Same Device

In this section, dual-threshold GOTFETs have been designed, which give LVT & HVT characteristics in the same device by changing the applied bias voltages. Table 5.7 shows the material and doping parameters for dual-threshold MOSFETs. These structures have been optimized such that symmetric GOTFET operation with front and back gate terminals electrically shorted (i.e. V_{FS}=V_{BS}=V_{GS}=1 V) provides the LVT characteristics having V_{TL}≈V_{DD}/3, whereas asymmetric GOTFET operation with back gate and source terminals electrically shorted (i.e., V_{FS}=V_{GS}=1 V & V_{BS}=0 V) provides the HVT characteristics with V_{TH}≈ 2V_{DD}/3 for V_{DD}=1 V.The I_D-V_{GS} characteristics of LVT & HVT nGOTFETs obtained using the non-local BtB generation model with increasing V_{DS} are shown in Fig. 5.15a. The lower V_{TLn} ≈0.36 V and higher V_{THn} ≈0.6 V for the proposed nGOTFETs were extracted using the third derivative method [74]. The I_S-V_{SG} characteristics of LVT & HVT pGOTFETs with increasing V_{SD} are shown in Fig. 5.15b. lower $|V_{TLp}|$ ≈0.32 V and higher $|V_{THp}|$ ≈0.6 V were obtained for the proposed pGOTFETs.

TABLE 5.7: Parameters of dual-threshold nGOTFET and pGOTFET

	LVT & HVT nGOT		LVT & HVT pGOT	
Region	Material	Doping /cm^3	Material	Doping /cm^3
Source	$Si_{.08}Ge_{.92}$	10^{20} p$^+$	$Si_{.28}Ge_{.72}$	9×10^{19} n$^+$
Channel	Si	10^{15} n	$Si_{.28}Ge_{.72}$	5×10^{16} p
Drain	Si	10^{20} n$^+$	$Si_{.28}Ge_{.72}$	10^{19} p$^+$
Front gate	$TiSi_2$	—	$TiSi_2$	—
Back gate	Al	—	TiN	—

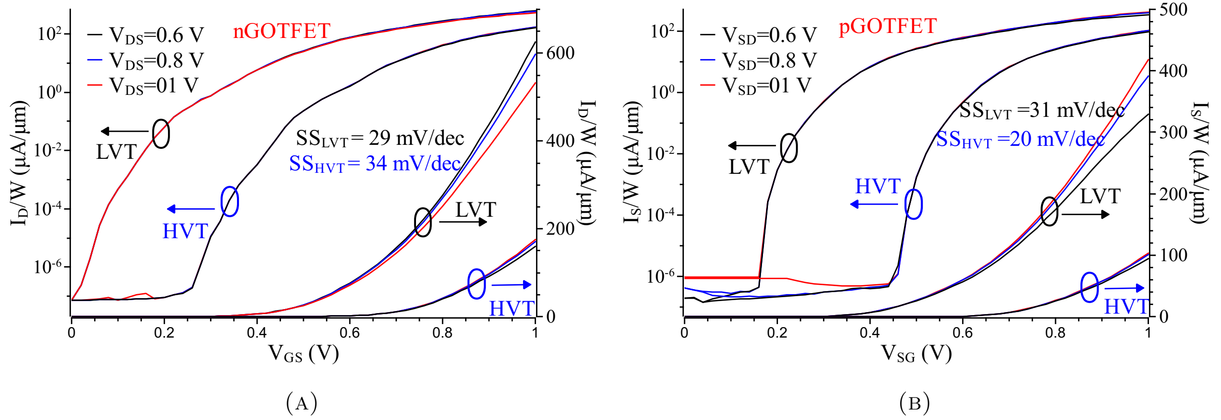


FIGURE 5.15: (A) I_D-V_{GS} characteristics of dual-threshold nGOTFETs for different values of V_{DS}. (B) I_S-V_{SG} characteristics of dual-threshold pGOTFETs for different values of V_{SD}.

5.6 Conclusions

The GOTFETs proposed in this chapter for ultra-low-power circuits have I_{off} at least an order of magnitude lower. At the same time, I_{on} exceeds double that of an equally sized standard MOSFET at the same 45 nm technology node. The higher I_{on} makes the circuits more robust with improved performance, while lower I_{off} leads to a significant reduction in static (leakage) power dissipation. The influence of various device parameters has been optimized to improve electrostatics, leading to better device characteristics. We further modified the structure to suppress the ambipolarity currents in negative gate biases for digital circuit applications. We have demonstrated that gate overlap on the drain side and drain doping concentration decreases the tunneling width at the drain-channel interface, resulting in the suppression of ambipolarity at high negative gate biases. In the proposed GOTFET, ambipolar current at V_{GS}=−1 V is six orders of magnitude lower than the ambipolar current of the GOTFET without gate-drain overlap and N_S=N_D=10^{20} /cm^3. Unlike most of the techniques reported in the literature, the

proposed technique does not deteriorate the I_{on} & I_{off} levels, maintaining I_{on} = 1.046 mA/μm and I_{off} = 0.27 pA/μm at V_{DS}=1 V. In addition to improving the GOTFETs' performance of digital circuits, this chapter also presents LVT & HVT GOTFET devices for ultra-low power ternary logic circuits. Ternary logic circuits have reduced interconnect delay, less area, and lower power than digital circuits. The LVT & HVT GOTFET devices proposed in this chapter have I_{off} at least an order magnitude lower than the MOSFET, while I_{on} is roughly twice that of the MOSFET at the same technology node. The higher I_{on} makes ternary logic circuits operate much faster, while lower I_{off} leads to a significant reduction in static power consumption. Appropriate material with appropriate work functions has been optimized so that the LVT & HVT voltages are $V_{DD}/3$ and $2V_{DD}/3$, respectively. The NTI, PTI & STI logic cells have been designed using LVT & HVT CGOT devices and compared with analogous CMOS ternary logic cells. The overall power delay product of CGOT logic cells is two orders lower than the corresponding CMOS logic cells. The NTI, PTI, and STI cells designed with the proposed LVT & HVT CGOT are excellent starting points for designing any practical ternary logic applications.

5.7 Publications Based on This Chapter

Conferences

1. **Simhadri Hariprasad***, Surya Shankar Dan, Ramakant Yadav and Sanjay Vidhyadharan, "Innovative Strained SiGe Nanoscale Low & High V_t Gate Overlap TFET Structures at 45 nm Standard CMOS Technology for Ultra-Low Power Yet High Performance Analog, Digital and Ternary VLSI Applications", XXth International Workshop on Physics of Semiconductor Devices (IWPSD 2019), Kolkata

Journals

1. Ramakant Yadav, Surya Shankar Dan*, Sanjay Vidhyadharan and **Simhadri Hariprasad**, "Innovative multi-threshold gate-overlap tunnel FET (GOTFET) devices for superior ultra-low power digital, ternary and analog circuits at 45-nm technology node ", Springer Journal of Computational Electronics, vol. 19, pp. 291-303, Jan 2020

2. Ramakant Yadav, Surya Shankar Dan*, Sanjay Vidhyadharan and **Simhadri Hariprasad**, "Suppression of Ambipolar Behavior and Simultaneous Improvement in RF Performance of

Gate-Overlap Tunnel Field Effect Transistor (GOTFET) Devices", Springer Silicon, vol. 13, pp. 1185–1197, Jul 2020.

3. Yadav, Ramakant, Surya Shankar Dan, and **Simhadri Hariprasad**. "Low and High V_t GOTFET Devices Outperform Standard CMOS Technology in Ternary Logic Applications." IETE Technical Review (2021): 1-10.

Chapter 6

Ultra-Low Power VLSI Applications of the Proposed GOTFET Devices

This chapter goes further beyond the device level and shows, with the help of the implementation of digital circuits using proposed GOTFETs in the previous chapters, that the proposed GOTFET devices outperform similar CMOS designs in both aspects of the speed of operation and power consumption.

6.1 Implementation of Digital Basic Building Blocks

Low power design circuits, GOTFET is a promising alternative for the MOSFET due to its SS and low leakage currents. Higher I_{ON} and SS enable the CGOT-based digital circuits to operate faster and lower static power consumption compared to the same circuit implemented with CMOS devices due to low I_{OFF}. The schematic of the inverter circuit design using CGOT and its delay characteristics are shown in Fig. 6.1.

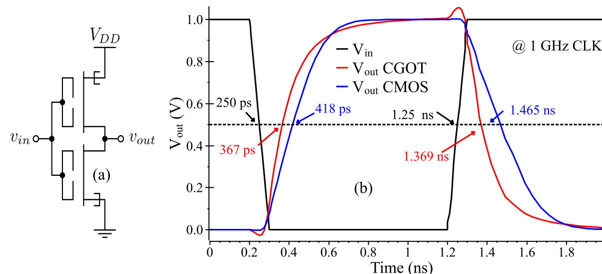


Figure 6.1: (a) Schematic of CGOT inverter (b) Delay comparison CGOT vs. CMOS inverter.

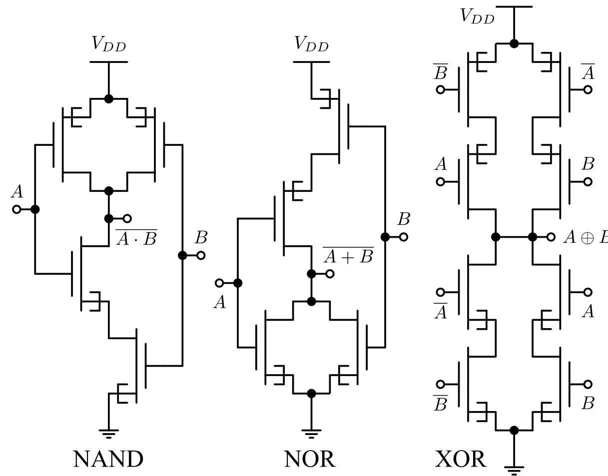


FIGURE 6.3: Schematic of CGOT digital circuits : 2 input (a) NAND (b) NOR (c) XNOR gates.

The performance of the CGOT inverter has been benchmarked with identical CMOS based inverter with same aspect ratio. The circuit has been simulated at 1 GHz clock frequency with a load capacitance of 10 fF. As evident from Fig. 6.1 the CGOT inverter operates 1.43 times faster than the corresponding CMOS inverter. The comparison of static power consumption of CGOT with CMOS inverter is shown in Fig. 6.2. The CGOT inverter consumes merely 0.009 times the power consumed by corresponding CMOS inverter. Overall a decrease of 99.45% in PDP can be achieved by replacing the CMOS devices with the proposed CGOT devices.

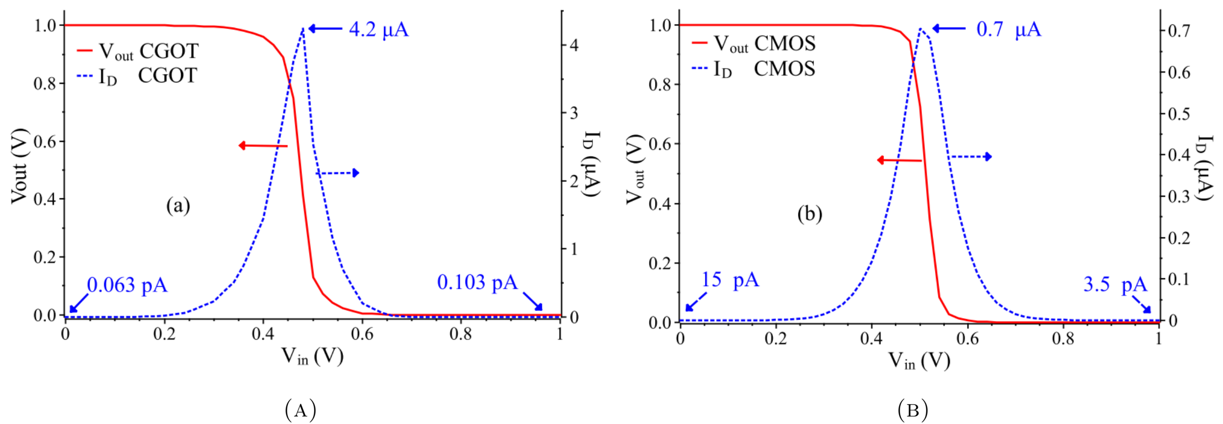


FIGURE 6.2: Comparison of static currents (a) CGOT vs. (b) CMOS inverter..

The schematic of the CGOT 2-input NAND, NOR and XNOR gates is shown in Fig. 6.3. The comparison of delay and static power characteristics for NAND, NOR and XNOR gates are shown in Figs. 6.4, 6.5 & 6.6 respectively. The improvement in the performance parameters is summarized in Table 6.1.

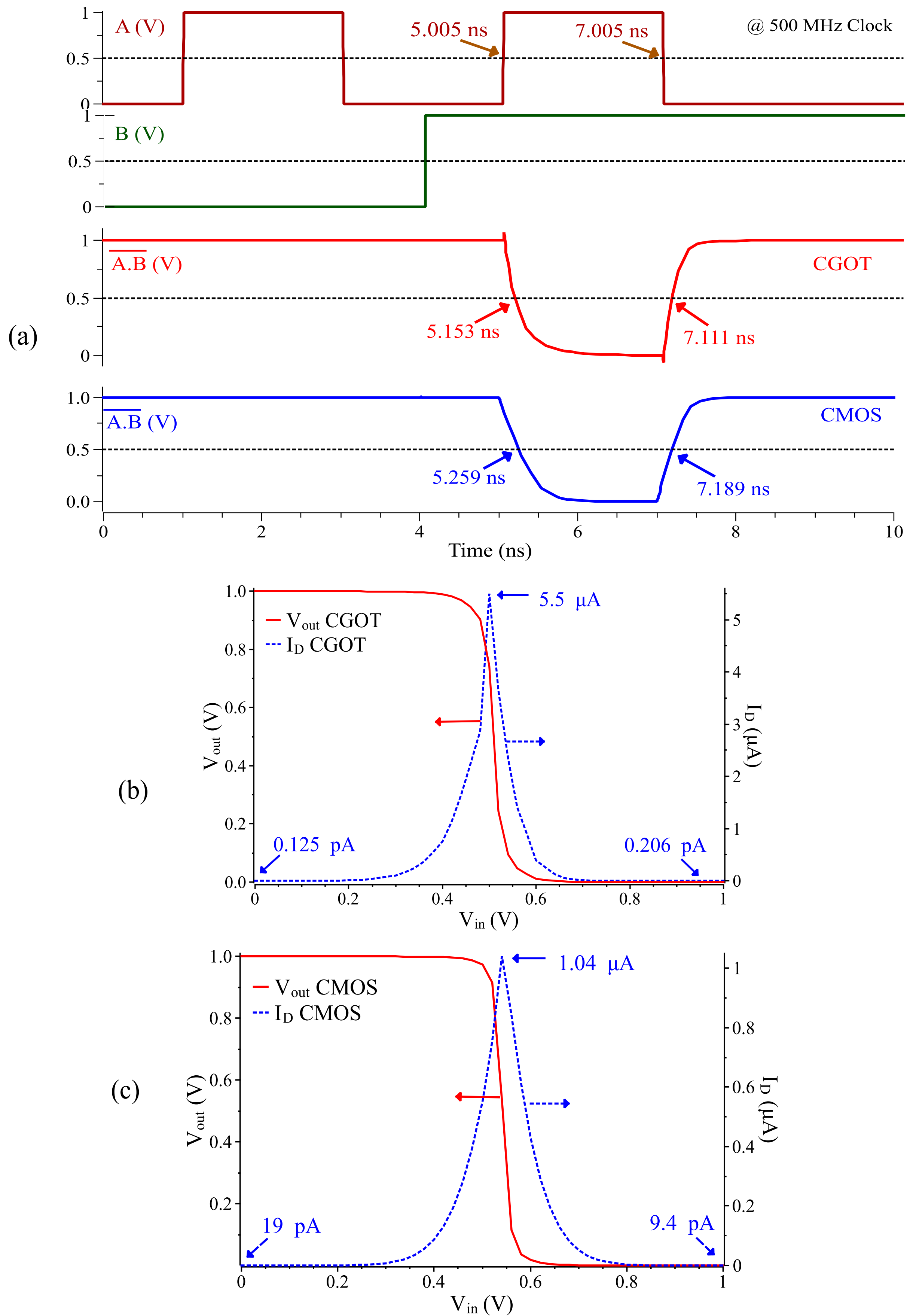


FIGURE 6.4: (a) Delay comparison CGOT vs. CMOS NAND gates. Comparison of static currents (b) CGOT vs. (c) CMOS NAND gates.

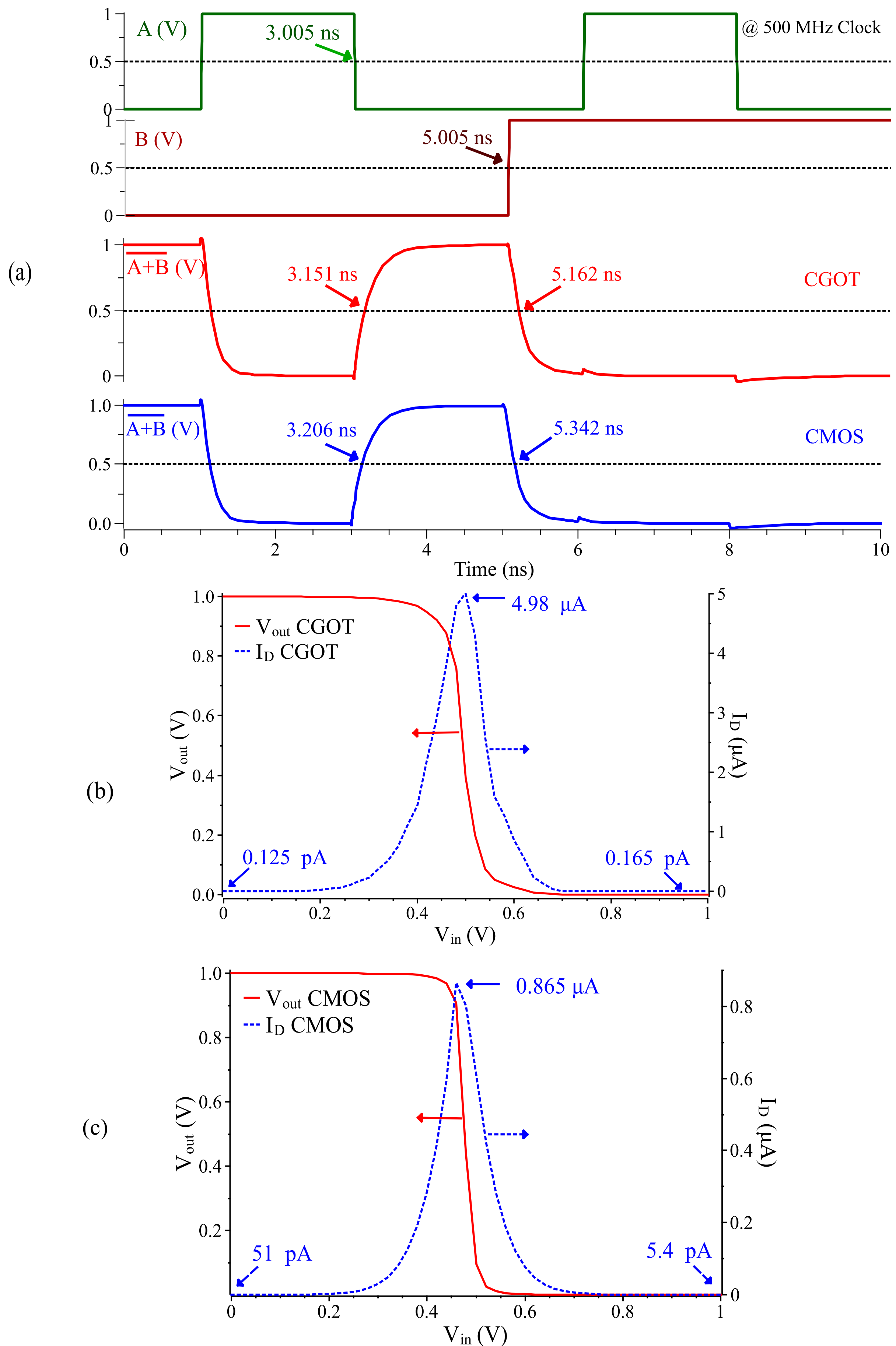


FIGURE 6.5: (a) Delay comparison CGOT vs. CMOS NOR gates. Comparison of static currents (b) CGOT vs. (c) CMOS NOR gates.

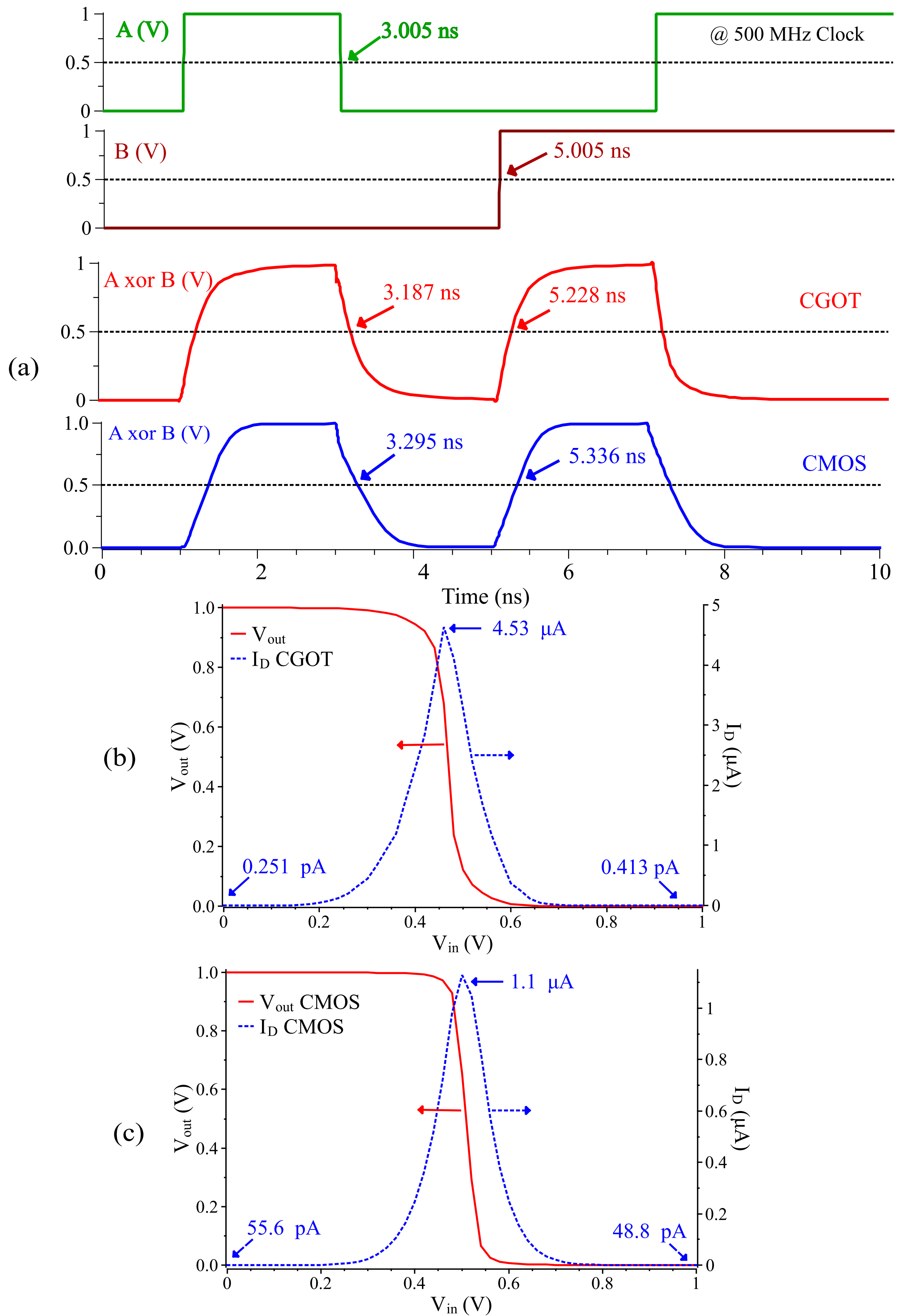


Figure 6.6: (a) Delay comparison CGOT vs. CMOS XOR gates. Comparison of static currents (b) CGOT vs. (c) CMOS XOR gates.

TABLE 6.1: Benchmarking the performance parameters of inverter NAND, NOR & XOR gates implemented with CGOT and CMOS technologies at 10 fF load capacitance

		Inverter		2-i/p NAND		2-i/p NOR		2-i/p XNOR	
Circuit parameter	Unit	CMOS	CGOT	CMOS	CGOT	CMOS	CGOT	CMOS	CGOT
Bias V_{DD}	V	1	1	1	1	1	1	1	1
Delay $\tau_{pd\ LH}$	ps	168	117	184	106	201	146	331	223
Delay $\tau_{pd\ HL}$	ps	215	119	254	148	337	157	290	182
Average delay	ps	191.5	118	219	127	269	151.5	310.5	202.5
Static I_{high}	pA	15	0.063	19	0.125	51	0.125	55.6	0.251
Static I_{low}	pA	3.5	0.103	9.4	0.206	5.4	0.165	48.8	0.413
Average P_{static}	pW	9.25	0.083	14.2	0.166	28.2	0.145	52.2	0.332
PDP ($\times 10^{-23}$)	J	177.1	0.98	310.98	2.1	758.6	2.2	1620.81	6.72
Decrease in PDP		99.45 %		99.32%		99.71%		99.58%	

GOTFETs have been found to perform better in digital circuits as compared to the standard MOSFET circuits and are an apt replacement for MOSFETs. The use of GOTFETs speeds up the operation and power wastage is reduced significantly and leading to a lower PDP as compared to MOSFET based circuits.

6.2 GOTFET Based Improved Double-Tail Dynamic Comparator

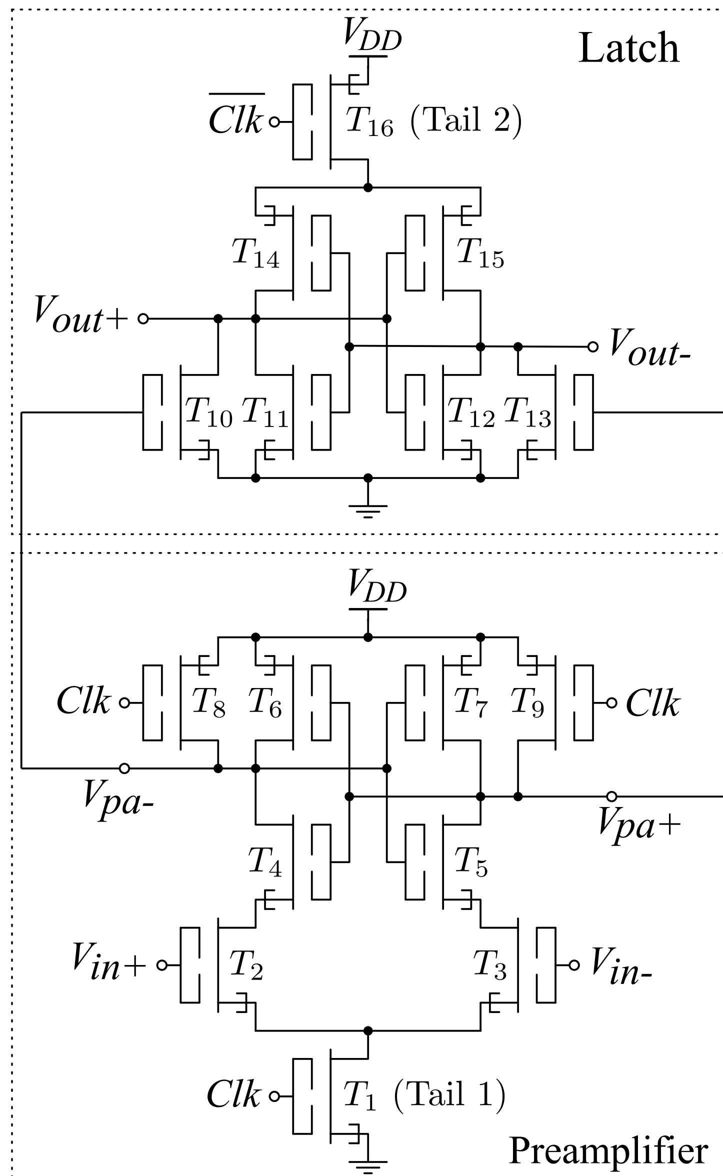


FIGURE 6.7: Schematic of the CGOT double-tail dynamic comparator with conventional design.

ADC is important block which connects analog & digital circuits in wide variety of DSP and mixed signal applications. Comparator are basic building block in ADC, requires high speed less delay. Usually, dynamic comparators are preferred in ADC because of less delay and low power dissipation. The double-tail CGOT comparator is formed by cascading a preamplifier with a latch. GOTFETs T_1-T_9 constitute the preamplifier and TFETs T_{10}-T_{16} form the latch as shown in Fig. 6.7.

The conventional Dynamic Comparator designed using the proposed CGOT paradigm exhibits 93 ps (25%) lower delay than similar CMOS designs and consumes merely 1.11 pW (99% lower than CMOS) of static power. The overall PDP in the CGOT comparator design has been shown to be only 0.5% of the PDP of a conventional CMOS comparator. The simulation result of delay characteristics, shown in Fig. 6.8, indicate that the CGOT comparator has a delay of only 277 ps while the analogous CMOS double-tail comparator exhibits a delay of 370 ps.

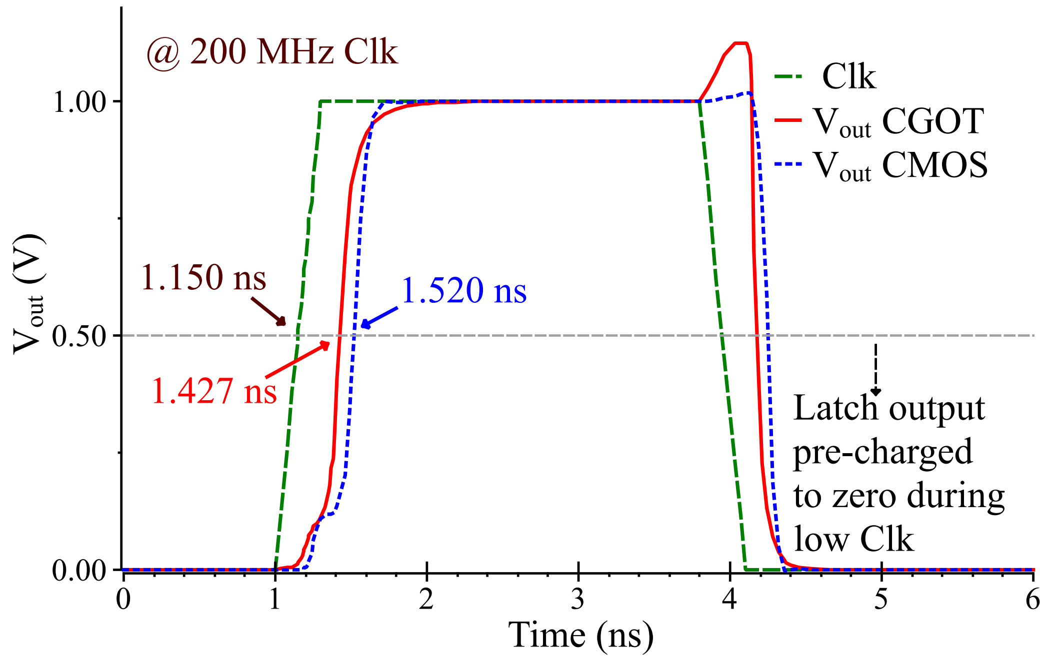


FIGURE 6.8: (a) Bench marking the delay characteristics of conventional CGOT vs. CMOS double-tail comparator.

The static power consumption of the comparator for the HIGH and LOW output states is compared with that of CMOS in Fig. of 6.9. The static power consumption of merely 1.11 pW in CGOT double-tail comparator is significantly lower than that of CMOS double-tail comparator which consumes 154 pW. The overall PDP of CGOT double-tail comparator is only 3.07×10^{-22} J, which is merely 0.5% of the PDP of the standard 45 nm CMOS double-tail comparator (5.7×10^{-20} J). The reduction in PDP by simply replacing MOSFETs with GOTFETs in conventional double-tail comparator circuit is 99.5%, as summarized in Table 6.2.

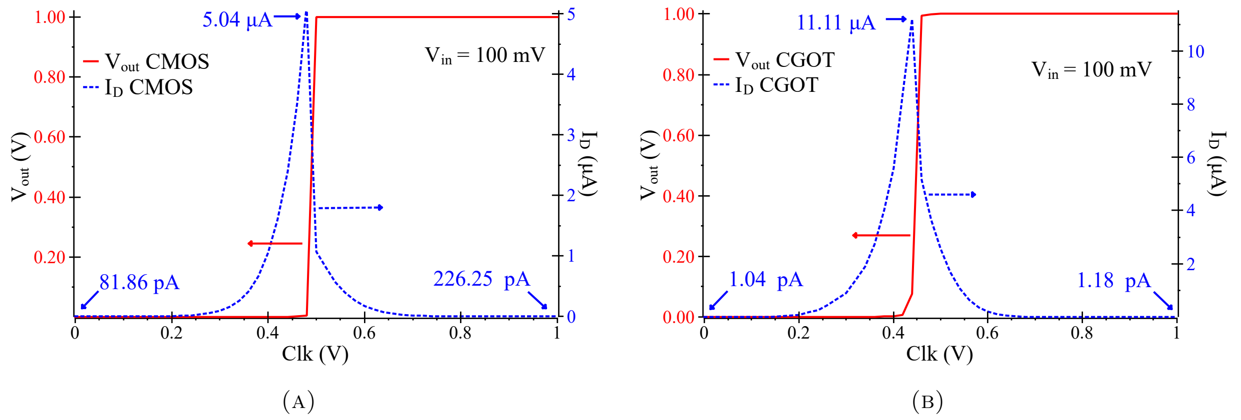


FIGURE 6.9: (a) Static power consumption of CMOS contrasted with that of (b) CGOT conventional double-tail comparator.

TABLE 6.2: Significant improvement in propagation delay and static power consumption of CMOS and CGOT conventional double-tail dynamic comparator design

Circuit parameter	Units	CMOS	CGOT
Power supply V_{DD}	V	1	1
Propagation delay	ps	370	277
Static power, LOW *Clk*	pW	81.86	1.04
Static power, HIGH *Clk*	pW	226.25	1.18
Average static power	pW	154	1.11
Power Delay Product (PDP)	$\times 10^{-22}$ J	570	3.07
Decrease in PDP			99.5%

The high ON currents I_{ON} of the optimized GOTFETs ensures faster operation of the CGOT comparator as compared to the CMOS based comparator. As expected out of TFET technology, immense savings in static power consumption has been achieved due to the low OFF currents I_{OFF} of the optimized GOTFETs. Overall, the decrement in PDP in the CGOT double-tail comparator circuit is 99.5%, with the PDP of the CGOT conventional double-tail regenerative comparator being less than 0.5% of the PDP of standard 45 nm CMOS based analogous circuit.

6.3 GOTFET Based Dynamic Full Adder (DFA)

Full adder (FA) is one of the basic building blocks for most of the arithmetic and logic circuits in DSP and microprocessors. The DFA performance has been benchmarked with the same circuit using industry standard 45 nm CMOS devices. By replacing the standard CMOS devices with the proposed CGOT devices, the overall PDP is further reduced to merely 0.9% of the standard

TABLE 6.3: Truth table of a Full Adder (FA)

Operand	*A*	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1
	C	0	0	0	0	1	1	1	1
Sum		0	1	1	0	1	0	0	1
Carry		0	0	0	1	0	1	1	1

Carry (CY) $= AB + BC + AC$

Sum (S) $= \overline{A}\overline{B}C + A\overline{B}\overline{C} + \overline{A}B\overline{C} + ABC$

$CY = AB + C(A+B)$
$S = \overline{CY}(A+B+C) + ABC$
} Simplified Expressions

CMOS designs. Conventional FA uses an nMOS based pull down network (PDN) with equal number of complementary pMOS based pull up network (PUN) to implement the FA functionality given in Truth Table 6.3. However a more efficient CGOT DFA is formed by cascading a *Carry Module* with a *Sum Module* as shown in Fig. 6.10. In the CGOT DFA, the entire PUN is replaced with a single precharging pGOTFET T_7 in the *Carry Module* and pGOTFET T_{18} in the *Sum Module*, significantly reducing the transistor count and gate capacitance, thereby improving the performance of the DFA. The carry logic is implemented using the simplified expression of carry $\overline{CY} = \overline{AB + C(A + B)}$ through the PDN formed by nGOTFETs T_2 - T_6 and the inverter formed by GOTFETs T_8 & T_9 generate the required CY signal. The simplified sum $\overline{S} = \overline{\overline{CY}(A + B + C) + ABC}$ is implemented by the PDN nGOTFETs T_{11}-T_{17}. GOTFETs T_{19}-T_{20} form the inverting buffer stage generating the required S signal.

The operation of the *Carry Module* and *Sum Module* with respect to Clk signal for all combinations of inputs are illustrated in Fig. 6.11. When the clock Clk is LOW, both the $\overline{CY}$ and $\overline{S}$ nodes are precharged to the HIGH state through pGOTFETs T_7 & T_{18} respectively. This forces CY and S nodes to the LOW state. Both the $\overline{CY}$ and $\overline{S}$ PDN networks are enabled as soon as the Clk signal goes HIGH and the output nodes $\overline{CY}$ & $\overline{S}$ are pulled down to LOW state if the inputs satisfy the corresponding logic, else the nodes remain at HIGH state. The inverters produce the required S and CY outputs when the Clk is HIGH and toggle back to the LOW state when the Clk goes LOW.

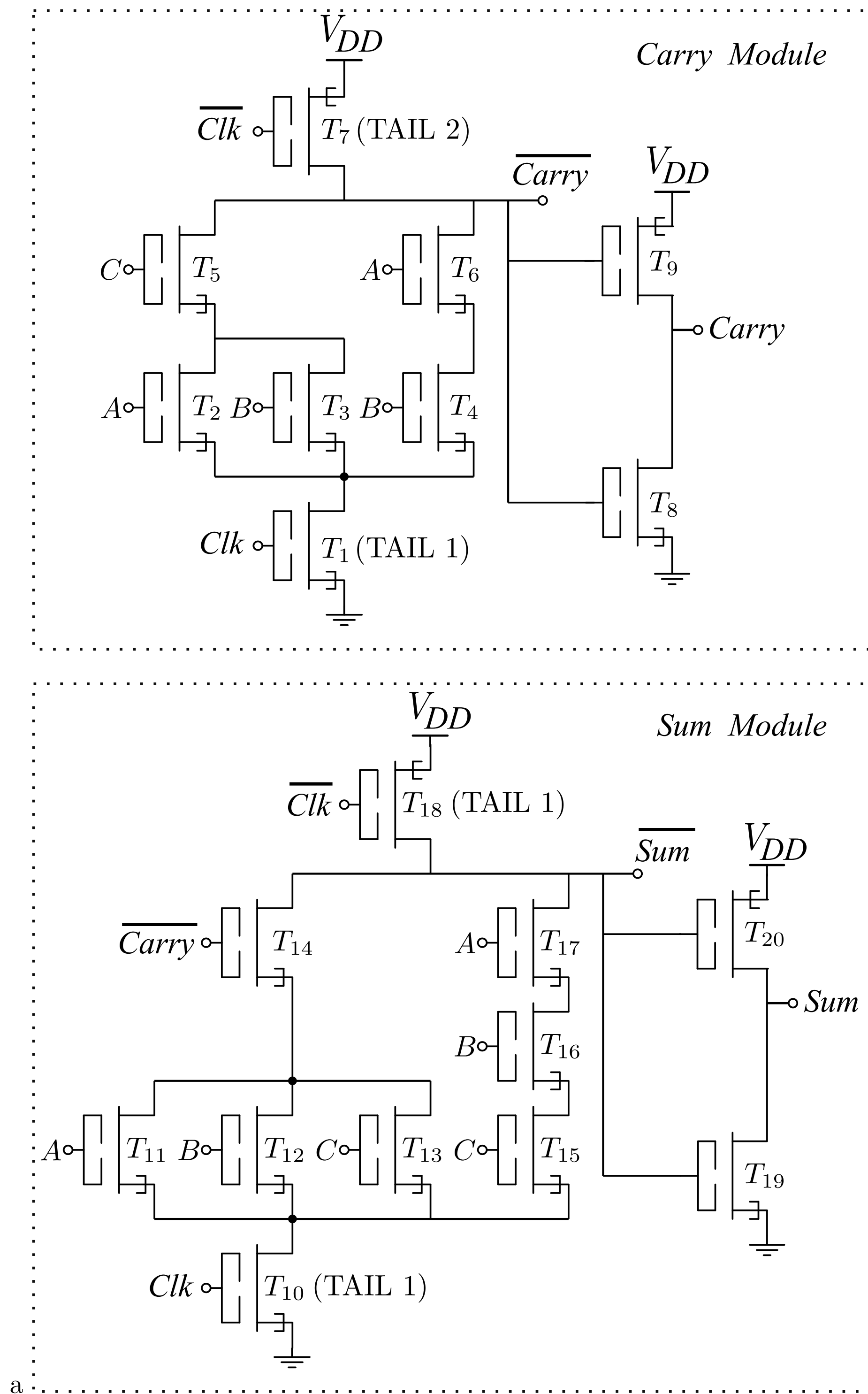


Figure 6.10: Schematic of the CGOT based conventional DFA.

6.3.1 Benchmarking CGOT DFA Against CMOS Dynamic Full Adder

Circuit performance of the CGOT conventional DFA was benchmarked with the same circuit using 45 nm CMOS library, since the effective channel lengths of the proposed GOTFETs are 45 nm. The widths of the corresponding device instances used in the two circuits being benchmarked

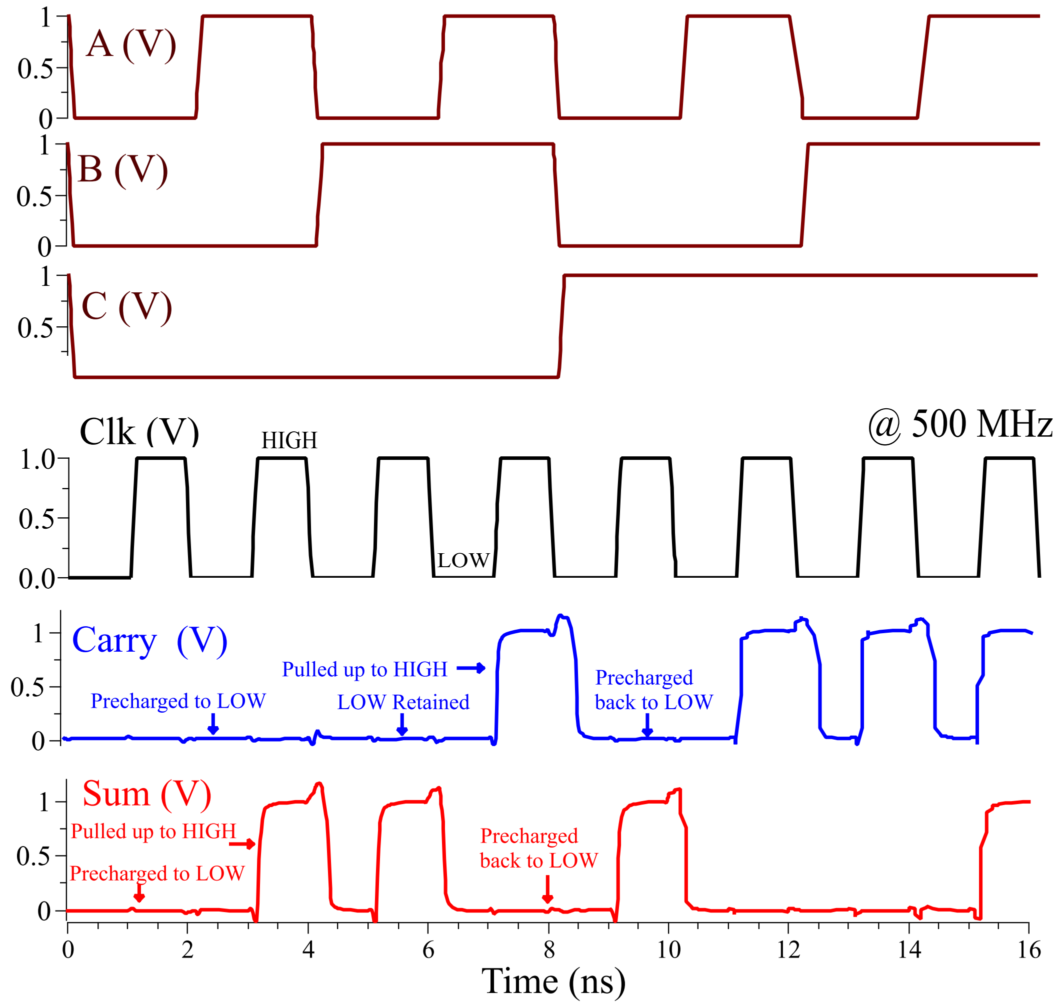
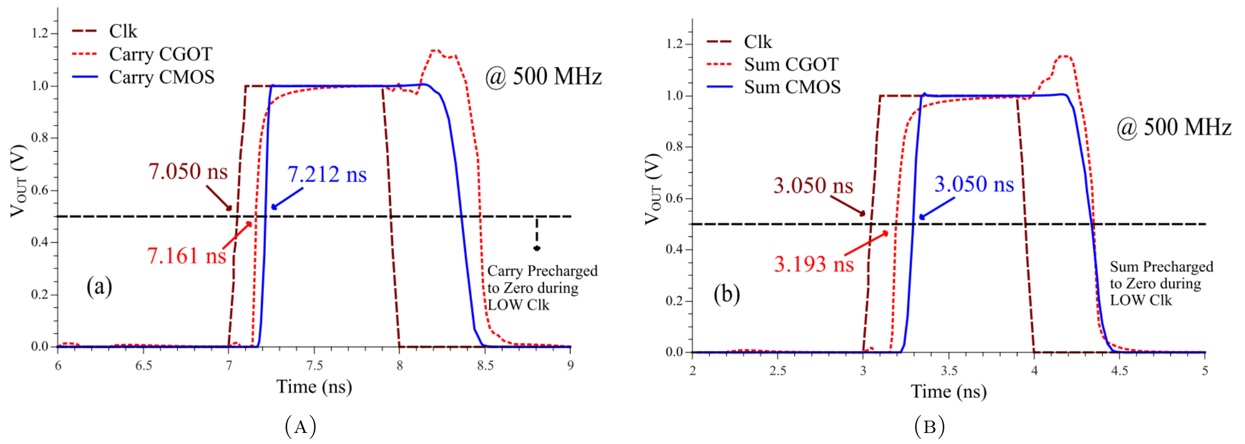


FIGURE 6.11: Operation of CGOT DFA at 500 MHz *Clk*.

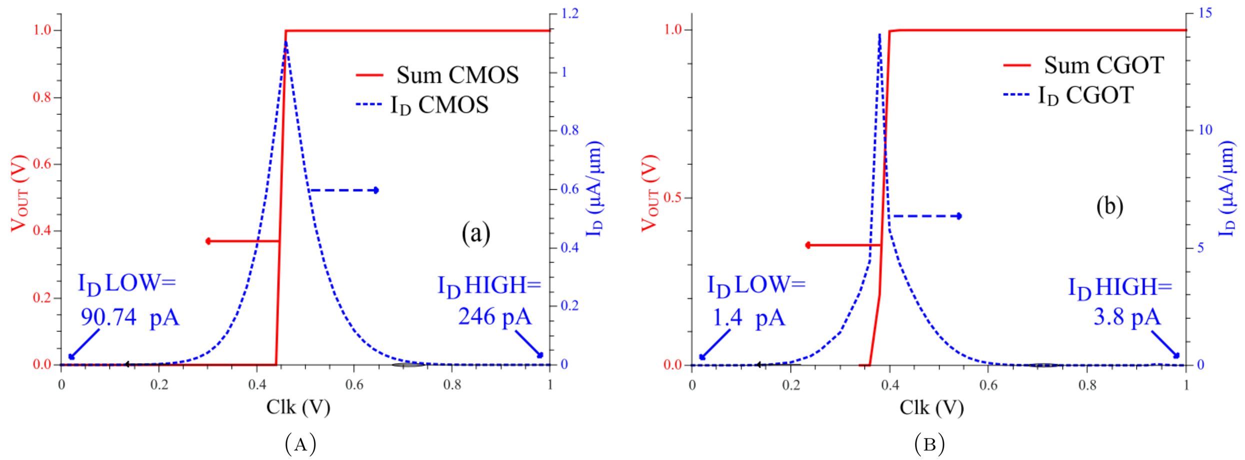
have been kept equal. Circuit simulations shown in Fig. 6.12 indicates that CGOT DFA has a carry and sum delays of only 111 ps and 143 ps respectively while CMOS DFA exhibits carry and sum delays of 162 ps and 242 ps respectively. Furthermore, the average static power in CGOT DFA is only 2.6 pW which is significantly lower than CMOS DFA which consumes 168.4 pW as indicated in simulation results of Fig. 6.13. The PDP of CGOT DFA is 3.72×10^{-22} J which is merely 0.009 times the PDP of CMOS DFA (4.01×10^{-20} J). Overall, the decrement in PDP by replacing MOSFETs by the proposed GOTFETs in same DFA circuit is 99.1% as listed in Table 6.4.

CGOT DFA is faster in operation than the CMOS DFA owing to the former's higher I_{ON} and higher transconductance g_m with respect to the standard CMOS. An overall reduction of 99.1% in PDP of conventional DFA can be achieved by replacing CMOS devices with proposed CGOT devices.



(A) (B)

FIGURE 6.12: Benchmarking the delay characteristics for the (a) carry CY and (b) sum S signals.



(A) (B)

FIGURE 6.13: Static Power Consumption of (a) CMOS DFA (b) CGOT DFA

6.4 GOTFET Based Regenerative-Latch Schmitt Trigger

Schmitt triggers are ideal candidates to implement computational and memory elements of low-voltage circuits as they have much larger NM than the corresponding static CMOS logic circuits [126, 127, 128]. Schmitt triggers are also widely used for shaping waveforms under noisy conditions in communication circuits. Schmitt triggers implemented with the proposed GOTFETs will consume substantially lower power than corresponding CMOS Schmitt triggers which is an added advantage since total power available on-board on IoT sensors is limited. The power supply voltage V_{DD} available for implementation of logic and arithmetic circuits is extremely low (less than 0.5 V) for IoT sensor applications. Decrease in V_{DD} reduces the noise margins of the circuit, making CMOS static circuits extremely susceptible to noise at ultra-low voltages. The circuit has an extremely poor average low noise margin (NM_L=180

TABLE 6.4: Comparison of delay and static power parameters of CGOT and CMOS based Dynamic FA (DFA) for a capacitive load equivalent to the fanout of 4.

Circuit parameter	Units	CMOS DFA	CGOT DFA
Power Supply V_{DD}	V	1	1
Carry Delay	ps	162	111
Sum Delay	ps	242	143
Static Power, LOW *Clk*	pW	90.74	1.4
Static Power, HIGH *Clk*	pW	246	3.8
Average Static Power, P_{static}	pW	168.4	2.6
PDP ($\times 10^{-22}$)	J	401	3.72
Overall Decrease in PDP w.r.to CMOS DFA			99.1%

mV & NM_H=185 mV) for a V_{DD}=400 mV making the CMOS static inverter quite unreliable. Furthermore, V_{DD} reduction in turn reduces the overdrive V_{ov}=($V_{GS} - V_t$) available at the gate terminals of the transistors, which in turn, reduces the switching currents resulting in larger propagation delays.

The schematic of the conventional Schmitt trigger inverter/buffer circuit [126, 129] implemented with CGOT is shown in Figs. 6.14. The performance of CGOT conventional Schmitt trigger circuit was compared with the same conventional Schmitt trigger circuit implemented using standard 45 nm CMOS devices and the comparative simulation results are shown in Fig. 6.15. The optimized GOTFET channel length is 45 nm and hence the same technology node for CMOS has been used for benchmarking. The noise margins (hysteresis width) have been kept same in

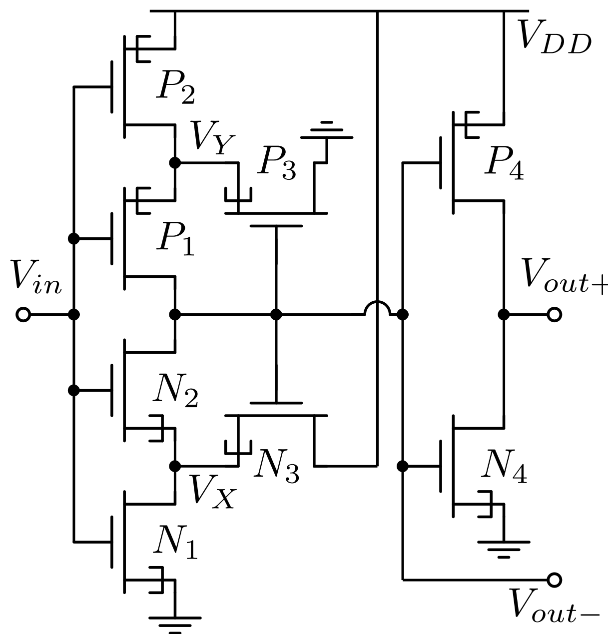


FIGURE 6.14: Schematic of the CGOT conventional Schmitt trigger inverter/buffer.

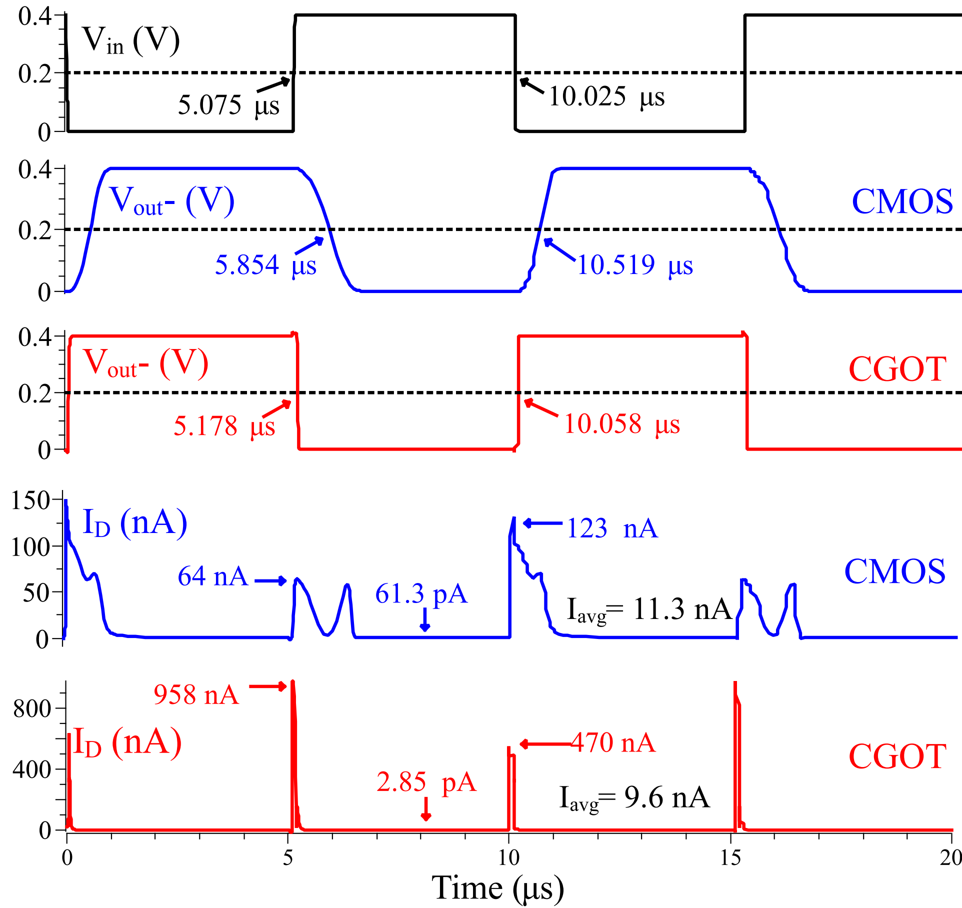


FIGURE 6.15: Transient switching characteristics of the CGOT vs. CMOS conventional Schmitt trigger inverter/buffer at a capacitive load of 20 fF.

both the circuits by appropriately sizing the transistors for accurate and meaningful comparison. An equal load capacitance of 20 fF was considered for both the circuits. On one hand, since our proposed GOTFETs have better I_{ON} than that of the corresponding MOSFETs, the delays of CGOT Schmitt trigger are significantly lower than the CMOS Schmitt trigger circuit. On the other hand, since the I_{OFF} of our proposed GOTFETs are at least one order lower than the corresponding MOSFETs, the static power consumption in CGOT Schmitt trigger is significantly lower. The simulation results indicate that CGOT conventional Schmitt trigger has significantly lower average delay of 82 ns as compared to CMOS conventional Schmitt trigger which has a delay of 847 ns. These results also indicate that the average static leakage current in the CGOT Schmitt trigger is merely 2.85 pA as compared to leakage current of 61.3 pA of CMOS Schmitt trigger. While the short circuit current in CGOT Schmitt trigger is higher, the average total power is lower (3.84 nW) than the CMOS Schmitt trigger (4.52 nW) due to faster switching of states (due to higher g_m and lower inverse sub-threshold slope (SS) of the proposed GOTFETs). The overall PDP of CGOT conventional Schmitt trigger is only 0.32 fJ which is merely 8.35%

of the PDP of the standard 45 nm CMOS conventional Schmitt trigger (found to be 3.83 fJ). Overall, the decrement in PDP in the CGOT conventional Schmitt trigger circuit is 91.7% (Table 6.5).

Table 6.5: Improvement in delay and power consumption of CGOT w.r.to CMOS Schmitt trigger for a capacitive load of 20 fF.

		Conventional Design	
Circuit parameters	Units	CMOS	CGOT
Power supply V_{DD}	mV	400	400
Noise margin	mV	260	260
Hysteresis width	mV	120	120
Inverter delay τ_{pLH}	ns	494	33
Inverter delay τ_{pHL}	ns	779	103
Buffer delay τ_{pLH}	ns	1223	144
Buffer delay τ_{pHL}	ns	890	49
Average delay τ_p	ns	847	82
Average power P_{avg}	nW	4.52	3.84
PDP	fJ	3.83	0.32
PDP w.r.to CMOS		91.7%	

The high I_{ON} of the optimized GOTFETs ensure faster operation of the proposed CGOT Schmitt trigger as compared to the CMOS based Schmitt trigger. As expected out of TFET technology, immense savings in static power consumption has been achieved due to the low OFF currents of the optimized GOTFETs. Overall, the decrement in PDP in the CGOT Schmitt trigger circuit is 91.7% as compared to the PDP of the conventional CMOS Schmitt trigger.

6.5 GOTFET Based Innovative Ternary Flash ADC

Recent studies have revealed that ternary logic significantly reduces transistor count besides enabling faster data transfer [130, 131, 118, 119]. Ternary logic circuits can be implemented using CMOS devices, but they consume considerably large power. Ternary ADC must be designed so as to receive analog input and provide ternary 2-bit output as depicted in Table 6.6. Unlike

binary, voltage levels V_{DD}, $V_{DD}/2$ & 0 are interpreted as logic states 2, 1 and 0 respectively. The analog input is first quantized into 9 discrete levels using 8 comparators as shown in Fig. 6.16. The next step is to design a combinational logic circuit to convert these 9 different quantized levels into signals which can drive two ternary encoders (Fig. 6.16).

TABLE 6.6: Quantization levels and equivalent 2-bit ternary output.

Quantization levels	*Ternary output*	
	B_1	B_0
Level 8	2	2
Level 7	2	1
Level 6	2	0
Level 5	1	2
Level 4	1	1
Level 3	1	0
Level 2	0	2
Level 1	0	1
Level 0	0	0

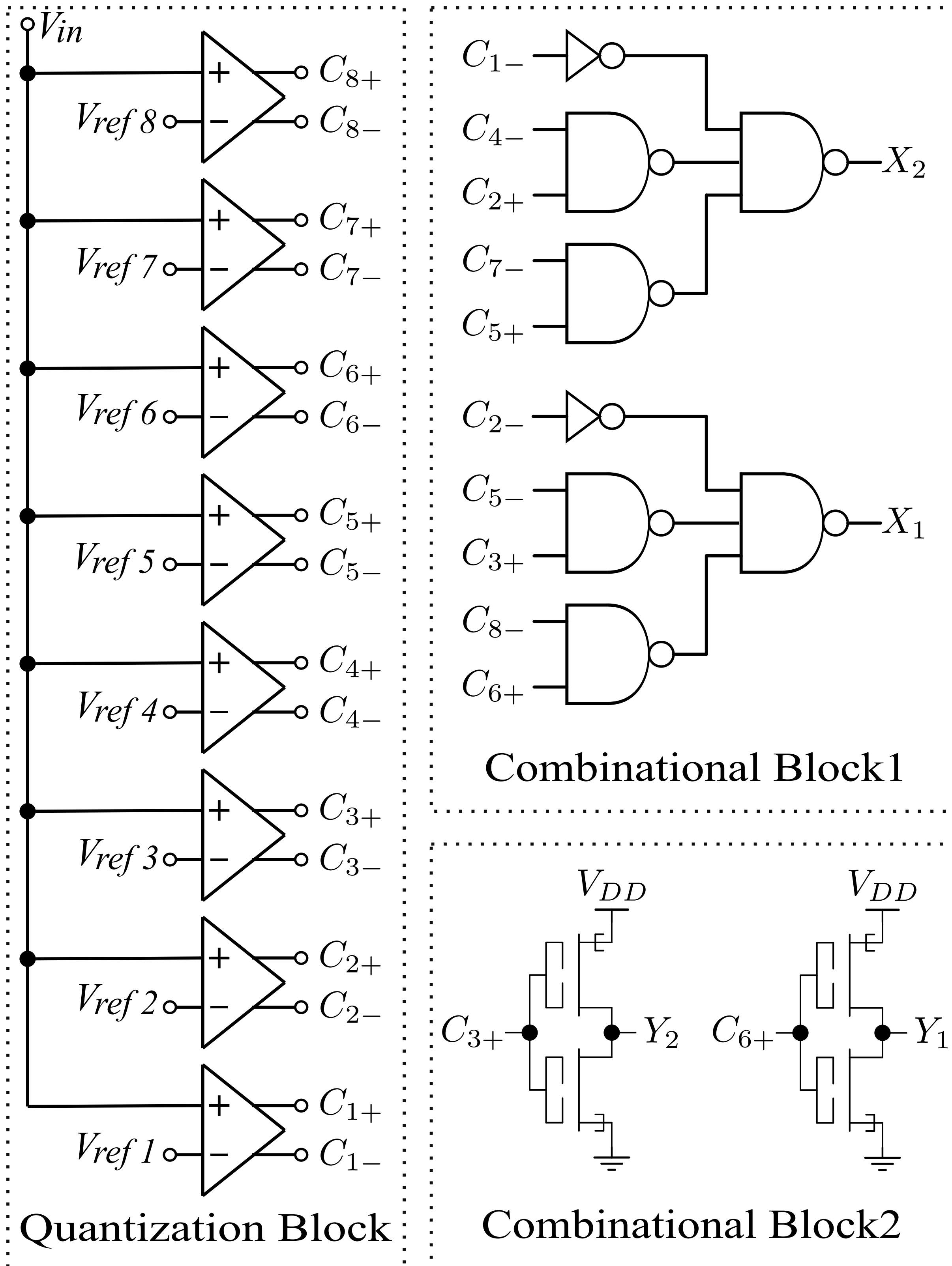


FIGURE 6.16: Schematic of the input stage & combinational logic circuit of the proposed GOTFET 2-bit ternary flash ADC.

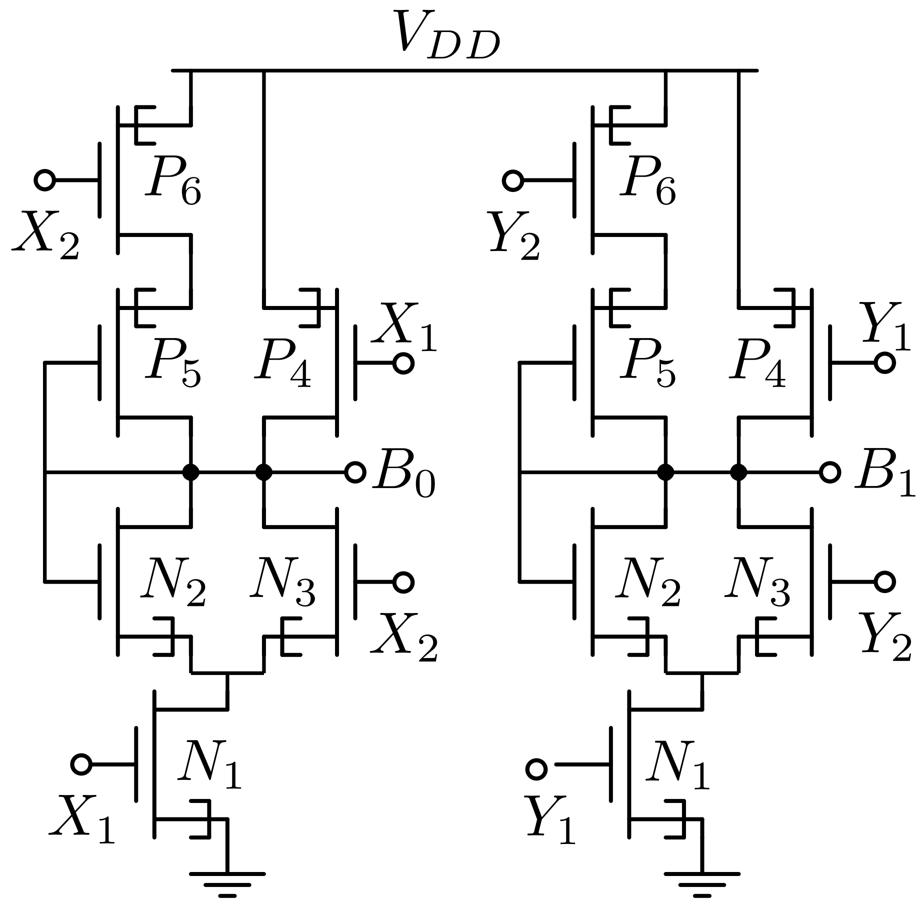


FIGURE 6.17: Schematic of the encoder used in the output stage of the proposed CGOT 2-bit ternary flash ADC.

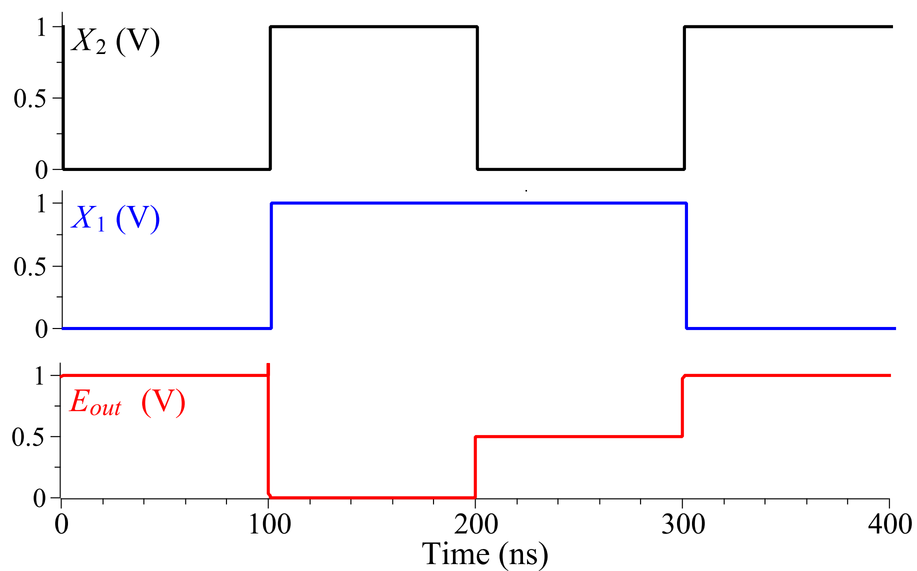


FIGURE 6.18: Performance plot of encoder.

The output stage consists of two independent encoders which generate the 2-bit ternary digital output as shown in Fig. 6.17. *Encoder1* generates the LSB B_0 with inputs X_2 & X_1 while *Encoder2* generates the MSB B_1 with inputs Y_2 & Y_1. Performance of the Encoder is shown in Fig. 6.18. Truth table for designing the combinational block with comparator outputs as input variables is shown in Table 6.7. The other combinations of comparator outputs are considered as don't care conditions while optimizing the combinational logic. On careful study, it can be seen that this novel ADC design requires only 48 transistors to encode the comparator outputs into the 2-bit ternary output which is significantly lower than the 70 transistors required for the 2-bit ternary flash ADC design reported earlier [132].

6.5.1 Validation of the Proposed ADC Design

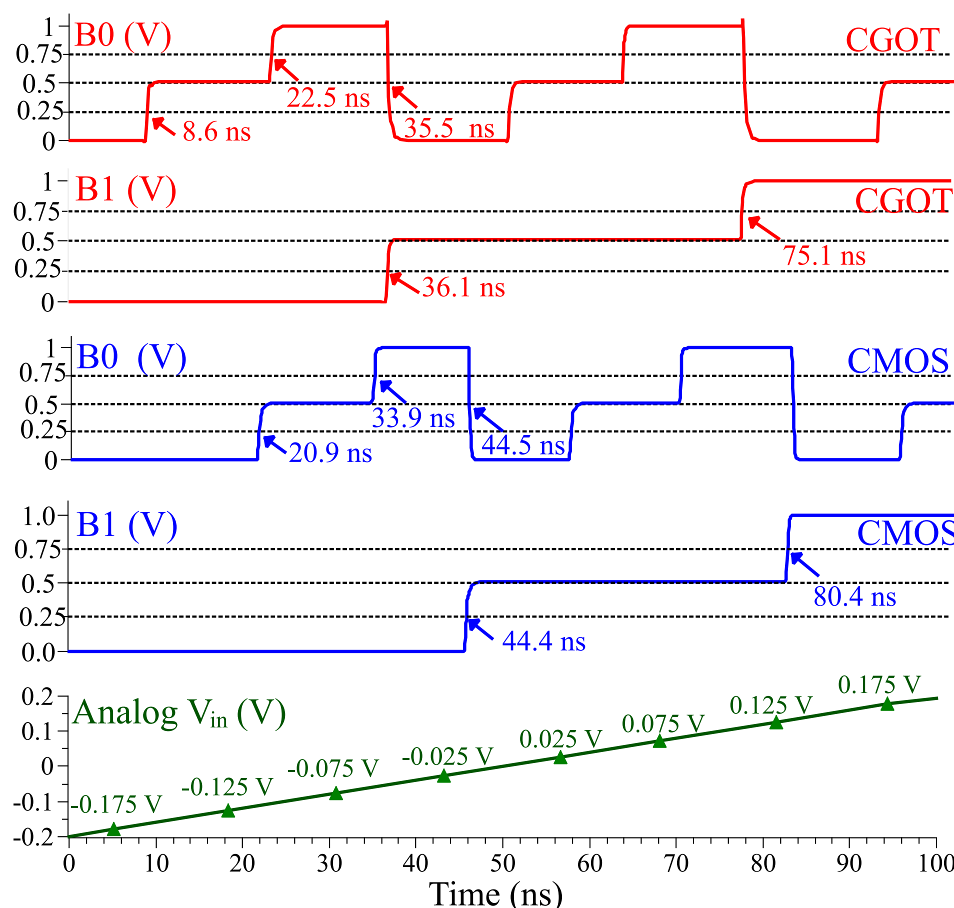


FIGURE 6.19: Transient response of the proposed CGOT Ternary ADC output vs. CMOS ADC for input signal sweep ±200 mV at 10 fF Load capacitance.

Circuit simulations were carried out by providing an input sweep from -200 mV to +200 mV, with an DC bias of 0.655 V and capacitive load of 10 fF. The simulation results are shown in

Fig. 6.19. The ADC output from both CGOT and CMOS ADC is shown in the figure. The quantization step size of 50 mV in order to generate 9 discrete quantized levels. The ternary output waveform (Fig. 6.19), perfectly matched with the desired truth table in Table 6.7. The static characteristics of the proposed ADC for analog input sweep from -200 mV to +200 mV with DC bias of 650 mV is shown in Fig. 6.20. The *Figures of Merit* (FOM) of the ADC as specified in [133, 134] are placed as Table 6.8. The *Differential Non-linearity* (DNL) and *Integral Non-linearity* (INL) plots are shown in Fig. 6.21.

Table 6.7: Truth table for the combinational block design.

Comparator output								*Encoder input*				*Encoder output*	
C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	Y_2	Y_1	X_2	X_1	B_1	B_0
0	0	0	0	0	0	0	0	2	2	2	2	0	0
0	0	0	0	0	0	0	2	2	2	0	2	0	1
0	0	0	0	0	0	2	2	2	2	x	0	0	2
0	0	0	0	0	2	2	2	0	2	2	2	1	0
0	0	0	0	2	2	2	2	0	2	0	2	1	1
0	0	0	2	2	2	2	2	0	2	x	0	1	2
0	0	2	2	2	2	2	2	x	0	2	2	2	0
0	2	2	2	2	2	2	2	x	0	0	2	2	1
2	2	2	2	2	2	2	2	x	0	x	0	2	2

6.5.2 Performance Benchmarking of the Proposed GOTFET Against CMOS Ternary Flash ADC

Performance of the proposed 45 nm CGOT ternary flash ADC is benchmarked with the same ADC circuit using industry-standard standard 45 nm CMOS library. The corresponding device widths have been kept same in the two circuits for meaningful benchmarking. In Table 6.8, the performance of the CGOT and CMOS circuits have been benchmarked. Clearly, for the same proposed circuit, we obtain the same *Signal to Noise Ratio* (SNR), *Effective Number Of Bits* (ENOB) along with DNL and INL values.

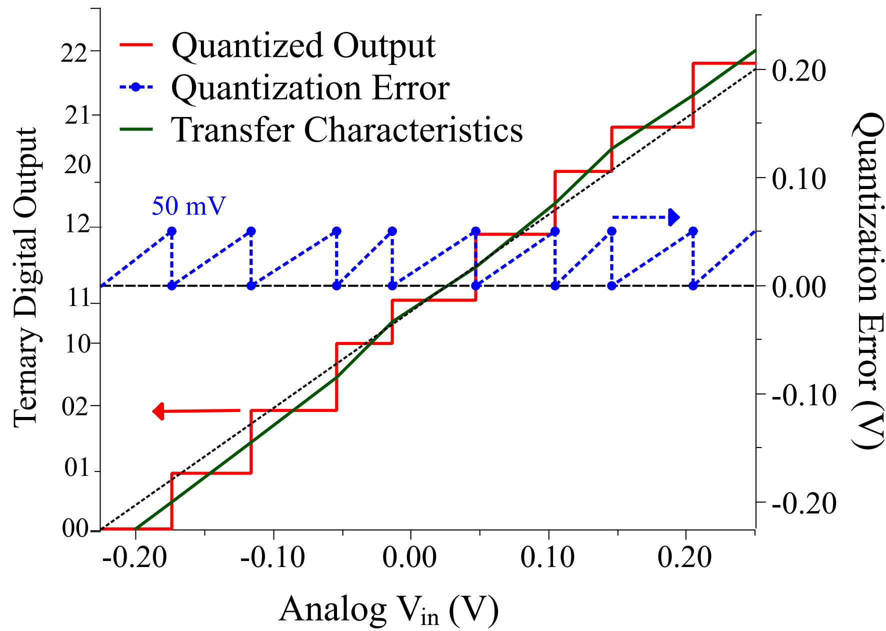


FIGURE 6.20: Static Characteristics of proposed ternary ADC.

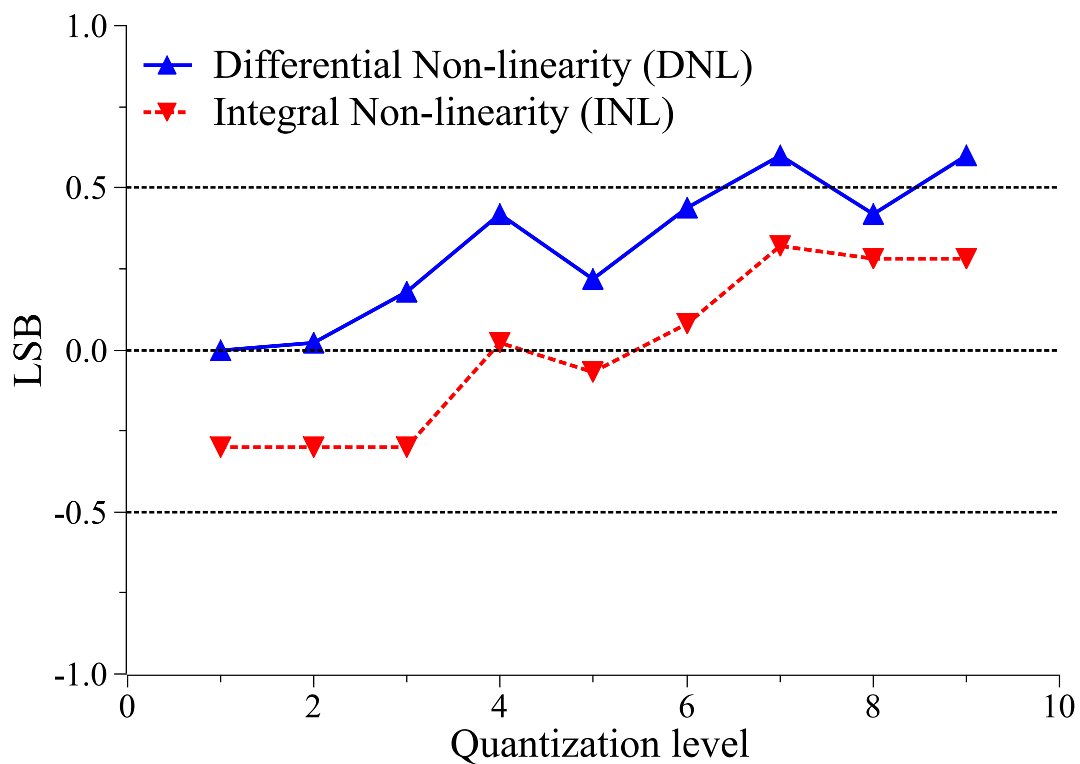


FIGURE 6.21: Differential Non-linearity (DNL) and Integral Non-linearity (INL) Characteristics of proposed ternary ADC.

Since our proposed GOTFETs have twice the I_{ON} of the corresponding MOSFETs, the delays of CGOT ternary flash ADC is much lower than the equivalent CMOS circuit. As GOTFET

I_{OFF} remains at least one order lower than the corresponding MOSFETs, the static leakage power consumption in CGOT ternary flash ADC is significantly lower than the CMOS designs. Higher I_{ON} leads to higher dynamic power consumption which has been minimized through the novel circuit design. Finally, the CGOT ternary ADC has an average delay of only 4.26 ns while CMOS based ternary ADC exhibits a delay of 13.52 ns. The results also indicate total power of only 12.4 μW in CGOT ternary flash ADC which is significantly lower than that of CMOS ternary flash ADC which consumes 59.9 μW. The overall PDP of CGOT ternary flash ADC is only 0.051 pJ which is merely 6.3% of the PDP of the standard 45 nm CMOS ternary flash ADC (0.81 pJ). Overall, the decrement in PDP due to the proposed GOTFET based improved ternary flash ADC circuit is 93.7% as compared in Table 6.8.

Table 6.8: Performance of proposed CGOT ternary ADC compared with CMOS ternary ADC at 10 fF capacitive load

		Ternary ADC	
Circuit parameter	Unit	CMOS	CGOT
Technology Node	nm	45	45
Power Supply V_{DD}	V	1	1
Resolution	mV	50	50
DC Bias	V	0.65	0.65
Dynamic range	mV	±200	±200
Signal to Nose Ratio (SNR)	dB	20.9	20.9
Effective Number of Bits (ENOB)	bit	3.2	3.2
Max.Differential Non-linearity (DNL)	LSB	0.6	0.6
Max.Integral Non-linearity (INL)	LSB	0.32	0.32
Average Delay	ns	13.52	4.26
Average Power	μW	59.9	12.4
PDP	pJ	0.81	0.051
PDP w.r.to ternary CMOS ADC			6.3%

6.6 An Advanced Adiabatic Logic Using GOTFET Devices

Internet of Things (IoT) envisages interconnecting all relevant physical objects, both living and non-living, through a reliable communication network so as to enable a wide variety of complex monitoring and control mechanisms. RFID tags and biomedical sensors are the most critical elements in IoT [135, 136]. These sensors generally operate at low frequencies and have very limited on-board power source. Adiabatic logic circuits are ideal candidates to implement computational and memory elements of RFID and biomedical sensors as they consume significantly lower power than the corresponding static CMOS logic circuits. The Energy Saving Factor (ESF) of the adiabatic circuits may be further increased significantly, by using the proposed GOTFETs instead of the standard CMOS devices.

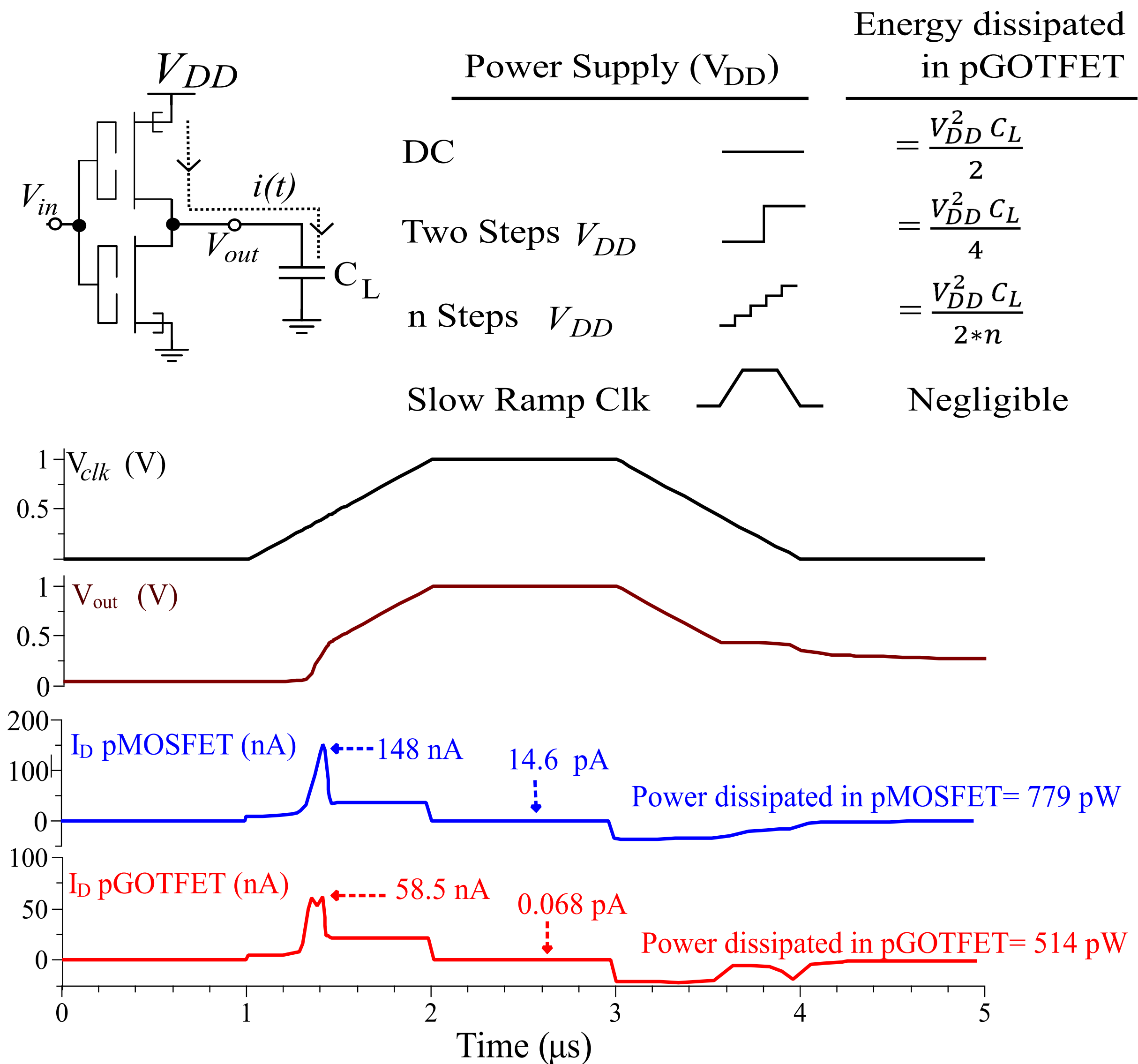


FIGURE 6.22: Performance plots of CGOT inverter in adiabatic mode.

6.6.1 Principle of Adiabatic Energy Recovery Cycle

A typical CGOT inverter is shown in Fig. 6.22 with a net capacitive load CL at the output node (including the intrinsic capacitance at the output node as well as the input and parasitics capacitances of the following stage). When the input changes from HIGH to LOW state, the output node gets charged to V_{DD} through the pGOTFET. In a conventional inverter design with constant DC power supply V_{DD}, the energy stored in the capacitor during this process is $V_{DD}^2 C_L/2$, while the energy consumed from the power source is $V_{DD}^2 C_L$,. The balance of $V_{DD}^2 C_L/2$ is dissipated as heat ($I^2 R$ loss) in the pGOTFET. If the power supply is ramped up in 2 steps, the energy dissipated in pGOTFET is reduced to $V_{DD}^2 C_L/4$ and it can be further reduced to $V_{DD}^2 C_L/2$n by ramping the power supply in n steps. Adiabatic Logic utilizes a slow ramp voltage (i.e. $n \rightarrow \infty$) instead of a standard DC supply V_{DD} [137, 138]. A low frequency ramp V_{DD} allows the output node to closely follow the power supply thus ensuring minimal voltage drop across the Pull Up Network which in turn,minimizes the power dissipation in the devices.

6.6.2 CMOS Symmetric Pass Gate Adiabatic Logic (SPGAL)

Fig.6.23 shows the schematic and performance plots of a standard CMOS SPGAL buffer. When the Clk signal is ramping up from LOW to HIGH logic states, one of the output nodes V_{out+} or V_{out-} is charged HIGH through the cross-coupled PMOSFETs M_1 or M_2. The complementary input signals are fed to nMOSFETs M_3 and M_4 ensuring that only the desired output node among V_{out+} and V_{out-} is charged HIGH when Clk goes HIGH. However, when Clk retreats back to LOW, the charge accumulated at the output nodes V_{out+} or V_{out-} is discharged back to the power supply through transistors M_1 or M_2 which have interchanged its source & drain terminals for the energy recovery phase. As a consequence of swapping terminals, the current during the energy recovery phase in performance plot (Fig. 6.23b) appears negative. Resonant energy recovery clock circuits [139, 140] can be used to harvest this energy and significantly reduce the power consumption of the circuit.

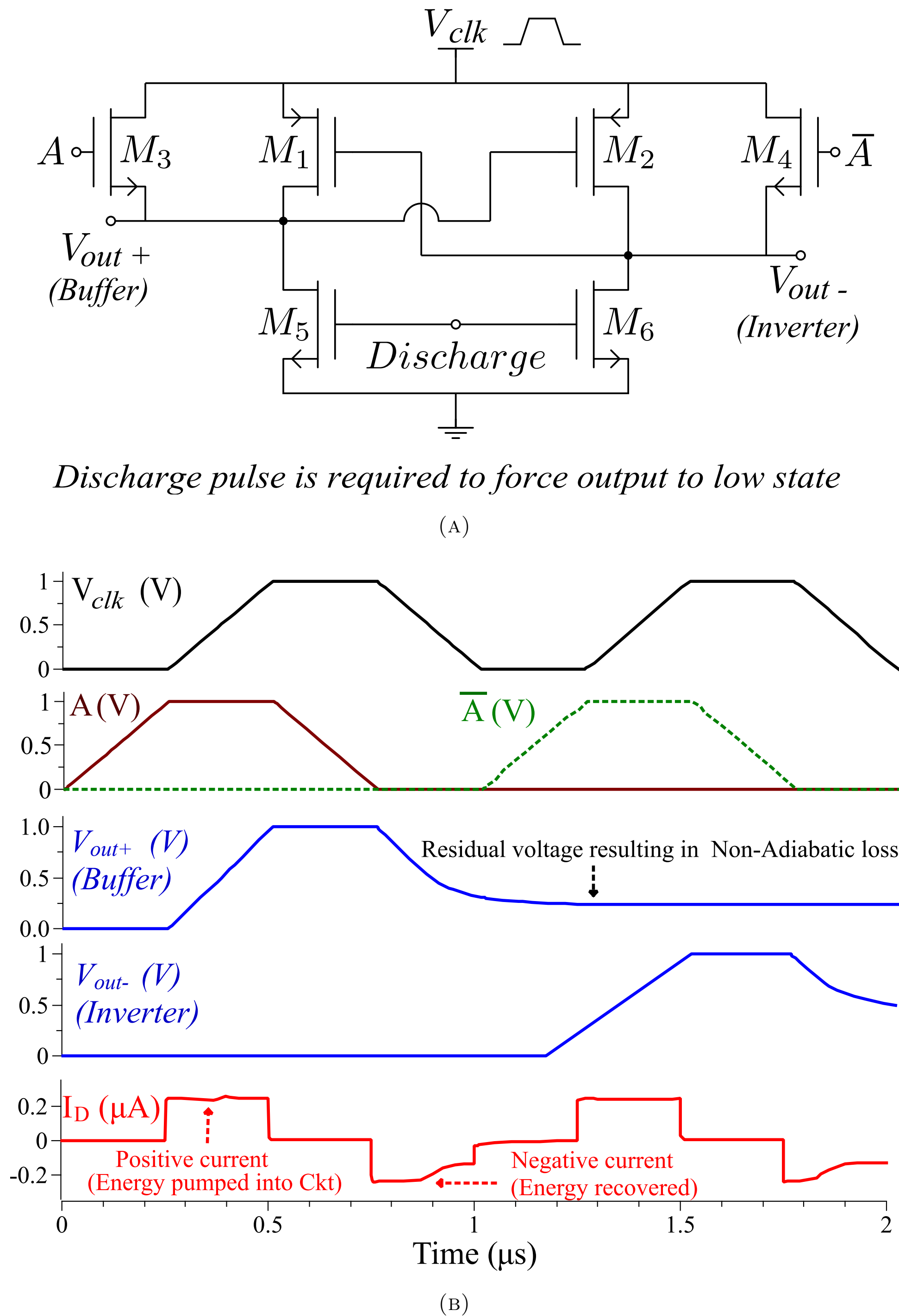


FIGURE 6.23: (a) Schematic and (b) performance plots of CMOS SPGAL.

6.6.3 Limitations of CMOS SPGAL Buffer

Firstly, the threshold voltage VTp of the pMOSFETs M_1 and M_2 limits the amount of charge that can be recovered back. M_1 or M_2 would conduct charge back to the clock only as along as the voltage at output nodes $|V_{out-}|$ or $|V_{out+}|$ is above $|V_{Tp}|$ of the corresponding pMOSFET.

This results in a residual voltage of around 0.4-0.45 V at the output nodes even when the Clk signal is LOW. Secondly, an additional Discharge signal must be applied at the gates of nMOSFETs M_5 or M_6 to reset the output nodes to their LOW state as illustrated in Fig. 6.23a. This unnecessarily complicates the circuit with additional resetting clock circuitry.

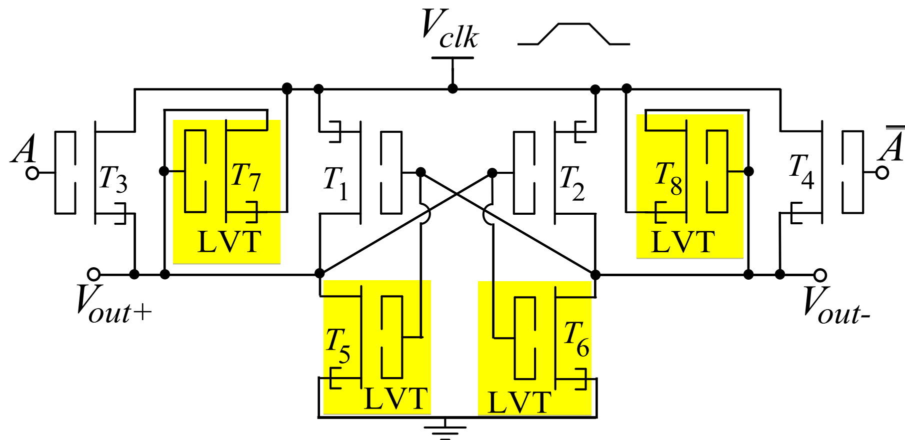
6.6.4 GOTFET Adiabatic Logic (GOTAL)

6.6.4.1 Advantages of CGOT Over CMOS for Adiabatic Logic

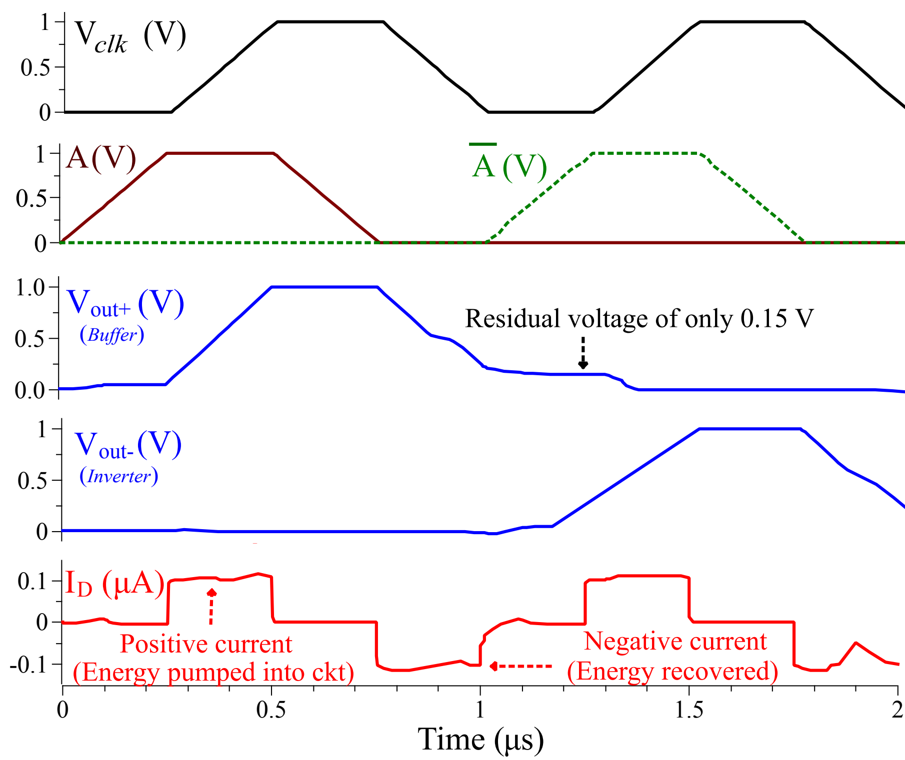
As the power supply signal retreats back, the charge on the output nodes are driven back to the power supply. The energy pumped back from the circuit during retreating power supply signal can be harvested by using specially designed resonant energy recovery clock circuits [139, 140]. Proposed GOTFETs having at least one order lower I_{OFF} and almost double the I_{ON} currents than analogous MOSFETs at the same technology node and same width are ideal replacement for MOSFETs in adiabatic circuits. Comparative performance plots for the CGOT vs. CMOS adiabatic inverters/buffers, with a slow V_{Clk} replacing V_{DD} as the power clock supply, along with LOW logic applied at the input are shown in Fig. 6.22. The static leakage current in CGOT inverter with V_{Clk} at HIGH logic state is 0.06 pA which is barely 0.41% of the analogous CMOS inverter which has a corresponding static leakage current of 14.6 pA. Higher I_{ON} of GOTFETs and lower channel resistance results in the output voltage closely following V_{Clk}, which in-turn results in lower power dissipation in the pGOTFETs (514 pW) than the corresponding pMOSFETs (779 pW) in CMOS inverter.

The schematic of the proposed GOTFET Adiabatic Logic (GOTAL) inverter/buffer and its characteristic performance are depicted in Figs. 6.24a & 6.24b respectively. GOTAL is a significant improvement over the SPGAL topology. The novelty in GOTAL topology is the usage of diode connected LVT nGOTFETs T_7 & T_8 for reducing the non-adiabatic losses and cross-coupled LVT nGOTFETs T_5 & T_6 to eliminate the requirement of the Discharge pulse. This circuit also uses complementary input and output structure like SPGAL.

6.6.4.2 GOTAL Inverter/Buffer

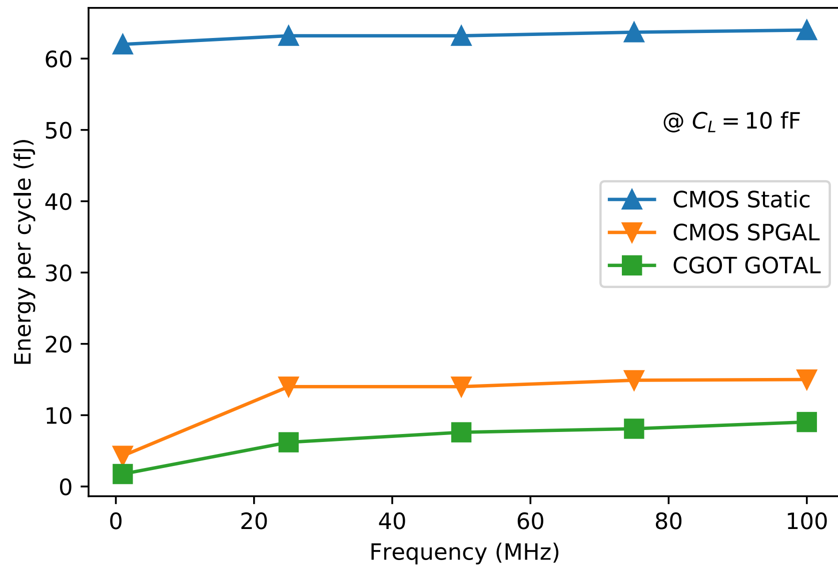


(A)

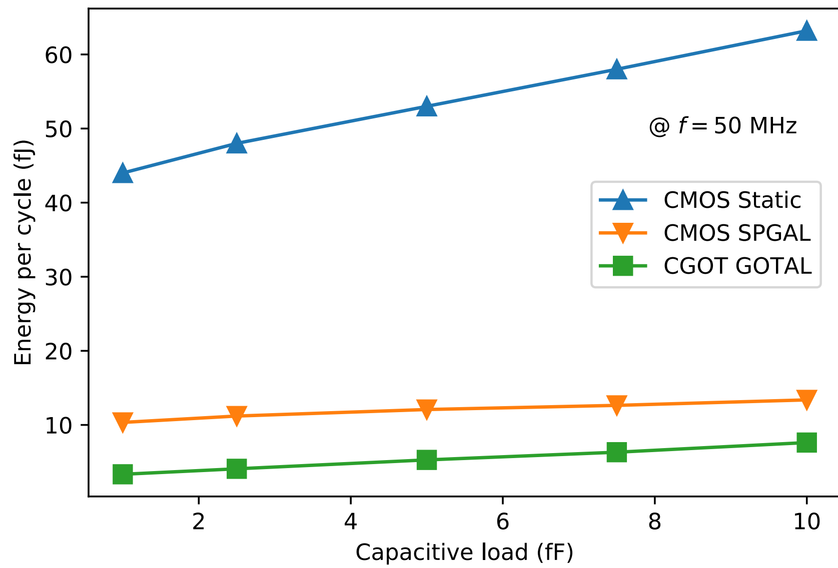


(B)

FIGURE 6.24: (a) Schematic and (b) performance plots of GOTAL inverter/buffer



(a)

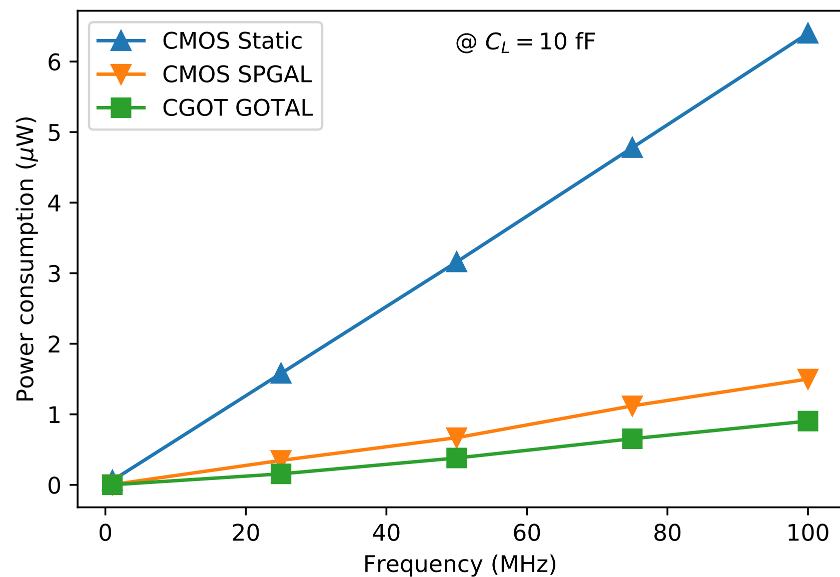


(b)

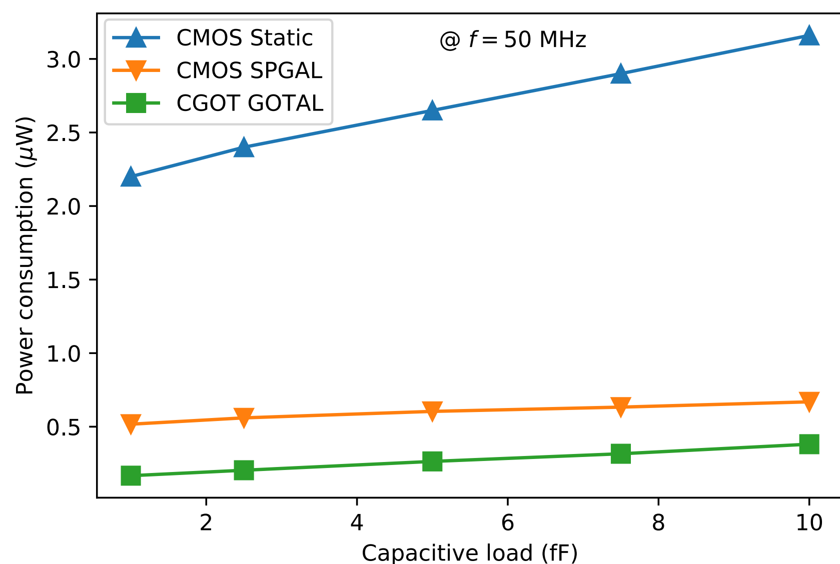
Figure 6.25: Variation of the energy consumed from the power clock per cycle in GOTAL inverter/buffer circuit with (a) power clock frequency under a capacitive load of 10 fF and (b) capacitive load at 50 MHz power clock frequency.

When Clk retreats back, the charge accumulated at the output nodes V_{out+} or V_{out-} is discharged back to the power supply not only through transistors M_1 or M_2 but also through the diode connected LVT nGOTFETs T_7 or T_8. Having V_t approximately 100 mV lower than the pGOTFETs T_1 or T_2, the LVT nGOTFETs T_7 or T_8 turns ON before T_1 or T_2 , ensuring higher

current resulting in greater charge recovery. The residual voltage is only 0.15 V at 1 MHz and 0.32 V at 100 MHz.



(A)



(B)

FIGURE 6.26: Variation of the power consumed in GOTAL inverter/buffer circuit with (a) power clock frequency under a capacitive load of 10 fF and (b) capacitive load at 50 MHz power clock frequency.

This low residual voltage is not likely to adversely affect the following stage of the circuit. The LVT nGOTFETs T_5 and T_6 help in clamping the complementary output node to zero during charging phase. If the input A is HIGH, V_{out+} is charged to HIGH when Clk goes HIGH. As V_{out+}

gets charged, LVT nGOTFET T6 clamps the complementary output node output node V_{out-} to zero, discharging any residual voltage, however low, accumulated during the previous cycle. The low residual voltage and LVT nGOTFETs T_5 or T_6 completely eliminates the requirement of Discharge pulse from an additional resetting clock circuitry.

Comparison of energy consumed per cycle for frequency range 1-100 MHz and the effect of change in load capacitance from 1 fF to 10 fF at 50 MHz frequency with respect to static CMOS design and CMOS SPGAL are shown in Fig. 6.25a & 6.25b respectively. GOTAL circuits are extremely power-efficient for low frequency VLSI sensor applications. The comparison of the power consumption in GOTFET Adiabatic Logic (GOTAL) for frequency range 1-100 MHz and effect of change in load capacitance from 1 fF to 10 fF at 50 MHz frequency with respect to static CMOS design and CMOS SPGAL are shown in Figs. 6.26a & 6.26b respectively.

6.6.5 Conclusions

In this chapter, we have implemented the digital circuits using GOTFET, and their performance parameters were benchmarked with a 45nm technology node. It has been demonstrated that the optimized GOTFET-based digital gates like inverter, NAND, NOR, and XOR consume significantly lower power compared to CMOS circuits and operate faster than the CMOS circuits. Compared to the corresponding CMOS-based digital circuits, a 98-99% reduction in PDP has been observed in CGOT digital circuits. A conventional dynamic comparator designed using the proposed CGOT paradigm in this chapter exhibits 93 ps (25%) lower delay than similar CMOS designs and consumes merely 1.11 pW (99% lower than CMOS) of static power. The overall PDP in the CGOT comparator design has been shown to be only 0.5% of the PDP of a conventional CMOS comparator. The overall PDP in the proposed CGOT regenerative-latch-based Schmitt trigger has been demonstrated to be merely 1.9% (98.1% lower than) of the PDP in the corresponding conventional CMOS design. A conventional DFA designed using the proposed CGOT paradigm in this chapter exhibits 100 ps (40%) lower & 50 ps (30%) delays for the sum and carry signals than similar CMOS designs. Furthermore, the CGOT DFA consumes merely 2.6 pW (99% lower than CMOS) of static power. The overall PDP in the proposed CGOT improved DFA design has been 0.9% of the PDP of a conventional CMOS DFA. The overall PDP in the proposed CGOT regenerative-latch-based Schmitt trigger has been demonstrated to be merely 1.9% (98.1% lower than) of the PDP in the corresponding conventional CMOS design. A novel ADC design is proposed in this chapter, which requires only 48 transistors to encode the

comparator outputs into the 2-bit ternary data which is significantly lower than the 70 transistors necessary for the 2-bit ternary ash ADC designs reported earlier. The overall PDP in the proposed in CGOT based ADC decrease to be 99.7% (two orders lower) than the corresponding CMOS design. GOTFET-based advanced Adiabatic Logic presented in this work consumes up to 67% lower power than the equivalent CMOS-based Symmetric Pass Gate Adiabatic Logic, the most power-efficient adiabatic topology reported in recent literature. GOTFET-based Adiabatic inverter consumes up to two orders (97%) lower power than the conventional static CMOS circuits at the same frequencies of operation under the same capacitive loads.

6.7 Publications Based on This Chapter

Journals

1. S. Vidhyadharan, Ramakant Yadav, **S. Hariprasad**, and S. S. Dan, “A Nanoscale Gate-Overlap Tunnel FET (GOTFET) Based Improved Double-Tail Dynamic Comparator for Ultra-Low-Power VLSI Applications”, Springer Analog Integrated Circuits and Signal Processing, Vol.101, pp-109-117, 2019. DOI:10.1007/ s10470-019-01487-x.

2. S. Vidhyadharan, S. S. Dan, Ramakant Yadav, and **S. Hariprasad**, ”A Novel Ultra-Low Power Gate-Overlap Tunnel FET (GOTFET) Dynamic Adder”, Taylor and Francis International Journal of Electronics, vol. 107, no. 10, pp. 1663-1681, Mar 2020. DOI:10.1080/00207217.2020.1740800.

3. S. Vidhyadharan, S. S. Dan, Ramakant Yadav, and **S. Hariprasad**, “An Innovative Ultra-Low Voltage GOTFET based Regenerative-Latch Schmitt Trigger”, Elsevier Microelectronics Journal, vol. 104, p. 104879, Oct 2020. DOI:10.1016/j.mejo.2020.104879.

4. S. Vidhyadharan, S. S. Dan, Abhay S,V, Ramakant Yadav, and **S. Hariprasad**, “Novel Gate-Overlap Tunnel FET based Innovative Ultra-Low Power Ternary Flash ADC”, Elsevier Integration, the VLSI Journal, vol. 73, pp. 101-113, Jul 2020. DOI:10.1016/j.vlsi.2020.03.006

5. S. Vidhyadharan, Ramakant Yadav, **S. Hariprasad**, and S. S. Dan, “An advanced adiabatic logic using Gate Overlap Tunnel FET (GOTFET) devices for ultra-low power VLSI sensor applications”, Springer Analog Integrated Circuits and Signal Processing, 2019. DOI: 10.1007/s10470-019-01561-4.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

This thesis proposes different TFET devices for analog, digital, and ternary logic applications. DGLTFET devices proposed in this work have twice the transconductance g_m, at least two orders higher output resistance r_o and at least two orders higher overall intrinsic gain $g_m r_o$ compared to an equivalent MOSFET with the same width and technology node. Proposed LTFETs provide higher output resistance r_o and higher pinch-off V_{DSsat}, leading to a lower saturation region in the $I_D - V_{DS}$ characteristics for analog applications. Improvement of the $g_m r_o$, a thin epitaxial (epi-) layer is sandwiched between the gate and the source regions to enable line tunneling. This work explained the effect of t_{ep} and n_{ep} on analog performance in DGLTFET devices. In this thesis work, we have shown the device and circuit methodology to design the DGLTFET-based circuits. For this work, device simulations have been performed in Synopsys TCAD tools, and circuit simulations have been done using behavioral Verilog A models in Industry standard Cadence EDA tools. We have designed a few analog circuits, benchmarking their performance with the CMOS technology node. The AC gain of CS amplifier-based DGLTFET devices with resistive load provides 8 dB higher than MOSFET technology. Similarly, the AC gain of cascode CS amplifier-based DGLTFET devices is 30 dB higher than MOSFETs. The DGLTFET-based current mirror circuits provide superior I_{out} saturation characteristics due to the negligible channel length modulation effect in the DGLTFET than the MOSFETs. Furthermore, the output resistance R_{out} of the DGLTFET is approximately three orders higher than the MOSFETs. The two-stage op-amp implemented with the DGLTFET yields 23.5 dB higher CMRR compared to the MOSFET-based design.

This thesis described the impact of L_{ov} in VLTFET devices on the analog circuit performance. We observed a significant increase in gain in the CS amplifier by changing the L_{ov} parameter over the width. Also, we observed that improvement in R_{out} in the cascode current mirror circuit using these devices. We concluded that L_{ov} place a significant role in addition to width in analog circuits.

Innovative Gate-Overlap Tunnel FET (GOTFET) devices are also proposed for high-speed operation and minimum static leakage in ultra-low-power digital applications. The GOTFETs proposed for ultra-low-power circuits have I_{off} at least an order of magnitude lower, while I_{on} is roughly double that of an equally sized standard MOSFET at the same 45 nm technology node. The higher I_{on} makes the circuits more robust with improved performance, while lower I_{off} leads to a significant reduction in static (leakage) power dissipation.

For the first time, innovative low and high-threshold GOTFET devices have been reported for ternary logic applications. These devices are designed so that the low and high threshold voltages (LVT & HVT) are $V_{DD}/3$ and $2V_{DD}/3$, respectively. The most exciting feature of the proposed GOTFET is that, in the same device structure, just by changing the material and doping parameters, we can get the optimal performance of LVT & HVT pGOTFETs. Proposed LVT & HVT GOTFETs have on-currents (I_{on}) roughly twice and off-currents (I_{off}) at least an order of magnitude lower than the corresponding MOSFETs. This work also presents dual-threshold GOTFETs giving both LVT & HVT characteristics by simply altering their terminal connections in the same device instead of the dedicated devices.

Finally, Ultra-Low-Power digital and analog circuits based on proposed GOTFET devices have been benchmarked with the same circuit using industry-standard 45 nm CMOS devices. We have benchmarked the standard digital gates, double tail comparator, Dynamic Full Adder, Schmitt Trigger, Ternary Flash ADC circuits, and advanced Adiabatic Logic circuits. Proposed GOTFETs-based digital circuits outperform similar CMOS designs in both aspects of operating speed and power consumption.

7.2 Future Work

Chapter 4 shows the performance improvement in CS amplifier and current mirror circuits with the change in L_{ov}.There is further scope also for significant improvement in designing the complex analog circuits with L_{ov} parameter in addition to the width parameter.

In this work, we have used the third derivative method for threshold voltage extraction. A compact analytical model for threshold voltage extraction can be developed in the future.

A compact SPICE model is also being developed to enable faster and easier simulation of TFET-based more, complex analog and digital circuits. Noise model and temperature dependence factors need to be incorporated in the SPICE model to enable RF analog circuit design with TFETs.

Ferroelectric materials stacked between the gate and oxide layer forms negative capacitance. These materials would be significantly improve the I_{on}, as well as g_m in TFET devices.

Chapter 8

Summary

Energy efficiency limit has become the main obstacle for power-constrained applications using the conventional silicon complementary metal-oxide-semiconductor (CMOS) technology. In particular, the supply voltage scaling has slowed down in the past few technology generations due to the 60 mV/decade fundamental limit for on-off switching in MOSFETs, which prevents the reduction of the energy per operation in today's circuits and systems. To mitigate this challenge, Tunnel FETs or TFETs are envisioned as a viable alternative to achieve the steep on-off switching (SS<60 mV/dec) at low supply voltages and fabrication process, which is compatible with CMOS technology. Gate-controlled BtB tunneling phenomena enable the switching in TFETs at the source channel p-n junction.Tunnel FETs, which are gated PIN diodes whose on current I_{on} arises from band-to-band tunneling, are desirable for ultra-low power applications due to their low off current I_{off} and reduced inverse Sub-threshold Slope SS. Furthermore, a fundamental disadvantage of TFETs is that their ON-state current is significantly lower than that of MOSFETs.

This thesis proposes different types of TFETs for digital, analog, and ternary logic applications. The first DGLTFET device has been optimized such that device characteristics are superior to equally sized 45 nm MOSFETs for analog applications. TFETs show excellent current saturation characteristics and negligible channel length modulation effect, which is detrimental in MOSFETs, especially at lower technology nodes. As a result, output resistance r_o in the saturation region is a high order of 10^6 Ohms. In the proposed TFETs, vertical BtB tunneling has been used compared to point tunneling in conventional TFETs given a more BtB generation rate, which improves I_{on} as well as g_m. DGLTFET has thrice the on currents I_{on}, at least one

order lower off currents I_{off}, twice the transconductance g_m, at least two orders higher output resistance r_o, and at least two orders higher overall intrinsic gain $g_m r_o$ than the equivalent metal oxide- semiconductor field-effect transistor (MOSFET) having the same width at the same technology node. Device optimization has been carried out by studying the impact of various device parameters and dimensions on performance. In this work, we have optimized the DGLTFET device by changing critical parameters like the epi-layer thickness t_{ep} and its doping concentration n_{ep}, which seriously influence the line-tunneling behavior. Optimizing the critical parameters for enhanced line-tunneling leads to improved analog performance parameters like g_m , r_o, and, finally, superior analog circuits.

We have compared the performance of the proposed devices with the TFETs reported earlier in the literature and the standard 45 nm MOSFETs. TFET characteristics were simulated using synopsys® TCAD tools, while circuit performance was benchmarked with the standard 45 nm CMOS library using cadence® EDA tools. The performance of the DGLTFET was benchmarked with the equivalent MOSFET in fundamental analog VLSI circuits, namely, Common Source CS amplifier (resistive and cascade loads), current mirror (single-stage and cascode configurations), and a two-stage op-amp. The AC gain of cascode CS amplifier based DGLTFET devices is observed to be 30 dB higher gain compared with MOSFETs. DGLTFET CS amplifier has a gain-BW product or unity-gain BW f_T of 15 GHz, while the MOSFET CS amplifier with the same bias current is 10 GHz. The DGLTFET current mirror has at least three orders of magnitude higher output resistance R_{out} than the corresponding MOSFET current mirror. Similarly, the common-mode rejection ratio (CMRR) of the DGLTFET op-amp is 57 dB compared to the CMRR of 33.5 dB of the equivalent design in the standard 45-nm complementary metal-oxide semiconductor(CMOS) technology.

Vertically grown TFETs are preferred as they allow the integration of more TFETs on a single chip, increasing device density. This thesis work presents a Vertical Line-Tunneling FET (VLTFET) optimized for superior performance in analog applications. The saturation mechanism, DC, and small-signal behaviors are physically explained with the help of energy band diagrams, electron density, and tunneling width parameters. VLTFET has higher output resistance r_o owing to the independence of the drain bias on the band-to-band (BtB) generation. Increasing the source-gate overlap length L_{ov} from 0.1 μm to 0.5 μm triples the transconductance g_m, maintaining r_o constant, resulting in thrice the intrinsic gain A_{vo}. In analog circuits using conventional MOSFETs, g_m increases and r_o decreases with increasing width W. On the other hand, in analog circuits using VLTFETs, A_{vo} can be enhanced by increasing L_{ov} which increases

g_m without affecting r_o. Unity-gain BW f_T (or the GBW product) is dominated by the relative change in the overall gate capacitance C_{GG} and g_m due to change in L_{ov}, since both g_m and C_{GG} are proportional to L_{ov}. However, in analog circuits with realistic capacitive loads, f_T rapidly increases with L_{ov}. VLTFET-based cascode CS amplifiers provide a 10 dB increment in its gain as L_{ov} is increased from 30 nm to 100 nm. Similarly, a VLTFET-based cascode current mirror shows a theoretical output resistance R_{out} in the order of 10^{11} Ω, behaving as an ideal current mirror/source.

In this thesis, we have proposed GOTFETs for prospective digital applications . Its on-state currents I_{on} at least twice ($I_{on,GOT} \geq 2I_{on,MOS}$) with off-state currents I_{off} remaining at least an order of magnitude lower ($I_{off,GOT} \leq 0.1 I_{off,MOS}$), than the corresponding equally-sized MOSFETs at the same 45 nm technology node. The proposed GOTFET designs are targeted for higher I_{on} leading to high-speed operation and lower I_{off} to minimize static leakage in ultra-low-power digital applications. This work further modified the GOTFETs for low and high threshold transistors (LVT & HVT) for ternary logic applications. These devices are designed in such a way that the low and high threshold voltages (V_{tn} & V_{th}) are $V_{DD}/3$ and $2V_{DD}/3$ respectively, with the ranges $\{0$ to $V_{DD}/3\}$, $\{V_{DD}/3$ to $2V_{DD}/3\}$ & $\{2V_{DD}/3$ to $V_{DD}\}$ representing the three logic states 0, 1 & 2 respectively. Proposed LVT & HVT TFETs have on currents (I_{on}) roughly twice and off currents (I_{off}) at least an order of magnitude lower than the corresponding MOSFETs. Dual threshold GOTFETs proposed in this work use single devices by altering their terminal connections.

Along with analog circuits, this thesis shows the performance of GOTFETs-based digital circuits. Proposed GOTFETs outperform similar CMOS designs in both aspects of the speed of operation and power consumption. This work proposes the GOTFET-based basic building blocks of digital circuits like an improved double tail comparator, ultra-low-power dynamic adder, an ultra-low voltage Schmitt trigger, and ultra-low-power ternary flash ADC circuits. The proposed circuit-level modifications in this Complementary GOTFET (CGOT) circuits have not only resulted in significantly lower static power due to TFET technology but also helped achieve faster circuit operation (lower delays) than the corresponding CMOS circuits. The overall Power Delay Product (PDP) in the proposed improved GOTFET-based circuits is only 1-5% of the PDP of the corresponding conventional CMOS-based circuits.

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