Design Exploration of Low Power Arithmetic and SRAM circuits using Subthreshold Design technique

THESIS

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By

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CERTIFICATE

This is to certify that the thesis entitled "**Design Exploration of Low Power Arithmetic and SRAM circuits using Subthreshold Design technique"** submitted by **Ms. Priya Gupta,** ID No **2011PHXF416P** for award of Ph.D. of the Institute embodies original work done by her under our supervision.

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ABSTRACT

Complete analyses of the arithmetic circuits and SRAM cells used for above-threshold operation have never been examined in the context of sub-threshold operation. The conventional arithmetic circuits and SRAM cells may not work in sub-threshold region at nanometer technologies due to ultra-low supply voltage.

This thesis work presents new functional designs and design space exploration for arithmetic circuits and SRAM cells in sub-threshold region. Exploration includes three parallel prefix adder architectures, two column compression multipliers and Static Random Access Memory (SRAM) cells, with transistor count ranging from 6 to 12, in terms of power consumption, propagation delay, and power-delay product. Their performance is also obtained at 45 nm and 180 nm technology nodes to find the impact of scaling on their performance. The work has been carried out in three parts.

In the first part, three power efficient parallel prefix adders namely Carry look-ahead adder (CLA), Kogge-Stone adder (KSA) and Han-Carlson adder (HCA) architectures are selected as per literature survey. These architectures are designed, simulated and analyzed, in sub-threshold region, with three different logic design styles namely Static-CMOS, Hybrid Pass Transistor (Hybrid PT), and Hybrid Transmission Gate (Hybrid TG) for operand sizes of 8, 16, 32 and 64 bits. At 45 nm technology, it is observed that in comparison among themselves of all three selected adder architectures, HCA is the most power efficient, and CLA is the high-speed adder architecture in sub-threshold region. In contrast to worst (maximum) value obtained, HCA shows 96.8% lesser power consumption, CLA shows 79.8% lesser propagation delay and KSA shows 63.7% lesser power-delay product. Reverse body bias technique in Static-CMOS logic only leads to functional circuits with 61.87% reduction in propagation delay but with the increments in average power consumption and power-delay product by 77.03% and 38.3%respectively. Same trend of power consumption, delay and power-delay product for all the adder architectures is observed at 180 nm technology.

In the second part, two power efficient column compression multipliers namely Wallace tree and Dadda are selected as per literature survey. Total sixteen new designs of these architectures have been developed using two different partial product accumulation schemes namely using lower order compressors (LOC) and Mixed lower and higher order compressors (Mixed L/H). These designs are developed with two logic design styles (Static-CMOS &

HYB-TG) for two sizes (4x4 & 8x8) at two technology nodes (45 nm & 180 nm) in sub-threshold region.

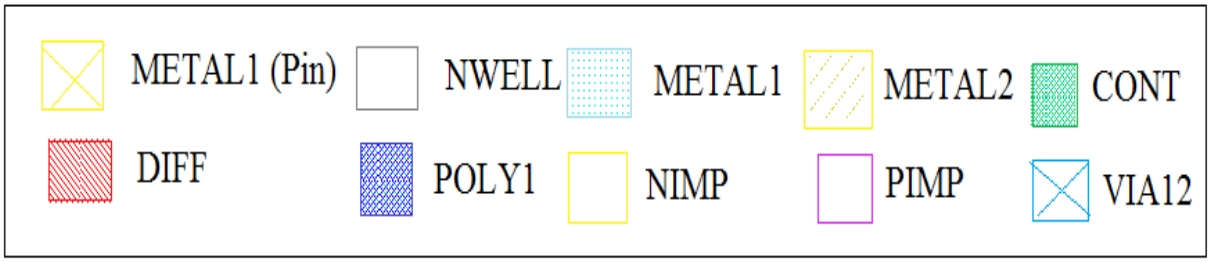
At 45 nm, among all eight multipliers implemented, Dadda-45-L/H-HCA has the least power-delay product. It has 49% (for 4x4-bit), and 31.5% (for 8x8-bit) lesser power-delay product in comparison to highest power-delay product obtained. Static-CMOS logic and HYB-TG design style are most power-delay product efficient design styles for LOC and Mixed L/H based multipliers respectively. Same trend of power-delay product is observed at 180 nm technology.

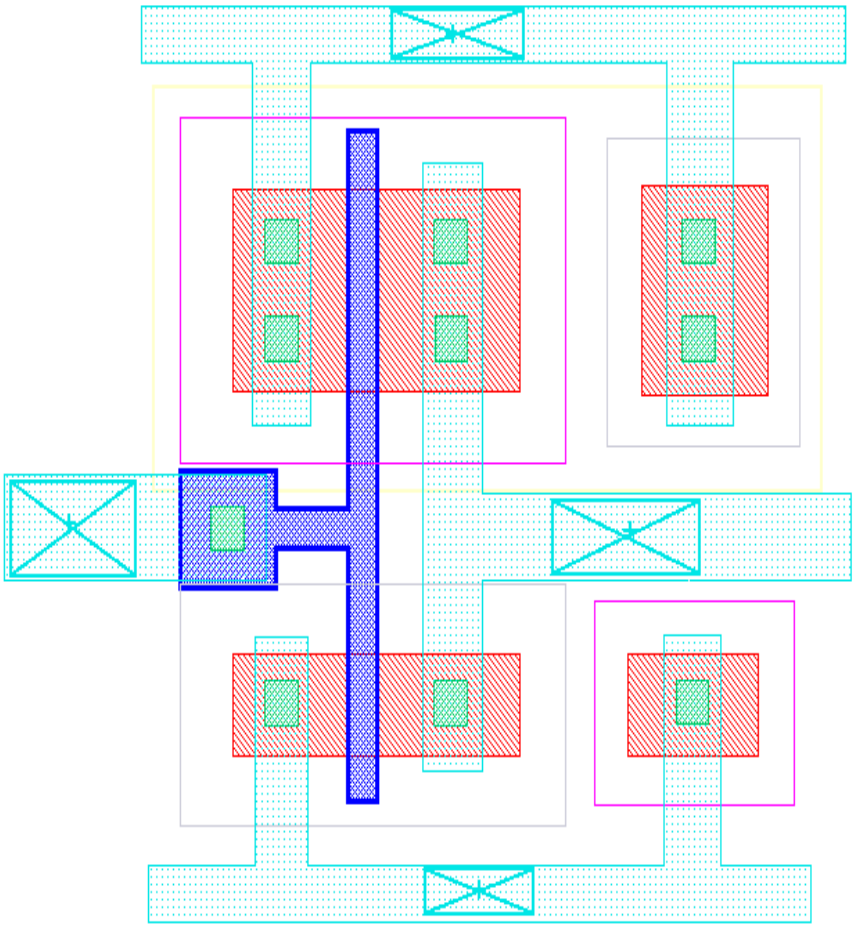
At 45 nm, the power consumption is higher than 180 nm technology for all adders and multiplier designs. The power consumption is increasing due to increments in the leakage current at 45 nm technology as compared to 180 nm technology since supply voltage is kept same at 0.4V.

In the third part, for sub-threshold operation at 45 nm technology, five new designs of SRAM cells have been proposed with 7, 8, 9 and 12 transistor configurations at 0.4V power supply. Cell stability analysis is done using standard measures like hold/ read/ writes static noise margins as well as N-curve cell stability metrics. For performance analysis, read/write delay and leakage power consumption in hold mode are considered. The results show improvement in all the design parameters over other published designs and conventional 6 transistor (6T) SRAM cell. The comparison of proposed designs among themselves exhibit that three new designs namely M8T, MPT8T and MI-12T have low leakage power consumption along with other improved design parameters such as high read stability, high write ability, fast read & write operation. Thus, these designs can be an attractive choice for low power application. In comparison to results of published designs at 180nm, all proposed designs show improvement in read stability, write ability, read delay and write delay but with increment in leakage power consumption in hold mode.

LAYOUT TEMPLATE

Layer Information:





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LIST OF ABBREVIATIONS

Si: Silicon
DIBL: Drain induced barrier lowering
SCE: Short channel effect
MAC: Multiply and Accumulator
LSB: Least Significant Bit
MSB: Most Significant Bit
PDP: Power-delay Product
WSN: Wireless sensor network
CSA: Carry save adder
CLA: Carry look-ahead adder
KSA: Kogge-Stone adder
HCA: Han-Carlson Adder
PP: Partial product
FA: Full Adder
HA: Half Adder
VLSI: Very large scale integration
MOS: Metal oxide semiconductor
SNM: Static noise margin
RSNM: Read static noise margin
WSNM: Write static noise margin
SRAM: Static random access memory
LOC: Lower order compressor
WTI: Write trip current
SINM: Static current noise margin
SVNM: Static voltage noise margin

CHAPTER 1
INTRODUCTION

1.1. BACKGROUND

Efficient power management has become a critical constraint with the rapid growth of portable, wireless and battery-operated applications. Higher power consumption increases the on-chip temperature which results in reduced operating life of the chip and battery life [1][2][3][4]. It is observed that in present scenario more than 50% power consumption occurs due to leakage current of the entire VLSI chip [5]. To overcome this leakage current problem, number of low power based design techniques like multi-threshold voltage technique, power gating schemes, back (substrate) bias scheme, sub-threshold design technique etc. have been investigated and explored by many researchers. Out of the different potential alternatives, sub-threshold technique has been found to be one of the most useful technique to obtain the ultra-low power consumption, which utilizes leakage current as main conduction current. In sub-threshold circuits, the power supply voltage (V_{DD}) is reduced below the threshold voltage (V_{th}) of metal oxide semiconductor (MOS) transistor i.e. ($V_{DD} < V_{th}$). Sub-threshold circuit manages to satisfy the ultralow power requirement due to the quadratic reduction in power with respect to the supply voltage [6].

The increasing demand of smaller, lighter and more durable low power electronic products highlights the importance of sub-threshold design technique. Sub-threshold circuits are promising for applications where performance can be scarified for low power. Some of applications are wireless sensor networks, electronic watch, radio frequency identification (RFID), cryptographic applications like electronic passport (where security and power consumption rather than performance are given high priority), battery operated applications (implantable biomedical devices), and other portable communication devices. These applications need ultra-low power consumption with medium performance of operation (e.g. tens to hundreds of MHz) [7][8][9].

Automatic supply and body biasing controller [10] has been developed to minimize total active power in digital circuits by dynamically adjusting both threshold voltage and supply voltage based on circuit operating conditions such as temperature, workload, or circuit architecture.

In system on chip (SOC) architectures, embedded cache memories and arithmetic circuits may occupy more than 90% of the total die area [11]. In the arithmetic circuits, adders and multipliers used in the MAC unit are the major power consuming units. Here, the sub-threshold design approaches appear to be suitable for low power/low energy application. Possibilities of making changes in the digital arithmetic circuits and on chip memory cell designs exists which can lead to many new efficient designs. This reflects the great need of the study and exploration of the alternative methods of efficient sub-threshold logic design.

1.2. SUB-THRESHOLD OPERATION

1.2.1. MOSFET in Sub-Threshold Region

The cross-sectional view of an n-channel MOSFET is shown in Figure 1.1 [12].

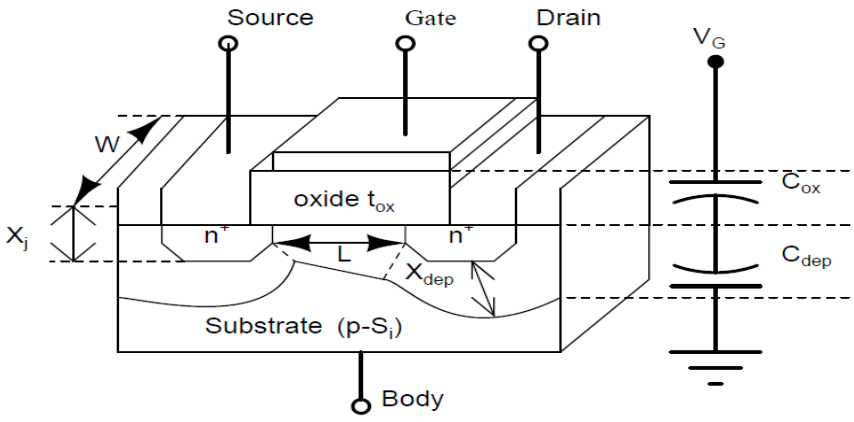

Figure 1.1: A cross-sectional view of an n-channel MOSFET

In the gradual channel approximation for n-channel MOS structures, the drain current is considered to zero if the gate to source voltage (V_{GS}) is less than the V_{th}, i.e. when $V_{GS} \leq V_{th}$.

However, in practical aspects, the drain current is present due to minority charge carriers available at the surface under the gate when the gate voltage is less than threshold, i.e. in 'sub-threshold' region. This population of mobile electrons under the gate provides a mechanism for charge flow between the drain and source even when $V_{GS} \leq V_{th}$. Thus, there is in fact a small, non-zero drain current through a MOSFET biased below threshold [13].

1.2.2. The MOSFET Drain Current in the Sub-threshold Region

Figure 1.2 shows a cross-sectional view of an n-channel MOSFET biased with a positive drain voltage i.e. $V_{DS} \geq 0$, a negative substrate voltage, i.e. $V_{BS} \leq 0$ and the gate to source V_{GS} is biased positively but below threshold voltage V_{th}.

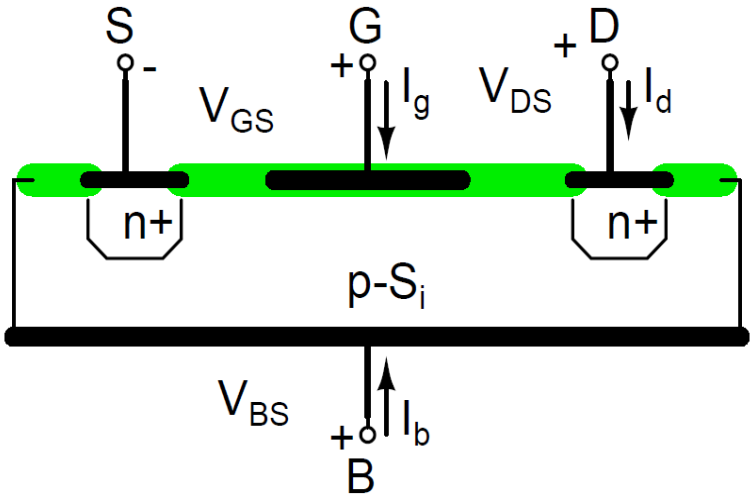

Figure 1.2: A cross-sectional view of an n-channel MOSFET operated in sub-threshold region

When the gate-to-source voltage, V_{GS}, is less than the threshold voltage, V_{th}, the semiconductor surface below the gate is a lightly doped n-channel [14] and [15]. The diffusion (due to the difference in the electron concentrations at the drain and source ends) of the thermally generated minority carriers of the substrate semiconductor material results in some conduction between the source and drain terminals through this weakly inverted channel [16]. This condition is known as weak inversion or the sub-threshold region. The off current, of a MOSFET operating in sub-threshold region, is defined here as the current flowing through the MOSFET transistor when its gate-to-source voltage, $V_{GS,}$ is equal to 0 V.

The sub-threshold drain current of n-channel MOSFET under ($V_{GS} \leq V_{th}$) is given by Eq. (1.1). It shows that sub-threshold drain current ($I_{D,\,SUB}$) is exponentially dependent on (V_{GS}-V_{th}) and it decreases with increase in V_{th} [17].

$$I_{D,SUB} = \begin{cases} I_S e^{\frac{V_{GS}-V_{th}}{nV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right), 0 \leq V_{DS} \leq 3V_T \\ I_S e^{\frac{V_{GS}-V_{th}}{nV_T}}, V_{DS} > V_T \end{cases} \quad (1.1)$$

Where I_S is the drain current when $V_{GS} = V_{th}$ and is given by Eq. (1.2).

$$I_S = \mu_0 C_{ox} \frac{W}{L} V_{th}^{\,2} (n-1) \quad (1.2)$$

The parameters in Eq. (1.1) and Eq. (1.2) are:

$\mu_{0:}$ Carrier mobility,

W: Channel width,

L: Channel length,

$C_{ox}= \varepsilon_{ox}/t_{ox}$: gate oxide capacitance (Where ε_{ox} and t_{ox} is the gate oxide dielectric constant and gate oxide thickness),

V_T: Thermal voltage (kT/q),

k: Boltzmann constant in joules per Kelvin,

T: Temperature in Kelvin,

q*:* Electronic charge in coulombs,

n*:* Sub-threshold slope factor of a long-channel uniformly doped device,

n can be calculated using following equation:

$$n = 1 + \frac{C_b}{C_g}, \text{where} \quad C_b = \frac{\varepsilon_{si}}{\omega_d} \quad \text{and} \quad C_g = \frac{\varepsilon_{ox}}{t_{ox}} \tag{1.3}$$

Where, C_g is the gate capacitance, C_b is the bulk capacitance, ε_{si} and ω_d denote the dielectric constants for silicon and depletion width under the channel respectively.

In sub-threshold operation, threshold voltage 'V_{th}' is defined as the gate-to source voltage after which the drain current ceases to depend exponentially on the gate-to-source voltage [18].

(i) $I_{D,SUB} - V_{DS}$ Characteristics

According to Eq. (1.1), sub-threshold drain current ($I_{D,SUB}$) does not depend on V_{DS} when $V_{DS} > 3V_T$ because ($e^{-3} << 1$), while at $0 \leq V_{DS} \leq 3V_T$ condition, its dependence on V_{DS} is ($1-e^{-V_{DS}/V_T}$).

The behavior of current ($I_{D,SUB}$) versus V_{DS} in the sub-threshold region is illustrated in Figure 1.3 [19].

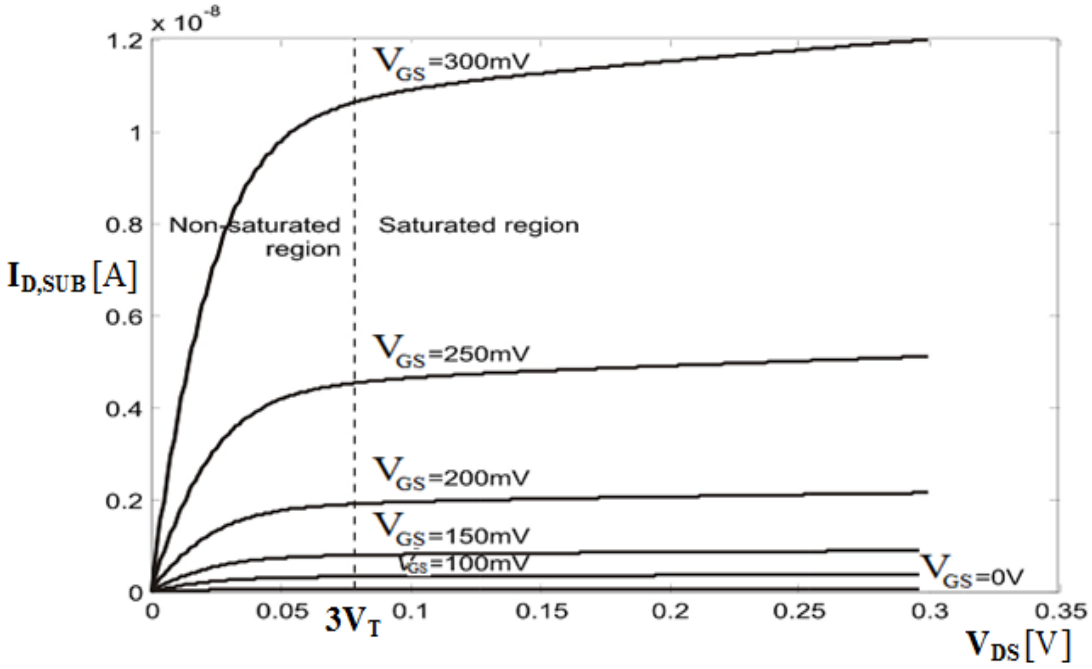

Figure 1.3: $I_{D,\,SUB} - V_{DS}$ characteristics in sub-threshold operation region

From the plot of $I_{D,\,SUB} - V_{DS}$, it is observed that MOSFET operates in non- current saturated region at below $3V_T$ and at above $3V_T$ (V_T is thermal voltage = 26mV), it operates in current saturation region.

(ii) $I_{D,\,SUB} - V_{GS}$ Characteristics

The exponential behavior of the sub-threshold drain current ($I_{D,\,SUB}$) versus V_{GS} is illustrated in Figure 1.4 [20][21].

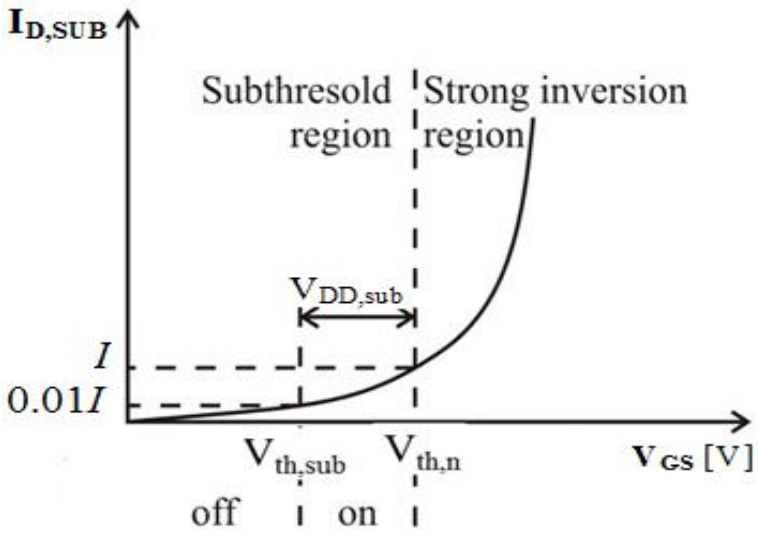

Figure 1.4: $I_{D,\,SUB}$- V_{GS} Characteristics

From the plot of $I_{D,\,SUB} - V_{GS}$, it is observed that MOSFET operates in sub-threshold region at below threshold voltage ($V_{th,n}$) and at above threshold point, it operates in strong inversion region. There are two states (off and on) in sub-threshold region. In on state, the sub-threshold current increases by tenfold and the voltage difference between the two voltage points ($V_{th,sub}$ and $V_{th,n}$) is called on state voltage range ($V_{DD,sub}$), whereas below $V_{th,sub}$ (off state), the magnitude of current is negligible.

For 45 nm / 180 nm process technologies at V_{DD} = 0.4 V, observed values are:

$V_{th,n}$ = 0.496V, $V_{th,sub}$ = 0.028 V (For 180 nm)

$V_{th,n}$ = 0.416V , $V_{th,sub}$ = 0.02 V (For 45 nm)

(iii) Sub-threshold Slope [22][23]

Sub-threshold Slope (SS) is defined as the amount of the gate voltage swing required to reduce the sub-threshold drain current by a decade. It is expressed in units (mV/decade) and is given by following equation:

$$SS \equiv \frac{dV_{GS}}{d(\ln I_{DS})} \ln 10 = \left(1 + \frac{C_{dep}}{C_{ox}}\right)\left(\frac{kT}{q}\right)\ln 10 \qquad (1.4)$$

Figure 1.5 shows the sub-threshold slope plot.

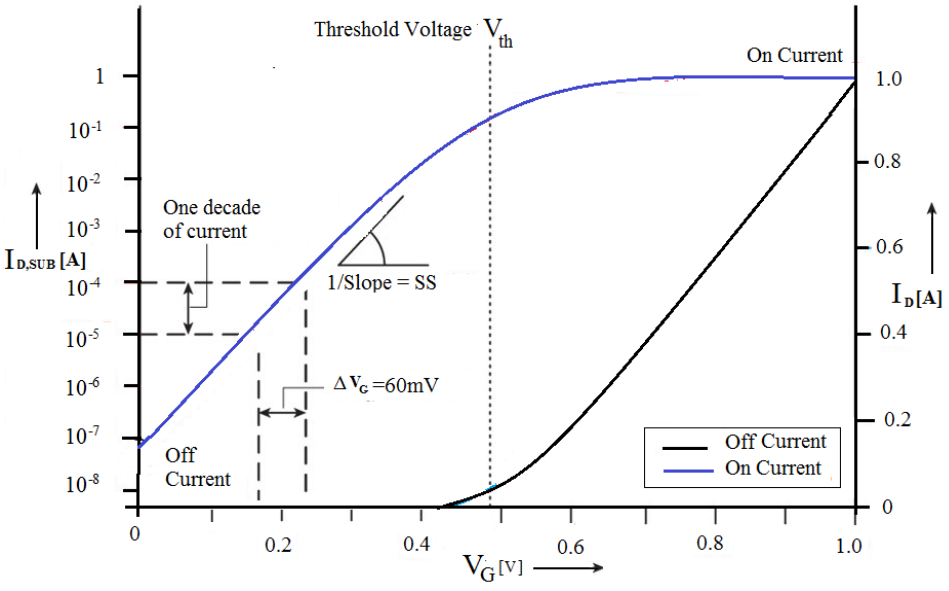

Figure 1.5: Sub-threshold slope plot at 180 nm technology

The two curves show identical data that have been plotted using a linear scale (on *y* axis, right side) and a logarithmic scale (on y axis, left side) on same plot.

When the gate voltage (V_G) is increased, the number of electrons in the channel increases. This, in turn, increases the current flowing between the source and the drain. The current at the minimum gate voltage (0 V) is called off current, and the current at the maximum gate voltage (1V in this case) is the on current. Above the threshold voltage V_{th} (dashed line), the drain current (I_D) increases linearly. Below the threshold voltage, the drain current ($I_{D,\ SUB}$) increases exponentially with the gate voltage.

In the present thesis work, sub-threshold slope value is observed as approximately 60 mV/dec for both, 45 nm / 180 nm process technologies.

1.3. SOURCES OF POWER CONSUMPTION IN CMOS LOGIC GATE

Power consumption is an important property of a design that affects feasibility, cost and reliability. It influences a greater number of critical design decisions, such as power supply capacity, the battery lifetime, supply line sizing, packaging and cooling requirements [24].

In sub-threshold region of operation, sub-threshold current is the main operating current which is otherwise considered as leakage current in strong inversion region.

The total power consumption in a CMOS circuit is constituted by dynamic, short circuit and static power consumption.

(i) Dynamic power consumption

This power consumption is due to logic transitions causing logic gates to charge/discharge output capacitances. It depends on the supply voltage, device threshold, the input rise/fall time and the operating frequency of the transistor.

Figure 1.6 shows the current flow in CMOS inverter resulting into dynamic power consumption.

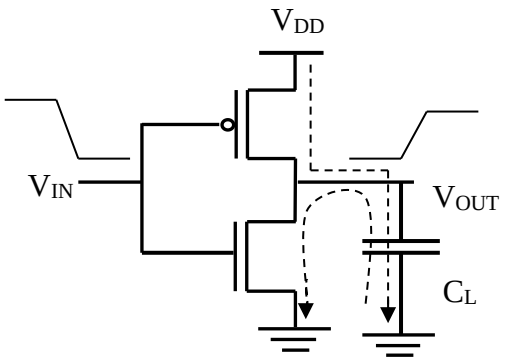

Figure 1.6: CMOS inverter mode for dynamic power consumption

The equation for dynamic power consumption is expressed as

$$P_{Dynamic} = \alpha_{0-1}.C_L.V_{DD}^2.f_{clk} \quad (1.5)$$

Where V_{DD} is the power supply voltage; C_L is the load capacitance; f_{clk} is the operating input signal frequency and α_{0-1} is the probability that a power consuming transition occurs (the activity factor).

(ii) Short-circuit power consumption

This power consumption is due to the direct current path from supply to ground when both NMOS and PMOS transistors are conducting current simultaneously for a brief duration due to non-zero rise/ fall times.

Figure 1.7 shows the current (Isc) flow in CMOS inverter causing short-circuit power consumption.

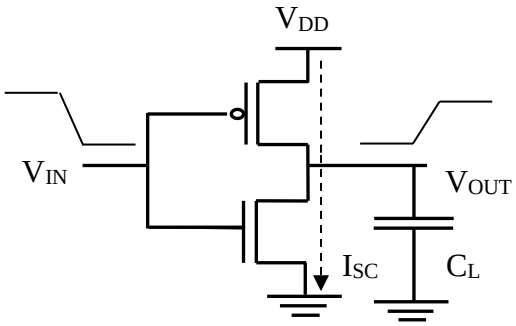

Figure 1.7: CMOS inverter mode for short-circuit power consumption

The equation for short circuit power consumption is expressed as

$$P_{shortcircuit} = I_{sc}.V_{DD} \quad (1.6)$$

Where, I_{SC} is short circuit current.

The short-circuit power consumption is the dominant component of power consumption which increases exponentially with the power-supply voltage. Reduction in the short-circuit power consumption in the sub-threshold region is achieved by reducing power supply voltage and by applying input pulses with rise/ fall time. In the present thesis, input signals have rise/ fall times of 1 pico-second, pulse width (ON time) of 1 micro-second and pulse period of 5 micro-second. [25].

(iii) Static power consumption

This power consumption occurs due to leakage current when the system is in standby mode. In sub-threshold region, the sources of leakage is the gate-oxide tunneling current that results

due to the tunneling of carriers across the very thin gate oxide [26], the edge-direct tunneling that appears between the source and drain extension, the gate overlap [27][28], the reverse currents of the source-substrate and the drain-substrate pn junctions. This power consumption does not depend on the input transition or load capacitance. It remains constant for a logic cell

Static power is expressed as

$$P_{Static} = I_{leakage} \cdot V_{DD} \tag{1.7}$$

Where $I_{leakage}$ is the leakage current as discussed above.

The total power consumption in digital CMOS circuit is the combination of the Eq. (1.5), (1.6) and (1.7), given by

$$\begin{aligned} P_{total} &= P_{dynamic} + P_{shortcircuit} + P_{static} \\ &= \alpha_{0-1}.C_L.V_{DD}^2.f_{clk} + I_{sc}.V_{DD} + I_{leakage}.V_{DD} \end{aligned} \tag{1.8}$$

During sub-threshold operation, these three components of the power consumption increase with V_{DD} but with different rates with dynamic and short-circuit power consumption increasing quadratically and exponentially with V_{DD} respectively [29]. Hence, all these components of power consumption can be reduced by reduction in power supply voltage. With technology scaling down, power consumption increases due to significant increments in the leakage current (as for CMOS inverter the leakage currents are found to be 1.05 nA and 0.18 nA at 45 nm / 180 nm technology respectively through simulation).

1.4. MOTIVATIONS AND CHALLENGES IN SUB-THRESHOLD DESIGN

In recent years, as technology of metal oxide semiconductor (MOS) transistors keeps scaling down to deep submicron region, sub-threshold region design focuses on to develop circuits operating at very low power supply voltage.

This is to support battery operated applications with very less power consumption, especially in ultra-low power application fields such as portable biosensors, wireless sensor nodes, RFID tags, hearing aids, pace-maker, wearable computing or implants, and personal digital assistants. These are dominated primarily by the need to minimize energy consumption and increase battery life time whereas speed is a secondary consideration.

To design these types of ultra-low power system, sub-threshold based SRAM and arithmetic circuits (adders and multipliers) are the basic units and the most power consuming modules [30]. Thus, it requires low power consuming memories and arithmetic circuits that are efficient with optimal performance at the same time.

Researchers have done exploration and design of Carry look-ahead adder, Kogge-Stone adder and Han-Carlson adder architectures, Wallace tree and Dadda multiplier architectures and SRAM cell designs operated in super-threshold region (gate voltage above threshold voltage region operation) using conventional Static-CMOS logic [31], transmission gate logic and pass transistor logic families. But these published architectures operation is degraded in sub-threshold region [32].

Therefore, it is important to design fully functional power efficient arithmetic and memory circuits which show least power-delay-product when operated in sub-threshold region.

Various challenges for circuit design in sub-threshold region have been discussed in the [33][34][35][36]. These mainly relate to reduced supply voltage, and device scaling as given below:

i. Exploring Logic Families for Robust Design: The current ratio I_{ON}/I_{OFF} decreases with low V_{DD} which leads to functional degradation and hence, reduces robustness of the circuits. Therefore, to design robust sub-threshold logic circuits, existing logic families need to be explored and modified.

ii. Impact of Device Scaling on circuit performance: The influence of scaling on circuits operating in the weak inversion region has been limited to device-level studies and few circuit-level simulations of simple circuits. Hence, a thorough investigation is necessary to find the impact of scaling on function of logic gates.

iii. Delay: Another challenging parameter of the circuit operation in the sub-threshold region is the longer propagation delay, hence lower frequency of operation due to weak current flow in the channel. This requires circuit optimization techniques for achieving optimum performance.

iv. Development of Sub-threshold Compatible and Robust Memory Design: SRAM is an important component of many ICs, and contributes a large fraction of the active and leakage power consumption. Process variation and reduced I_{ON}/I_{OFF} are the major parameters which degrade the read/write operation and affect read/write access time in sub-threshold region.

v. Noise Margin: It is directly affected by the choice of supply voltage and has high sensitivity to process variations. Therefore, in the presence of process variations, there is need to study noise margin of logic gate and SRAM cell in sub-threshold region.

1.5. RESEARCH GAPS

A detailed literature review of published research work of logic design style, arithmetic circuits, and SRAM cell has been carried out and reported in Chapter 2. Based on it, following research gaps are identified:

i. *Exploration of basic logic gates using different logic families in sub threshold logic is missing in literature*

The current research scenario focuses on the power efficient architectures of arithmetic circuits and SRAM cell design that requires minimum supply voltage and increase the operating frequency of a circuit for sub-threshold operation. For the implementation of these architectures, there is great need to do extensive exploration of basic logic gates using different logic families which is currently missing.

ii. *Comprehensive exploration of Adder/ Multiplier/ SRAM circuits has not been carried out in the sub-threshold region*.

A limited study of the arithmetic circuits using different architectures has been published in the area of sub-threshold region. Therefore, design and exploration of these circuits with possible modifications in design of internal blocks at circuit and architectural level are required to ensure functional and power-efficient designs in sub-threshold region.

Similarly, operation and analysis of sub-threshold SRAM cells during read, write and hold mode have been least explored. SRAM cells designed for super-threshold operation give degraded function and performance at scaled down technologies Therefore designs of power efficient SRAM cells operating in sub-threshold region with higher noise margin during read/write/hold mode at ultra-low power supply in deep sub-micron technology are required.

iii. *Impact of technology scaling on circuits designed in sub-threshold region.*

The impact of technology scaling in arithmetic/ memory circuits has not been analyzed out in the sub-threshold region.

1.6. OBJECTIVES OF THE THESIS

Complete analyses of the arithmetic circuits and SRAM cells used for super-threshold operation have never been examined in the context of sub-threshold operation. The conventional arithmetic circuits and SRAM cells may not be either functional or not give efficient result in sub-threshold region due to ultra-low supply voltage and process variation effect. Therefore, there is a great need to modify the conventional arithmetic circuits and SRAM cells with improved functional parameters of the design. The main objective of this work is based on structural optimizations to reduce very long critical path delay and to improve the overall power-delay-product of the arithmetic circuits in sub-threshold operation. The sub-threshold based SRAM cells are more sensitive to power, voltage and temperature variations and their effects have discussed in published work to some extent [37][38]. But comprehensive analysis of SRAM cell design in terms of various parameters like process sensitivity, area overhead, read stability, write ability, hold stability, read/write access time and leakage power consumption is not carried out in sub-threshold region [39]. The proposed work aims to design low power SRAM cells with improvement in above mentioned design parameters in sub-threshold region. The arithmetic circuits and SRAM cells are designed and implemented at two different technology nodes (45 nm / 180 nm) which shows the effect of scaling in sub-threshold region.

In this thesis, the research is carried out with following objectives:

i. Explorations and design of functional **basic logic gates using different logic families** in sub-threshold region.

ii. Design and analysis of **power efficient functional adder architectures** in sub-threshold region using two different technology nodes.

iii. Design and analysis of **power efficient functional multiplier architectures** in sub-threshold region using two different technology nodes. Overall comparative analyses to be performed to get a full view of the improvements with respect to power, delay and power-delay product for arithmetic circuits.

iv. Design and analysis of **low power functional SRAM cells** in sub-threshold region. A comprehensive analysis of SRAM cells with read stability, write ability, hold stability, read/write access time and leakage power consumption is to be carried out.

1.7. ORGANIZATION OF THE THESIS

This thesis is divided into six chapters. The organization of this thesis is as follows:

Chapter 1 presents an introduction of sub-threshold design technique. It is followed by sub-threshold operation of MOSFET and sources of power consumption. This chapter also explains motivation and challenges of sub-threshold logic design. The research gaps and objectives chosen for this research work are discussed in this chapter.

Chapter 2 describes the detailed literature review on arithmetic circuits and SRAM cells. The characteristics and performance parameters of various power efficient arithmetic circuits such as power, delay and power-delay product at different technology nodes have been discussed. Various low power SRAM cell designs and their parameters in terms of read stability, write ability, hold stability, read/write access time and leakage power consumption have been discussed in detail.

Chapter 3 explores and proposes new designs of the frequently used adders like Carry look-ahead adder, Kogge-Stone adder and Han-Carlson adder architectures with different logic design style and operand size in sub-threshold region.

The comparative analysis of logic gates is given which are used to implement adder architectures using different logic families along with their post layout simulation results. For additional power-delay-product optimization, the effects of reverse body bias scheme on logic gates have been discussed. The design and analysis of chosen adders is done at 45 nm as well as 180 nm technology to find the impact of scaling.

Chapter 4 explores and proposes new designs of column compression multipliers namely Wallace tree and Dadda multiplier architectures, for different bit-widths and different logic design styles in sub-threshold region. The partial product generation scheme, the partial product accumulation scheme used in Wallace tree and Dadda multipliers have been discussed in detail. The design and analysis of chosen multipliers is done at 45 nm as well as 180 nm technology to find the impact of scaling.

Chapter 5 proposes new designs of SRAM cells at 45 nm technology in sub-threshold region. Their comprehensive analysis includes thorough evaluation in terms of read stability, write ability, hold stability, read/write access time and leakage power consumption in comparison

to conventional 6 transistor SRAM cell. To see the impact of scaling, comparison of results of these SRAM cells is done with designs at 180 nm technology at 0.4 V power supply voltage.

Analytical equations, obtained under steady state condition for read, write and hold operation, have been developed to obtain WSNM, RSNM, and Hold SNM theoretically and compared with simulated values.

Chapter 6 finally concludes the outcomes of this research and suggests future scope of this work.

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CHAPTER 2

LITERATURE REVIEW

2.1. INTRODUCTION

Digital systems normally comprise a central processing unit (CPU) that executes arithmetic functions (for instance addition, subtraction, and division), cache on chip SRAM memory for holding the data. The arithmetic circuits are executed by a number of logic gates, or circuit elements, which are interconnected, and form a network with multiple logic depths [1].

A low power microprocessor and digital signal processor (DSP) includes a cache SRAM memory to fetch the data and an arithmetic and logic unit that contains at least one of an adder and a multiplier. In most of the digital systems, adder and multiplier lies in the critical path that affects the overall speed of the system and the performance of adder may determine the whole system performance [2][3]. The choice of arithmetic module architecture is of utmost importance, since its performance determines the whole system response.

In recent years, sub-threshold design technique has been used that tradeoff the overall power-delay-product of the arithmetic circuits by removing or reconfiguring blocks. This is especially important on low-power battery-operated devices, where a longer life could be preferred over a higher output precision [4]. Many papers have been published based on power efficient arithmetic circuits and low power SRAM cells design using different methodology and different design techniques in sub-threshold region which show the importance of this area. Both modules are the part of developing technology that is becoming more creative with the advancement of microchip technology [5]. The arithmetic circuits and SRAM cell operated in sub-threshold region minimizes the switching and leakage energy but it would be slow due to ultra-low supply voltage [6].

Hence there is an interesting tradeoff between speed and switching energy in sub-threshold region. For leakage-aware CMOS circuits, it is a major challenge to find the optimal tradeoff between switching speeds and low leakage currents.

As discussed in Chapter 1, to design these types of ultra-low power system, sub-threshold based SRAM and arithmetic circuits (adders and multipliers) are the basic units and the most power consuming module in the modern-day application for Wireless Sensor Node (WSN).

Sub-threshold based SRAM, Parallel Prefix Adders and column compression multipliers have been established as the most efficient circuits in modern digital systems. There are different kinds of parallel adder, parallel prefix adder and column compression multiplier architectures available. Some of these which are frequently used in ultra-low power based VLSI system designs are analyzed in the present work, are:

- Carry Look-ahead Adder
- Han-Carlson Adder
- Kogge stone Adder
- Wallace tree multiplier
- Dadda Multiplier
- SRAM Cells

Therefore, this chapter explains the detailed literature review of arithmetic circuits (Carry Look-ahead Adder, Han-Carlson Adder, Kogge stone Adder, Wallace tree multiplier, Dadda Multiplier) and SRAM cells. The initial sections of the chapter include the existing architectures of arithmetic circuits with their parameters such as power, delay and power-delay-product using different logic design styles at different technology nodes.

The last section of this chapter describes various low power SRAM cell designs and their parameters in terms of read stability, write ability, hold stability, read/write access time and hold power consumption.

2.2. ARITHMETIC CIRCUITS

With the advent of battery-operated applications like portable computing and personal communication systems, power efficient circuits are needed because of the difficulty in providing adequate cooling to high density chips and for increasing the battery life time [7] [8][9]. For portable applications, low power adder and multiplier circuits along with optimum performance are needed.

Hence, designers need to estimate the delay as well as the average power consumption accurately before the circuit goes to fabrication. Accurate timing analysis has been the subject of numerous investigations over the years. Auvergne et al. [10] have defined delays $t_{HL}(t_{LH})$ in enhancement-depletion MOS logic gate as the time spent by the output to fall (rise) from the static high level (static low level) to $1/2V_{DD}$ respectively. Callaway et al. [11] have investigated the worst-case delay and average power dissipation of adders and multipliers.

They have analyzed the worst-case delay and average number of gate-output transitions per addition for 16-bit adders designed in fully static logic family from the three sources: (1) from gate level simulation, (2) detailed circuit simulation, and (3) actual measurement from a test chip. The circuits are subjected to 10,000 pseudo-random inputs. Results show that number of transitions for each adder, except the conditional sum adder, increases linearly with the word size, whereas the power consumption is normally distributed. These results are then compared with circuit simulation results and actually measured results. It is found that the simple unit gate delay model is inaccurate for carry look ahead and conditional sum adders due to either large fan-in or large fan-out gates in worst-case path. Similarly, the unit power model underestimates the power consumption for adders with large fan-in and fan-out [12].

Hence, unit-delay, unit-power gate model can be used to generate only a first estimates of the power consumption and worst-case delay of parallel adder, parallel prefix adder and column compression multiplier.

As bigger bit widths are desirable for achieving higher precisions, they result in bigger adders and multipliers with high toggling profiles and higher power figures. In recent years, some techniques that trade power for accuracy by removing or reconfiguring blocks of the adder/multiplier have been made available. Choosing the correct technique and implementing it can make a big difference regarding power.

The choice of the logic families provides a good comparison between ultra-low power and high speed based adder architectures. Typically, to design power efficient arithmetic circuits, a static implementation is preferred due to its low power consumption. Dynamic circuits and other logic styles are not preferred due to their high activity factors in sub-threshold region [13].

Static-CMOS logic (e.g. complementary CMOS, pass transistor, transmission gate) based arithmetic circuits are most suitable and widely accepted for many VLSI circuit implementations due to its important properties like low power, high speed, large noise margins, no logic degradation and validity of logic design style at scaled down technologies. These are commonly more reliable, simpler and are lower power consuming than dynamic ones.

The following researchers have presented different arithmetic circuits design using Static logic design style:

J. D. Lee has proposed a logic redundancy technique which share maximum number of transistors among multiple output static CMOS complex gates for the speed improvement [14].

C. Nagendra et al. [15] have adopted a uniform static CMOS layout strategy to design a several class of parallel and synchronous arithmetic modules. The adopted layout designs technique has reduced the short circuit power consumption and improve the speed of the circuit.

A. Asati et al. [16] have presented a MUX based 16x16 unsigned multiplier circuits, which utilize an efficient partial product generation and partial product addition technique. The time and space complexity of such multiplier was much better than simpler array multiplier techniques. The multiplier has been designed using optimized static CMOS logic cells to provide best area, power and delay performance.

Apart from these detailed studies, efforts have also been made to optimize particular adder architecture I. S. Hwang et al. [17], I. S. Abu-Khater et al. [18], and J. Lim et al. [19].

Besides considering different adder architectures, another approach is to employ different CMOS circuit design styles to design power efficient arithmetic circuits:

P. Chuang et al. [20] have proposed a constant delay logic (CDL) style targeting at full-custom high-speed applications. The proposed logic demonstrates high speed, energy-delay product (EDP) reduction across all data activities as compared to static and dynamic domino logic, respectively.

Y. Moon et al. [21] have proposed an efficient charge recovery logic (ECRL) technique having cascade voltage switch logic structure for low-energy adiabatic logic circuit to design an arithmetic module.

M. M. Nipun, et al. [22] have designed a 4-by-4 array multiplier and a fifty-fifth order FIR filter using modified STSCL differential logic techniques for the reduction of overall total leakage consumption within a system.

J. Crop et al. [23] have designed a 4-bit asynchronous multiplier in the sub-threshold region. The designed asynchronous multiplier was more tolerant to process variation than conventional synchronous sub-threshold circuits and operates with a low supply voltage and minimum energy voltage.

A. Tajalli et al. [24] have presented a technique for implementing sub-threshold based source couples logic (STSCL) gates. Fundamental circuits such as ring oscillators and frequency dividers, as well as more complex digital blocks such as parallel multipliers designed by using the STSCL topology have been experimentally characterized. The bias current of the STSCL

gate can be scaled over several decodes using the same device dimensions, which makes this circuit topology very suitable for ultra-low power configurable digital systems.

S. K. Chang et al. [25] have presented a multiplexer-based carry-skip algorithm to design a hybrid adder which reduces the delay time of the adder. The hybrid adder combines both carry-lookahead and multiplexer-based carry-skip architectures to speed up its performance.

C. Burwick et al. [26] have designed digital CMOS threshold logic circuits for low power applications. The threshold logic function reduces the logic depth of the circuit due to smaller capacitance and reduces the power dissipation with improved circuit performance.

E. Angel et al. [27] have presented and compared sign extension techniques to decrease switching activity and improve the performance in parallel multipliers. A significant reduction in power dissipation has been achieved through the use of an efficient sign extension scheme. The implementation of the sign extension scheme does not require additional hardware or any penalty in delay.

M. Solaz et al. [28] have designed two 16-bit Wallace tree multiplier using operand reduction and truncated techniques synthesized in 90 nm low power standard cells. The results show that truncation technique based multiplier offers 30% reduction in power due to the lower weight profile of discarded bits, as compared to operand reduction based multiplier.

Analysis of different logic styles operating in the sub-threshold region is necessary due to the dependency of performance parameters (power, delay and power-delay-product) in different arithmetic circuits.

2.2.1. Parallel Adder Architectures

Although, adder design is a well-researched area, but limited research works have been carried out to improve adders' performance in the power-delay space [29][30][31].

On the other hand, several optimization techniques have been proposed that try to reduce the power consumption of the circuit, either by lowering supply voltages in non-critical paths or by trading gate sizing with an increase in the maximum delay of the circuit [32][33].

The arrangement of the prefix network specifies the type of the parallel-prefix adders (PPA). It is apparent that a key advantage of the tree structured adder is that the critical path due to the carry delay is on the order of $\log_2 N$ for an N-bit wide adder. The arrangements of the prefix network give rise to various families of adders. There are many parallel-prefix adders that have been invented so far.

Among them radix-2 carry look-ahead adder which is most important block of parallel prefix adders, two different radix-2 parallel prefix adders (Kogge Stone Adder and Han Carlson Adder) were widely known parallel prefix adders. There exist various architectures for the carry calculation part.

Tradeoffs in these architectures involves

- Area of the Adder
- The fan out of the nodes
- The overall wiring network

The biggest difference between the full adder and parallel prefix adder is that in the full adder, summation and carry calculation is done in the same one bit block but in the prefix adder, summation and carry calculation are separated from the bit block and all calculation is treated as a whole in the carry graph. The carry graph uses the prefix circuit and this is the origin of the name, “Prefix Adder”.

Conventionally parallel adder structure employs three main parts: the propagate/generate generator, sum generator, and carry generator These parts of the circuit decide the overall circuit performance, power consumption, speed, area, power-delay product etc.

Extensive research has been done to improve the power and performance of these basic building blocks to design power efficient arithmetic circuits in super-threshold region.

Many papers have been published based on the optimization of power efficient adders using different methodology and different design techniques to improve the power consumption performance, size which shows the importance of this area [35]-[68].

Their research outcomes of analysis based on Carry look-ahead, Kogge-stone and Han-Carlson adder architecture, different logic design style at different technology are discussed below:

(i) CLA architectures

CLA is fast adder architecture optimized at the logic-level, and used to design addition-based arithmetic circuits using cell based VLSI design. It generates the carry signals in O(log n) time for n bits. The parallel CLA adder has been commonly used for fast carry computation in the

design of energy efficient parallel prefix circuits [34]. Some of the most cited referenced CLA architectures using different techniques and technology nodes are given in Table 2.1.

Table 2.1: Comparison of various referenced CLA architectures

Types of CLA's	Techniques	Technology	Improvements
64-bit CLA [35]	Using modified carry select adder block	0.5 µm	Speed and area
64-bit CLA [36]	Dual-V_{th} domino circuit	0.25-µm	Performance, less power-consumption with reduced standby leakage current.
4-bit carry-ripple adder and modified CLA (MCLA) [37]	NAND gate instead of AND gate at the end of the generating path	65nm and 90nm	Delay, power-delay and energy-delay product
16-bit CLA [38]	Multi-threshold CMOS (MTCMOS)	0.35µm	Propagation delay time and power consumption
32-bit CLA [39]	Non-full voltage swing true-Single-phase- Clocking Logic (NSTSPC)	0.35 µm	To speed up the generation of the carry
32-bit tree-structured CLA [40]	Modified ANT (all-N-transistor) logic	0.35 µm	Speed and area
8-bit CLA [41]	Two-phase all-N-transistor (ANT) logic blocks	0.25 µm	Dynamic power consumption
64-bit CLA [42]	Sparse CLA trees adder based on buffering techniques	0.13 µm	Energy efficiency
Mixed-radix look ahead cells of the CLA network [43]	The hierarchical expansion of the carry equation for the reverse conversion algorithm creates a regular multilevel structure	0.18 µm	Speed
64-bit [44]	Optimize transistors size in the different Manchester carry chain blocks and by adjusting the block widths within the carry Tree	0.35 µm	Critical delay paths of the carry signals
4-bit CLA [45]	Differential PTL a novel technique	non-self-aligned 1-µm D-MESFET GaAs technology	Circuit performance
32-bit CLAs [46]	Complementary all-N transistor (CANT) comprising ANT logic and inverted ANT logic	90 nm	Power and performance

(ii) HCA architectures

HCA offers a highly efficient solution to binary addition problem, assures a low computation delay and low power in sub-threshold region. The hybrid construction of a HC logarithmic prefix adders are the combinations of Kogge-Stone structure which have $\log_2 n$ stages and Brent-Kung structure which have $2\log_2 n-1$ stages. The combine effects of both the adders provide a reasonably high speed at less complexity [47]. Some of the most cited referenced HCA architectures using different techniques and technology nodes are given in Table 2.2.

Table 2.2: Comparison of various referenced HCA architectures

Types of HCA's	Techniques	Technology	Improvements
N ≤ 64-bit [48]	A new prefix algorithm for carry computation.	4 µm	Delay and area
64-bit HCA [49]	Optimization of prefix level in carry-computation units	0.25 µm	Power consumption
8-bit, 16-bit and 32-bit HCA [50]	CMOS logic and transmission gate logic design style	65 nm	Area, delay and power consumption
32-bit HCA [51]	Reduction in prefix operations by adjusting the number of stages	---	Area and power consumption
32-bit, 64-bit and 128-bit HCA [52]	A novel variable latency speculative method	65 nm	High speed
16-bit, 24-bir, 32-bit, 40-bit, 48-bit, 56-bit, 64-bit, 80-bit, 96-bit,112-bit and 128 bit HCA [53]	Hybrid HCA (combination of two Brent-Kung stages each at the beginning and at the end and with Kogge-Stone stages in the middle)	45 nm	Area and power consumption
32-bit HCA [54]	Reduces the number of prefix operation	Xilinx ISE 13.1 Tool implemented using Spartan 6	Area and power consumption
16-bit HCA [55]	HCA implemented with the help of cells like black cell and white cell operations for carry generation and propagation.	Xlinx design suite 14.5, implemented using Spartan-3E FPGA (XC3S500E-4FG320C).	Speed
32-bit HCA [56]	Pipelined based techniques and Folding architecture	---	Area and power consumption

(iii) KSA architectures

The Kogge–Stone adder is a parallel prefix form carry look-ahead adder. It generates the carry signals in O (log n) time, and is widely considered the fastest adder design possible. It is the common design for high-performance adders in industry. It takes more area to implement than the Brent– Kung adder, but has a lower fan-out at each stage, which increases performance. Wiring congestion is often a problem for Kogge–Stone adders as well [57]. Some of the most cited referenced KSA architectures using different techniques and technology nodes are given in Table 2.3.

Table 2.3: Comparison of various referenced KSA architectures

Types of KSA's	Techniques	Technology	Improvements
n-bit [58]	Proposed recurrence equation by using recursive doubling technique in an algorithm	All	Speed
64-bit KSA [49]	Reduced switching activity of the novel carry-computation units	0.25 µm	Power consumption
8-bit, 16-bit and 32-bit KSA [50]	Using both CMOS logic and transmission gate logic design style	65 nm	Area and delay
64-bit KSA [59]	The four-new dot-operator cells based Dynamic pass-transistor technique	0.35 µm and 0.13 µm	Area and power consumption
16-bit, 32-bit, 64-bit, 128-bit, and 256-bit KSA [60]	Reconfigure a wide KSA by using cascading technique	90 nm	Power-delay product
16-bit, 32-bit and 64-bit [61]	Used conventional equations of KSA	130 nm, 90 nm, 65 nm and 40 nm	Speed
64-bit adder [62]	Logical effort method has been used on transistor-level	0.18µm	Delay
128-bit KSA [63]	A new efficient structure based on the operation of each stage is dependent only to a lower significant stage	Xilinx 14.3 software	Power-delay product
8-bit KSA [64]	Re-routing (wiring) and black-cell reduction	XILINX ISIM simulator, Synthesized for the Spartan-3 FPGA XC3S400	Speed
64-Bit KSA [65]	Fault tolerant technique using Adaptive Clocking	180 nm	Speed

2.2.2. Column Compression Multipliers

Multipliers require high amount of power and delay during the partial products accumulation stage. At this stage, most of the multipliers are designed with different kind of compressors that are capable to add two/three or at most 4, 5, 6 and 7 bits by using lower order (2-2/3-2) or high order compressors (4-2,5-2, 6-2 and 7-2 compressors).

These lower/higher order compressors are used to perform parallel computation to accumulate the partial products [66][67].

Therefore, its power and performance determines the overall multiplier response. The power consumption of these partial product accumulation modules in multipliers depends upon the choice of logic design style.

Foster and Stockton have developed a counter implemented with full and half adders which are used in partial product reduction process to optimize the overall performance of the multipliers [68].

S. Asif et al. have been discussed a strategy to reduce the area of traditional Wallace (TW) multiplier by reducing the number of half adders [69]. This innovative method allows for an effective utilization of half adders in such a way that the size of the final adder is also got reduced. The speed of the reduced complexity Wallace (RCW) multiplier is expected to be the same as of TW multiplier due to the equal number of reduction stages in both multipliers.

P. Ramanathan et al. presented a decomposition logic based technique which improves the performance of the Dadda multipliers with little increase in power dissipation [70]. The designed multiplier was faster and energy efficient with a negligible power penalty in spite of extra logic circuitry. Choices of different varieties of logic families to design adders also give improvement in the overall performance of multipliers [71][72][73].

L. Dadda has introduced the concept of (n, m) parallel compressors to reduce the partial product matrix which is the generalized the idea of using HA and FA's. This (n, m) parallel compressors are a combinational network with n inputs and m outputs where the outputs express the count of the number of inputs that are ones. Thus, a HA and FA is a (2-2) and (3-2) parallel compressors respectively.
The compressors are the bit-compressing cells with principal application in multi-operand addition and multiplication hardware.

Some of the details of most cited referenced compressor design used in Wallace tree and Dadda multiplier using different techniques and technology nodes are summarized in Table 2.4.

Table 2.4: Comparison of various referenced compressor designs

Types of Compressors	Techniques	Technology	Improvements
4-2 [74]	Non-full-swing pass-transistor carry generator	0.8 µm and 0.35µm	Power, delay and power-delay product
4-5 and 5-2 [75]	Modified XOR and MUX circuits	0.35µm	Delay and power consumption
4-5 and 5-2 [76]	Feedback concept in pass transistor logic.	0.18 µm	Power consumption
4-3, 5-3, 6-3 and 7-3 [77]	Designed only half adder and full adders	90 nm	Delay
3-2 and 4-2 compressor [78]	Double pass transistor logic (DPL)	0.6 µm	Delay
3-2, 4-2 and 5-2 [79]	Analyzed using CMOS and CMOS+ implementations of XOR and the MUX blocks	0.18µm	Area, power, delay and power-delay product
3-2 and 4-2 [80]	Combination of two logic design style	65 nm	Power consumption
4-2 [81]	Decomposing each XOR gate to three simpler gates among AND/NAND and OR/NOR	45 nm	Power, delay and power-delay product
5-2 [82]	Designed with XOR–XNOR circuits	0.25 µm	Delay
5-3 [83]	Fast 2-bit adder cell, which utilizes two XOR gate delays	0.225 µm	Delay

2.3 SRAM CELLS

SRAM is an important component in ultra-low power systems. Operation of standard 6T SRAM at sub-threshold voltages has degraded static noise margin (SNM) and fluctuations in MOSFET currents because of process variations at ultra-low voltages SRAM cell stability is a major challenge in sub-threshold region [84]. Numerous prominent publications have

appeared over the recent years targeted at low power SRAM cells design to improve cell stability in sub-threshold region.

- B. H. Calhoun et al. [85] have evaluated static noise margin (SNM) of conventional 6T (C6T) SRAM bit-cell operating in sub-threshold region. The detailed analysis of the statistical distribution of SNM with process variation provides a model for the tail of the probability density failure (PDF) that dominates SNM failures. Low power C6T SRAM cell fails to achieve reliable sub-threshold operation [86]. Single-ended low power C6T suffers from stability during read/write analysis [87].
- S. Mukhopadhyay et al. [88] have explored the operation of single-ended 6T SRAM cell at 32 nm technology node. This design saves dynamic read/write power more than 50% with marginal penalty in read/write delay and standby power. The analyzed results show that the design offers narrower spread in read access time, which shows its robustness against process and temperature variations at the expense of 5% penalty in read static noise margin.
- M. F. Chang et al. [89] have done the study of differential data-aware power-supplied (DAP) 8T SRAM cell with 45 nm and 40 nm processes. This study addresses the stability and trade-off-issues between write and half-select accesses in the conventional 8T and 6T cells. The designed 8T cell applies differential data-aware-supplied voltages to its cross-coupled inverters to increase both stability margins for write and half-select accesses. This DAP-8T cell employs a boosted-BL scheme to improve read speed and read stability. This design improves the write margin, half-select stability, and read stability for low-V_{DD} applications.
- T. H. Kim et al. [90] have presented a technique for improving write margin and read performance of 8T sub-threshold SRAMs by using long channel devices to utilize the pronounced reverse short channel effect. The results show that the designed 8T cell at 0.2V has a write margin equivalent to a conventional cell at 0.27V, improved write margin, better variation tolerance and increased I_{ON}-to-I_{OFF} ratio in the read port.
- G. Razavipour et al. [91] have presented two 8T and 9T SRAM cells at 45nm technology to reduce the static power dissipation due to gate and sub-threshold leakage currents. The first 8T cell structure results in reduced gate voltages for the NMOS pass transistors, and thus lower the gate leakage current. It reduces the sub-threshold leakage current by increasing the ground level during the idle (inactive) mode. The second 9T cell structure

makes use of PMOS pass transistors to lower the gate leakage current. In addition, dual threshold voltage technology with forward body biasing is utilized with this structure to reduce the sub-threshold leakage while maintaining performance. Compared to a conventional SRAM cell, the first cell structure decreases the total gate leakage current by 66% and the idle power by 58% and increases the access time by approximately 2% while the second cell structure reduces the total gate leakage current by 27% and the idle power by 37% with no access time degradation.

- N. Verma et al. [92] have designed a high density 8T-SRAM cell to achieve a minimum operating voltage of 350 mV at 65nm technology. To ensure read stability, buffered read is used, and peripheral control of both the bit-cell supply voltage and the read-buffer's foot voltage enable sub- write and read without degrading the bit-cell's density. An overall result shows that the entire 256 kb SRAM consumes 2.2 W in leakage power at 350mV.
- L. Sheng et al. [93] have done the design and evaluation of nine transistors (9T) which utilizes a scheme with separate read and write word lines. The result shows improvements in power dissipation, performance and stability.
- L. Zhiyu et al. [94] have designed a nine-transistor (9T) SRAM cell at 65nm technology for reducing leakage power and enhancing data stability. This cell completely isolates the data from the bit lines during a read operation, thereby enhanced by 2, leakage power consumption of a super cutoff 9T SRAM cell was reduced by 22.9% as compared to a conventional six-transistor SRAM cell.
- M. Zamani et al. [95] have presented a scheme that uses dynamic mechanism cutting the feedback to improve the write SNM and lowering the write access time. The 9T-cell SRAM design shows robust stability, 80% and 50% improvement in read and write SNM respectively in comparison to the 6T.
- M. Majid et al. [96] have presented a nine-transistor (9T) SRAM cell operating in the sub-threshold region at 90nm technology. This 9T cell uses a common bit-line during read and writes operation. A suitable read operation is achieved by suppressing the drain-induced barrier lowering effect and controlling the body–source voltage dynamically. Proper usage of low-threshold voltage (L-V_{th}) transistors in 9T design helps to reduce the read access time and enhance the reliability in the sub-threshold region.
- A. R. Ahmadi Mehr et al. [97] have designed two 12T SRAM cell for a better write margin using 32nm standard bulk MOSFET technology. In these structures, two new transistors

have been added to cut the feedback of the back to back inverters. The improved static power consumption, read and write noise margins have been obtained at the cost of additional area as compared to conventional 6T SRAM cell.

- H. Chen et al. [98] have presented a schmitt trigger based SRAM 12T bit-cell which operates under optimum-energy supply voltage for medical device application. Results show that the design has 45% and 30.2% improvement of the read and hold noise margins as compared to the conventional 6T SRAM bit-cell.

- Y. W. Chiu et al. [99] have designed the new bit-interleaving scheme based 12T subthreshold SRAM cell with Data-Aware Power-Cutoff (DAPC) Write-assist which improve the Write-ability of the cell. The disturb-free feature facilitates the bit-interleaving architecture that can reduce multiple-bit errors in a single word and enhance soft error immunity by employing error checking and correction (ECC) techniques. The 4 kb SRAM has been implemented at 40 nm general purpose (40GP) CMOS technology. Data can be written successfully for down to 300 mV. The measured maximum operation frequency is 11.5 MHz with total power consumption of 22 µW at 350 mV.

- K. Takahiro et al. [100] have developed a ratio-less full-complementary 12-T SRAM cell using 180 nm technology, operates under an ultra-low supply voltage range of 0.22 V. The ratio-less SRAM design concept enables a memory cell design that is free from the consideration of the SNM. Furthermore, it enables a SRAM function without the restriction of transistor parameter (W/L) settings and the dependence on the variability of device characteristics. The measured results show that the ratio-less full-complementary 12-T SRAM has superior immunity to device variability, and its inherent operating ability as compare to conventional 6T SRAM cell in sub-threshold region.

- D. Roy et al. [101] have presented a low write power and variability-aware 13-transistor (13T) SRAM design in sub-threshold region using 22 nm technology node. The cell achieves low write power dissipation due to reduction of activity factor and breakage of feedback path in the cross-coupled inverter during write operation. It also achieves higher read static noise margin at the expense of 49.5% decrease in write static noise margin and 27% tighter spread in read delay distribution compared with standard 6T SRAM cell at nominal V_{DD} at the expense of 76% higher read delay.

  Different existing low power SRAM cell designs and their performance, discussed above, are summarized in Table 2.5.

Table 2.5: Comparison of various referenced low power SRAM cells

Types of SRAM Cells	Techniques	Technology	Improvements
4T [102]	Two word-lines and one pair bit-line	65 nm	Power consumption and area
5T [103]	Single-ended read and differential write scheme	40 nm	Static power consumption
5T [104]	Asymmetric cell sizing concepts	45 nm	Static-noise-margin and area
6T [105]	Single-ended	0.13 µm	Power consumption
6T [88]	Single ended	32 nm	Dynamic read/write power consumption
7T [106]	Feedback connection and disconnection are performed through an extra NMOS transistor	180 nm	Write power consumption
8T [107]	Access pass gates are replaced with full transmission gates	16 nm	Read/write access time
8T [89]	Differential data-aware power-supply with boosted-BL scheme	45 nm and 40 nm	Write margin and read stability
8T [90]	Reverse short channel effect in sub-threshold design technique	0.36 µm	Write margin, read delay and better variation tolerance
8T and 9T [91]	Dual threshold voltage technology with forward body biasing	45 nm	Static power consumption
8T [92]	Buffered read foot voltage enable	65 nm	Leakage power consumption
9T [94]	Isolates the data from the bit lines during a read operation	65 nm	Leakage power consumption and enhancing data stability
9T [95]	Dynamic mechanism to cut the feedback		Read and write SNM
9T [96]	Uses of common bit-line during read and writes operation	90nm	Read access time and reliability
12T [97]	Cut the feedback of the back to back inverters	32 nm	Static power consumption, read and write SNM
12T [98]	Schmitt trigger	0.13 µm	Hold and read noise margins
12T [99]	New bit-interleaving	40 nm	Write-ability, power consumption
12T [100]	Ratio-less full-complementary	180 nm	Superior immunity to device variability

Hence, the cell structures with more transistors are widely deemed to be inevitable in order to support future process technologies as well as in sub-threshold region of operation.

Summary: This chapter has reviewed the published works on low power architectures of arithmetic circuits (CLA, KSA, HCA, Wallace tree and Dadda multipliers) with their performance parameters such as power, delay and power-delay-product using different logic design styles at different technology nodes.

Also, different existing low power SRAM cell designs and their performance parameters in terms of read stability, write ability, hold stability, read/write access time and leakage power consumption have been reviewed.

Outcome: From the Table 2.1 to Table 2.4, it is clear that power efficient Carry look-ahead adders, Kogge stone adders, Han-Carlson adders, Wallace tree and Dadda multipliers have been developed using different logic styles for super-threshold region.

Thus, fewer explorations have been done in the area of sub-threshold based basic logic gates, arithmetic circuits and SRAM cell designs including the impact of technology scaling on their performance. Therefore, design issues and required circuit modification of arithmetic blocks and SRAM cell (at different technology nodes) at circuit and architecture level is needed to be explored and analyzed thoroughly. This forms the research gaps as already mentioned in Chapter 1.

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CHAPTER 3

ADDERS

3.1. INTRODUCTION

The arithmetic circuits are designed to handle the data in units; each unit has a fixed number of binary digits which compromises with available memory capacity, operating speed, required accuracy of numerical data, and other considerations [1]. Adders are the core elements of arithmetic circuits as they are widely used in arithmetic logic units (ALU), in the floating-point units, and for address generation in the case of cache or memory access. These are frequently required in VLSI from processors to application specific integrated circuits (ASICs) as well as in fundamental arithmetic operations within contemporary electronic system. Adders are essential used not only for addition, but it is also the nucleus of the basic arithmetic operations such as multiplication, subtraction and division. Addition is performed to increment program counters, multiplication is performed with multiple addition, subtraction is performed as an addition when negative numbers are represented in their 2'complement form, division is done by successive subtraction, and it requires no extra correction operations, if either dividend or divisor is negative that can also be performed by using adder circuits [2][3]. Even for programs that don't do explicit arithmetic, addition must be performed to increment the program counter and to calculate addresses of the memory.

In most of the digital systems, adder's lies in the critical path that affects the overall speed of the system and the performance of adder may determine the whole system response. Adder logic is thus of obvious importance and has received attention from computer designers. The most important and widely accepted metrics for measuring the quality of adder designs in the past were propagation delay and area. Efforts in the past were focused towards increasing the speed of computing system. As a result, high-speed computation has become an expected norm for the average user. But with the rise of portable, battery operated devices reducing power consumption has become an important design goal. Increased power consumption also leads to increased heat, which makes low power design important even for non-portable applications. Circuit designers now seek to meet performance requirements for adder circuits with the lowest power consumption possible. Digital arithmetic circuits operating in the sub-threshold region of the transistor are being used as an ideal option for ultra-low power CMOS

design. To operate a circuit in sub-threshold region the operating voltage scaled down below the device threshold [4]. However, the weak driving current due to the supply voltage below the threshold voltage, limits the circuit performance.

Power efficient adders under sub-threshold operation are also essential part of micro sensors, WSN's and MAC core unit. Thus, optimizing the adder circuitry with minimum power consumption will have a beneficial effect on low power based above mentioned applications.

Extensive research has already been done in the design and implementation of serial adders using different logic families in sub-threshold region [5][6][7]. Ripple carry adder (RCA) has been found the most power efficient architecture operated in sub-threshold region as compared to all types of serial adder architecture [8]. In paper [9], it has been discussed that for low operand size, serial addition can match the speed of parallel addition when operating in sub-threshold, while still dissipating less (power). Whereas, for high operand size, serial adder gives low performance due to overall carry computation delay. In other words, for 32-bit addition, a parallel adder is 4.7 times faster than a serial one. For 64-bit addition, the parallel adder would be around 8.1 times faster than the serial adder, based on a similar calculation. Thus, parallel adders are so attractive in order to deliver high performance in terms of computational speed [10]. In paper [11], it has also been investigated that the major problem for binary addition is the propagation delay in the carry chain. As the width of the input operand increases, the length of the carry chain increases. To address the carry propagation problem, most of the modern adder architectures are represented as a parallel prefix adder structure consisting of pre-processing, Carry look-ahead and post processing sections. The carry-look-ahead adders are being used for parallel computation of carry bits in parallel prefix adders. These parts of the circuit decide the overall circuit performance, power consumption and power-delay product.

Parallel Prefix Adders have been established as the most efficient circuits for binary addition in digital systems. The power and delay of a parallel prefix adder is directly proportional to the number of levels in the carry propagation stage. In research work [11], design and analysis of different parallel prefix adders such as Kogge-Stone adder, Brent Kung adder, Han-Carlson adder, Sklansky adder, Lander Fischer adder, and Knowles adder have been done in super-threshold region. The comparative results show that Kogge-Stone adder and, Han-Carlson adder have best results in terms of overall power-delay-product [12].

To design an energy-efficient addition-based arithmetic circuits using cell based VLSI design, designers must rely on power efficient adder architectures that are optimized at the logic-level.

This reduces the number of power efficient adder architecture operated in sub-threshold region to a few classic ones, the Carry look-ahead adder, Kogge-Stone adder and Han-Carlson adder [13][14][15].

For power efficient adders design, radix-2 is suitable network depth due to less complex circuit design, whereas the radix-4 and higher increases the stage efforts, power and delay of each stage but reduces the number of required stages [16]. Therefore, the implementation of above mentioned adders use radix-2 as this is most power efficient network depth, suitable for sub-threshold operation and conventionally used in practical applications [17].

The main aim of this work is to design and implementation of radix-2 Carry look-ahead adder which is most important block of parallel prefix adders, two different radix-2 parallel prefix adders (Kogge-Stone Adder and Han-Carlson Adder) using two different technology nodes (45 nm / 180 nm) operated in sub-threshold region. The performance metrics considered for the analysis of the adders are: power, delay and power-delay-product.

The rest of the chapter is organized as follows. Section 3.2 presents internal circuitry of basics building blocks of adder architectures and their functional overview. Section 3.3 presents comparative analysis of logic gates which are used to implement adder architectures using different families and their post layout simulation results for sub-threshold operation. Section 3.4 presents effects of reverse body scheme on logic gates and their post layout simulation results for sub-threshold operation. Section 3.5 describes the design and analysis of three different architecture and their post layout simulation results for sub-threshold operation. Section 3.6 presents final results and discussion of three different architectures and Section 3.7 presents a summary of the chapter and the concluding remarks.

3.2. ADDER ARCHITECTURES

Power efficient adders are used starting from very low speed arithmetic calculations, medium speed applications to high-speed real multimedia computations. So, depending upon the energy efficiency, trade-offs are done at architecture and circuit levels to have small silicon area and high performance. Designing power efficient adders operated in sub-threshold region with moderate speed is a significant goal of this work. The power consumption of the adder varies with the choice of architecture, logic family and operand size. Different combinations of these choices lead to many different adder designs. This chapter explores three different adders like Carry look-ahead adder, Kogge-Stone adder and Han-Carlson adder architectures with different logic design style and operand size in sub-threshold region. Based on the

simulation results with different operand size and preferred figure of merit (power, delay and power-delay product) the best architecture is proposed in sub-threshold region. This section briefly describes the internal circuitry of basics building blocks of adders.

3.2.1. CLA

The most commonly used scheme for accelerating carry propagation is the Carry look-ahead scheme. The main idea behind Carry look-ahead addition is an attempt to generate all incoming carries in parallel and avoid the need to wait until the correct carry propagates from the stage of adder where it has been generated. CLA is formed by three main logical blocks, pre-calculation of generate/propagate generator blocks used to increase the speed of carry computation, the most intensive parallelizable carry generator blocks which reduces overall computation time and adder blocks to generate the sum. CLA avoids the linear growth of carry delay by generating carries in parallel by using generate and propagate signals. Figure 3.1 shows the block diagram of n-bit CLA.

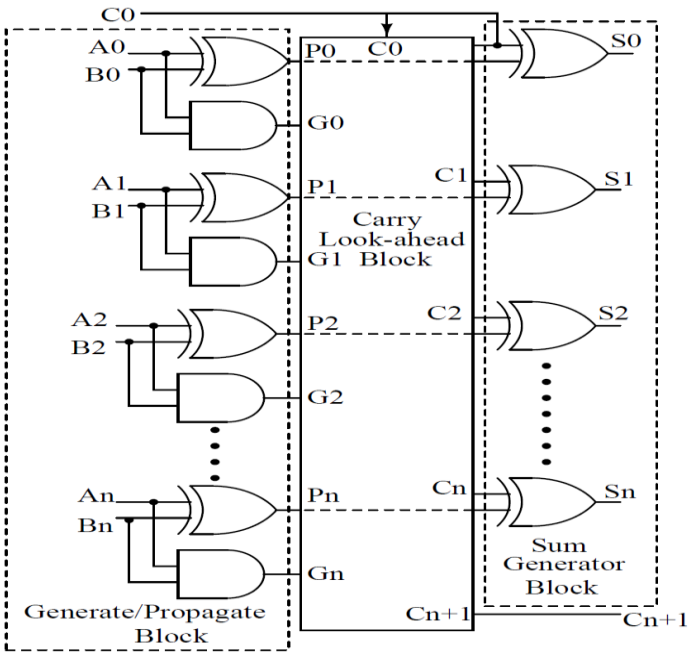


Figure 3.1: Block diagram of n-bit CLA

The logic expressions of the logical generate/propagate blocks, carry generator and sum generator blocks are given by (3.1) - (3.4) [18].

$$G_i = A_i \bullet B_i \tag{3.1}$$

$$P_i = A_i \oplus B_i \tag{3.2}$$

Notices that both generate and propagate signals depend only on the input bits and thus will be valid after one gate delay. When the adder inputs are loaded in parallel, all the G_i and P_i signals will be generated at the same time.

The carry of the i^{th} stage which is also the input carry of the $(i+1)^{th}$ stage can be calculated by outputs of i^{th} stage using equation (3). The logic expressions for the carryout and sum signals are given by:

$$C_i + 1 = G_i + P_i \bullet C_i \tag{3.3}$$

$$S_i = P_i \oplus C_i \tag{3.4}$$

Where A_i and B_i are the augends and addend inputs, C_i the carry input, S_i and $C_i + 1$, the sum and carry-out to the i^{th} bit position and the auxiliary functions, G_i and P_i are generate and propagate signals respectively.

Equation (1) and (2) shows the i^{th} partial full adders (PFA) equations and their outputs are labelled as the generate (G) and propagate (P) signals needed for the carryout equations. The values of G and P are then used to find the group generate and group propagate for a group of two successive PFA at the next level of the tree. For example, to represent the generation of a carry in position 0, 1, 2 and 3 and its propagation to C_4, we need to consider the generation of carry in each of the positions, as represented by G_0 through G_3, and the propagation of each of these four generated carries to position 4. This gives the group generate (G_{0-3}) for a 4-bit CLA.

$$G_{0-3} = G_3 + G_2 \bullet P_3 + G_1 \bullet P_3 \bullet P_2 + G_0 \bullet P_3 \bullet P_2 \bullet P_1 \tag{3.5}$$

Similarly, to propagate a carry from C_0 to C_4, we need to have all four of the propagate functions equal to 1, giving the group propagate function (P_{0-3})

$$P_{0-3} = P_0 \bullet P_1 \bullet P_3 \bullet P_3 \tag{3.6}$$

Whereas equation (3.3) and (3.4) shows that as increase the number of bits in the CLA adders, the complexity increases because the number of gates in the expression $C_i + 1$ increases which increases power and area too. Applying these equations for a 4-bit CLA:

$$C_1 = G_0 + P_0 \bullet C_0 \tag{3.7}$$

$$C_2 = G_1 + P_1 \bullet C_1 = G_1 + P_1 \bullet (G_0 + P_0 \bullet C_0) = G_1 + P_1 \bullet G_0 + P_1 \bullet P_0 \bullet C_0 \tag{3.8}$$

$$C_3 = G_2 + P_2 \bullet C_2 = G_2 + P_2 \bullet G_1 + P_2 \bullet P_1 \bullet G_0 + P_2 \bullet P_1 \bullet P_0 \bullet C_0 \quad (3.9)$$

$$C_4 = G_3 + P_3 \bullet C_3 = G_3 + P_3 \bullet G_2 + P_3 \bullet P_2 \bullet G_1 + P_3 \bullet P_2 \bullet P_1 \bullet G_0 + P_3 \bullet P_2 \bullet P_1 \bullet P_0 \bullet C_0 \quad (3.10)$$

These carry values can be used to compute the carry-ins at a higher level of hierarchy. The Generate and Propagate signal can be a single bit or many bits in look ahead block. The meaning of the equations remains the same.

3.2.2. KSA

The KSA is one of the fundamental parallel adder which is widely used in arithmetic circuits using cell based VLSI design. The circuit employed the scheme of multilevel look-ahead adder with improved delay and generates the carry signals in O (log n) time, where n is the number of bits per input. The addition is performed in three stages and the basic blocks of this adder are the bitwise propagate/generate logic block, group propagate/generate logic block and sum/carry logic block as illustrated in Figure 3.2.

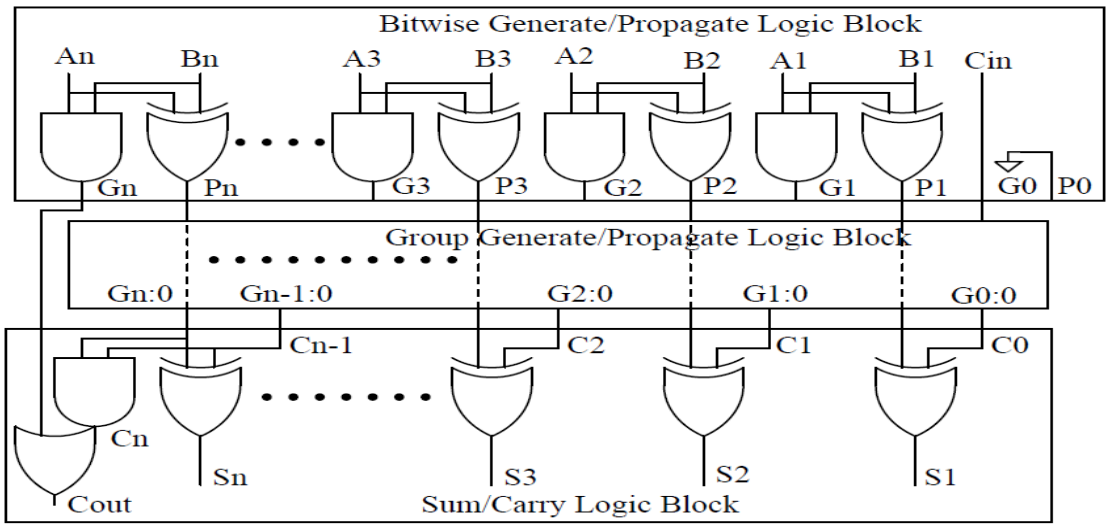


Figure 3.2: Block diagram of n-bit KSA

The first stage or bitwise pre-processing stage produces the Generate and Propagate signals of two input operands Ai and Bi. Eq.

$$G_i = A_i \bullet B_i \quad (3.11)$$

$$P_i = A_i \oplus B_i \quad (3.12)$$

Where ($\cdot$, + and $\oplus$) represents AND, OR and XOR operations. Notices that both propagate and generate signals depend only on the input bits and thus will be valid after one gate delay.

In the second stage, group generates and group propagates signals are produced and are defined according to (3.13) and (3.14) respectively [19].

$$G_{i+1} = G_i + P_i \cdot G_{i-1} \tag{3.13}$$

$$P_{i+1} = P_i \cdot P_{i-1} \tag{3.14}$$

This stage is the major functional unit with dense orientation of calculations and logical functionalities to produce carry signal. The complexity and function rich feature of the stage plays a major impact on power consumption.

The third stage is called post processing which results the sum bits by XOR of carry and propagate signals from previous stages. The first stage and last stage are intrinsically fast because they involve only simple operations on signals local to each bit position.

3.2.3. HCA

Due to the slow speed and high power consumption of conventional CLA's has led to the implementation of parallel prefix-based HCA's, particularly where large amount of adders are required. Small group of intermediate prefixes computes the carry first then large group prefixes compute the carry till the computation of all the carry bits. In prefix-based adders, the carry computation scheme significantly increases the speed of the adder (at the expense of increased complexity, delay increases with order $\log_b$ (n), where b is the radix and *n* is the number of bits per input). The basic block diagram of n-bit logarithmic parallel -prefix HC structures is shown in Figure 3.3.

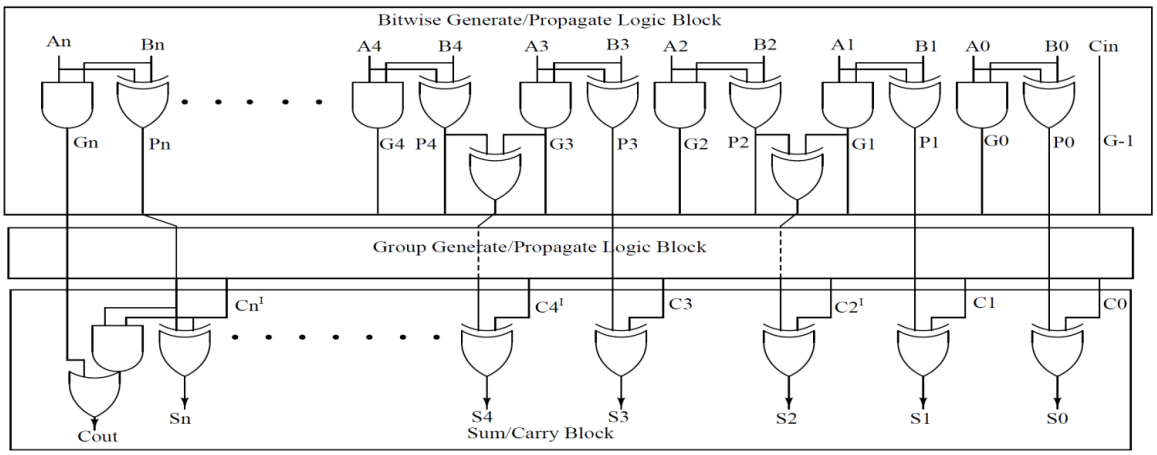


Figure 3.3: Block diagram of n-bit HCA

The performance of the final addition is divided into three stages. In the first stage also known as pre-computation logic stage, generate signals, propagate signals and temporary sum signals

of two input operands A_i and B_i are computed bitwise. For any given bit-position, G_i and P_i signal expressions are defined as follows:

$$G_i = A_i \cdot B_i \qquad P_i = A_i \oplus B_i \tag{3.15}$$

Where ($\cdot$, $\oplus$ and +) represents AND, XOR and OR operations and 'i' is an integer and $0 \leq i < n$. Both propagate, generate and temporary sum signals depend only on the input bits and thus will be valid after one gate delay.

The group generates and group propagates signals are produced in prefix tree block and are given in equation (3.16) and equation (3.17) respectively [20].

$$G_{i+1} = G_i + P_i \cdot G_{i-1} \tag{3.16}$$

$$P_{i+1} = P_i \cdot P_{i-1} \tag{3.17}$$

This stage is the major functional unit with dense orientation of calculations and logical functionalities to produce carry signal. The complexity and function rich feature of the stage plays a major impact on power consumption. In the final stage known as post-computation logic block, the final sum and carry-out are computed and are defined according to following given equation.

$$S_i = P_i \oplus G_{i:-1} \tag{3.18}$$

$$C_{out} = G_{i-1} + P_{i-1} \cdot G_{i-2:-1} \tag{3.19}$$

Where -1 is the position of carry-input $(G_{i:-1} = C_i)$.

All logarithmic prefix structures can be implemented with the equations above; however, to get the same carries, equation (3.16) and (3.17) can be interpreted in various ways which leads to variety of parallel trees. The first stage and last stage involve only simple operations on signals local to each bit position, so these stages are intrinsically fast.

3.3. LOGIC FAMILIES FOR SUB-THRESHOLD CIRCUIT DESIGN

Analysis of different logic styles operating in the sub-threshold region is necessary due to the dependency of performance parameters (power, delay and power-delay-product) in different adder architectures. The choice of the logic families provides a good comparison between ultra-low power and high speed based adder architectures.

Typically, to design power efficient arithmetic circuits, a static implementation is preferred due to its low power consumption. Dynamic circuits are not preferred due to their high activity factors in sub-threshold region [21].

This study aims to provide some insights on different logic style performance in the sub-threshold region. As per reported literature, Static-CMOS, pass transistor, double pass-transistor logic, transmission gate logic, complementary pass-transistor logic, swing restored pass-transistor logic families are the most suitable for low power operation in CMOS technology in sub-threshold region [22].

Out of these, complementary pass-transistor logic and swing restored pass-transistor logic families give differential outputs (OUT/ OUT_bar) whereas other give single ended output (OUT).

For implementation of the Boolean expressions of CLA, KSA and HCA architectures discussed in section 3.2, AND, OR, XOR gates are the three widely used logic gates. Therefore, the design and comparative analysis of these logic gates (AND, OR, XOR) in sub-threshold region, using six above mentioned logic styles, along with the tradeoff is necessary.

The basics of logic families and their in-sight effects for the designing of basic logic gates with some tradeoff are given below.

3.3.1. Static-CMOS Logic [23][24]

The schematics and layouts of logic gates using Static-CMOS logic family are shown in Figure 3.4. Conventional fully Static-CMOS logic is a common CMOS logic design style choice since it involves low power consumption, large noise margin and fully functional at scaled down technologies, thus more reliable operation at low voltages.

The conventional Static-CMOS logic is built from NMOS pull-down and a dual PMOS pull-up logic network. Static-CMOS logic function can be realized very efficiently by these pull-down and pull-up networks connected between the gate output and the power lines.

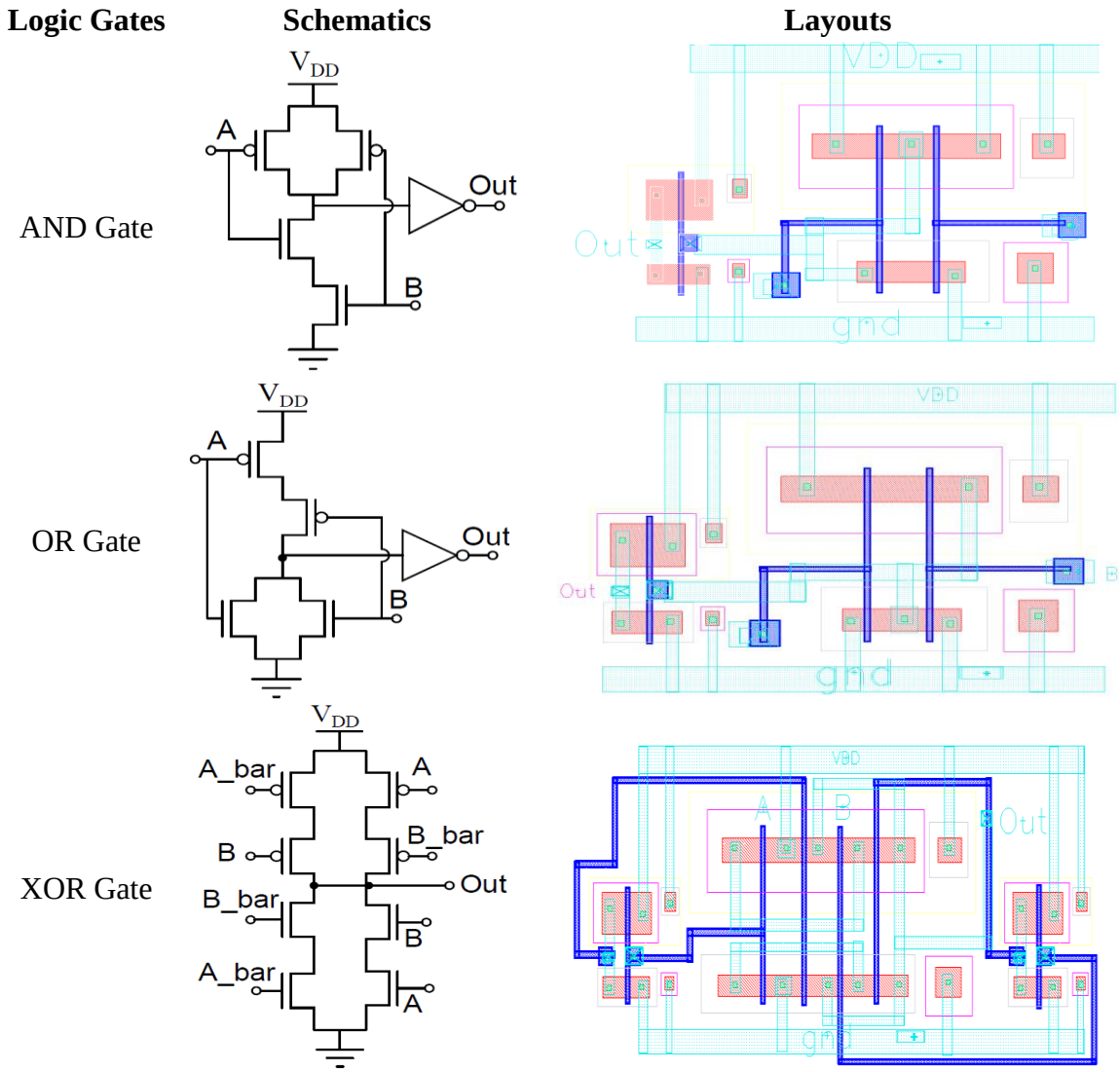


Figure 3.4: Schematics and layouts of logic gates using Static-CMOS logic family

This logic style is reported to give negligible DC power consumption, as there is no direct path form between power supply and ground for any of the logic input combinations. The main drawback of this logic style is the substantial number of large PMOS transistors, resulting in high gate input capacitances which increase the delay, area requirements, relatively weak output driving capability due to series transistors in the output stage, and therefore high dynamic power consumption.

3.3.2. Pass Transistor (PT) Logic Family [25][26]

The schematics and layouts of logic gates using PT logic family are shown in Figure 3.5. Conventionally, the PT logic is built from an NMOS network topology. It requires minimum MOS's to implement logic function very effectively. Primary input signals drive gates and source-drain terminals only, which facilitates the usage and characterization of logic cells.

This PT topology do not have direct path from supply voltage to ground, due to this, standby power consumption is approx. zero.

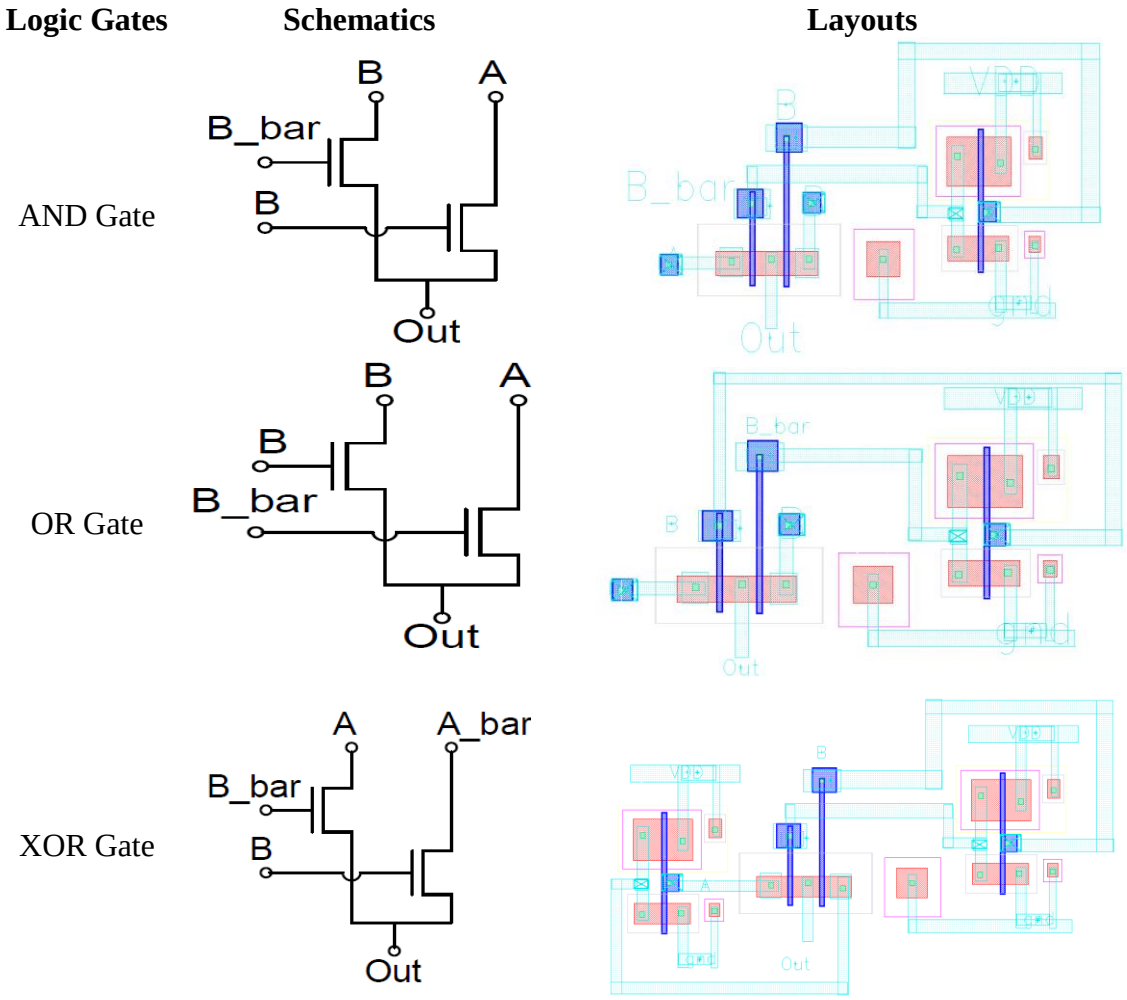


Figure 3.5: Schematics and layouts of logic gates using PT logic family

The PT logic also gain their speed and power advantage due to high logic functionality, reduced transistor count and node capacitance as compared to conventional Static-CMOS logic. However, this PT logic presents the inherent problem of the undesirable threshold voltage effects across a transistor which degrades the high level of PT output nodes and imposes the addition of level restoring transistors. It has poor noise margin.

3.3.3. Complementary Pass-Transistor Logic (CPL) [27]

The schematics and layouts of logic gates using CPL logic family are shown in Figure 3.6. CPL belongs to the conventional PT logic family which overcomes the problem of undesirable threshold voltage drop of NMOS transistor, benefits from the small input capacitances (NMOS network only) and improves the output driving capability. The CPL circuit consists of NMOS

PT logic driven by complementary inputs and producing complementary outputs driven by two CMOS inverters used as buffers.

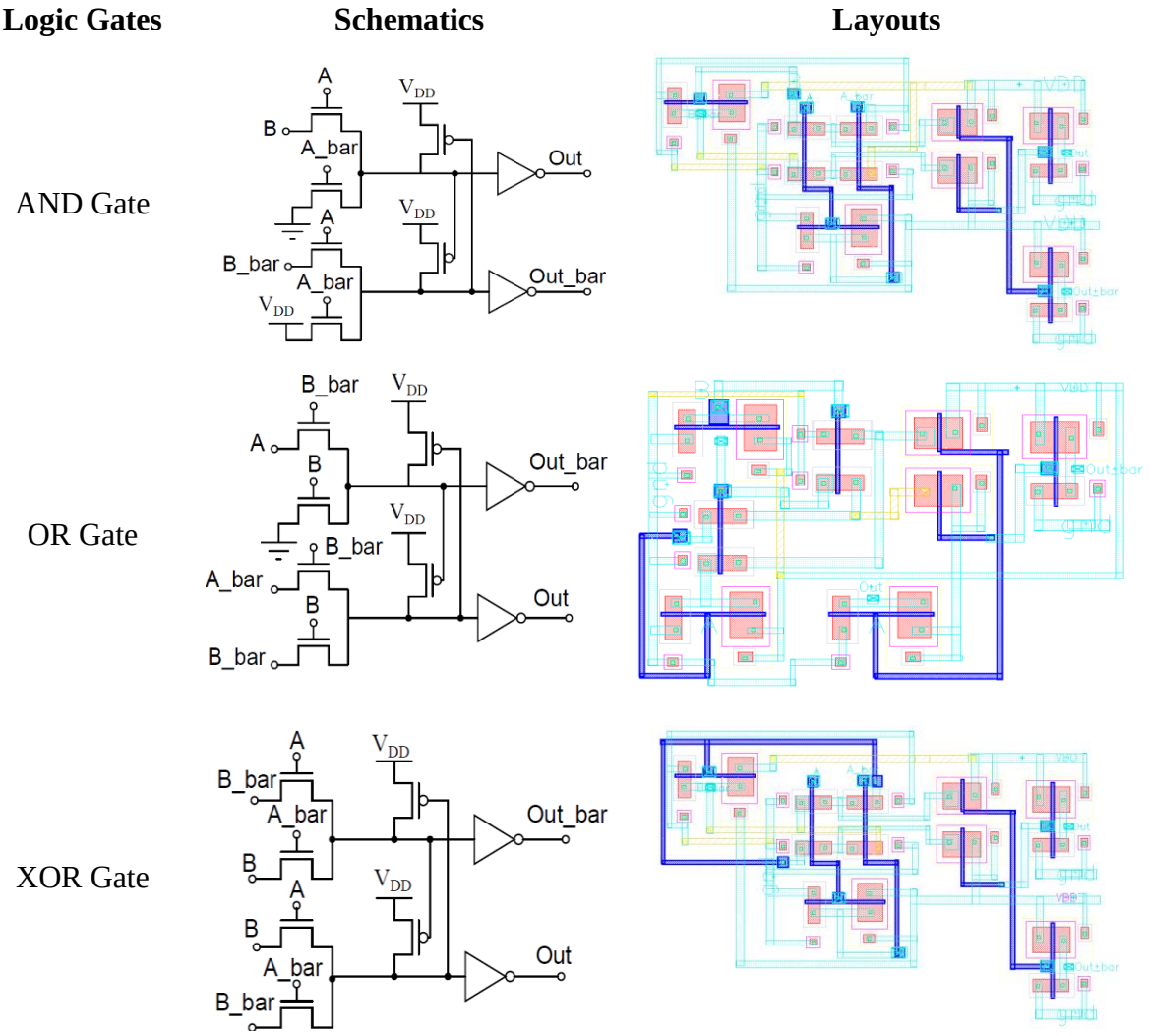


Figure 3.6: Schematics and layouts of logic gates using CPL logic family

However, at lower supply voltage, CPL circuit suffers the inherent problem of the threshold drop across the NMOS transistor, which results in reduced current drive and slower operation at reduced supply voltages which proves that it is not suited for sub-threshold design technique. In comparison to the conventional Static-CMOS logic, this logic is having larger short-circuit currents and higher wiring overhead due to dual-rail signals, hence increases the overall power consumption.

3.3.4. Swing Restored Pass-Transistor Logic (SRPL)[28]

The schematics and layouts of logic gates using CPL logic family are shown in Figure 3.7. SRPL is modified version of CPL which is used to implement high-speed and low-power logic circuit for VLSI applications. The generic construction of this SRPL logic gate consists of two

main parts. First, is the latch type swing restoring circuit which combines two cross coupled CMOS inverters to dive the gate output and the second part is complementary output of n channel devices based PT logic network. The complimentary outputs of the PT logic network are restored to full swing by the swing restoration circuit.

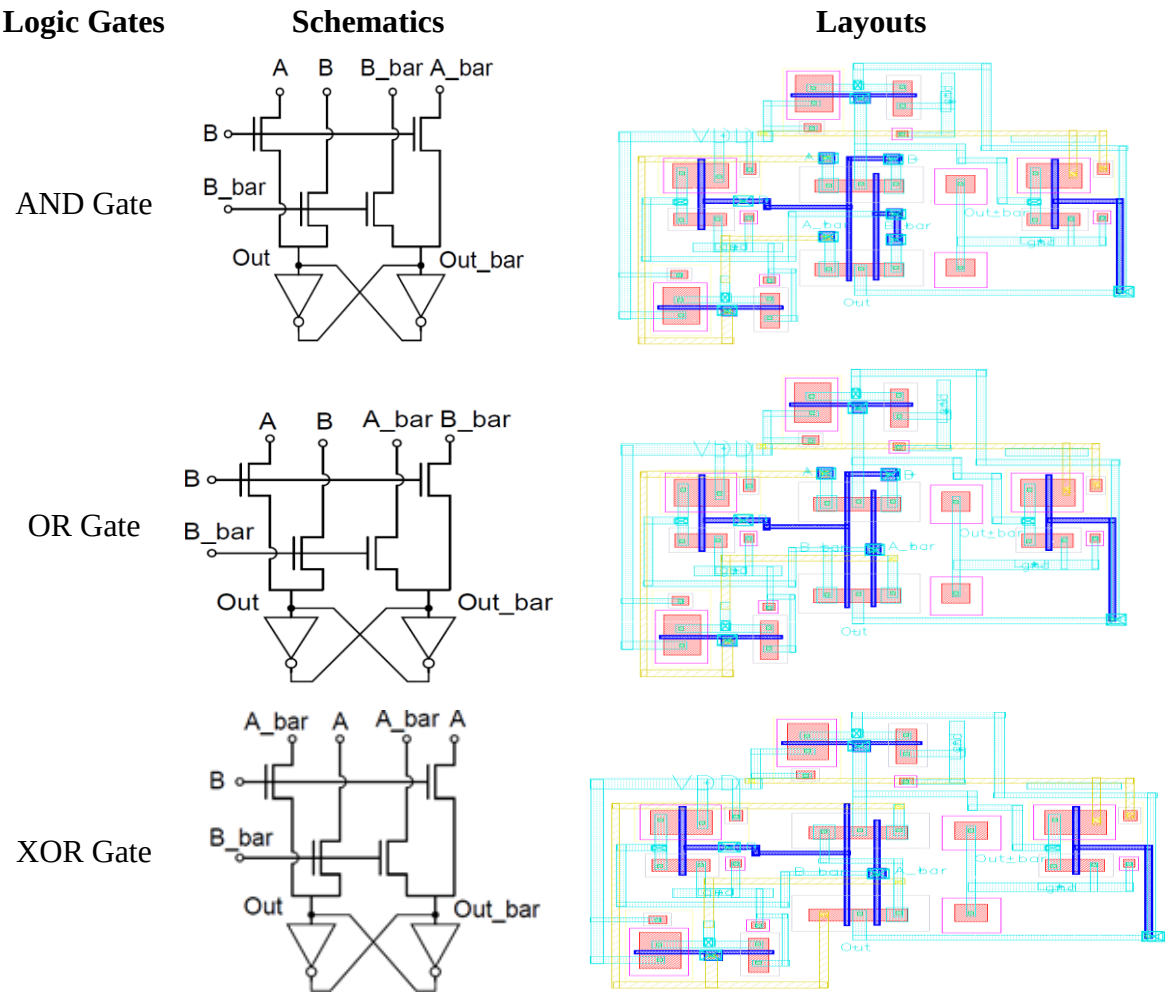


Figure 3.7: Schematics and layouts of logic gates using SRPL logic family

Area and power reduction are also facilitated by its structure due to low transistor count and the low-input capacitance. SRPL overcomes the noise margin problems present in CPL. But, the SRPL performance is not good as claimed in paper [24]. The reason is quite unknown. Overall result in terms of power and performance shows that it is well suited in sub-threshold design technique.

3.3.5. Double Pass-Transistor Logic (DPL) [29]

The schematics and layouts of logic gates using DPL logic family are shown in Figure 3.8. DPL overcomes the noise margin and speed degradation problems occur in CPL and SRPL at

reduced power supply. It works efficiently in sub-threshold region and meets the requirement of power efficient arithmetic circuits. DPL circuit consists of symmetrical arrangement of both PMOS transistor branches in parallel with NMOS-tree which avoids the series sizing issues of the full static circuits.

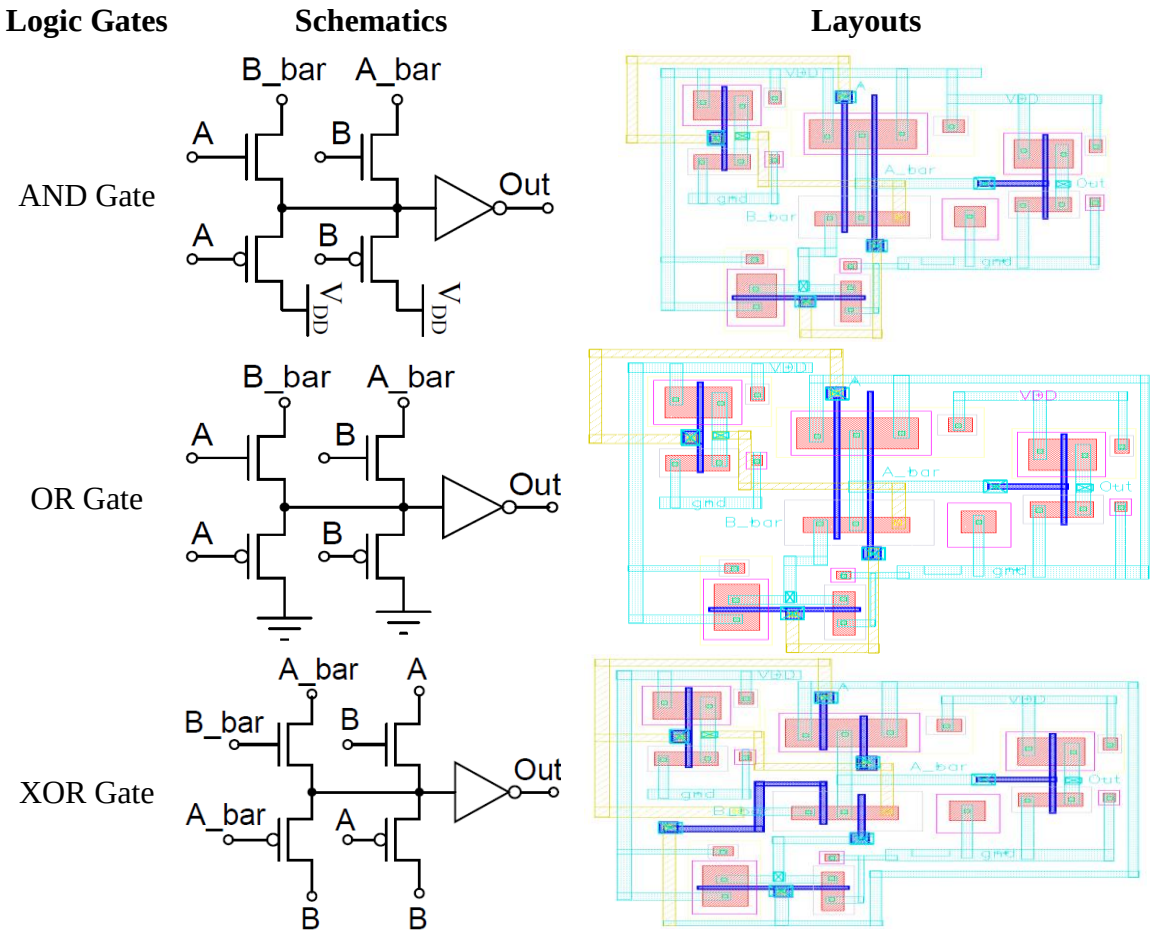


Figure 3.8: Schematics and layouts of logic gates using DPL logic family

It attains full-swing operation. As a result, for each input combination, these PMOS and NMOS transistors always posses dual current path, resulting in smallest equivalent resistance compared to other logic styles.

DPL gates are symmetrical whereby the load in them is distributed equally among the inputs. The basic gates AND/NAND, OR/NOR, XOR/XNOR can be constructed by simply exchanging the input nodes. The main drawback of DPL is its redundancy, i.e. it requires more transistors than actually needed for the realization of a function. DPL is one of the power efficient logic style among the discussed logic styles by Uming et al. [24].

3.3.6. Transmission Gate Logic (TG) [30]

The schematics and layouts of logic gates using TG logic family are shown in Figure 3.9.

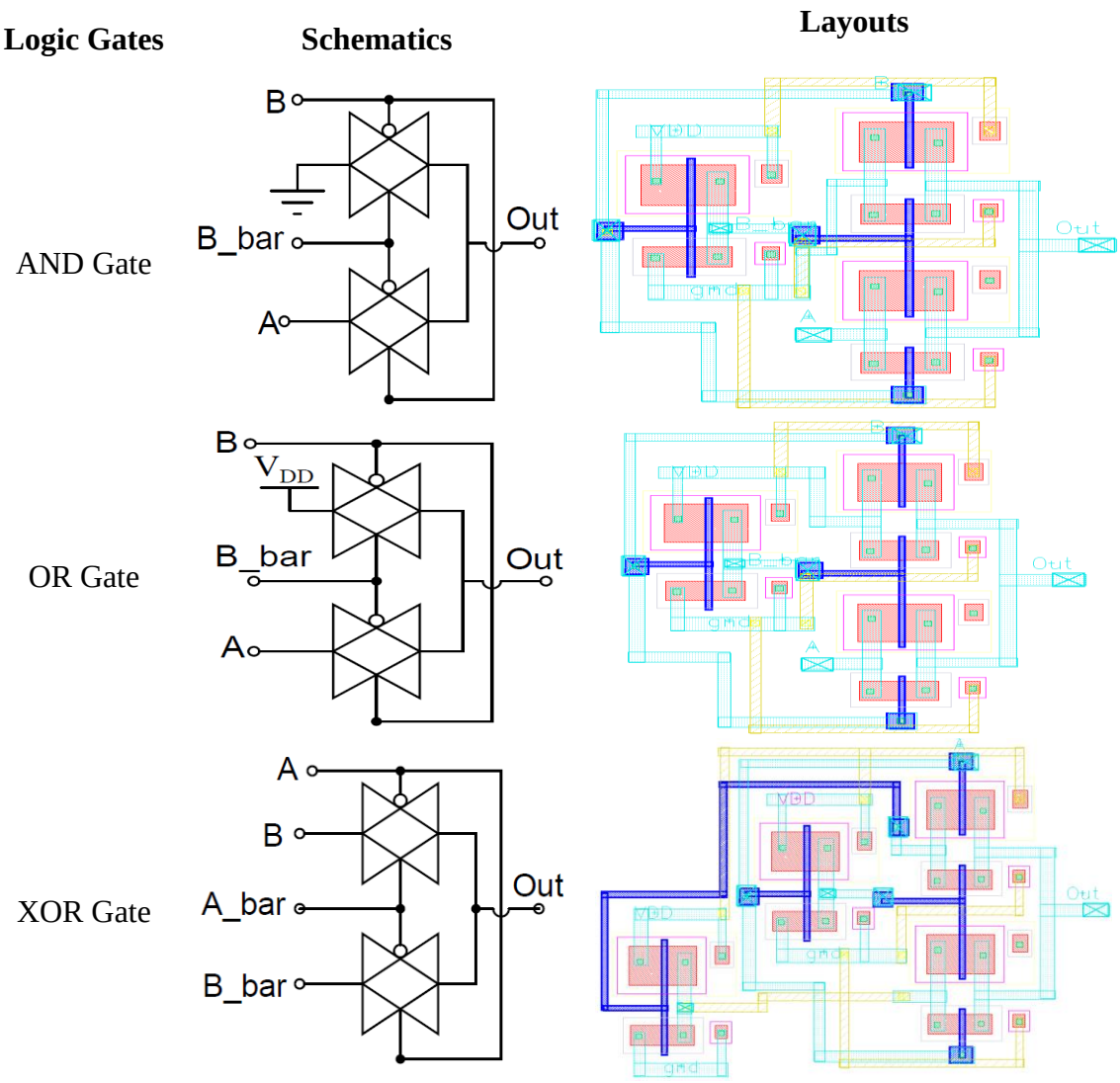


Figure 3.9: Schematics and layouts of logic gates using TG logic family

As discussed, poor conduction of logic 1 by NMOS transistors in PT logic families results in voltage degradation and poor noise margin. To overcome these issues, lot of modification has been done in the PT logic family. TG logic is well known and one of the best logic family which enables rail-to-rail swing, improves noise margin and works efficiently in sub-threshold region. The TG circuitry has two paths but the same input is passed along both paths in contrast to DPL family.

It has the lower transistor count which provides high logic functionality, improving speed in low supply voltage but unbalanced input capacitance as compared to Static-CMOS logic gates.

3.3.7. Comparative Analysis of Basic Logic Gates using Different Logic Families for Sub-Threshold Operation

This section gives the comparative analysis of AND, OR and XOR gates using Static-CMOS logic, PTL logic, CPL logic, SRPL logic, DPL logic and TG logic families.

Table 3.1-3.3 gives the measured power, delay and power-delay product of logic these three gates using Static-CMOS logic style, TG, PT, SRPL, CPL and DPL logic families at 0.4V power supply voltage for sub-threshold operation. These results show that all gates are properly functional at supply voltage as low as 0.4 V. The schematic and layouts are designed and simulated using two different technology (45 nm / 180 nm). The design metrics are characterized in terms of power, delay and power delay product (power-delay product). The power consumption is least at minimum size of both NMOS and PMOS in sub-threshold region. For minimum power-delay product, the W/L's of all designed logic gates are kept in the ratio of 2:1 for the pull up and pull down network respectively.

Table 3.1: Simulation results for AND Gate

Logic Style	**Number of Transistors**	**Power (nW)**		**Delay (ns)**		**Power-Delay Product (watt*sec10^{-18})**	
		45 nm	**180 nm**	**45 nm**	**180 nm**	**45 nm**	**180 nm**
Static-CMOS	6	0.938	0.255	0.181	28.14	0.1697	07.175
TG	6	0.588	0.231	**0.120**	**27.42**	**0.0705**	**06.334**
PT	14	**0.363**	**0.209**	1.250	39.60	0.4537	08.276
CPL	14	1.030	0.388	5.006	45.40	5.1562	17.615
SRPL	12	1.176	0.623	12.58	45.24	014.79	28.184
DPL	10	4.911	0.796	4.949	86.10	24.304	68.530

Table 3.2: Simulation results for OR Gate

Logic Style	**Number of Transistors**	**Power (nW)**		**Delay (ns)**		**Power-Delay Product (watt*Sec10^{-18})**	
		45 nm	**180 nm**	**45 nm**	**180 nm**	**45 nm**	**180 nm**
Static-CMOS	6	1.231	0.322	1.567	52.210	01.927	16.811
TG	6	0.592	0.299	**0.162**	**20.540**	**00.096**	**06.141**
PT	14	**0.491**	**0.305**	0.688	57.400	00.338	17.510
CPL	14	1.639	0.572	5.258	44.900	08.617	25.682
SRPL	12	1.203	0.844	13.100	48.920	15.750	41.288
DPL	10	5.610	1.089	5.245	78.700	29.424	85.704

Table 3.3: Simulation results for XOR Gate

Logic Style	Number of Transistors	Power (nW)		Delay (ns)		Power-Delay Product (watt*sec10^{-18})	
		45 nm	**180 nm**	**45 nm**	**180 nm**	**45 nm**	**180 nm**
Static-CMOS	12	1.621	0.399	2.378	58.020	3.854	23.140
TG	8	0.628	0.362	**0.342**	**31.410**	**0.215**	**11.106**
PT	6	**0.539**	**0.225**	0.699	073.20	0.376	16.470
CPL	14	1.891	1.015	6.088	52.170	11.512	52.950
SRPL	12	1.659	1.334	13.215	59.540	21.923	79.420
DPL	10	6.128	2.007	6.665	55.320	40.843	111.027

From Table 3.1, 3.2 and 3.3, it is observed that at the system level, the single ended logic families do not work properly due to degraded output voltage level for sub-threshold operation. Generally, having a large delay and power spread at the gate level itself is not desirable because when these gates are used at system level the spread will add cumulatively which leads to a poor system power-delay product.

It is observed that CPL, DPL and SRPL have the poor power-delay product because of poor noise margin, low noise immunity and output voltage degradation. Therefore, it is unsuitable for practical application at ultra-low power supply voltages. One of the drawbacks of these logic families is that it requires more transistors due to differential implementation of a function.

Key Points: The Static-CMOS, TG and PT logic family having less (TG with lowest) power-delay product and also possess the advantage of reliability and simpler designs at both technology nodes (45 nm / 180 nm). Migrating from 180 nm to 45 nm shows same trend but reduces the overall power-delay product for all different logic families.

Hence Static-CMOS, PT and TG have been chosen to implement CLA, KS and HC adders.

3.4. EFFECT OF REVERSE BODY BIAS (RBB) SCHEME

In order to minimize the power consumption and improve the performance in sub-threshold arithmetic circuits, body biasing scheme has been investigated which manage threshold voltage (V_{th}) and power supply voltage (V_{DD}) at the same time. For instance, effective body biasing techniques can adjust the transistor V_{th} to compensate for changes in the transistor as the product ages. It can also adjust the transistor V_{th} for temperature fluctuation, maintaining a uniform performance and thus adjusting leakage current.

RBB scheme is well suited for devices with low threshold voltages and power supply voltages below threshold because at high power supply voltage band-to-band tunneling raises the junction leakage dramatically. Therefore, it works efficiently in sub-threshold region [31].

In the conventional configuration, the bulk terminal of both NMOS and PMOS devices are tied to ground and V_{DD} respectively. This type of bulk connection prevents forward body biasing at the source/drain-to-bulk p/n+ junctions in normal region of operation (V_{DD} above than threshold voltage). Under RBB, the bulk terminal of both the devices is interchanged i.e. PMOS tied to ground and NMOS tied to V_{DD} in sub-threshold region of operation, a noticeable increase in the drain current is observed which leads to increased switching speeds and potentially dissipating power. This is due to high electric field across a reverse biased p-n junction which causes significant current to flow through the junction due to tunneling of electrons from the valence band of the p-region to the conduction band of the n-region (Band-To-Band-Tunneling (BTBT)) [32].

The cross-sectional view of NMOS with their six short-channel leakage currents (I_1- I_6) operated in sub-threshold region mechanisms is illustrated in Figure 3.10. The body terminal is connected at V_{DD} in contrast to conventional N-MOS.

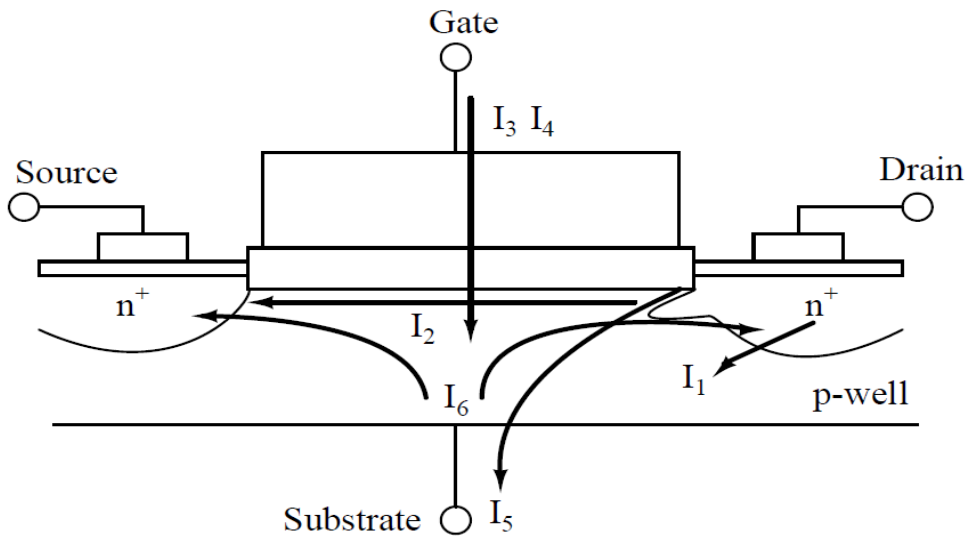


Figure 3.10: Cross sectional view of N-MOS with all leakage currents

Where,

I_1 = reverse-bias pn junction leakage current;

I_2 = sub-threshold current;

I_3 = oxide tunneling current;

I_4 = gate current due to hot-carrier injection;

I_5 = gate-induced drain lowering current;

I_6 or I_{RBB} = reverse body bias current;

I_{RBB} is the additional current flow in NMOS due to band-to-band tunneling of electrons.

The effect of RBB on performance is investigated in CMOS inverter circuit as shown in Figure 3.11

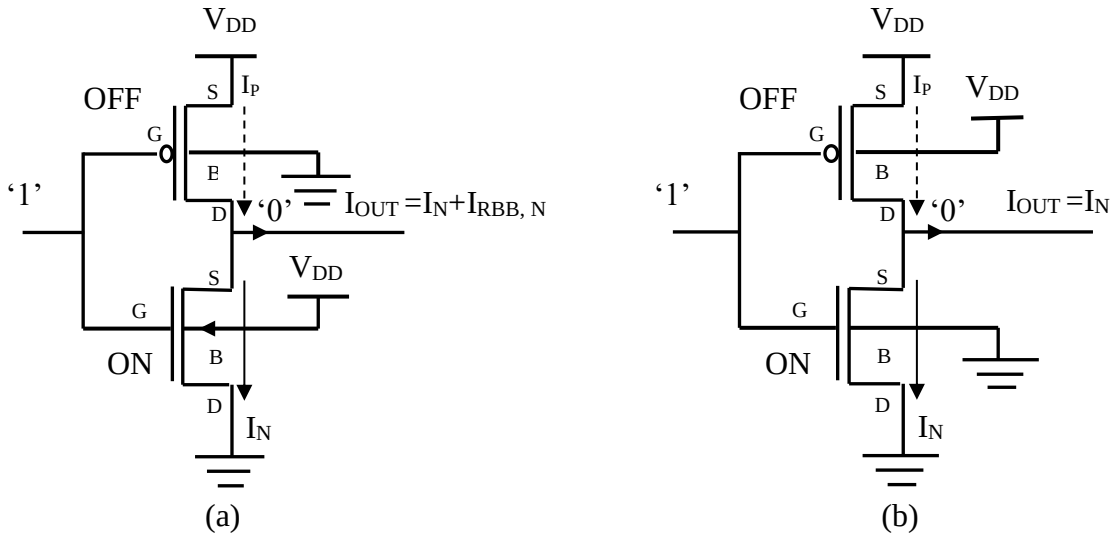
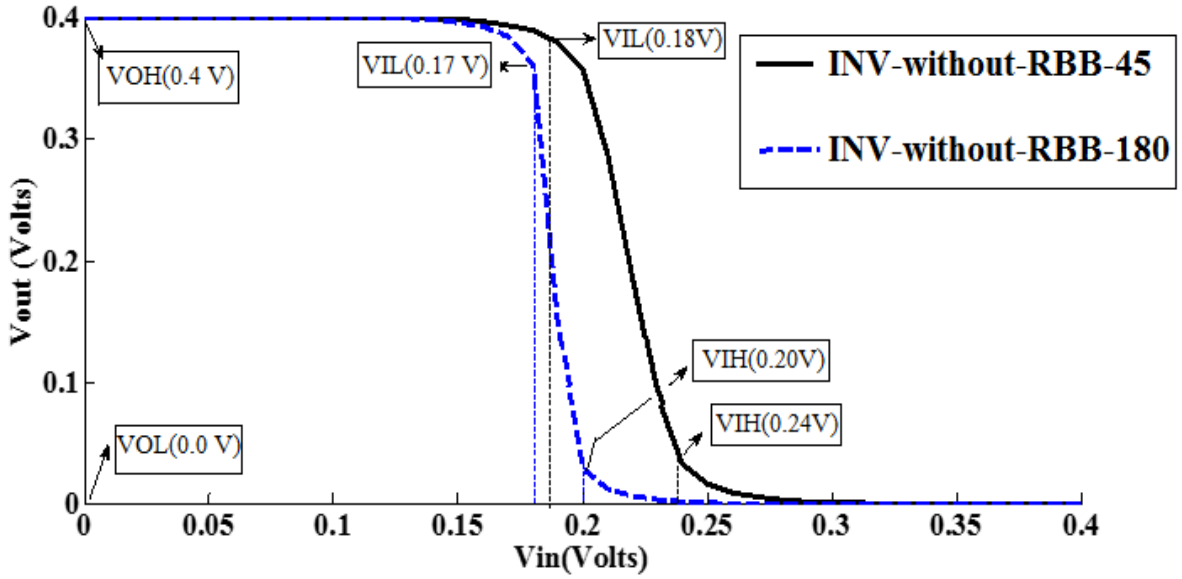
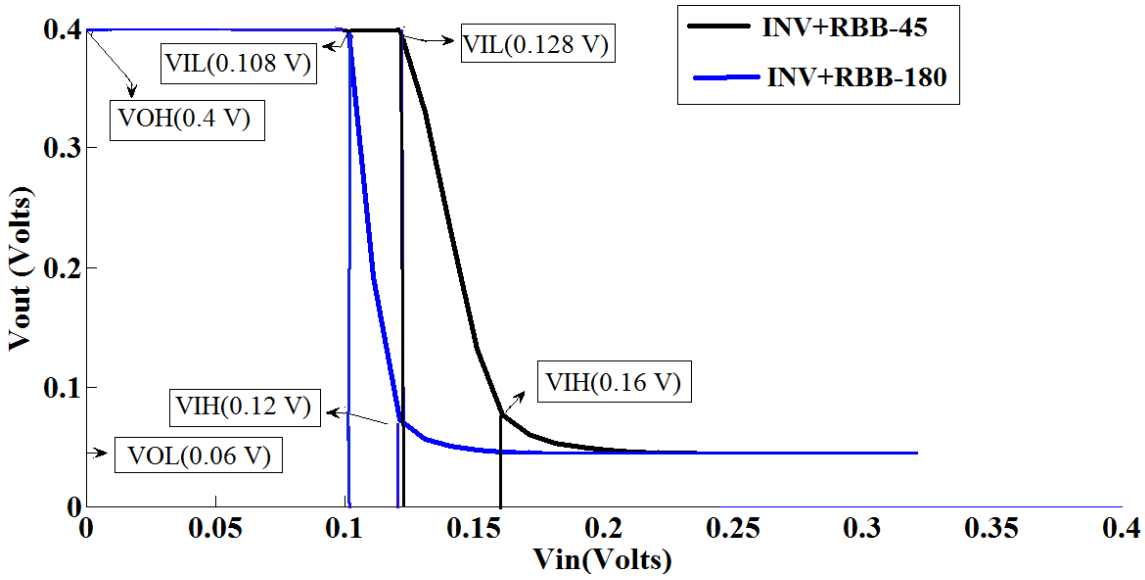


Figure 3.11: Schematic diagram of CMOS inverter (a) with RBB (b) without RBB

The voltage transfer characteristic (VTC) of CMOS inverter with/without RBB at both technology nodes is shown in Figure 3.12.



(a)



(b)

Figure 3.12: VTC's of CMOS inverter (a) with RBB (b) without RBB

Noise margin calculations of CMOS inverter with/without RBB are given in Table 3.4.

Table 3.4: Noise margin of CMOS inverter with/without RBB

Parameters	**Inverter at 45 nm**		**Inverter at 180 nm**	
	Voltage (V) With RBB	**Voltage (V) Without RBB**	**Voltage (V) With RBB**	**Voltage (V) Without RBB**
V_{IH}	0.160	0.24	0.120	0.20
V_{IL}	0.128	0.18	0.108	0.17
V_{OH}	0.400	0.40	0.400	0.40
V_{OL}	0.060	0.00	0.060	0.00
NM_L (V_{IL}- V_{OL})	**0.068**	0.18	**0.048**	0.17
NM_H (V_{OH}- V_{IH})	0.24	0.16	0.28	0.20

Table 3.4 shows that, with RBB, Noise-Margin high (NM_H) value increases as technology scales down. But at both, 45/ 180 nm technology, Noise-Margin high (NM_L) value is very small (0.068/ 0.048V) which leads to reduced noise insensitivity of circuits.

In reference to Figure 3.10 and 3.11, with RBB and without RBB, the total current of PMOS (or NMOS) i.e. I_P (or I_N) = I_1+ I_2+ I_3+ I_4+ I_5 + $I_{RBB, P}$ (or $I_{RBB, N}$) = RBB current in PMOS (or NMOS).

Graph in Figure 3.13 shows nearly 2.3 × increment in I_{OUT} current with RBB in CMOS inverter simulated at 45 nm. This can reduce the delays significantly.

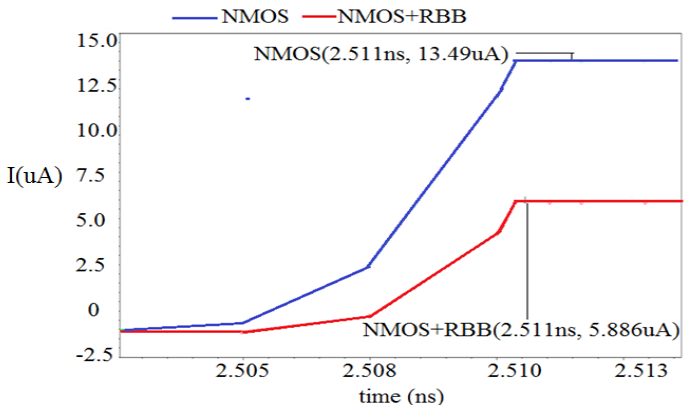


Figure 3.13: Current characteristics of NMOS in CMOS inverter with RBB/without RBB at 45 nm technology

Due to this extra current (I_N) in NMOS, the magnitude of the overall current in CMOS inverter with RBB increased which leads to increased switching speeds at cost of increase in power-delay product as shown in Table 3.5. The frequencies of CMOS logic gates with RBB scheme are observed to be higher than conventional body biasing scheme at low voltages [19].

Table: 3.5: Simulation results for Inverter with/without RBB at 0.4V

Module Name	Power (nW)		Delay (ns)		Power-Delay Product (watt*sec 10^{-18})	
	With RBB	Without RBB	With RBB	Without RBB	With RBB	Without RBB
Inverter (45 nm)	1.18	**0.421**	**0.014**	0.033	0.016	**0.014**
Inverter (180 nm)	0.127	**0.072**	**0.645**	0.845	0.081	**0.061**

The detailed analysis of AND, OR and XOR logic gates using six different logic families with RBB scheme is given in section 3.4.1.

3.4.1. Simulation Results of Logic Gates with RBB using Different Logic Families

This section gives the design and comparative analysis of AND, OR and XOR gates with RBB scheme using Static-CMOS logic, PTL logic, CPL logic, SRPL logic, DPL logic, TG logic families. Table 3.6-3.8 gives the measured power, delay and power-delay product of logic gates using Static-CMOS logic style, TG, PT, SRPL, CPL and DPL logic families at 0.4V power supply voltage for sub-threshold operation.

The schematic and layouts are designed and simulated using two different technology (45 nm / 180 nm).

The obtained simulation waveforms confirmed proper function of all gates at supply voltage as low as 0.4 V. The basic gates are characterized in terms of power, delay and power-delay product.

For minimum power-delay product, the W/L's of all designed logic gates were kept in the ratio of 2:1 for the pull up and pull down network respectively.

Table 3.6: Simulation results for AND Gate with RBB

Logic Style	Number of Transistors	Power (nW)		Delay(ns)		Power-Delay Product (watt*sec10^{-18})	
		45 nm	180 nm	45 nm	180 nm	45 nm	180 nm
Static-CMOS	6	1.123	0.375	0.155	21.090	0.174	7.908
TG	6	0.612	0.329	**0.094**	**17.700**	**0.057**	**5.823**
PT	14	**0.401**	**0.239**	0.823	25.870	0.331	6.182
CPL	14	1.144	0.545	4.501	32.210	5.149	17.55
SRPL	12	1.352	0.799	10.25	35.220	13.581	28.140
DPL	10	5.041	0.899	4.758	55.400	23.985	49.800

Table 3.7: Simulation results for OR Gate with RBB

Logic Style	Number of Transistors	Power (nW)		Delay(ns)		Power-Delay Product (watt*sec10^{-18})	
		45 nm	180 nm	45 nm	180 nm	45 nm	180 nm
Static-CMOS	6	1.388	0.342	1.482	50.100	2.057	17.134
TG	6	0.603	0.341	**0.151**	**17.100**	**0.091**	**05.841**
PT	14	**0.502**	**0.315**	0.670	35.10	0.337	11.050
CPL	14	1.704	0.646	4.932	38.110	8.405	24.619
SRPL	12	1.331	0.779	11.501	43.010	15.307	33.504
DPL	10	5.714	1.149	5.041	70.300	28.804	80.774

Table 3.8: Simulation results for XOR Gate with RBB

Logic Style	Number of Transistors	Power (nW)		Delay(ns)		Power-Delay Product (watt*sec10^{-18})	
		45 nm	180 nm	45 nm	180 nm	45 nm	180 nm
Static-CMOS	12	1.746	0.540	2.305	53.250	4.024	28.755
TG	8	0.707	0.418	**0.201**	**29.810**	**0.142**	**12.460**
PT	6	**0.596**	**0.302**	0.622	69.10	0.370	20.86
CPL	14	1.906	1.385	6.011	49.140	11.456	68.050
SRPL	12	1.891	1.459	12.591	52.320	23.809	76.330
DPL	10	6.221	2.102	6.509	50.240	40.492	105.610

Key Points: The Static-CMOS, TG and PT logic family with RBB scheme shows less (with TG lowest) power-delay product at both technology nodes (45 nm / 180 nm). Migrating from 180 nm to 45 nm reduces the overall power-delay product for all different logic families. The

results conclude that Static-CMOS, PT and TG with RBB scheme, are three power efficient logic families. Hence these are used to implement CLA, KS and HC adder's in sub-threshold region in this chapter.

3.5. DESIGN AND ANALYSIS OF PARALLEL ADDERS

The power consumption and speed of adders depend upon the choice of logic design style and architectures. Since different logic and architectures are available consequently, it is important to explore the adders for different bit-widths in sub-threshold region. In this section, design and analysis of adders using three architectures (CLA, KSA and HCA) in three different logic families- Static-CMOS, TG, and PT logic style or their combination operated in sub-threshold region are presented. These adders are analysed in terms of power, delay and power-delay product. The effect of technology scaling is observed by implementing the designs at 45 nm / 180 nm technology nodes. The internal architecture of adders and their circuit implementations are given in following sections.

3.5.1. Design Implementation using CLA

In this section, the design of parallel adder is implemented using CLA architecture. The basic blocks of CLA are implemented using the logical Boolean expressions given by eq. (1) - eq. (4), discussed in section 3.2.1. The adder is implemented at different operand sizes as 4-bit, 8-bit, 16-bit, 32-bit and 64-bit using three different logic families in sub-threshold region.

Figure 3.14 and Figure 3.15 show block level diagram of 4-bit CLA as basic building unit for large operand size adders.

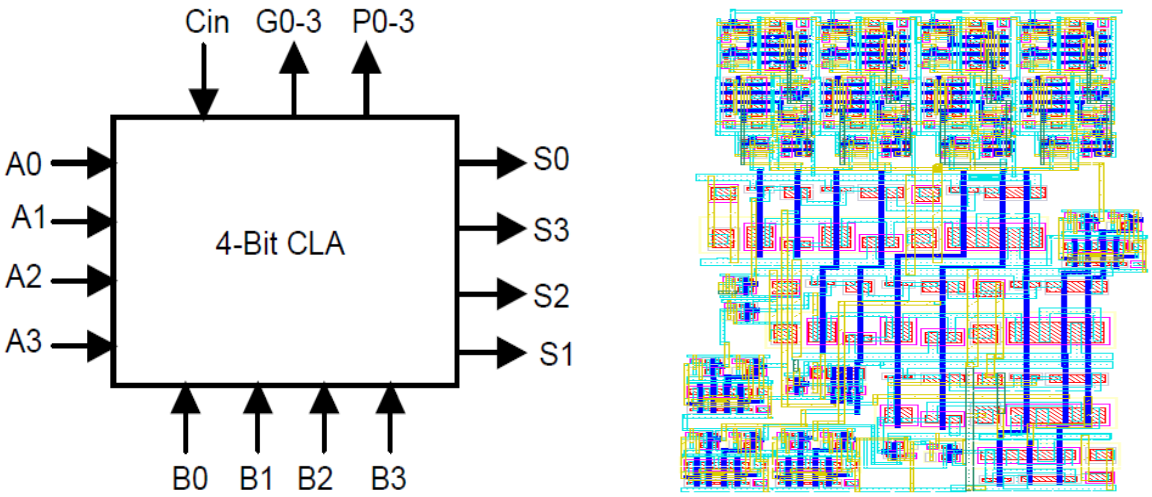


Figure 3.14: Basic block diagram of 4-bit CLA

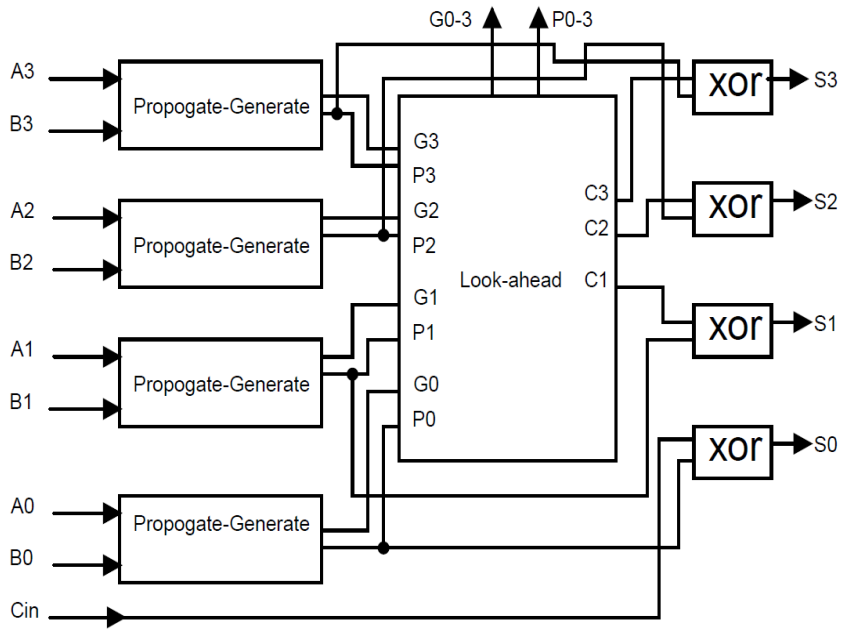


Figure 3.15: Internal blocks of 4-bit CLA

4-bit CLA blocks are used as basic building blocks to build large operand size CLA by combining these blocks hierarchically.

Block diagrams of 8-bit, 16-bit, 32-bit and 64-bits CLA's are shown in Figure 3.16 - Figure 3.19.

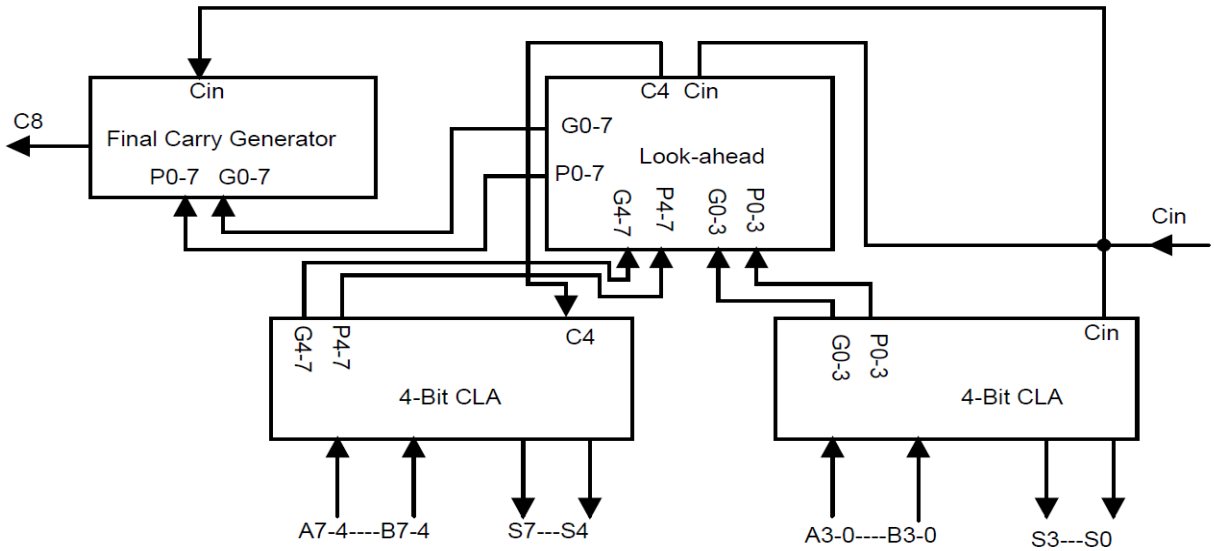


Figure 3.16: Block diagram of 8-bit CLA built using 4-bit CLA unit

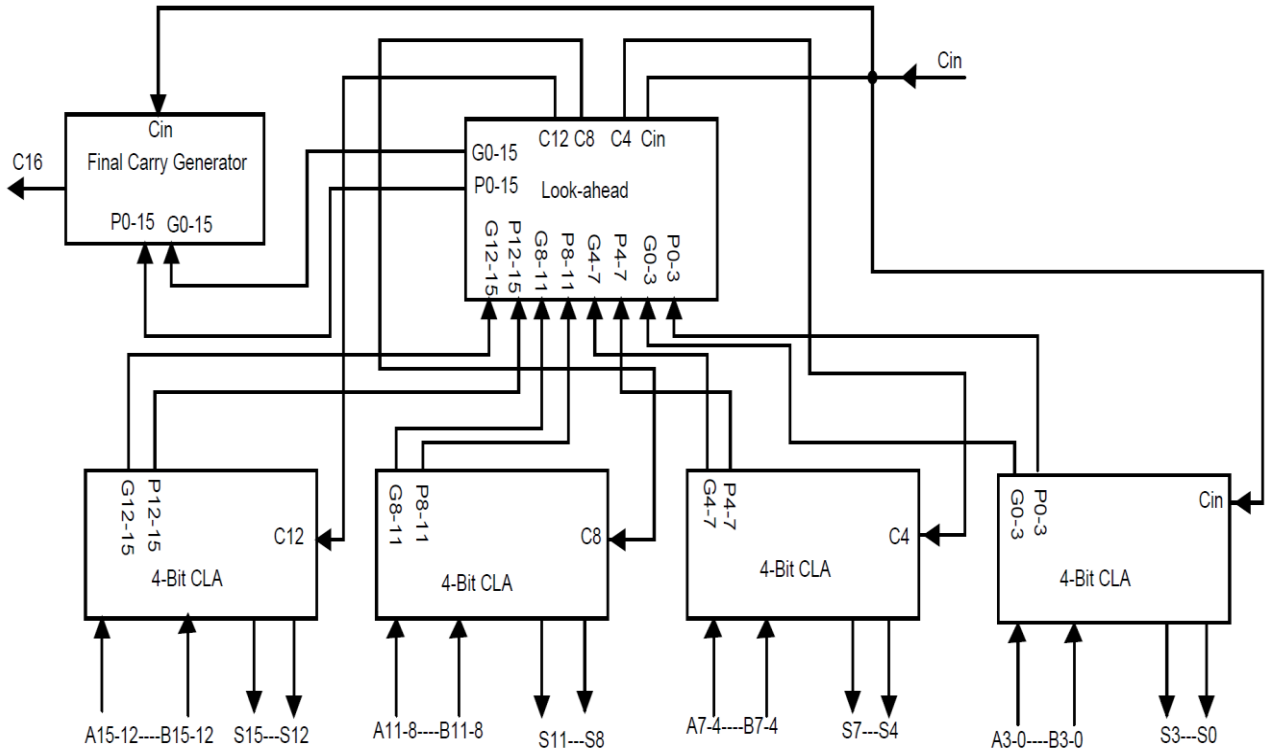


Figure 3.17: Block diagram of 16-bit CLA built using 4-bit CLA unit

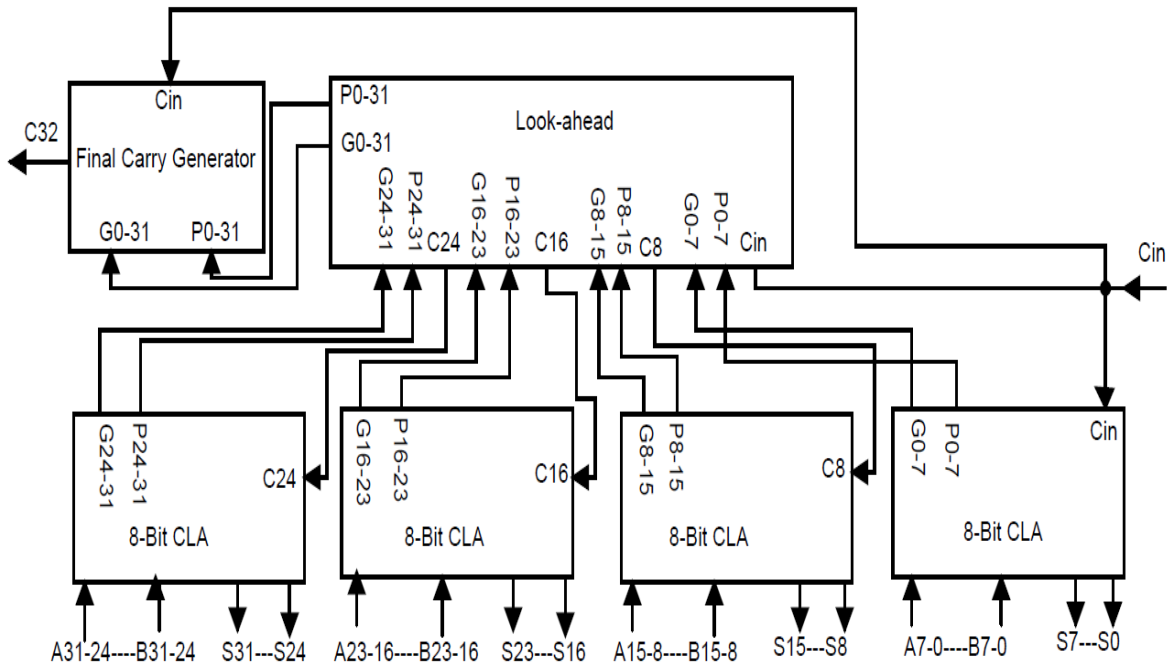


Figure 3.18: Block diagram of a 32-bit CLA built using 8-bit CLA unit

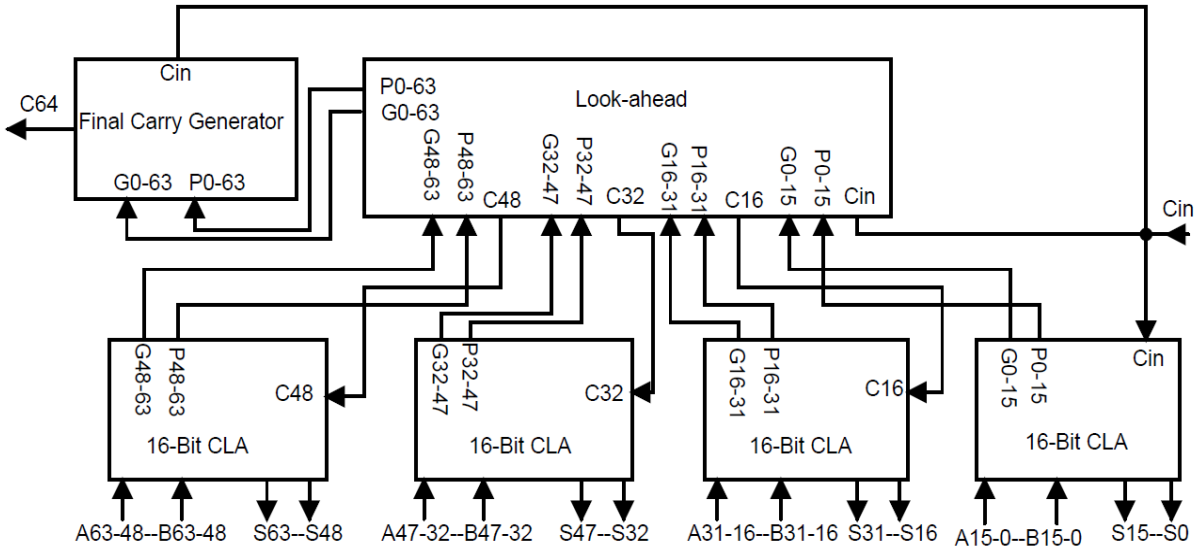


Figure 3.19: Block diagram of a 64-bit CLA built using 16-bit CLA unit

Based on the generate and propagate values, the look-ahead blocks compute the carry bits. The partial full adders (PFA) inside 4-bit CLA produce the sum values based on the inputs (A_i, B_i) and the carry input C_i value for each bit position. Final carry generator block generates the final carries (C_8, C_{16}, C_{32} and C_{64}) for 8-bit 16-bit, 32-bit and 64-bit CLA's respectively.

- The implementation of the 64-bit CLA is done using three hierarchical levels. The first level of the hierarchical structure in 64-bit CLA, computes carry values from look-ahead blocks, G0-3 and P0-3, are defined as “group Generate” and “group Propagate” of a group of 4-bits.

- In the second level, using the group generate and group propagate signals, the 16-bit carryout signals is obtained for each adder block as shown in Figure 3.19. The CLA logic creates three carry signals (C_{16}, C_{32}, and C_{48}) are being used as carry input to the 16-bit adder blocks and the C_{64} as the sum (S_{64}) signal. An extra final carry generator is used in contrast to conventional 64-bit CLA to generate the C_{64} as the sum (S_{64}) signal. This extra added final carry generator optimizes the levels of the carry chain which gives minimum area, power as well as delay in sub-threshold region. The delay of a CLA adder is dependent on the number of levels of carry logic, and not on the length of the adder. The conventionally designed 64-bit CLA using multi-level logic generally gives larger area with slower circuit than optimized three level of carry logic implementation. Thus, overall power-delay product of designed 64-bit CLA gets improved.

- The third level contains one Carry look-ahead generator. It is used to compute the input

carries for the Carry look-ahead generators in the second floor, and to compute the 'carry-propagated' and 'carry-generated' bits for the entire 64-bit. This bit can then be used either to compute the carry of the entire adder or to further extend the adder.

Conventional Static-CMOS, TG and PT logic families have been identified most suitable for designing more robust adder circuits operated in sub-threshold region [22] as discussed in section 3.3. Internal units of CLA with Static-CMOS, TG and PT logic families are discussed in following sections.

3.5.1.1. CLA with Static-CMOS Logic (Static-CMOS CLA)

The internal units (carry generator, group generate/propagate circuitry, bit-wise generate/propagate circuitry and sum generator circuitry) of CLA's are implemented using Static-CMOS logic are shown in Figure 3.20-Figure 3.24. Bit-wise generate/propagate circuitry and sum generator circuit are called as pre-computation and post-computation logic blocks.

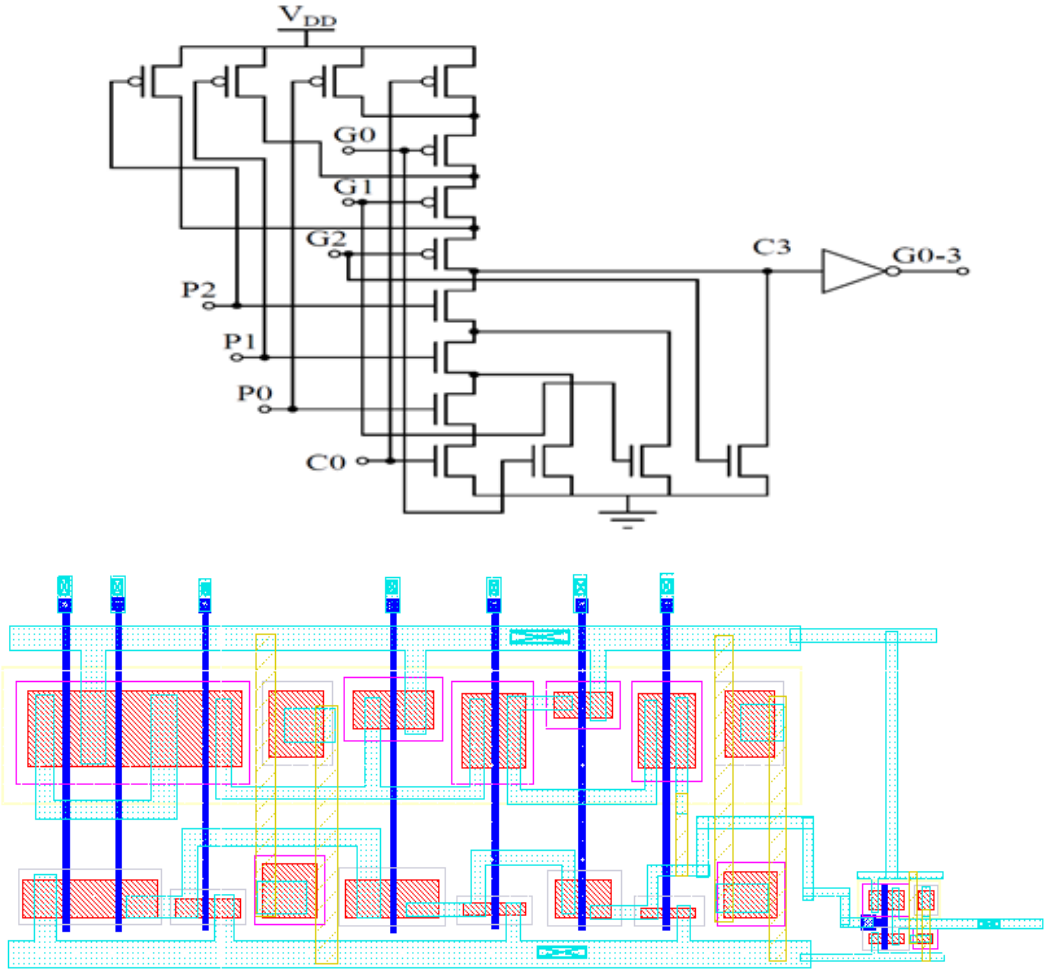


Figure 3.20: Circuit diagram of 4-bit group generate

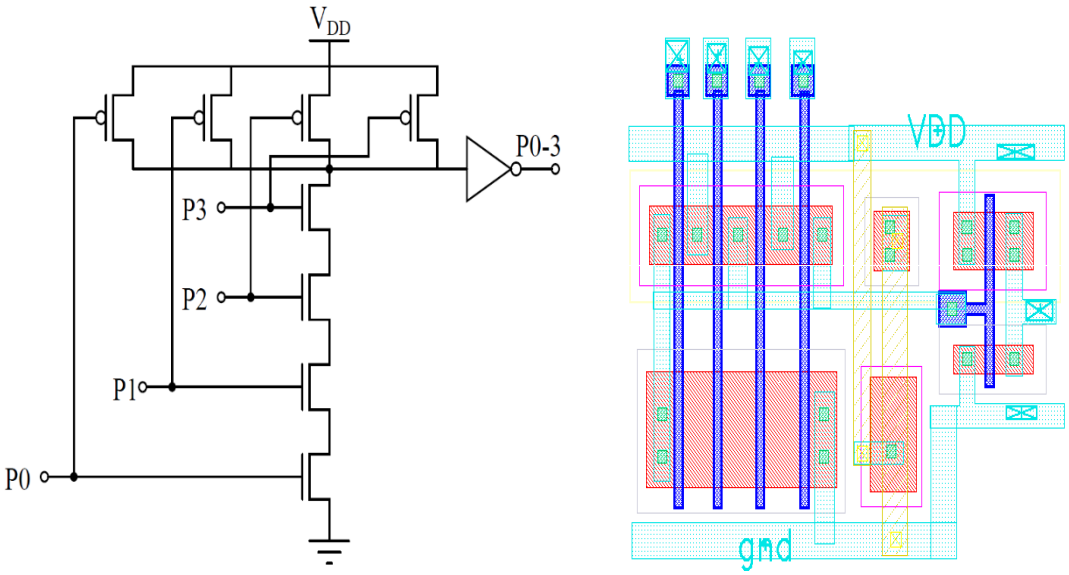
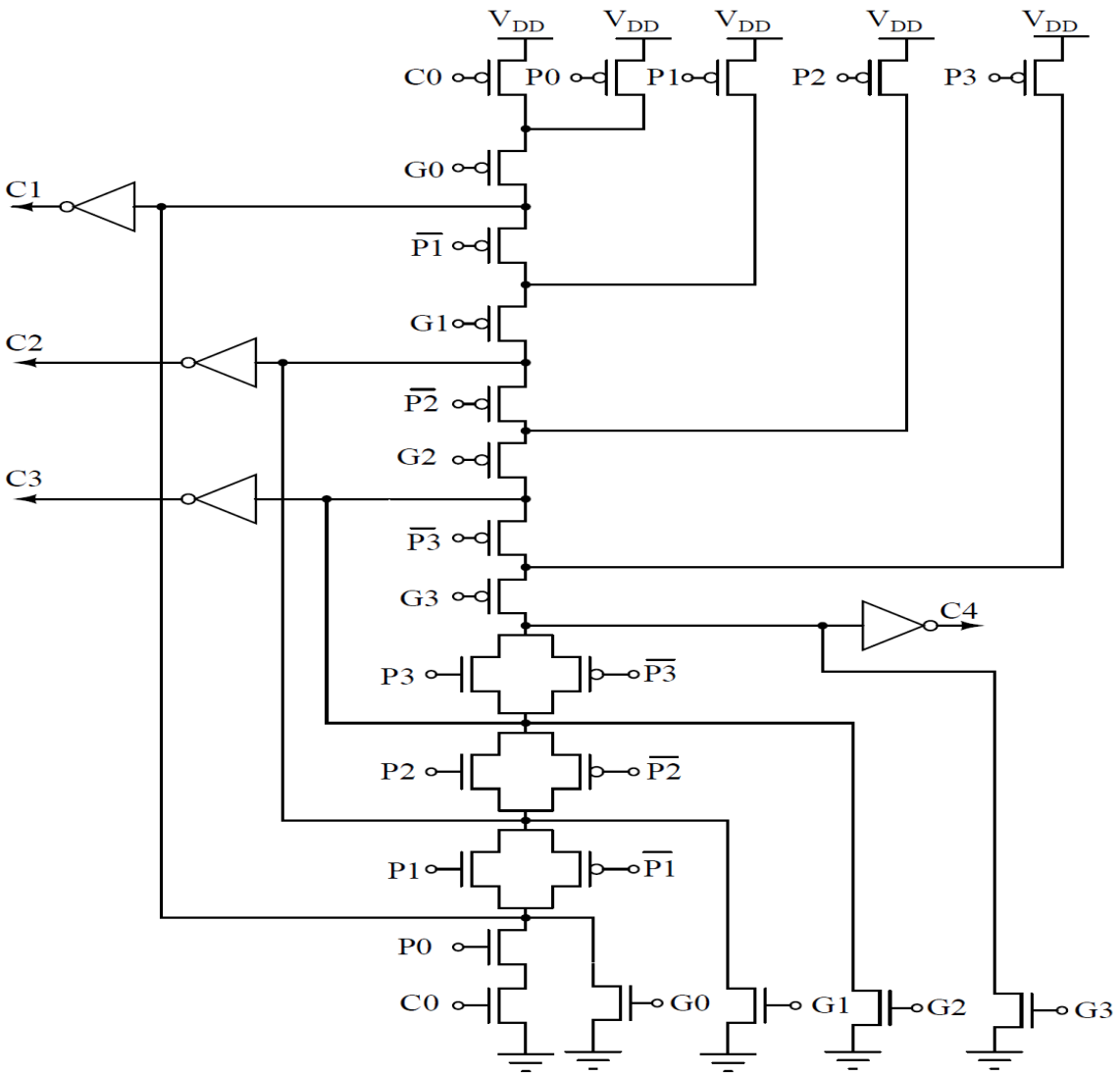


Figure 3.21: Circuit diagram of 4-bit group propagate



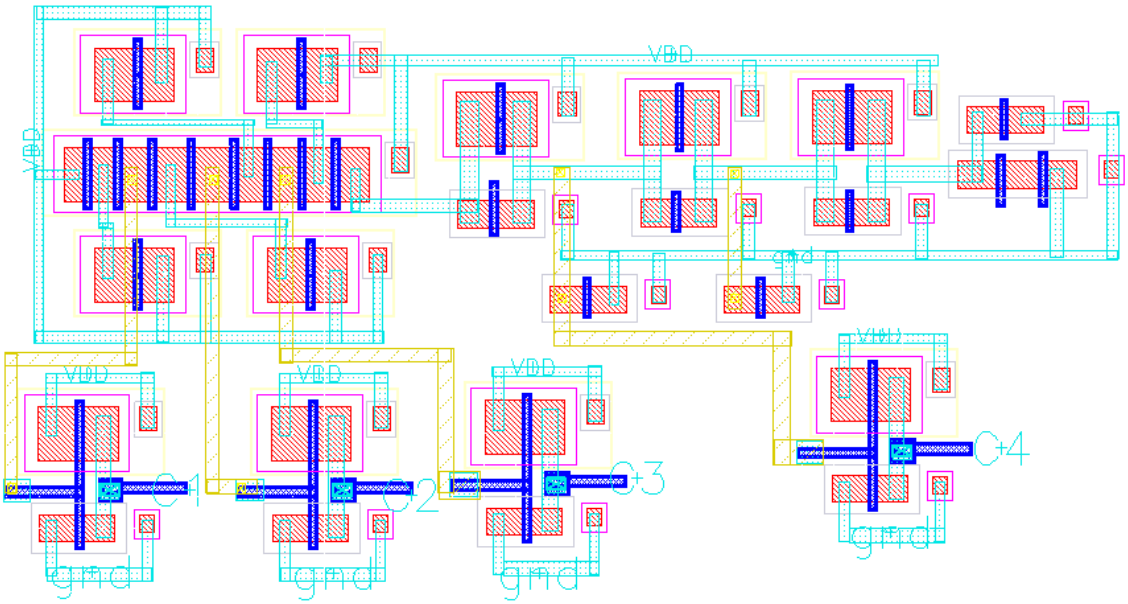


Figure 3.22: Circuit diagram of 4-bit carry generator

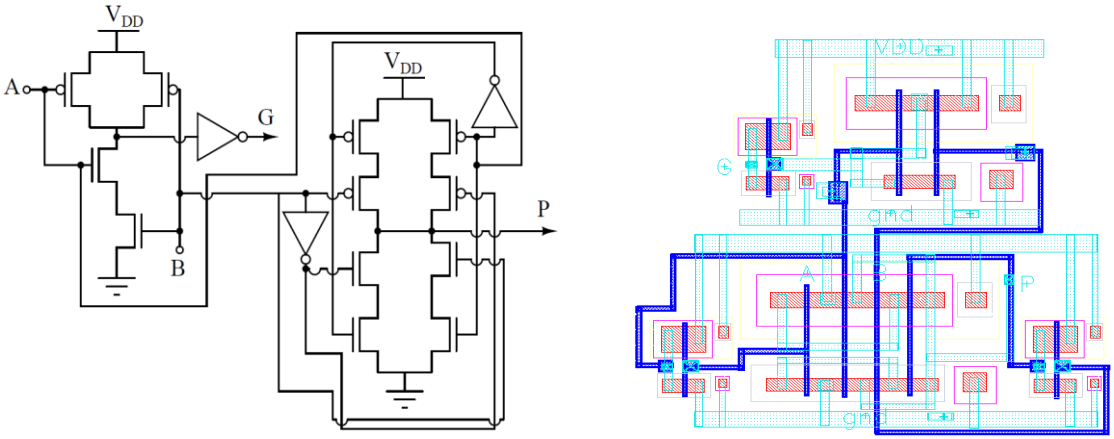


Figure 3.23: Circuit diagram of bit-wise generate/propagate

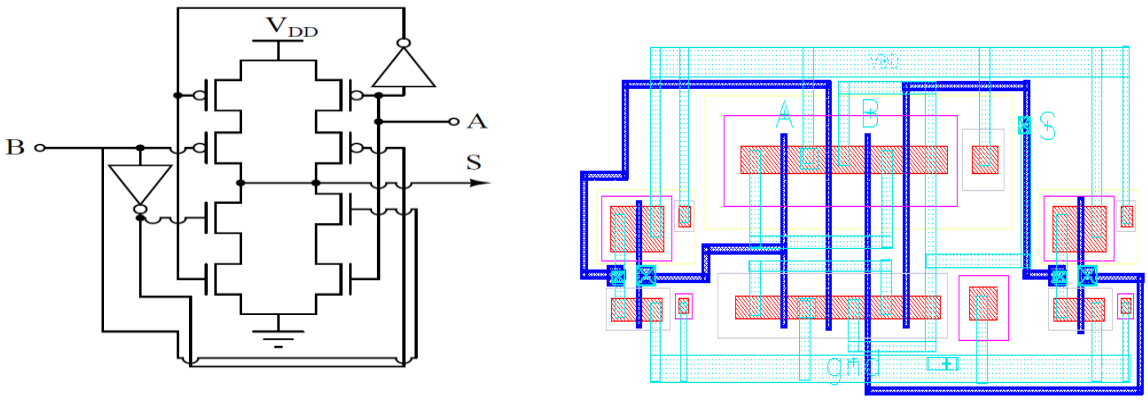


Figure 3.24: Circuit diagram of bit-wise sum-generator

3.5.1.2. CLA with Hybrid TG Logic (HYB-TG CLA)

Conventional TG logic leads to compact design but shows voltage degradation problem in two or more cascaded TG stage at ultra-low power supply voltage for sub-threshold operation. Therefore, to overcome this voltage degradation problem the implementation of circuits is done by coupling TG logic with Static-CMOS buffer at appropriate stages rather than using complete Static-CMOS or TG gate designs. The combination of Static-CMOS buffer with TG logic is represented here as HYB-TG logic.

The output buffer formed by the cascaded inverters is designed in such a way that the first inverter is half the size of the second inverter in order to cut down the power consumption.

To check for proper operation of HYB-TG logic with RBB, a series combination of TG and two Static-CMOS inverters (TG-2INV block), as shown in Figure 3.25, under following different conditions of body bias has been simulated and analysed.

- State a----TG1, 2INV without RBB
- State b----TG1, 2INV with RBB
- State c----TG1 without RBB, 2INV with RBB

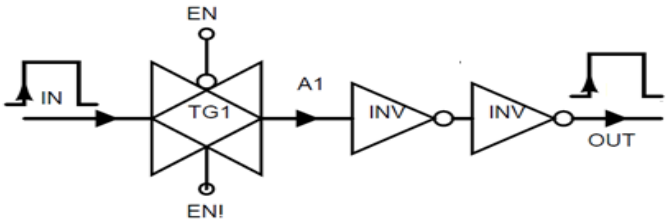


Figure 3.25: TG-2INV block

The results are given in Table 3.9 and wave forms at node 'OUT' are given in Figure 3.26.

Table 3.9: Operations of TG-2INV block

State	Enable [EN/EN! = 1 for NMOS = 0 for PMOS] (ON Condition)		Operation	Enable [EN/EN! = 0 for NMOS = 1 for PMOS] (OFF Condition)		Operation
	Input given at node IN (V)	Output at node OUT (V)	Turn ON	Input at node IN (V)	Output at node OUT (V)	Turn OFF
(a)	0.4	0.400	Proper	0.4	0.000	Proper
(b)	0.4	0.400	Proper	0.4	0.348	Not turning off properly
(c)	0.4	0.400	Proper	0.4	0.000	Proper

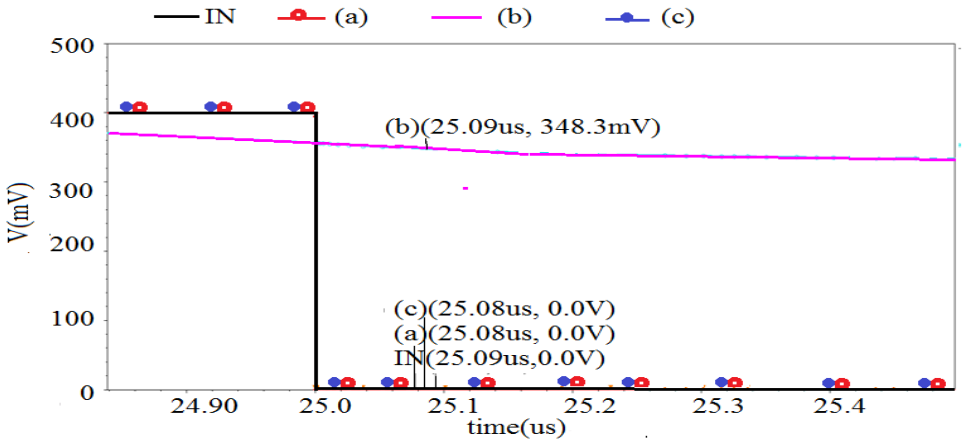


Figure 3.26: Graph for TG-2INV block at OFF condition

From the above results, it is clear that TG-2INV block operates properly for ON condition for all three states, whereas at OFF condition the output is not proper for state b. Therefore, in this adder, HYB-TG logic without RBB is used in design. Each output node in HYB-TG logic is followed by a buffer (which is composed of two inverters).

Further, only internal units like bit-wise generate/propagate circuitry and sum generator circuitry are designed using HYB-TG logic without RBB.

A complete adder implementation using HYB-TG logic with buffer showed increased power consumption during simulation results. Therefore, only simple circuits like bit-wise generate/propagate circuitry and sum generator circuit of CLA's are implemented using HYB-TG logic as shown in Figure 3.27 and Figure 3.28 respectively to get the advantage of reduced transistor count. Whereas (carry generator and group generate/propagate circuitry) of CLA's are implemented using Static-CMOS logic only.

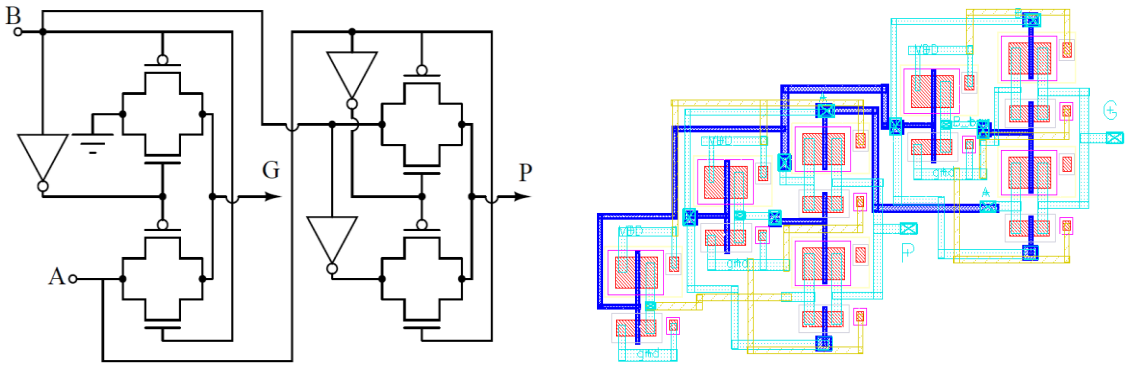


Figure 3.27: Circuit diagram of bit-wise generate/propagate

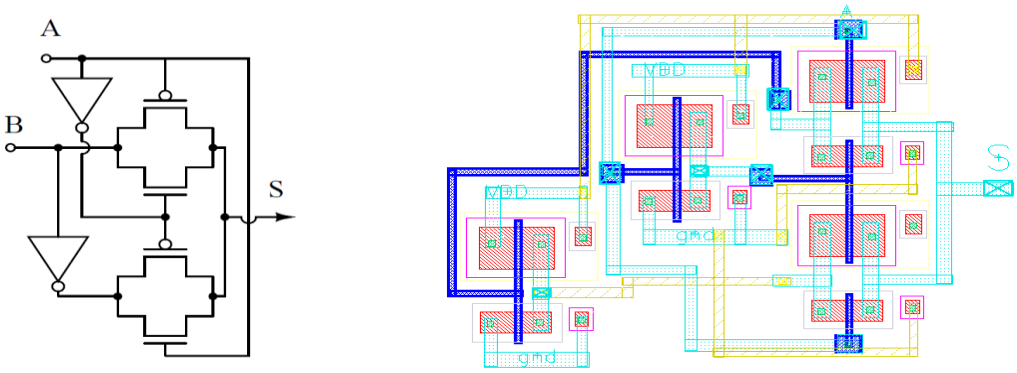


Figure 3.28: Circuit diagram of bit-wise sum-generator

3.5.1.3. CLA with Hybrid pass transistor Logic (HYB-PT CLA)

Conventional PT logic leads to compact design but shows voltage degradation problem in two or more cascaded PT stage at ultra-low power supply voltage for sub-threshold operation. Therefore, to overcome this voltage degradation problem the implementation of circuits is done by coupling PT logic with Static-CMOS buffer at appropriate stages rather than using complete Static-CMOS or PT gate designs. The combination of Static-CMOS buffer with PT logic is represented here as HYB-PT logic.

To check for proper operation of HYB-PT logic with RBB, a series combination of PT and two Static-CMOS inverters (PT-2INV block), as shown in Figure 3.29, under following different conditions of body bias has been simulated and analysed.

- State a----PT1, 2INV without RBB
- State b----PT1 2INV with RBB
- State c----PT1 without RBB, 2INV with RBB

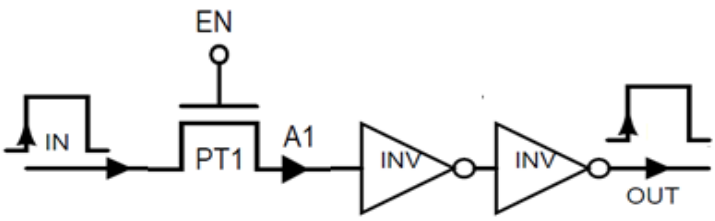


Figure 3.29: PT-2INV block

The results are given in Table 3.10 and wave forms at node 'OUT' are given in Figure 3.30

Table 3.10: Operations of PT-2INV block

State	Enable [EN = 1 for NMOS] (ON Condition)		Operation	Enable [EN = 0 for NMOS] (OFF Condition)		Operation
	Input given at node IN (V)	Output at node OUT (V)	Turn ON	Input at node IN (V)	Output at node OUT (V)	Turn OFF
(a)	0.4	0.400	Proper	0.4	0.000	Proper
(b)	0.4	0.400	Proper	0.4	0.391	Not turning off properly
(c)	0.4	0.400	Proper	0.4	0.000	Proper

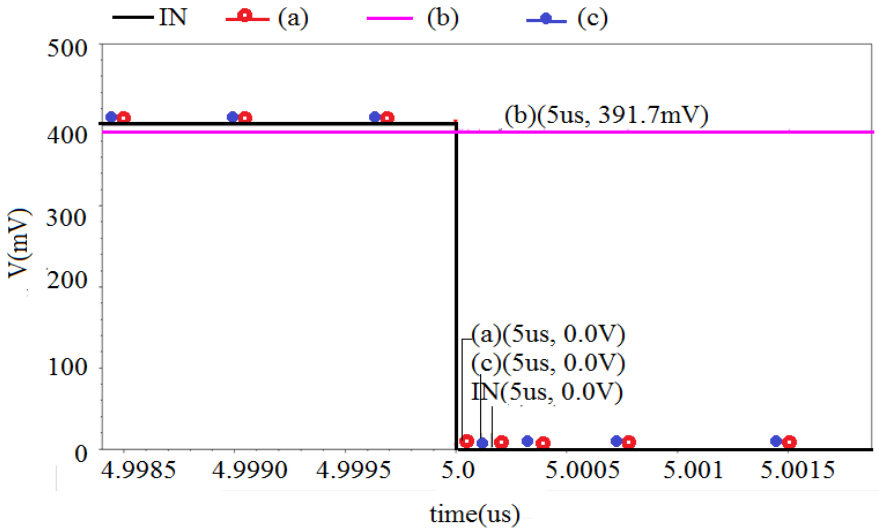


Figure 3.30: Graph for PT-2INV block at OFF condition

From the above results, it is clear that PT-2INV block operates properly for ON condition for all three states, whereas at OFF condition the output is not proper for state b. Therefore, in this adder, HYB-PT logic without RBB is used in design. Each output node in HYB-PT logic is followed by a buffer (which is composed of two inverters).

Further, only internal units like bit-wise generate/propagate circuitry and sum generator circuitry are designed using HYB-PT logic without RBB.

A complete adder implementation using HYB-PT logic with buffer showed increased power consumption during simulation results. Therefore, only simple circuits like bit-wise generate/propagate circuitry and sum generator circuit of CLA's are implemented using HYB-PT logic as shown in Figure 3.31 and Figure 3.32 respectively to get the advantage of reduced transistor count. Whereas (carry generator and group generate/propagate circuitry) of CLA's are implemented using Static-CMOS logic only.

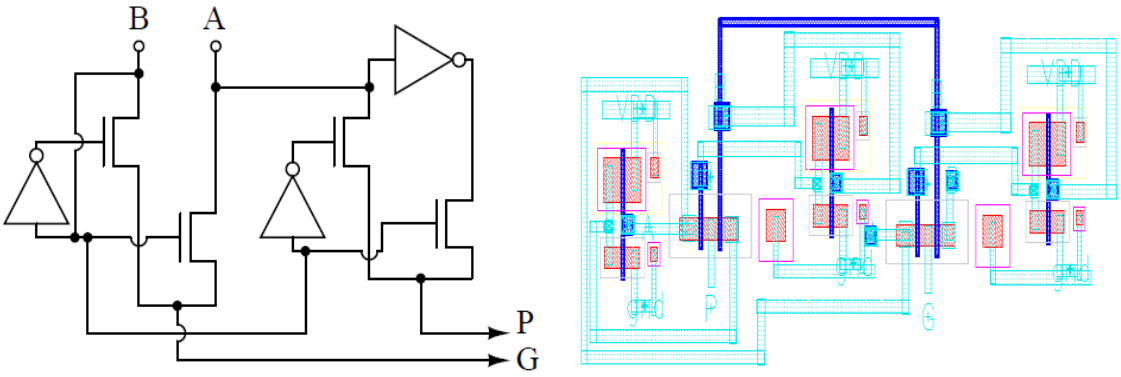


Figure 3.31: Circuit diagram of bit-wise generate/propagate

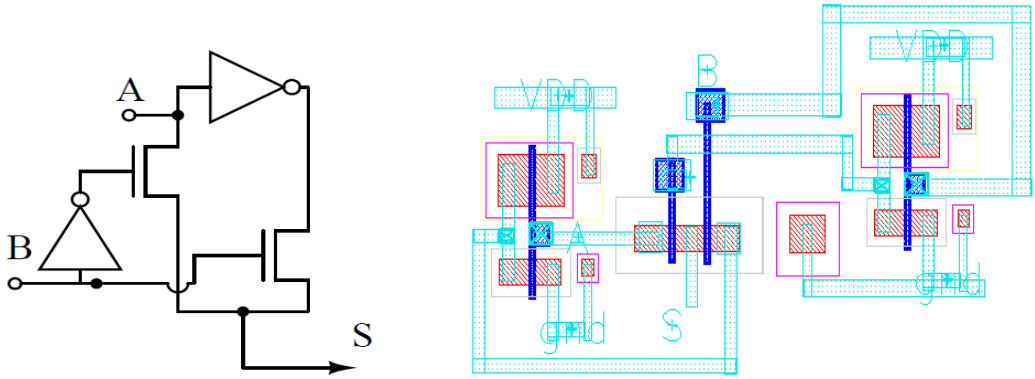


Figure 3.32: Circuit diagram of bit-wise sum-generator

The CLA's have been implemented at different operand sizes as 8-bit, 16-bit, 32-bit and 64-bit using Static-CMOS, HYB-TG, and HYB-PT logic style in sub-threshold region.

3.5.2. Simulation Methodology and Results of CLA

To obtain the simulation results for the CLA's in sub-threshold region, the following methodology is followed.

The 8-bit, 16-bit, 32-bit and 64-bit versions of each of the above three parallel CLA's were designed in Cadence Virtuoso (Schematic and Layout design). The pre-computation stage is designed using an AND gates and a XOR gates to generate the individual bit generate and propagate signals respectively.

A look-ahead block is designed using an AND gate and an AND-OR implementation (AOI) cell. The multiple carries are computed with proper buffering necessary, according to the implementation. The post-computation stage is designed using XOR gates to generate the sum bits.

In sub-threshold based circuits, leakage currents play very important role in terms of power, delay and power-delay product. Leakage current, including sub-threshold leakage current and gate leakage current, becomes more significant below 100nm. Therefore, to analyze the effect of leakage current at above and below 100nm, two different technology nodes i.e. 45 nm / 180 nm technology have been considered in implementation. The schematic and layouts were designed using 45 nm / 180 nm technology libraries and simulated using the BSIM3 (V3.24) model, at a supply voltage of 0.4 V.

This setup is common to all circuits designed in chapters 3, 4, and 5 in the present work.

A sequence of random inputs is applied to identify input pattern for worst case power consumption and propagation delay. Then, worst case power consumption and propagation delay values are obtained individually through transient simulations for each design. Transient simulations have been done by applying input pulses with rise and fall times of 1 pico-second, pulse width (ON time) of 1 micro-second and pulse period of 5 micro-second [33].

The power, delay and power-delay product values are evaluated for CLA's using Static-CMOS logic, HYB-TG logic and HYB-PT logic style for different operand sizes.

In this thesis, the following nomenclature as shown in Table 3.11, is used to represent the proposed designs of CLA adders:

Architecture (**CLA**) - technology (**45/ 180**) – logic family (**STA-CMOS, HYB-TG, and HYB-PT**)

Table 3.11: Nomenclature used for the proposed designs of CLA

S. No.	Adder Design Descriptions	Nomenclature
1	CLA at 45 nm using Static-CMOS logic family	CLA-45-STA-CMOS
2	CLA at 45 nm using hybrid TG logic family	CLA-45-HYB-TG
3	CLA at 45 nm using hybrid PT logic family	CLA-45-HYB-PT
4	CLA at 180 nm using Static-CMOS logic family	CLA-180-STA-CMOS
5	CLA at 180 nm using hybrid TG logic family	CLA-180-HYB-TG
6	CLA at 180 nm using hybrid PT logic family	CLA-180-HYB-PT

Table 3.12 and Table 3.13 gives the measured power, delay and power-delay product CLA's using different logic families. All modules function properly at supply voltage as low as 0.4 V.

Table 3.12: Simulation results of CLA's at 45 nm technology

Module Name	No. of Bits	Power (µW)	Delay (ns)	Power-Delay Product (watt*sec10^{-15})	Area (µm^2)
CLA-45-STA-CMOS	8	0.380	**1.241**	**00.471**	0359.71
	16	0.625	**2.369**	**01.481**	0647.14
	32	**0.957**	**3.697**	**03.538**	1175.25
	64	3.413	**4.065**	**13.871**	1894.81
CLA-45-HYB-TG	8	0.452	1.332	00.602	0293.19
	16	0.747	2.655	01.983	0597.74
	32	2.045	3.874	07.922	1090.31
	64	4.364	4.230	18.459	1727.87
CLA-45-HYB-PT	8	**0.307**	1.682	00.516	**0257.12**
	16	**0.587**	2.970	01.743	**0501.78**
	32	1.661	4.178	06.939	**0997.23**
	64	**3.271**	4.321	14.133	**0898.01**

Table 3.13: Simulation results of CLA's at 180 nm technology

Module Name	No. of Bits	Power (µW)	Delay (ns)	Power-Delay Product (watt*sec10^{-15})	Area (µm^2)
CLA-180-STA-CMOS	8	**0.204**	**045**	**009.180**	015,541
	16	0.575	**065**	**037.375**	026,790
	32	0.748	**098**	**073.304**	077,410
	64	2.740	**100**	**274.000**	128,030
CLA-180-HYB-TG	8	0.396	035	013.860	011,954
	16	0.799	055	043.945	020,574
	32	1.274	085	108.290	069,578
	64	3.081	155	477.550	114,841
CLA-180-HYB-PT	8	0.242	050	012.100	**009,741**
	16	**0.528**	072	038.016	**018,655**
	32	**0.688**	112	077.056	**062,178**
	64	**1.964**	180	353.520	**109,221**

Key Points: The overall results of the CLA show that

- CLA operates down to 0.4 V power supply at both technology nodes in sub-threshold region.
- The simulation results show that power, delay and power-delay product of the CLA designs increases with the increase in operand size as expected.
- In comparison to 180 nm technology, at 45 nm, the propagation delay is smaller, power consumption is higher (due to increased leakage currents) and power-delay product is smaller for all designs of CLA [34]. For CMOS inverter, the leakage currents are found to be 1.05 nA and 0.18 nA at 45 nm / 180 nm technology respectively through simulation.

- The overall power-delay product of the Static-CMOS is smaller than HYB-TG and HYB-PT logic. This demonstrates that changing the logic style from Static-CMOS to TG or Static-CMOS to PT logic, increase the overall circuit power-delay product for sub-threshold operation in both technologies.
- Fully Static-CMOS logic design style is the most power efficient design style for CLA at both technologies in sub-threshold region.

The overall power consumption, propagation delay and power-delay product graphs of CLA's at 45 nm / 180 nm technology using different logic families are shown in Figure 3.33.

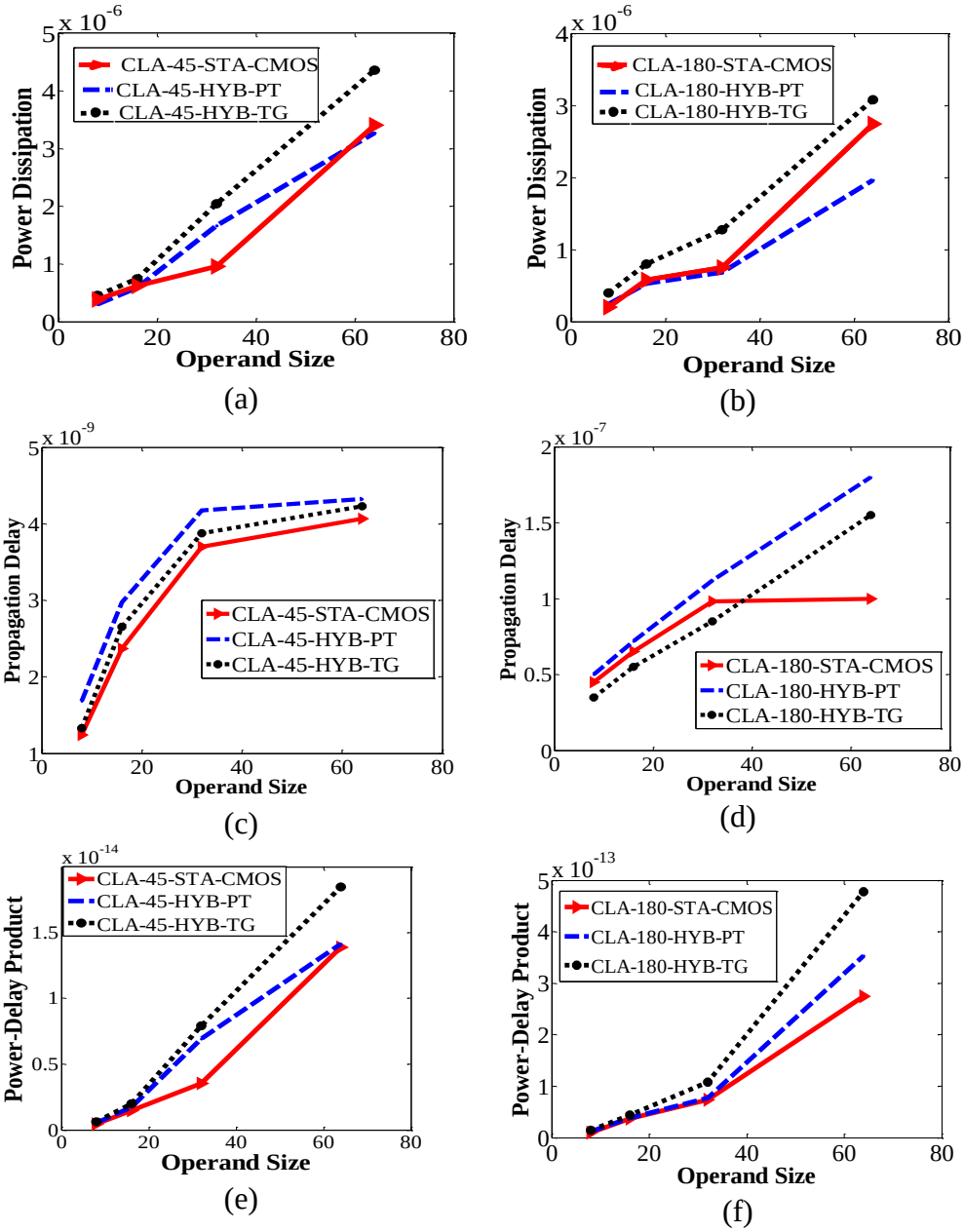


Figure 3.33: The overall power consumption, propagation delay and power-delay product graphs of CLA at 45 nm / 180 nm technology

3.5.3. Design Implementation using KSA

KSA offers an efficient solution to binary addition problem, assures a low computation delay and low power in sub-threshold region. Conventionally, the parallel prefix adders compute addition in two steps: one to obtain the carry at each bit, with the next to compute the sum bit based on the carry bit. The internal architecture of 16-bit KSA is shown in Figure 3.34. The pre-computation and post-computation blocks are commonly used in all three adders (CLA, KSA and HCA). The transistor level diagrams of these blocks using Static-CMOS, HYB-TG and HYB-PT logic style are given in section 3.5.1.2, 3.5.1.2 and 3.5.1.3 respectively.

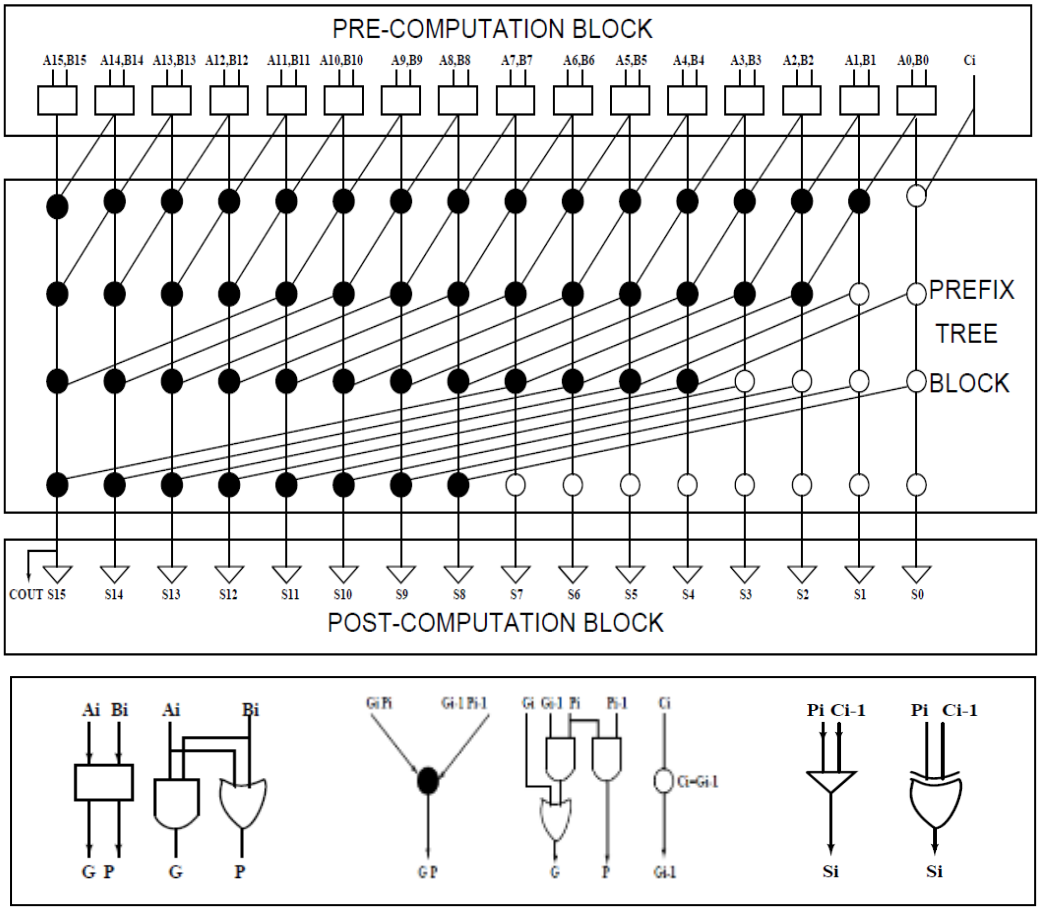


Figure 3.34: Internal architecture of KSA

Design Methodology: The basic blocks of the KSA are the bitwise propagate/generate logic block, group propagate/generate logic block and sum/carry logic block. For implementation of these basic blocks the Boolean expressions of KSA are given by Eq. (3.11) - Eq. (3.14) as discussed in section 3.2.2, AND, OR, XOR gates are the three widely used logic gates.

The circuit realization of these basic logic gates with competing logic families have already been discussed in section 3.3. The KSA is implemented at different operand sizes using three different logic families i.e. Static-CMOS, HYB-TG and HYB-PT.

3.5.4. Simulation Methodology and Results of KSA

To obtain the simulation results for the KSA's in sub-threshold region, the following methodology is followed.

The 8-bit, 16-bit, 32-bit and 64-bit KSA' using three different logic families were designed in Cadence Virtuoso (Schematic and Layout design). The pre-computation stage is designed using an AND gates and a XOR gates to generate the individual bit generate and propagate signals respectively.

A prefix tree for generating group generate and group propagate signals is designed using an AND gate and an AND-OR implementation (AOI) cell. The multiple carries are computed with proper buffering necessary, according to the implementation. The post-computation stage is designed using XOR gates to generate the sum bits. Two different technology nodes i.e. 45 nm / 180 nm technology have been considered in implementation of schematic and layouts and simulated using the BSIM3 (V3.24) model, at a supply voltage of 0.4 V. The methodology followed for simulation of KSA in sub-threshold region is same as given in Section 3.5.2.

The power, delay and power-delay product values are evaluated for KSA's using Static-CMOS logic, HYB-TG logic and HYB-PT logic style for different operand sizes.

In this thesis, the following nomenclature as shown in Table 3.14, is used to represent the proposed designs of KSA adders:

Architecture (**KSA**) - technology (**45/ 180**) – logic family (**STA-CMOS, HYB-TG, and HYB-PT)**

Table 3.14: Nomenclature used for the proposed designs of KSA

S. No.	Adder Design Descriptions	Nomenclature
1	KSA at 45 nm using Static-CMOS logic family	KSA-45-STA-CMOS
2	KSA at 45 nm using hybrid TG logic family	KSA-45-HYB-TG
3	KSA at 45 nm using hybrid PT logic family	KSA-45-HYB-PT
4	KSA at 180 nm using Static-CMOS logic family	KSA-180-STA-CMOS
5	KSA at 180 nm using hybrid TG logic family	KSA-180-HYB-TG
6	KSA at 180 nm using hybrid PT logic family	KSA-180-HYB-PT

The measured power, delay and power-delay product of KSA's using 45 nm / 180 nm technology are given in Table 3.15 and Table 3.16, which operates at 0.4V power supply voltage for sub-threshold operation.

These results show that all modules function properly at supply voltage as low as 0.4 V.

Table 3.15: Simulation results of KSA's at 45 nm technology

Module Name	No. of Bits	Power (µW)	Delay (ns)	Power-Delay Product (watt*sec10^{-15})	Area (μm^2)
KSA-45-STA-CMOS	8	**0.014**	2.571	**0.037**	240.7
	16	**0.157**	4.297	**0.676**	619.9
	32	**0.215**	12.96	2.792	1521.7
	64	**0.317**	17.24	5.472	3079.2
KSA-45-HYB-TG	8	0.101	**1.597**	0.161	189.7
	16	0.299	**2.354**	0.705	498.3
	32	0.367	**3.412**	**1.253**	1374.1
	64	0.587	**5.698**	**3.349**	2873.1
KSA-45-HYB-PT	8	0.389	10.63	4.138	**107.1**
	16	0.589	16.97	10.01	**288.3**
	32	0.962	22.52	21.67	**1187.5**
	64	1.470	29.71	43.88	**2542.2**

Table 3.16: Simulation results of KSA's at 180 nm technology

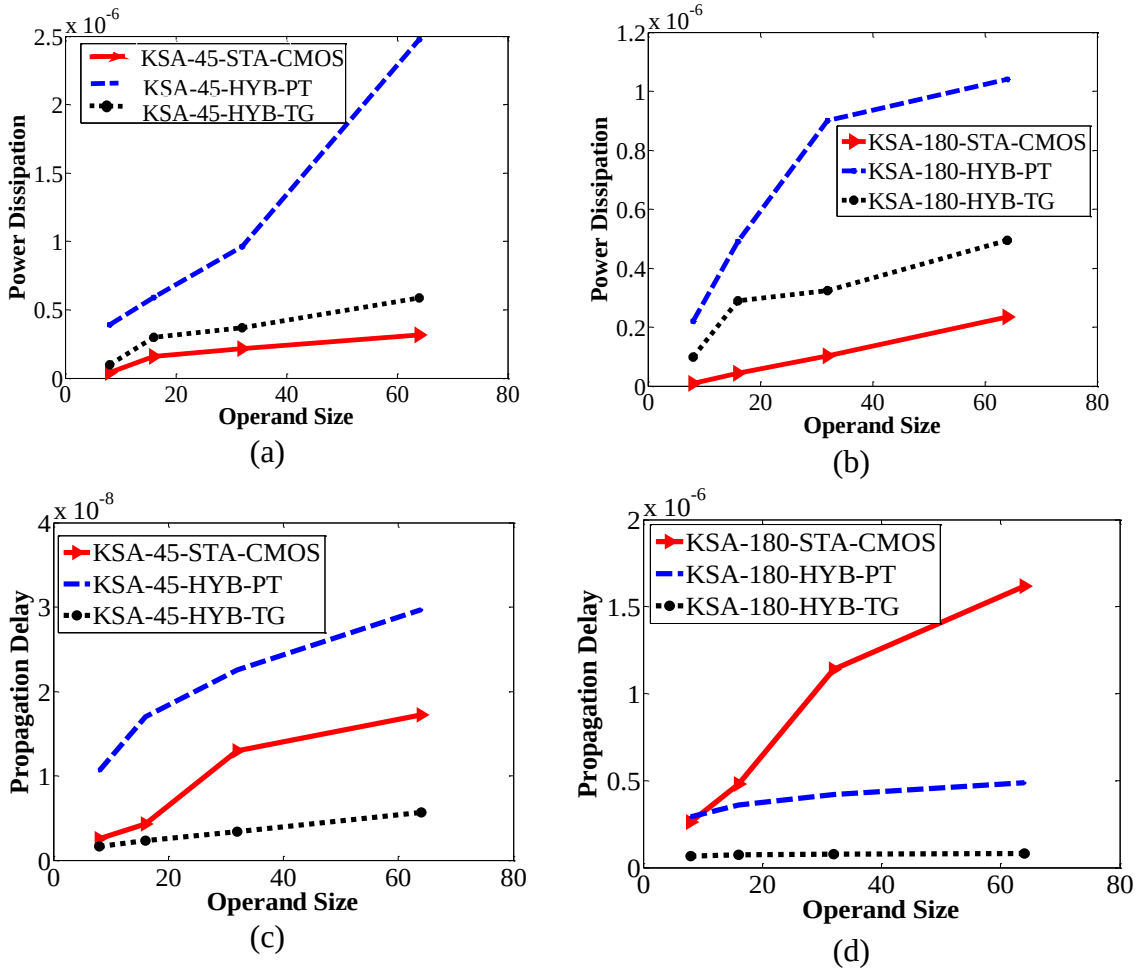
Module Name	No. of Bits	Power (µW)	Delay (ns)	Power-Delay Product (watt*sec10^{-15})	Area (μm^2)
KSA-180-STA-CMOS	8	**0.009**	0260.0	**002.34**	016,741
	16	**0.041**	0479.0	**019.63**	028,221
	32	**0.103**	1140.0	117.00	080,415
	64	**0.234**	1618.0	378.00	129,774
KSA-180-HYB-TG	8	0.098	**0067.6**	006.63	013,221
	16	0.289	**0073.1**	021.15	022,542
	32	0.323	**0078.7**	**026.29**	075,471
	64	0.495	**0081.4**	**040.29**	120,021
KSA-180-HYB-PT	8	0.221	0293.1	064.77	**011,512**
	16	0.491	0358.1	175.80	**018,785**
	32	0.901	0421.2	379.50	**068,712**
	64	1.040	0489.0	508.56	**101,146**

Key points: The overall results of the KSA show that

- KSA operates down to 0.4 V power supply in sub-threshold region at both technology nodes.
- The simulation results show that power, delay and power-delay product of the KSA increases with the increase in operand size as expected.

- The KSA's using STA-CMOS logic exhibits the lowest power-delay product for low bit operands (i.e. 8b & 16b input data width) adder. Whereas for higher bit operands (i.e. 32b & 64b), HYB-TG logic has less power-delay product at both technologies. Hence, logic family greatly affects the power-delay product of the circuits.
- The KSA using HYB-PT show worst power-delay product at both technologies due to higher power consumption and delay.
- In comparison to 180 nm technology, at 45 nm, the propagation delay is smaller, power consumption is higher (due to increased leakage currents) and power-delay product is smaller for all designs of KSA.

The overall power consumption, propagation delay and power-delay product graphs of KSA's at 45 nm / 180 nm technology using different logic families are shown in Figure 3.35.



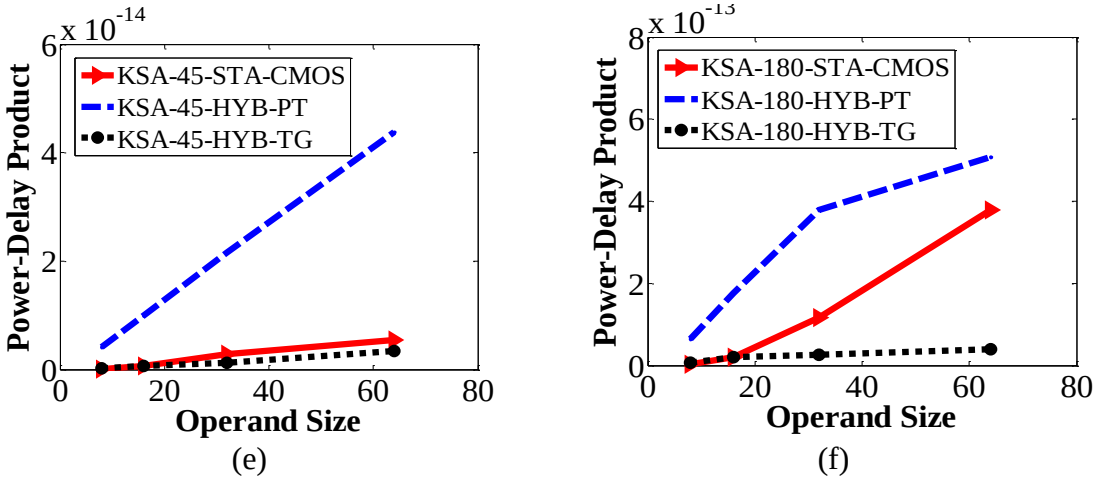


Figure 3.35: The overall power consumption, propagation delay and power-delay product graphs of KSA at 45 nm / 180 nm technology

3.5.5. Design Implementation using HCA

HCA offers an efficient solution to binary addition problem, assures a low computation delay and low power in sub-threshold region.

Conventionally, theparallel prefix adders compute addition in two steps: one to obtain the carry at each bit, with the next to compute the sum bit based on the carry bit. The HCA are the combinations of two adders KSA with $\log_2 n$ stages and Brent-Kung with $2\log_2 n–1$ stages.

The combined effects of both the adders provide a reasonably high speed at less complexity.

The internal architecture of 16-bit HCA is shown in Figure 3.36 which reveals that for the same word size, the number of prefix computation stages are one extra logic level than the KS design, whereas in the transistor level design the number of the prefix operations is fewer in the HC design than in the KS design [35].

Thus, the HCA reduces the area in return for one extra stage of delay as compared to the KS adder.

In each logic level of HC prefix tree places cells every other bit and the last logic level accounts for the missing carries. The pre-computation and post-computation blocks are commonly used in all three adders (CLA, KSA and HCA). The transistor level diagrams of these blocks using Static-CMOS, HYB-TG and HYB-PT logic style are given in section 3.5.1.2, 3.5.1.2 and 3.5.1.3 respectively.

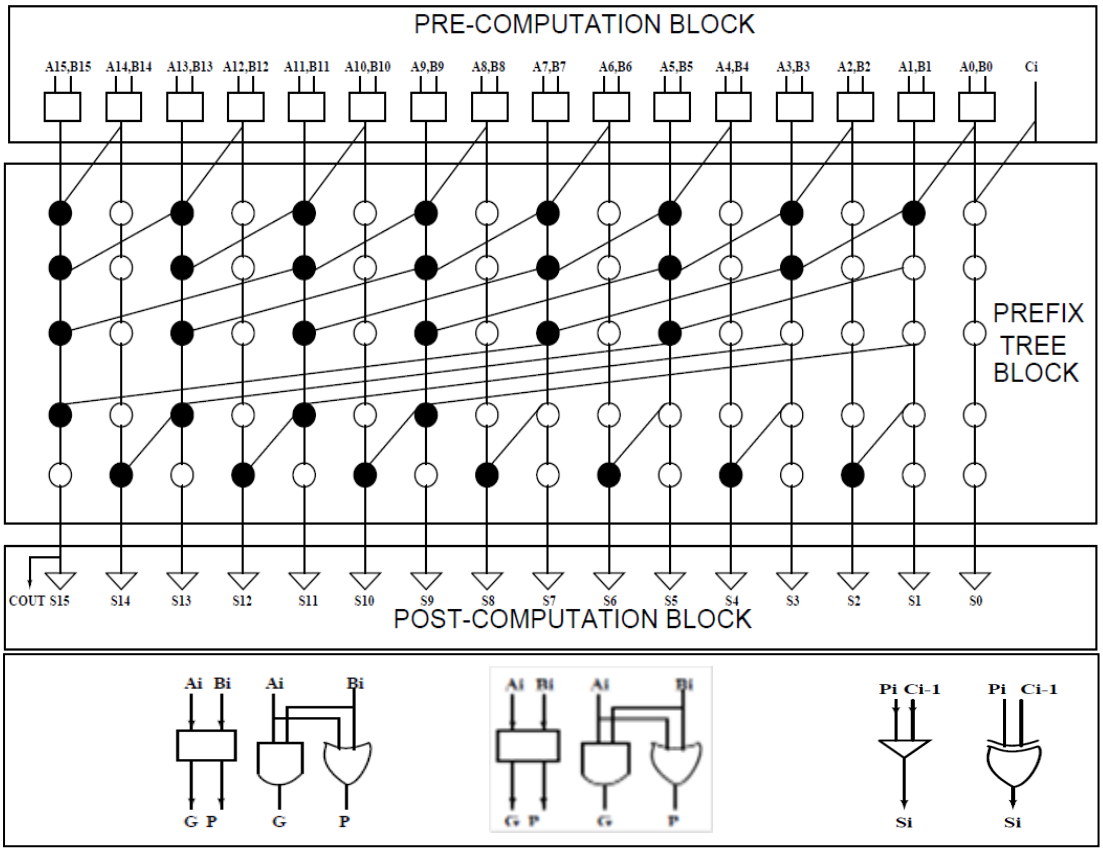


Figure 3.36: Internal architecture of HCA

Design Methodology: The basic blocks of the HCA are the bitwise propagate/generate logic block, group propagate/generate logic block and sum/carry logic block. For implementation of these basic blocks the Boolean expressions of HCA architecture are given by Eq. (3.15) - Eq. (3.19) as discussed in section 3.2.3, AND, OR, XOR gates are the three widely used logic gates. The circuit realization of these basic logic gates with competing logic families have already been discussed in section 3.3. The HCA is implemented at different operand sizes using three different logic families i.e. Static-CMOS, HYB-TG and HYB-PT.

3.5.6. Simulation Methodology and Results of HCA

The methodology followed for simulation of HCA in sub-threshold region is same as given in Section 3.5.2. The power, delay and power-delay product values are evaluated for HCA's using Static-CMOS logic, HYB-TG logic and HYB-PT logic style for different operand sizes. In this thesis, the following nomenclature as shown in Table 3.17, is used to represent the proposed designs of HCA adders:

Architecture (**HCA**) - technology (**45/ 180**) – logic family (**STA-CMOS, HYB-TG, and HYB-PT)**

Table 3.17: Nomenclature used for the proposed designs of HCA

S. No.	Adder Design Descriptions	Nomenclature
1	HCA at 45 nm using Static-CMOS logic family	HCA-45-STA-CMOS
2	HCA at 45 nm using hybrid TG logic family	HCA-45-HYB-TG
3	HCA at 45 nm using hybrid PT logic family	HCA-45-HYB-PT
4	HCA at 180 nm using Static-CMOS logic family	HCA-180-STA-CMOS
5	HCA at 180 nm using hybrid TG logic family	HCA-180-HYB-TG
6	HCA at 180 nm using hybrid PT logic family	HCA-180-HYB-PT

The measured power, delay and power-delay product of HCA's using 45 nm / 180 nm technology are given in Table 3.18 and Table 3.19, which operates at 0.4V power supply voltage for sub-threshold operation.

Table 3.18: Simulation results of HCA's at 45 nm technology

Module Name	No. of Bits	Power (µW)	Delay (ns)	Power-Delay Product (watt*sec10^{-15})	Area (µm^2)
HCA-45-STA-CMOS	8	**0.012**	**03.74**	**0.044**	0196.17
	16	**0.035**	07.20	**0.252**	0468.36
	32	**0.197**	15.90	3.158	1084.08
	64	**0.291**	19.89	5.802	2254.74
HCA-45-HYB-TG	8	0.098	04.08	0.403	0114.35
	16	0.302	**06.39**	1.933	0217.24
	32	0.401	**07.09**	**2.846**	0893.21
	64	0.506	**09.06**	**4.587**	1835.74
HCA-45-HYB-PT	8	0.279	33.67	9.421	**089.351**
	16	0.398	40.12	15.99	**0112.41**
	32	0.725	55.10	39.95	**0474.35**
	64	1.795	64.12	115.1	**1565.54**

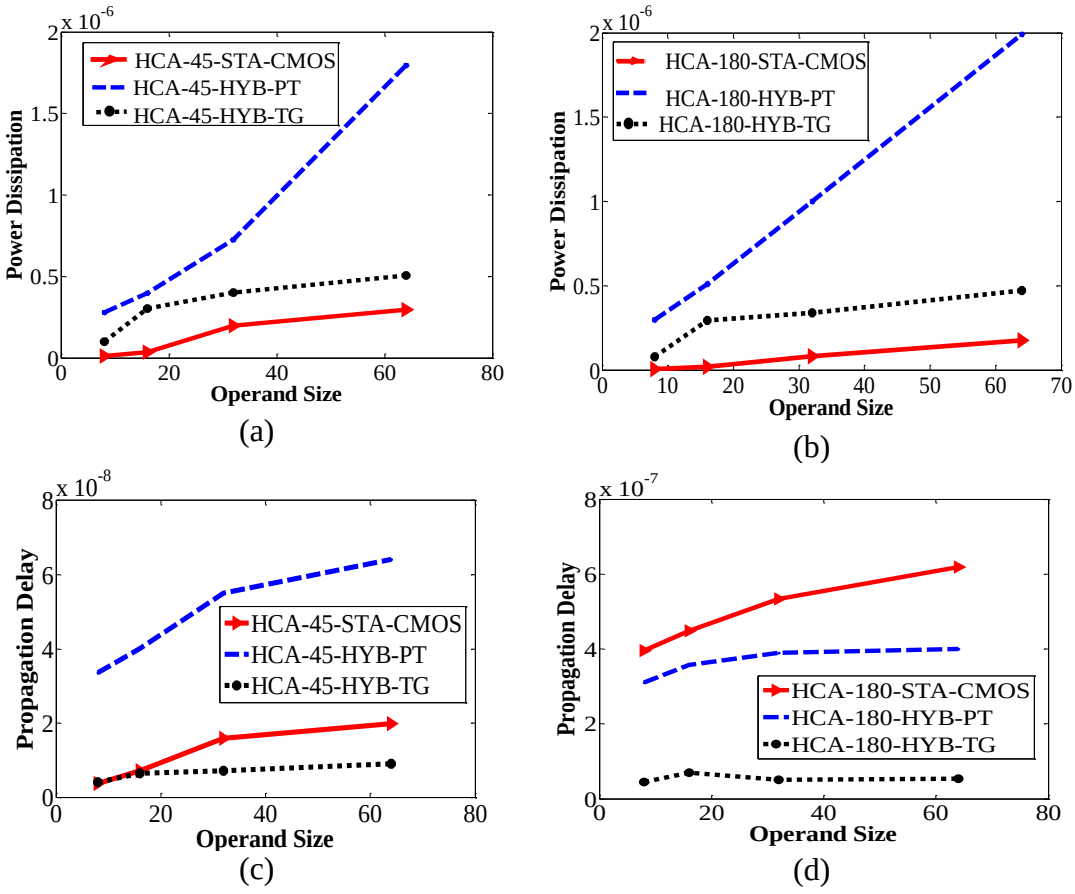
Table 3.19: Simulation results of HCA's at 180 nm technology

Module Name	No. of Bits	Power (µW)	Delay (ns)	Power-Delay Product (watt*sec10^{-15})	Area (µm^2)
HCA-180-STA-CMOS	8	**0.006**	395.1	**002.3**	016,214
	16	**0.018**	449.0	**008.1**	025,784
	32	**0.081**	534.0	043.3	072,547
	64	**0.177**	619.0	109.0	125,141
HCA-180-HYB-TG	8	0.079	**044.2**	003.4	012,874
	16	0.295	**050.1**	014.7	019,542
	32	0.338	**061.4**	**020.7**	068,562
	64	0.473	**073.1**	**034.5**	114,260
HCA-180-HYB-PT	8	0.196	309.8	060.7	**010,780**
	16	0.308	356.8	109.8	**015,745**
	32	0.549	389.4	213.7	**059,541**
	64	1.692	400.5	677.6	**096,347**

Key Points: The overall results of the HCA show that

- HCA's operate down to 0.4 V power supply in sub-threshold region at both technology nodes.
- The simulation results show that power, delay and power-delay product of the HCA designs increases with the increase in operand size as expected.
- The HCA's using Static-CMOS logic exhibits the lowest power-delay product for low bit operands (i.e. 8b & 16b input data width) adder. Whereas for higher bit operands (i.e. 32b & 64b), HYB-TG logic has minimum power-delay product at both technologies.
- The HCA using HYB-PT show worst power-delay product at both technologies due to higher power consumption and delay.
- In comparison to 180 nm technology, at 45 nm, the propagation delay is smaller, power consumption is higher (due to increased leakage currents) and power-delay product is smaller for all designs of HCA.

The overall power consumption, propagation delay and power-delay product graphs of HCA's at 45 nm / 180 nm technology using different logic families is shown in Figure 3.37.



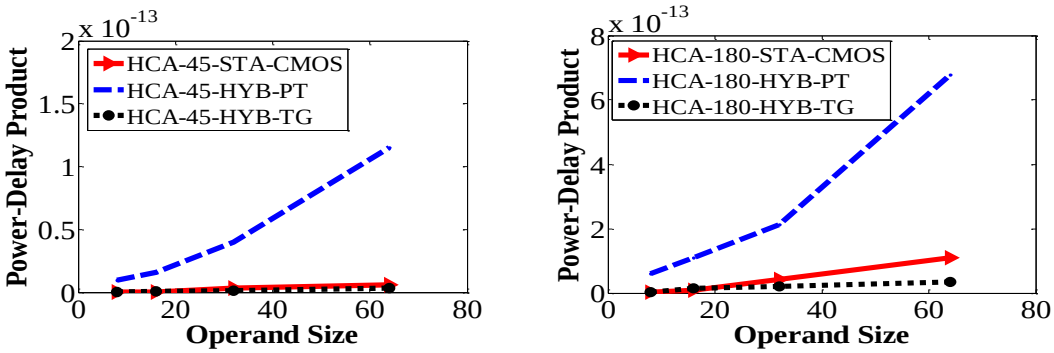


Figure 3.37: The overall power consumption, propagation delay and power-delay product graphs of HCA at 45 nm / 180 nm technology

3.6. IMPACT OF RBB ON STATIC-CMOS ADDERS

Table 3.20 and Table 3.21 show the comparative result of adders using with/without RBB scheme at 45 nm / 180 nm technology respectively. All three adders (CLA, KSA and HCA) operate at 0.4V power supply voltage for sub-threshold operation.

Table 3.20: Simulation results of adders at 45 nm technology

Module Name	No. of Bits	Power (µW)		Delay (ns)		Power-Delay Product (watt*sec10^{-15})	
		Without RBB	With RBB	Without RBB	With RBB	Without RBB	With RBB
CLA-45-STA-CMOS	8	0.380	**2.514**	01.24	**00.42**	00.471	**01.073**
	16	0.625	**4.061**	02.36	**00.87**	01.480	**03.549**
	32	0.957	**7.021**	03.69	**01.02**	03.538	**07.168**
	64	3.413	**9.741**	04.06	**02.01**	13.871	**19.618**
KSA-45-STA-CMOS	8	0.014	**0.041**	02.57	**01.74**	00.037	**00.071**
	16	0.157	**0.324**	04.29	**02.91**	00.676	**00.944**
	32	0.215	**0.474**	12.96	**10.27**	02.792	**04.867**
	64	0.317	**0.511**	17.24	**15.98**	05.472	**08.165**
HCA-45-STA-CMOS	8	0.012	**0.037**	03.74	**02.47**	00.044	**00.091**
	16	0.035	**0.054**	07.20	**06.57**	00.252	**00.355**
	32	0.197	**0.285**	15.96	**14.69**	03.158	**04.186**
	64	0.291	**0.334**	19.89	**18.87**	05.802	**06.302**

Table 3.21: Simulation results of adders at 180 nm technology

Module Name	No. of Bits	Power (µW)		Delay (ns)		Power-Delay Product (watt*sec10^{-15})	
		Without RBB	With RBB	Without RBB	With RBB	Without RBB	With RBB
CLA-180-STA-CMOS	8	0.204	**0.323**	0045	**0030.0**	009.18	**009.96**
	16	0.575	**0.711**	0065	**0057.0**	037.37	**040.52**
	32	0.748	**0.964**	0098	**0079.0**	073.30	**076.15**
	64	2.740	**3.512**	0100	**0085.0**	274.00	**298.52**
KSA-180-STA-CMOS	8	0.009	**0.034**	0260	**0174.0**	002.34	**005.91**
	16	0.041	**0.091**	0479	**0347.0**	019.63	**031.64**
	32	0.103	**0.294**	1140	**1081.0**	117.00	**317.80**
	64	0.234	**0.374**	1618	**1557.0**	378.00	**582.30**
HCA-180-STA-CMOS	8	0.006	**0.014**	0395	**0257.8**	002.37	**003.61**
	16	0.018	**0.034**	0449	**0338.4**	008.08	**011.50**
	32	0.081	**0.107**	0534	**0487.3**	043.30	**052.14**
	64	0.177	**0.221**	0619	**0540.2**	109.00	**119.30**

Keypoint: The overall results of the adder with/without RBB scheme show that

- With RBB the propagation delay is smaller, power consumption is higher (due to increased leakage currents) and power-delay product is higher for all designs of adder as compared to without RBB scheme.
- At 45 nm (180 nm) technology, the RBB scheme helps in reducing average delay by 61.8% (18.5%), increases average power consumption by 76.8% (22.5%) and increases the overall average power-delay product by 38.3% (7.3%) with the increase in operand size using Static-CMOS logic.

3.7. FINAL RESULTS AND DISCUSSION

Comparison of proposed designs with results of published architectures

This section presents the comparative analysis of 8-bit, 16-bit, 32-bit and 64-bit of CLA, KSA and HCA designs with referenced architectures operated in sub-threshold region at 45/ 180 nm CMOS technology for 0.4V supply voltage at same frequency of operation (200 KHz).

Here, for comparison 16-bit and 32-bit of CLA, KSA and HCA of the referenced architectures [36][37][38][39] are designed using Static-CMOS logic style to obtain their results in the same simulation setup for sub-threshold operation.

Table 3.22 and 3.23 shows the comparison of Static-CMOS based proposed adder designs (as obtained from Table 3.12, 3.13, 3.15, 3.16, 3.18 and 3.19) with the referenced architectures in sub-threshold region.

Table 3.22: Comparative results between proposed and referenced adder designs at 45 nm

References	Module name	No. of bits	Power (µW)	Delay (ns)	Power-Delay Product (Watt*Sec 10^{-15})	% reduction in Power-Delay Product
Ref [36]	CLA	16	1.287	8.872	11.41826	(16-bit) – 87.03% (32-bit) – 91.4%
		32	2.789	14.879	41.49753	
Proposed	CLA	16	**0.625**	**2.369**	**1.480625**	
		32	**0.957**	**3.697**	**3.538029**	
Ref [37]	KSA	16	0.741	16.784	12.43694	(16-bit) – 94.5% (32-bit) -89.9 %
		32	0.987	28.221	27.85413	
Proposed	KSA	16	**0.157**	**4.297**	**0.674629**	
		32	**0.215**	**12.96**	**2.764**	
Ref [37]	HCA	16	0.689	20.798	14.32982	(16-bit) – 98.2% (32-bit) – 92.8%
		32	0.774	57.114	44.20624	
Proposed	HCA	16	**0.035**	**7.201**	**0.252035**	
		32	**0.197**	**15.96**	**3.1441**	

Table 3.23: Comparative results between proposed and referenced adder designs at 180 nm

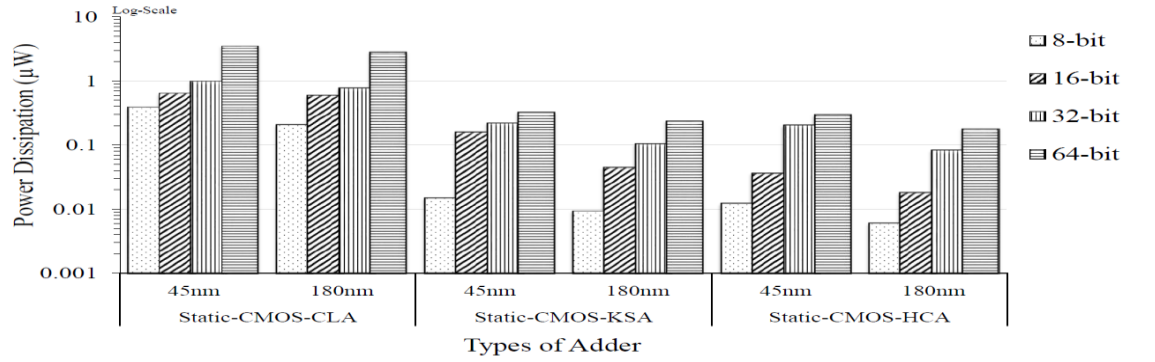
References	Module name	No. of bits	Power (µW)	Delay (ns)	Power-Delay Product (Watt*Sec 10^{-15})	% reduction in Power-Delay Product
Ref [38]	CLA	16	0.977	110.5	107.9585	(16-bit) – 65.3%
		32	1.465	172.2	252.273	
Proposed	CLA	16	**0.575**	**65**	**37.375**	(32-bit) – 70.9%
		32	**0.748**	**98**	**73.304**	
Ref [39]	KSA	16	0.551	532.2	293.2422	(16-bit) – 93.3%
		32	0.787	1232	969.584	
Proposed	KSA	16	**0.041**	**479.0**	**19.639**	(32-bit) – 87.8%
		32	**0.103**	**1140**	**117.42**	
Ref [11]	HCA	16	**0.489**	**511.5**	**250.1235**	(16-bit) – 96.7%
		32	0.674	779	525.046	
Proposed	HCA	16	**0.018**	**449.0**	**8.082**	(32-bit) – 91.7%
		32	**0.081**	**534.0**	**43.254**	

The comparative results show that all proposed designs show minimum power-delay product as compared to published referenced architectures.

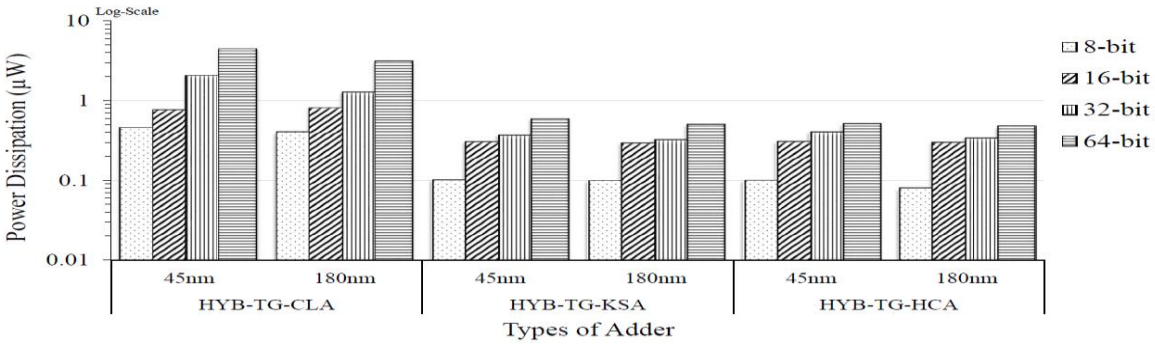
Comparison of results of proposed designs among themselves

All proposed designs show minimum power-delay product as compared to published referenced architectures. Thus, a comparison of these designs, among themselves, is done to obtain the best design in terms of overall power-delay product at both technology. For

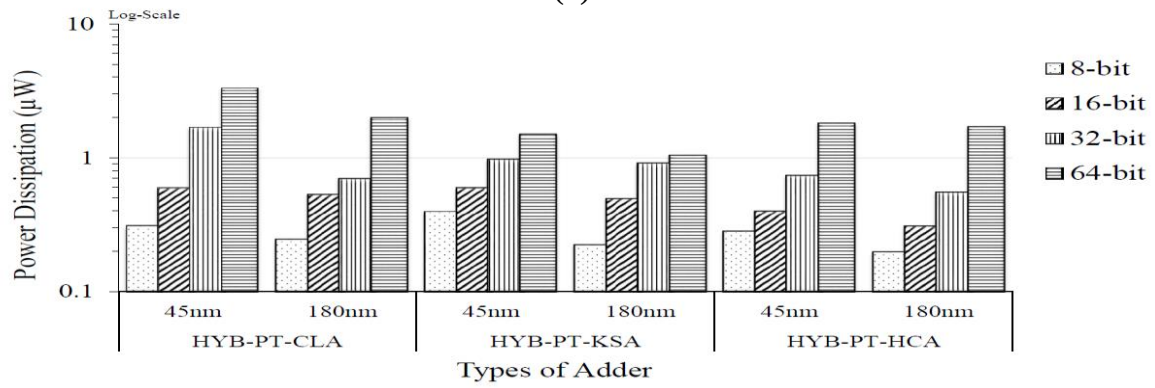
comparison purpose, Figure 3.38, Figure 3.39 and Figure 3.40 show the power consumption, propagation delay and power-delay product histograms of all proposed eighteen designs using Static-CMOS logic, HYB-TG and HYB-PT respectively.



(a)

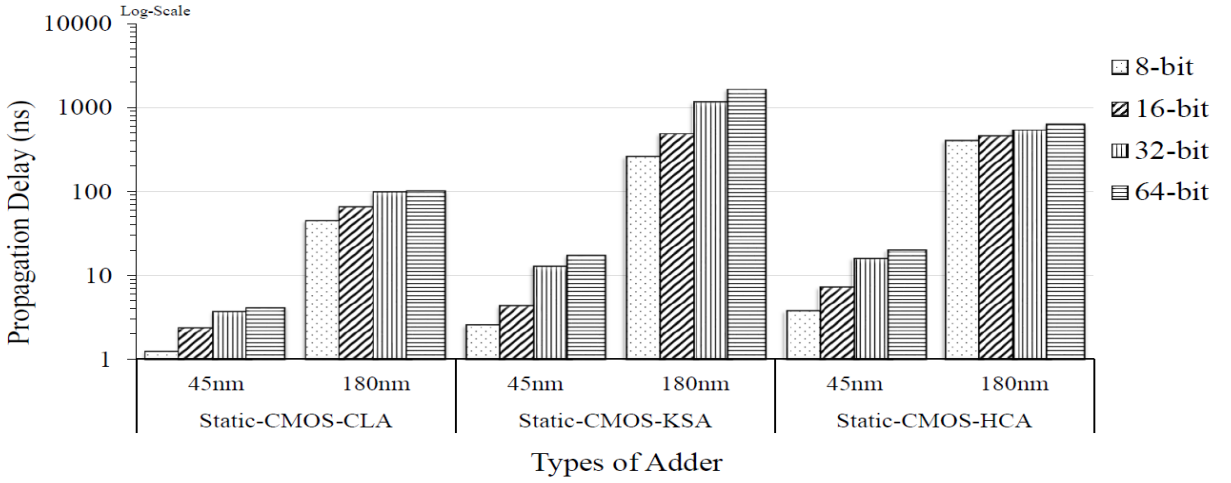


(b)

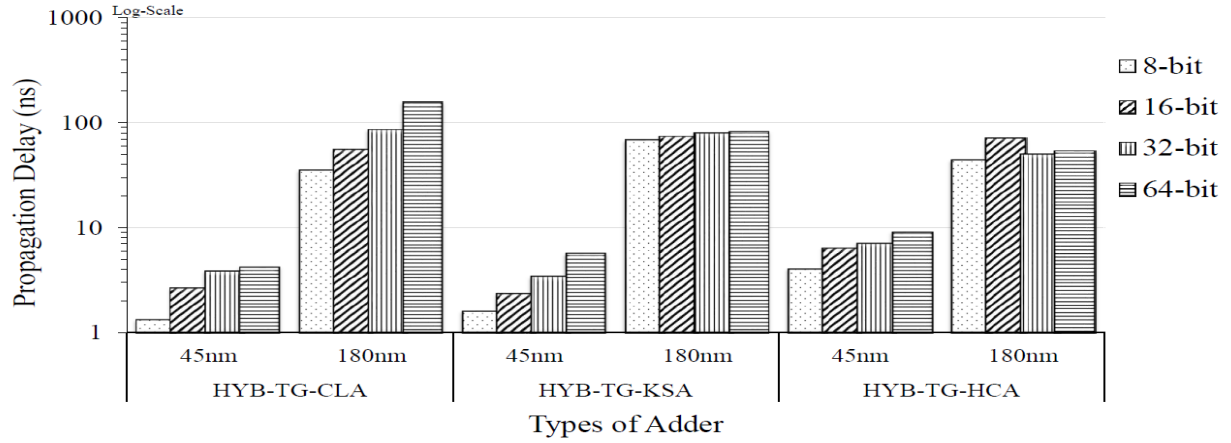


(c)

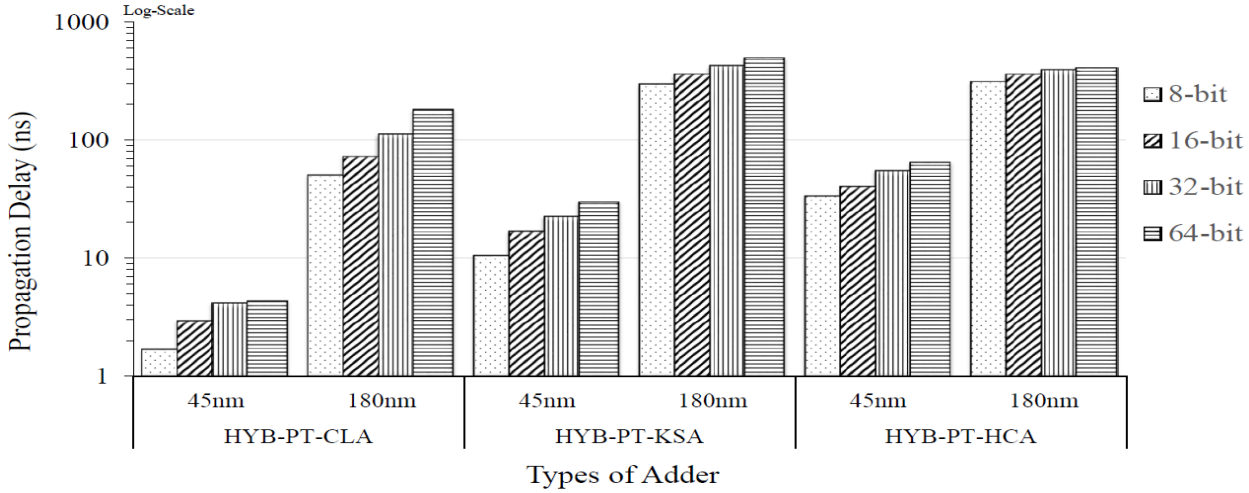
Figure 3.38: The power consumption graph between CLA, KSA and HCA at 45 nm / 180 nm technology (a) using Static-CMOS logic (b) using HYB-TG logic (c) using HYB-PT logic



(a)

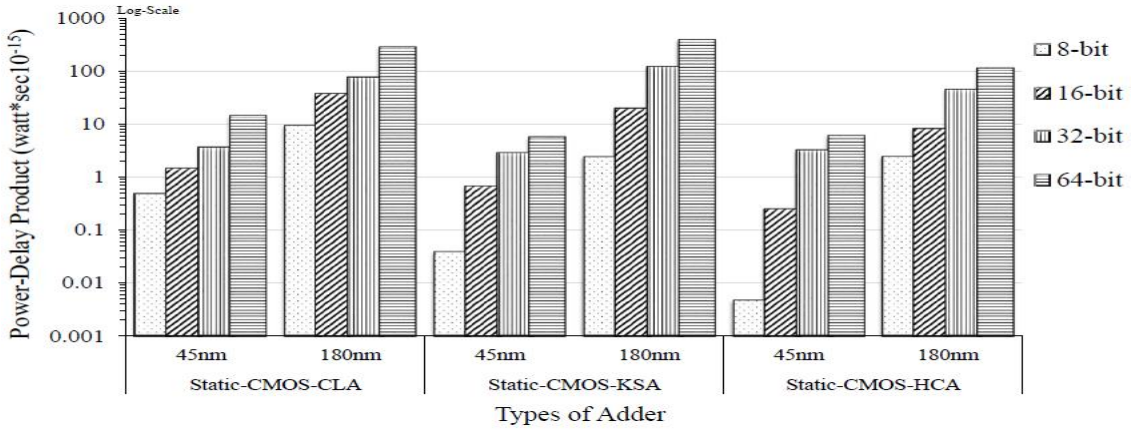


(b)

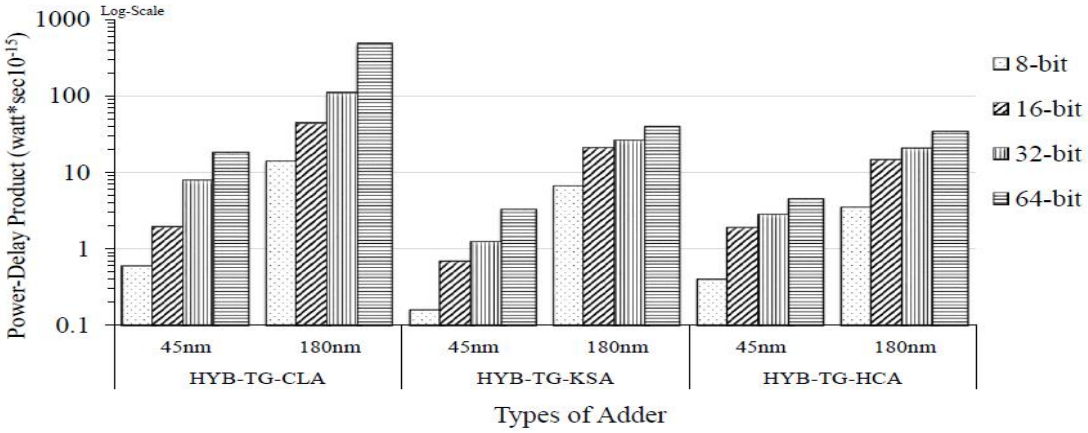


(c)

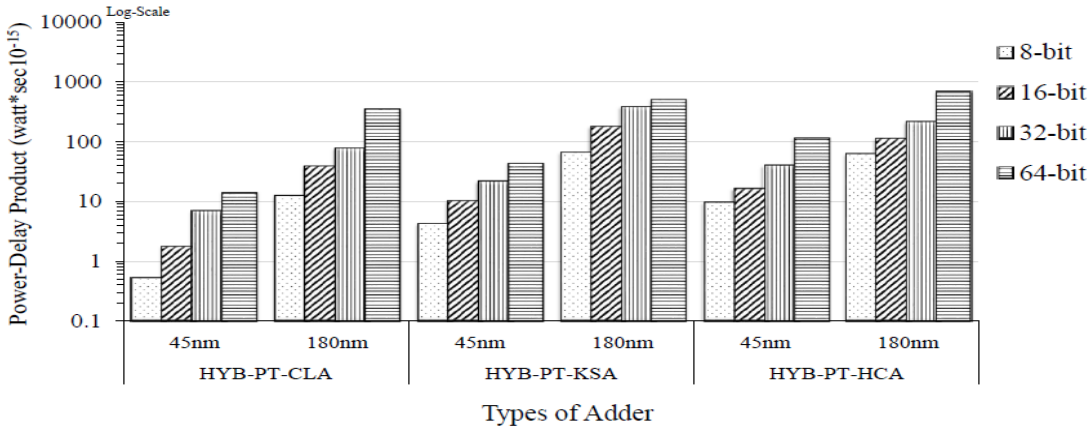
Figure 3.39: The propagation delay graph between CLA, KSA and HCA at 45 nm / 180 nm technology (a) using Static-CMOS logic (b) using HYB-TG logic (c) using HYB-PT logic



(a)



(b)



(c)

Figure 3.40: The power-delay product graph between CLA, KSA and HCA at 45 nm / 180 nm technology (a) using Static-CMOS logic (b) using HYB-TG logic (c) using HYB-PT logic

Observations

The comparative results of the CLA, KSA and HCA show that

- All three-adder architectures operate down to 0.4V with correct functionality using all three different logic families (Static-CMOS, HYB-TG and HYB-PT) in sub-threshold region.
- The power, delay and power-delay product of all these three adder designs increases with the increase in operand size.

(i) Effect of Logic Design Style:

- Static-CMOS logic gives lowest power consumption because of simpler logic cells for all three adder designs at both technology nodes in sub-threshold region.
- HYB-TG gives lowest propagation delay because of shorter critical paths for all three designs at both technology nodes in sub-threshold region.
- In KSA and HCA, Static-CMOS logic exhibits the lowest power-delay product for low bit operands (i.e. 8b & 16b input data width) adder.
- For higher bit operands (i.e. 32b & 64b), HYB-TG logic gives the lowest power-delay product at both technology nodes in sub-threshold region.

(ii) Effect of Technology Scaling:

- At 45 nm technology nodes: The propagation delay is smaller and power consumption is higher than 180 nm technology for all three adder designs using three different logic design styles. The power consumption is increasing due to increments in the leakage current at 45 nm technology as compared to 180 nm technology since supply voltage is kept same at 0.4V. For CMOS inverter, the leakage currents are found to be 1.05 nA and 0.18 nA at 45 nm / 180 nm technology respectively through simulation.
- The overall power-delay product is smaller in 45 nm technology.

(iii) Effect of Adder Architecture:

- HCA is the most power efficient architecture for all logic design styles at both technology nodes (45 nm / 180 nm).
- CLA is the high-speed adder architecture for all logic design styles at both technology nodes (45 nm / 180 nm).

- For low bit operands (i.e. 8b & 16b input data width): KSA and HCA using Static-CMOS logic style provides minimum power-delay product
- For higher bit operands (i.e. 32b & 64b), KSA and HCA using HYB-TG logic style provides minimum power-delay product.
- HCA shows lowest area at both technology nodes using all three different logic design styles.

3.8. CONCLUSIONS

This chapter explores the design space of CLA, KSA and HCA architectures with different logic design style and operand size at two technology nodes (45 nm / 180 nm) in sub-threshold region. Therefore, selecting appropriate logic families with a view to understand the contribution of power, delay, and power-delay product in sub-threshold region can significantly improve the overall adder computations.

The overall results of the CLA, KSA and HCA show following conclusions at 45 nm / 180 nm technology nodes

(i) Power Consumption

The amount of power consumption directly depends on operand sizes and the complexity of the adder architectures. The large operand size adders consume more power for all logic design style at the same voltage supply and both technology nodes.

Comparison of proposed Static-CMOS based (CLA, KSA and HCA) adders with referenced designs [36][37] at 45 nm, [11][38][39] at 180 nm

- At 45 nm: For 16-bit and 32-bit, the proposed designs have lesser power consumption with respect to referenced designs. The range of reduction in power consumption varies from 34.6% to 92.8 %
- At 180 nm: For 16-bit and 32-bit, the proposed designs have lesser power consumption with respect to referenced designs. The range of reduction in power consumption varies from 41.1% to 96.3%.

Comparison of all proposed CLA, KSA and HCA designs among themselves

- At 45 nm, HCA has the least power consumption. HCA based designs consume lesser power consumption varying from 8.2% to 77.7 % as compared to KSA based designs.

Whereas as compared to CLA designs, they consume lesser power consumption, ranging from 79.4% to 96.8 %, for all bit operands.

- Similarly, for 180 nm, HCA (based designs) has the least power consumption. It consumes lesser power consumption varying from 21.2% to 56.1 % as compared to KSA. Whereas as compared to CLA, it consumes lesser power consumption varying from 89.4% to 97.1 % for all bit operands.

Therefore, HCA is the most power efficient architecture as compared to KSA and CLA in sub-threshold region.

(ii) Propagation Delay

As operand size increases, the complexity of the circuits and the number of gates count in the propagation path also increase leading to increase in propagation delay. The large operand size adders show higher propagation delay for all logic design style at the same voltage supply and both technology nodes.

Comparison of proposed Static-CMOS based (CLA, KSA and HCA) adders with referenced designs [11][36][37][38][39]

- At 45 nm: For 16-bit and 32-bit, the proposed designs give a lesser propagation delay varying from 54.6% to 75.1 %.
- At 180 nm: For 16-bit and 32-bit, the proposed designs give a lesser propagation delay varying from 7.46% to 43.1%.

Comparison of all proposed CLA, KSA and HCA designs among themselves

- At 45 nm, CLA (based designs) has the least propagation delay. It consumes lesser propagation delay varying from 44.8% to 76.4 % as compared to KSA. Whereas as compared to HCA (based designs), it gives lesser propagation delay varying from 66.6% to 79.8 % for all bit operands.
- Similarly, for 180 nm, CLA has the least propagation delay. It consumes lesser propagation delay varying from 82.6% to 93.8 % as compared to KSA. Whereas for HCA, it gives lesser propagation delay varying from 81.2% to 88.6 % for all bit operands.

Therefore, CLA is the high-speed adder architecture as compared to KSA and HCA for sub-threshold operation.

(iii) Power-Delay Product

Comparison of proposed Static-CMOS based (CLA, KSA and HCA) adders with referenced designs [11][36][37][38][39]

- At 45 nm: For 16-bit and 32-bit, the proposed designs give lesser power-delay product varying from 87% to 98.2%.
- At 180 nm: For 16-bit and 32-bit, the proposed designs give lesser power-delay product varying from 65.3% to 96.7%.

Comparison of all proposed CLA, KSA and HCA designs among themselves

In comparison to other proposed design showing highest power-delay product (at both technology nodes):

- For low bit operands (i.e. 8b / 16b), KSA and HCA using Static-CMOS logic gives lowest power-delay product.
    - (63.7% / 29.24%) lesser power-delay product for KSA
    - (32.69% / 43.64%) lesser power-delay product for HCA
- For higher bit operands (i.e. 32b / 64b), KSA and HCA using HYB-TG logic gives lowest power-delay product
    - (40.59% / 58.99%) lesser power-delay product for KSA
    - (3.23% / 15.32%) lesser power-delay product for HCA.

(iv) Effect of RBB Scheme

HYB-TG and HYB-PT logic families with RBB do not function properly at both technology nodes in sub-threshold region.

The use of RBB scheme improves sub-threshold conduction current to perform circuit operations in Static-CMOS logic. At 45 nm / 180 nm technology, the average decrement in propagation delay compared to circuit design without RBB is approximately 61.87% / 18.5%. The increments in average power consumption and power-delay product is by 77.03% / 22.5% and 38.3% / 7.3% respectively.

The use of RBB scheme in CMOS inverter shows that NM_L reduces by 62.2% / 71.7 % at 45nm /180nm technology respectively.

(v) Effect of Technology Scaling

At 45 nm, the power consumption is higher than 180 nm technology for all adder designs using different logic design styles.

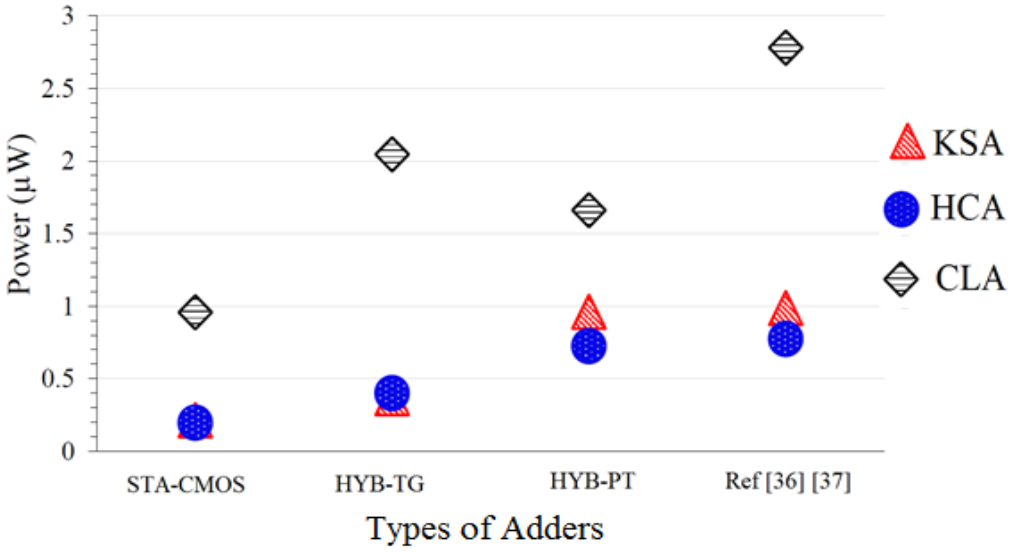
The power consumption is increasing due to increments in the leakage current at 45 nm technology as compared to 180 nm technology since supply voltage is kept same at 0.4V. Appendix A shows that simulation time has little impact on power consumption of adder.

Figure 3.41 shows the Design Space Exploration (DSE) chart of all published and proposed 32-bit CLA, KSA and HCA architectures using different logic design styles at 45 nm technology.

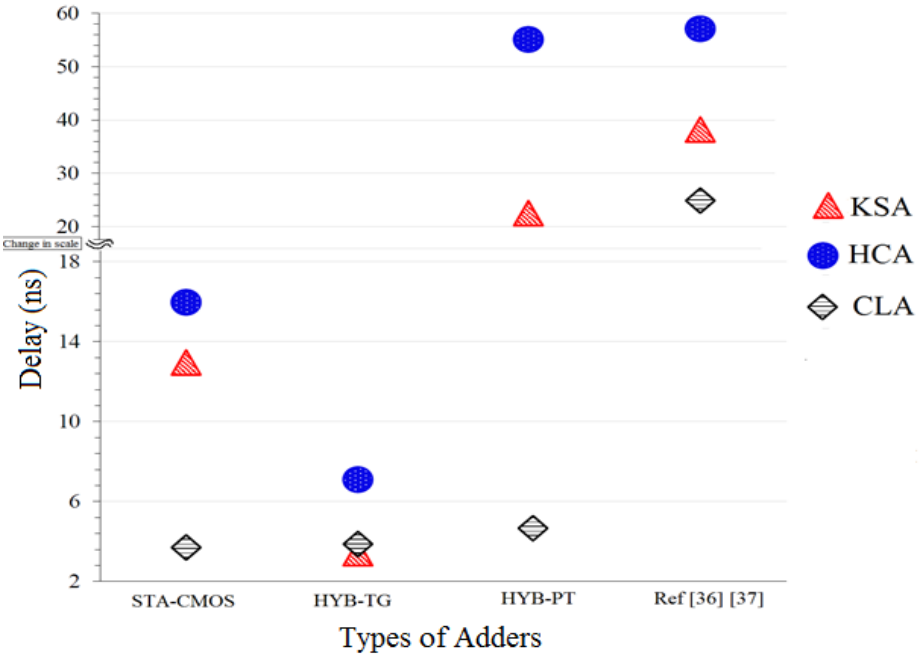
In Figure 3.41, a change of scale on y-axis is shown with a kink (~) to show the histograms for delay and power-delay product using different logic design styles in its entire range.

This is done to show the comparisons of power-delay product and delay using different logic design styles in same figure.

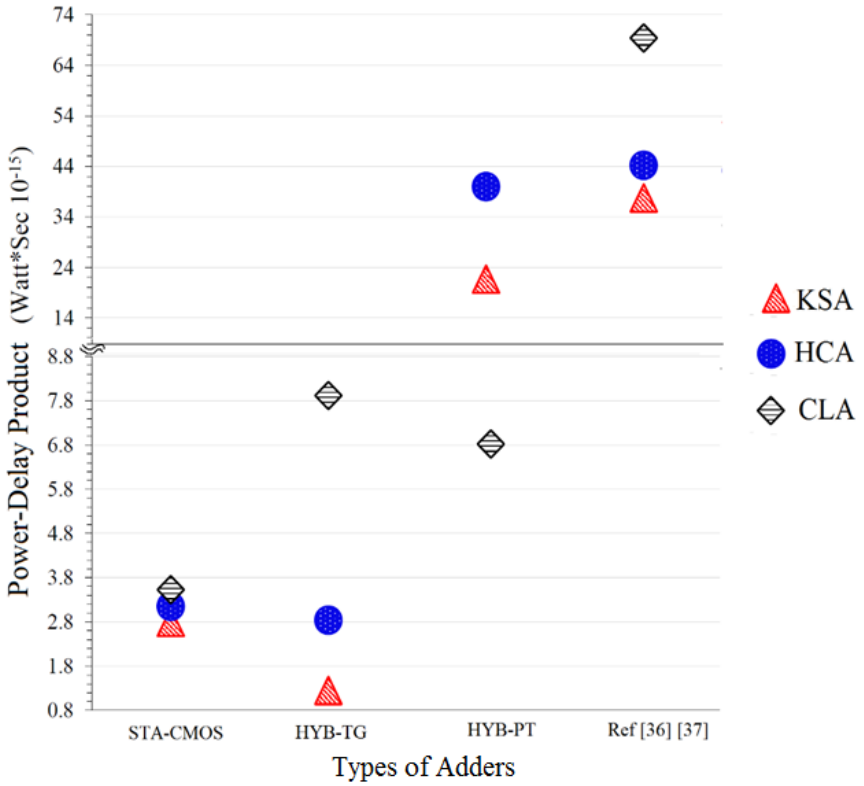
The same distribution pattern of power, delay and power-delay product of all the adder architectures are found at 180 nm technology.



(a)



(b)



(c)

Figure 3.41: DSE chart of all published referenced and proposed 32-bit CLA, KSA and HCA architectures using different logic design styles (a) power (b) delay (c) power-delay product

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CHAPTER 4

MULTIPLIERS

4.1. INTRODUCTION

Power efficient multiplication is an important fundamental function in low power arithmetic operations. Multiplication-based operations such as multiply & accumulate and inner product are among some of the frequently used computation- intensive arithmetic functions currently implemented in many Digital Signal Processing applications such as convolution, fast fourier transform, digital filters and in arithmetic & logic unit of microprocessors.

In order to maintain the rapid increase of high performance applications, emphasis will be on incorporation of low power power efficient modules in present system design. The designs of such modules partially rely on reduced power consumption in fundamental arithmetic computation units such as adders and multipliers. Improving multiplier design directly benefits the low power embedded processors used in consumer and industrial electronic products.

In the past five decades, multiplication method has moved away from the slow add-and-shift techniques to faster, parallel multiplication schemes. In the large-scale digital systems, multiplication is performed as a series of additions and shifts. The hardware typically consists of a parallel adder and registers. Therefore, the choice of multiplier architecture is of utmost importance, since its performance determines the whole system response.

In paper [1], it is found that Wallace tree and Dadda multipliers are power efficient architectures and are well suited for super-threshold operation because of reduced complexity and use of efficient adders/compressors. Also, their propagation delay is proportional to the logarithm of the operand word length in comparison to array multipliers whose delay is directly proportional to operand word length as discussed in [2][3].

Therefore, the main aim of this work is design and implementation of power efficient column compression multipliers using Wallace tree and Dadda multipliers for sub-threshold region, as few published works are available in this area [4][5].

The multiplication process is a three-step process [6]. The block diagram of n x n bit multiplier is shown in Figure 4.1.

This process begins with the generation of all partial-products which comprise of AND gate array and involves the multiplication of every multiplicand bit by every multiplier bit. Simple partial product generation method is used for the partial product generation.

Second step involves the partial-product reduction module to reduce the partial products matrix to an addition of only two operands addition. To perform parallel computation, lower/higher order compressors (Mixed L/H) are used to accumulate the partial products into two operands together in Wallace tree and Dadda multipliers.

Third step is final computation of the binary result by adders. Ripple carry adder (RCA) and HCA is used for the final computation in Wallace tree and Dadda multipliers [7].

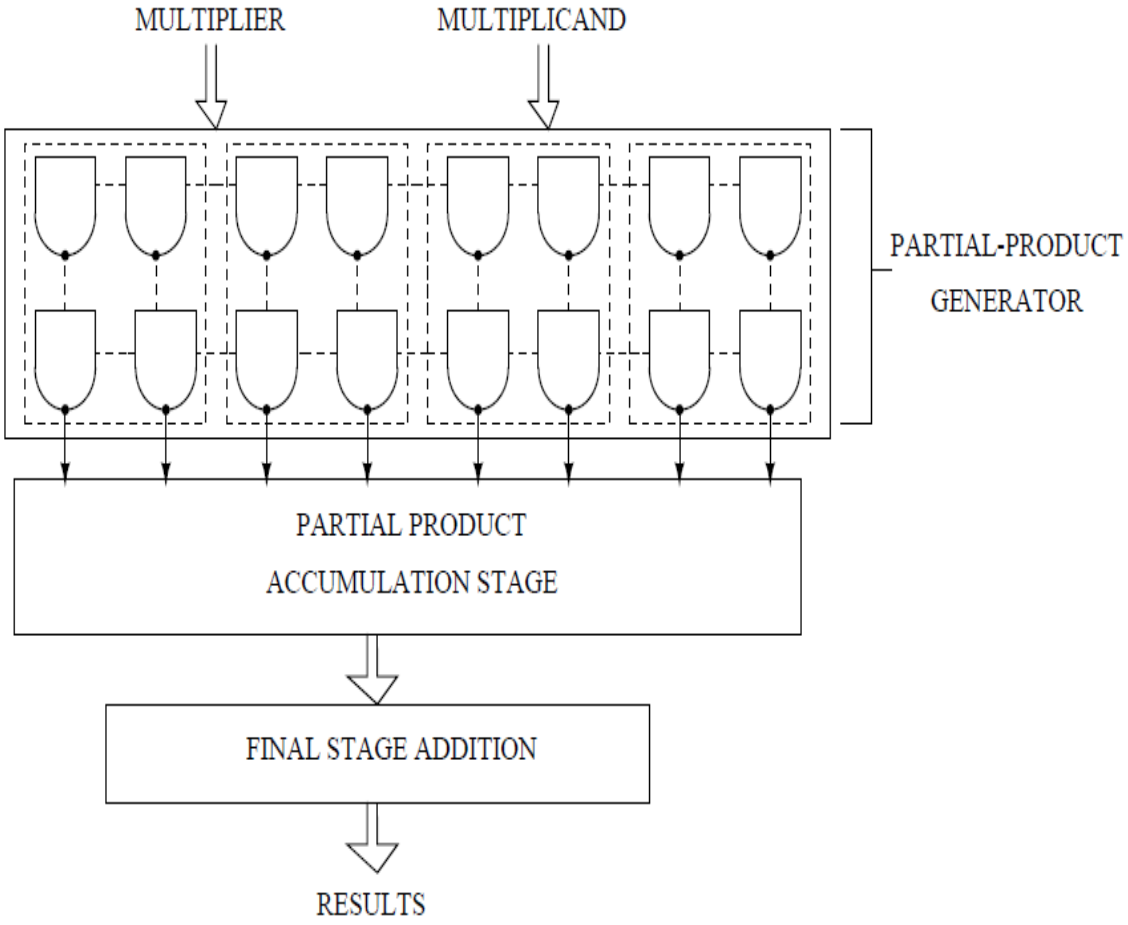


Figure 4.1: Block diagram of n x n bit multiplier

Multipliers require high amount of power and delay during the partial products accumulation stage. At this stage, most of the multipliers are designed with different kind of compressors that are capable to add two/three or at most 4, 5, 6 and 7 bits by using (2-2/3-2) lower order compressors (LOC's) or (4-2,5-2, 6-2 and 7-2) high order compressors (HOC's). These compressors are used to perform parallel computation to accumulate the partial products [8].

Therefore, its power and performance determines the overall Wallace tree and Dadda multiplier response. The power consumption of these partial product accumulation modules in multipliers depends upon the choice of logic design style.

Hence, there exist possibilities of making changes in accumulation modules of Wallace tree and Dadda multipliers in sub-threshold region for different bit-widths and different logic design style.

The main aim of this work is design and implementation of Wallace tree and Dadda multipliers by modifying partial product accumulation modules (LOC's and HOC's) using two different technology nodes (45 nm / 180 nm) operated in sub-threshold region. The performance metrics considered for the analysis of the partial product accumulation modules and multipliers are power, delay and power-delay-product.

The rest of the chapter is organized as follows:

Section 4.2 presents the partial product generation scheme. Section 4.3 presents the partial product accumulation scheme using LOC or Mixed L/H in Wallace tree and Dadda multipliers. Section 4.4 presents the internal circuitry of final adders used in Wallace tree and Dadda multipliers. Section 4.5 presents the design and analysis of partial product accumulation modules (LOC's and HOC's) used in Wallace tree and Dadda multiplier and their post layout simulation results for sub-threshold operation.

Section 4.6 presents design and analysis of Wallace tree and Dadda multipliers and their post layout simulation results for sub-threshold operation. Section 4.7 describes the final results and discussions for Wallace tree and Dadda multipliers and Section 4.8 presents a summary of the chapter and the concluding remarks.

4.2. PARTIAL PRODUCT GENERATION

Partial product generation is the first step of multiplication process. Partial products are the intermediate terms which are generated based on the value of multiplier.

The efficient partial product generation process is illustrated by the use of dot diagram. Figure 4.2 shows the dot diagram for the partial products of an 8x8 bit simple multiplication.

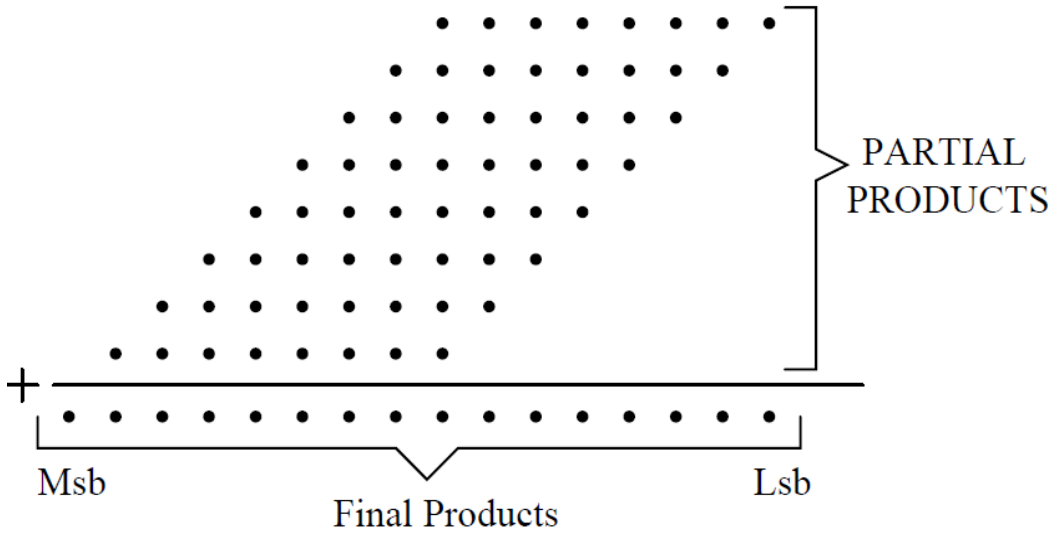


Figure 4.2: Partial products generation of 8x8-bit simple multiplication

The partial products are represented by a horizontal row of dots. Each dot in the diagram is a place holder for a single bit which can be a zero or one. If the multiplier dot bit is '0', then partial product row is also zero and if it is '1', then the multiplicand is copied as it is. From the 2nd bit multiplication onwards, each partial product row is shifted one unit to the left as shown in the Figure 4.2. The final product is represented by the double length row of dots at the bottom. For the simple multiplication algorithm, the logic consists of a single AND gate per bit as shown in Figure 4.3.

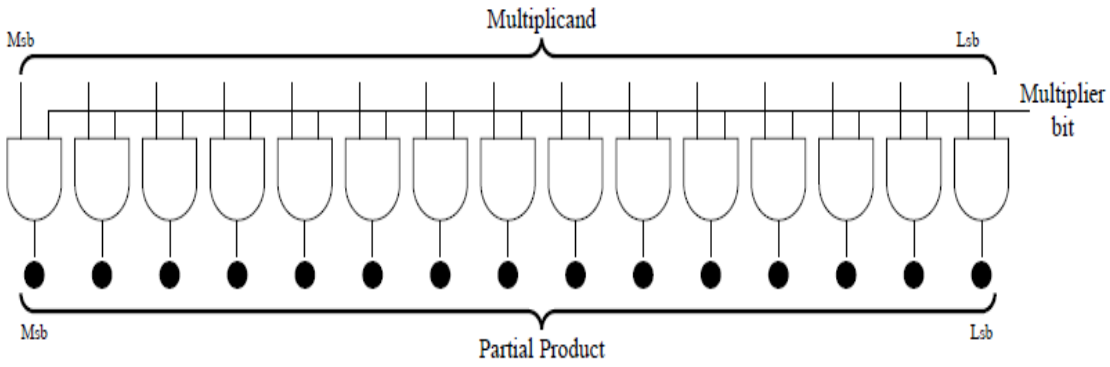


Figure 4.3: Partial products generation logic for simple multiplication

This figure shows the generation logic for a single partial product (a single row of dots). Frequently, this logic can be merged directly into whatever hardware is being used to sum the partial products.

This merging can reduce the delay of the logic elements to the point where the extra time due to the selection elements can be ignored.

However, in a real implementation, there will still be interconnect delay due to the physical separation of the common inputs of each AND gate, and distribution of the multiplicand to the selection elements [9].

4.3. PARTIAL PRODUCT ACCUMULATION

Partial product accumulation is the second step of multiplication process in which the partial products matrix is reduced to an addition of only two operands addition. Conventionally LOC designs, like 2-2 and 3-2 LOC's, are used to perform parallel computation to accumulate the partial products into two operands together.

A Full Adder's (FA's) itself is a 3-2 LOC which compresses three bits into two bits.

Similarly, the operation of the 2-2 LOC is same as the Half adder's (HA's). Alternatively, circuits that are capable to add four/five/six/seven bits are designed. These are called as higher order compressors (HOC's).

The internal architecture of a HOC is composed of LOC's. Use of Mixed L/H designs simplifies the compression and accumulation process through manipulating carry propagation used in its design [10][11].

The arrangement of the partial products and their reduction stages using LOC's and HOC's in 8x8-bit Wallace tree and Dadda multipliers are described in the sub-sections [4.3.1 - 4.3.4].

4.3.1. Partial Product Accumulation using LOC in Wallace Tree

The partial product matrix is reduced to a height of two using LOC based partial product accumulation scheme developed by Wallace tree.

The arrangement of the partial products and the reduction stages using adders in 8x8-bit Wallace tree is shown in Figure 4.4. The dots represent the partial products.

The partial products are re-arranged in a reverse pyramid style as shown in Figure 4.4 (a).

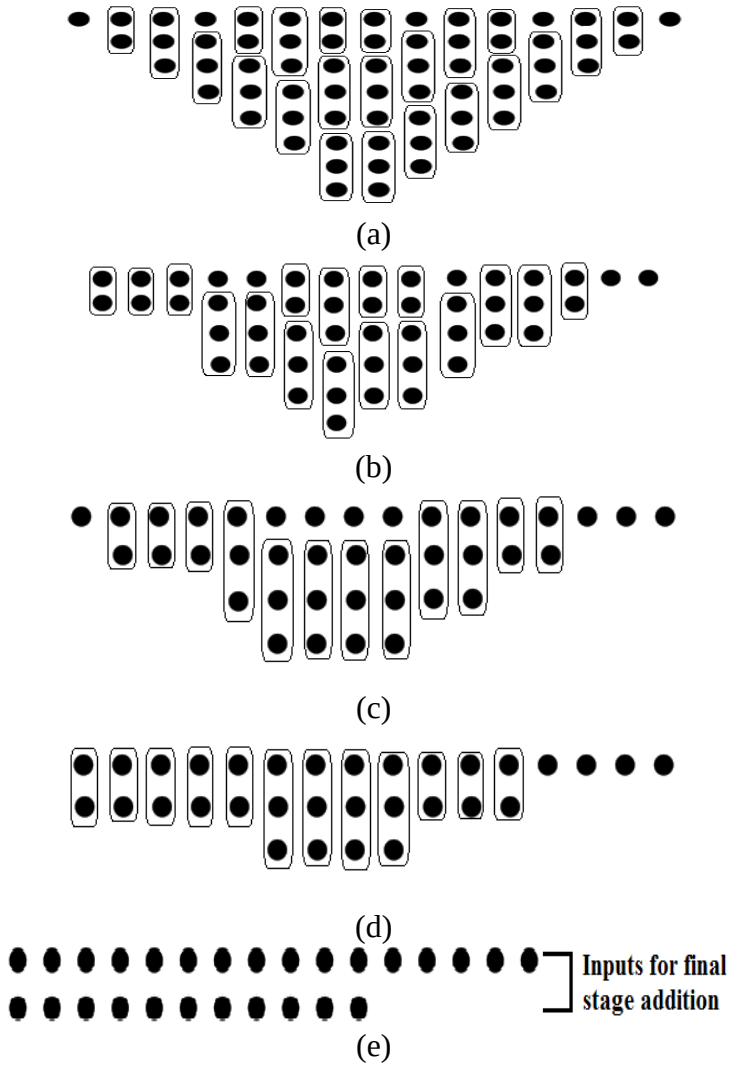


Figure 4.4: Partial product accumulation using LOC's in 8x8-bit Wallace tree

The iterative procedure for doing this is as follows:

In Figure 4.4 (a), Find out the maximum height of columns in the dot matrix array. If it is greater than 2, reduce the height by following the recursive procedure described below.

i. Check the height of each column. If it is 1, no reduction is done. If it is 2, use a 2-2 LOC else use a 3-2 LOC and check the height of column again. Continue the reduction till the height of column becomes ≤ 1.

ii. Repeat the above step for all other columns and at the end, en-queue the 'sum' strings of all 2-2 LOC and 3-2 LOC into the same columns and carry strings into the adjacent columns.

iii. Again, find out the maximum height of columns and continue the reduction using the above recursive procedure till maximum height reaches 2.

Figure 4.4 (a), (b), (c), (d) and (e) show the reduction stages for an 8x8-bit Wallace tree.

Once the height of matrix is reduced to two, final stage adder is used to generate the final product which is described later.

4.3.2. Partial Product Accumulation using Mixed L/H in Wallace Tree

The partial product matrix is reduced to a height of two using Mixed L/H based partial product accumulation scheme developed by Wallace tree.

The arrangement of the partial products and the reduction stages using compressors in 8x8-bit Wallace tree is shown in Figure 4.5. The dots represent the partial products.

The partial products are re-arranged in a reverse pyramid style as shown in Figure 4.5 (a)

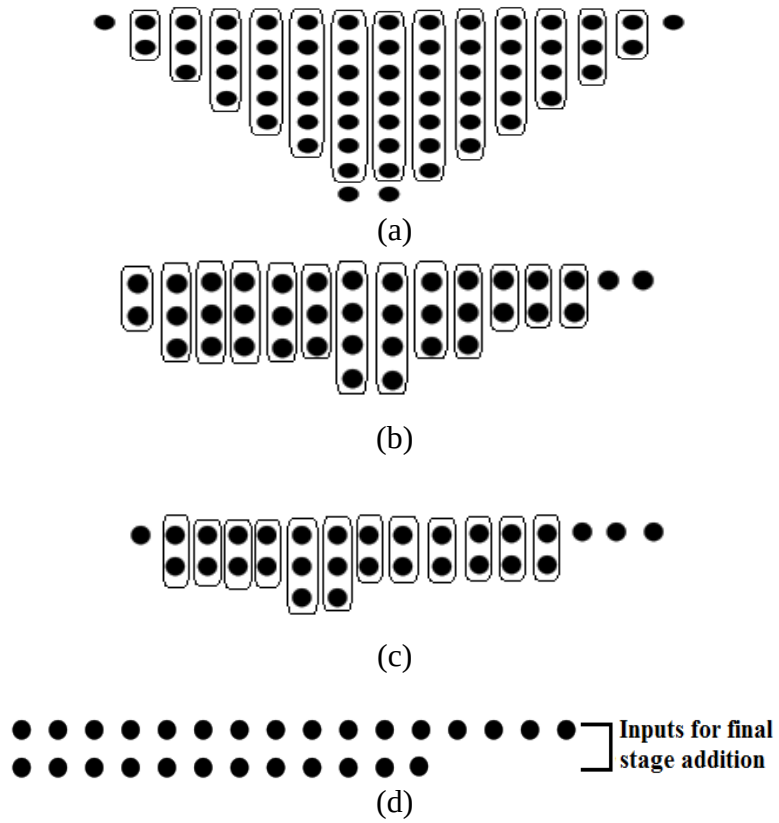


Figure 4.5: Partial product accumulation using Mixed L/H in 8x8-bit Wallace tree

The iterative procedure for reduction of column compression matrix to a height of 2 using compressors is described below.

In Figure 4.5 (a), find out the maximum height of columns in the dot matrix array. If it is greater than 2, reduce the height by following the recursive procedure described below

i. Check the height of each column. If it is 1, no reduction is done. If it is 2, use a 2-2 compressor which is nothing but a 2-2 LOC. Use 3-2 LOC, 4-2 compressor, 5-2 compressor

and 6-2 compressor if the height of the column is 3, 4, 5 and 6 respectively else use a 7-2 counter and check the height of column again. Continue the reduction till the height of column becomes ≤ 1.

ii. Repeat the above step for all other columns and at the end, en-queue the 'sum' strings of all the counters into the same queues. The only carry in case of 2-2 and 3-2 compressors are en-queued into the next queue. In case of 4-2, 5-2, 6-2 and 7-2 compressors, the carry c1 is en-queued into the next queue and the carry c2 is en-queued into the queue following it.

iii. Again, find out the maximum height of columns and continue the reduction using the above recursive procedure till maximum height reaches 2.

Figure 4.5 (a), (b), (c), (d) and (e) show the reduction stages for an 8x8 Wallace tree.

Once the height of matrix is reduced to two, final stage adder is used to generate the final product which is described later.

4.3.3. Partial Product Accumulation using LOC in Dadda Tree

The partial product matrix is reduced to a height of two using LOCs based partial product accumulation scheme developed by Dadda. The arrangement of the partial products and the reduction stages using adders in 8x8-bit Dadda tree is shown in Figure 4.6. The dots represent the partial products. The partial products are re-arranged in a reverse pyramid style as shown in Figure 4.6 (a).

The iterative procedure for reduction of column compression matrix to a height of 2 using adders is described below.

In Figure 4.6 (a), find out the maximum height of columns in the dot matrix array. If it is greater than 2, reduce the height by following the recursive procedure described below:

i. Let $h_1 = 2$ and repeat $h_{j+1} = \text{floor}(1.5*h_j)$ for increasing values of j. Continue this until the largest j is reached, for which there exists at least one column in the present stage of the matrix with more dots than h_j. Using this equation, we get $h_1=2$, $h_2=3$, $h_3=4$, $h_4=6$, $h_5=9$ and so on. e.g. in the first stage of the 8x8 Dadda tree shown in Figure 4.6 (a), the maximum height of columns is 8 therefore, the value of h_j is 6 means heights of the columns are reduced to a maximum of 6. Similarly, in the second stage, shown in Figure 4.6 (b) the maximum height of column is 6 and value of h_j is 4 heights of the columns are reduced to a maximum of 4.

ii. All the columns, with heights greater than h_j, are reduced to a height of h_j using either 2-2 LOC or 3-2 LOC. If the column height has to be reduced by one, use a 2-2 LOC else use a 3-2 LOC and continue this step till the column height is reduced to h_j.

iii. Stop the reduction if the height of the matrix becomes two, after which it can be fed to final adder.

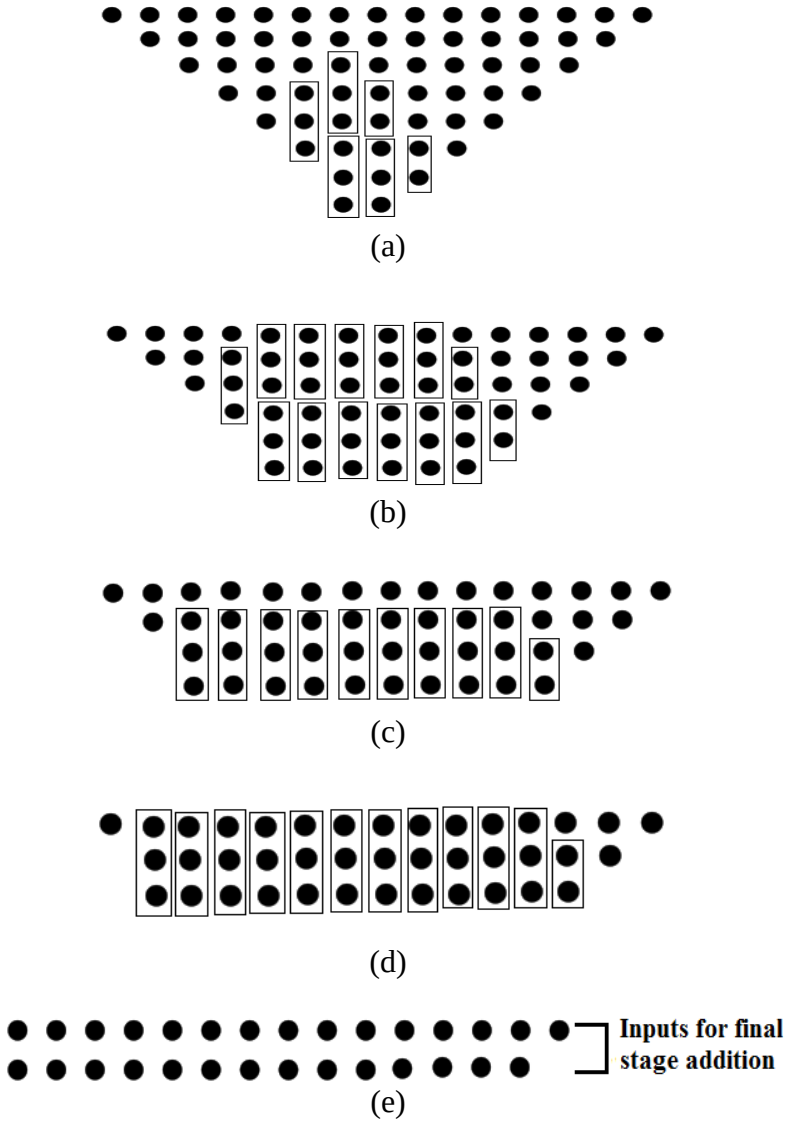


Figure 4.6: Partial product accumulation using LOC in 8x8-bit Dadda tree

Figure 4.6 (b), (c), (d) and (e) show the reduction stages for an 8x8-bit Dadda tree.

Once the height of matrix is reduced to two, final stage adder is used to generate the final product which is described later.

4.3.4. Partial Product Accumulation using Mixed L/H in Dadda Tree

The partial product matrix is reduced to a height of two using Mixed L/H based partial product accumulation scheme developed by Dadda. The arrangement of the partial products and the reduction stages using compressors in 8x8-bit Dadda tree is shown in Figure 4.7. The dots represent the partial products.

The partial products are re-arranged in a reverse pyramid style as shown in Figure 4.7 (a)

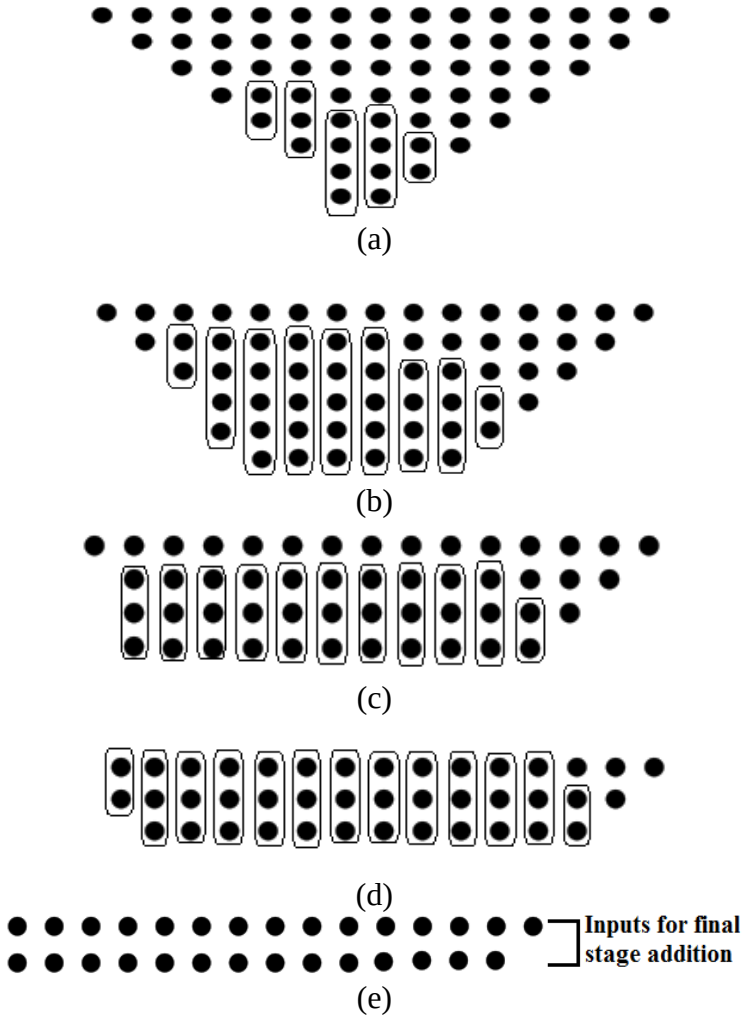


Figure 4.7: Partial product accumulation using Mixed L/H in 8x8-bit Dadda tree

i. Assuming the minimum column height i.e. $h_1 = 2$ and calculating remaining column height using formula $h_{j+1} = \text{floor}(1.5*h_j)$ for increasing values of j. Continue this until the largest j is reached such that maximum column height for the multiplier to be designed is attained. Using this equation, we get $h_1=2$, $h_2=3$, $h_3=4$, $h_4=6$, $h_5=9$ and so on. For example, in the first stage of the 8x8-bit Dadda multiplication shown in Figure 4.7 (a), the maximum height of columns is 8, therefore, the value of h_j is 6, meaning that heights of the columns are reduced to a maximum of 6. Similarly, in the second stage, shown in Figure 4.7 (b), the maximum

height of column is 6 and value of h_j is 4, meaning that heights of the columns are reduced to a maximum of 4.

ii. All the columns, with heights greater than h_j, are reduced to a height of h_j using higher order compressors of different sizes. If the column height has to be reduced by one, use a 2-2 LOC, else use a 3-2 LOC. A 4-2 compressor is used if the height has to be reduced by 3, a 5-2 compressor is used if it has to be reduced by 4, and so on and continue this step till the column height is reduced to h_j.

iii. The iterations continue until two elements remain in each queue. Once such a state has been reached then the reduction phase is completed and then it can be fed to the final adder.

iv. The first element of all queues form the first input to the adder and the second element forms the second input to the adder.

Figure. 4.7 (b), (c), (d) and (e) show the reduction stages for an 8x8-bit Dadda tree. Once the height of matrix is reduced to two, RCA and HCA is used for the final summation of the Wallace tree and Dadda multipliers.

4.4. FINAL STAGE ADDITION IN WALLACE TREE AND DADDA MULTIPLIERS

In Wallace tree's scheme, the partial products are reduced as soon as possible. Whereas Dadda's method does minimum reduction necessary at each level and requires the same number of levels as required by the Wallace tree method resulting in a design with fewer adders or compressors module. The disadvantage of Dadda's method is that it requires a slightly wider, fast final stage adder and has a less regular structure than Wallace tree's. As a result, final adder in Wallace tree multiplier is slightly smaller in size as compared to the final adder in Dadda multiplier.

Once the size of all partial-products has been reduced into two rows or less, the elements in the rows are ready to be summed using adder. The first elements of the first row form the first input to the adder/compressor and the second elements form the second input to the adder/compressors as shown in Figure 4.7.

In paper [12], it has been shown that for low operand size, RCA can match the speed of parallel addition when operating in sub-threshold, while still dissipating less (power). HCA has been found the power efficient architectures operated in sub-threshold region as compared to KSA

and CLA architecture as discussed in Chapter 3. Therefore, either RCA or HCA is used for the final computation of the binary products in Wallace tree and Dadda multipliers.

4.4.1. RCA

An 8-bit RCA is built using eight numbers of full adders where carry input (C_{in}) of each of the full adders is the carry output (C_{out}) of the previous full adders. The block diagram of 8-bit RCA is shown in Figure 4.8. C_{in} of the 1st full adder is assumed to be 0 and the C_{out} of each of the full adders ripple to the next adder. The delay of RCA is relatively high, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit.

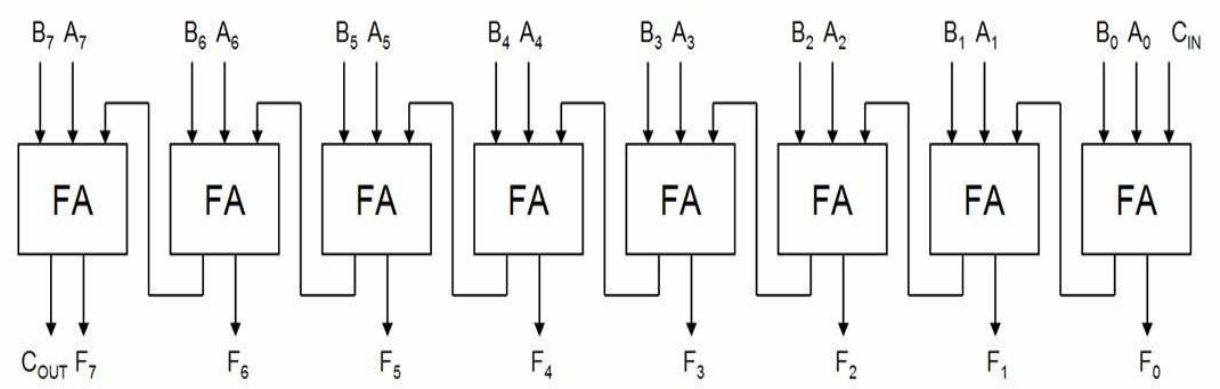


Figure 4.8: Block level diagram of 8-bit RCA

4.4.2. HCA

The HCA compute addition in two steps: one to obtain the carry at each bit, with the next to compute the sum bit based on the carry bit. The hybrid construction of a HC logarithmic prefix adder combines two designs: the KS construction which takes log2n stages and the Brent-Kung construction which takes 2log2n–1 stages. Basically the HC adder takes the best feature of KS adder, i.e., high speed, and best feature of the Brent-Kung design, i.e., low area, and combines both to provide a reasonably good speed at low complexity [13][14].

The detailed achitecture of HCA has already been discussed in Chapter 3 Section 3.5.4. The gate level architechture of HCA is used for final computation of the binary result of Wallace tree and Dadda multipliers in sub-threshold region.

4.5. DESIGN AND ANALYSIS OF PARTIAL PRODUCT ACCUMULATION MODULES

The internal standard modules are similar for both architectures (Wallace tree and Dadda) with the difference occurring in the procedure of reduction of the partial products and the size of the final adder [15].

To avoid larger power consumption and larger operation time, different accumulation circuits are developed. Implementation of basic partial product accumulation modules (using Mixed L/H) and their circuits are given in following sections.

4.5.1. LOC DESIGNS

In partial product accumulation stage, each row of the partial product matrix is input to an array of compressors to perform parallel computation.

Researchers have improved the performance of these two multipliers by reducing the number of compressor cells used in conventional multipliers, by developing a counter based Mixed L/H and by using the decomposition logic based new technique [16][17][18].

In chapter 3, three logic designs styles, Static-CMOS, HYB-PT, HYB-TG, are used to implement adders. Out of these three, HYB-PT logic based adder designs are, compact, but have higher power-delay product for all operand sizes (8 to 64) and all architectures (CLA, KSA, HCA). Thus, in present chapter, only two design styles (Static-CMOS, and HYB-TG) are used in implementation of multipliers.

Therefore, in this work, 2-2 and 3-2 LOC's are designed using Static-CMOS and HYB-TG logic in sub-threshold region.

The circuit implementation of 2-2 and 3-2 LOC's using Static-CMOS and-HYB-TG logic are given in following section:

4.5.2. LOC Design using Static-CMOS Logic

i. The 2-2 LOC is an important partial product accumulation module. The 2-2 LOC using Static-CMOS logic family gives the best results in sub-threshold region as per the literature [19]. The internal transistor level schematic diagram and its layout of 2-2 LOC using Static-CMOS logic is shown in Figure 4.9.

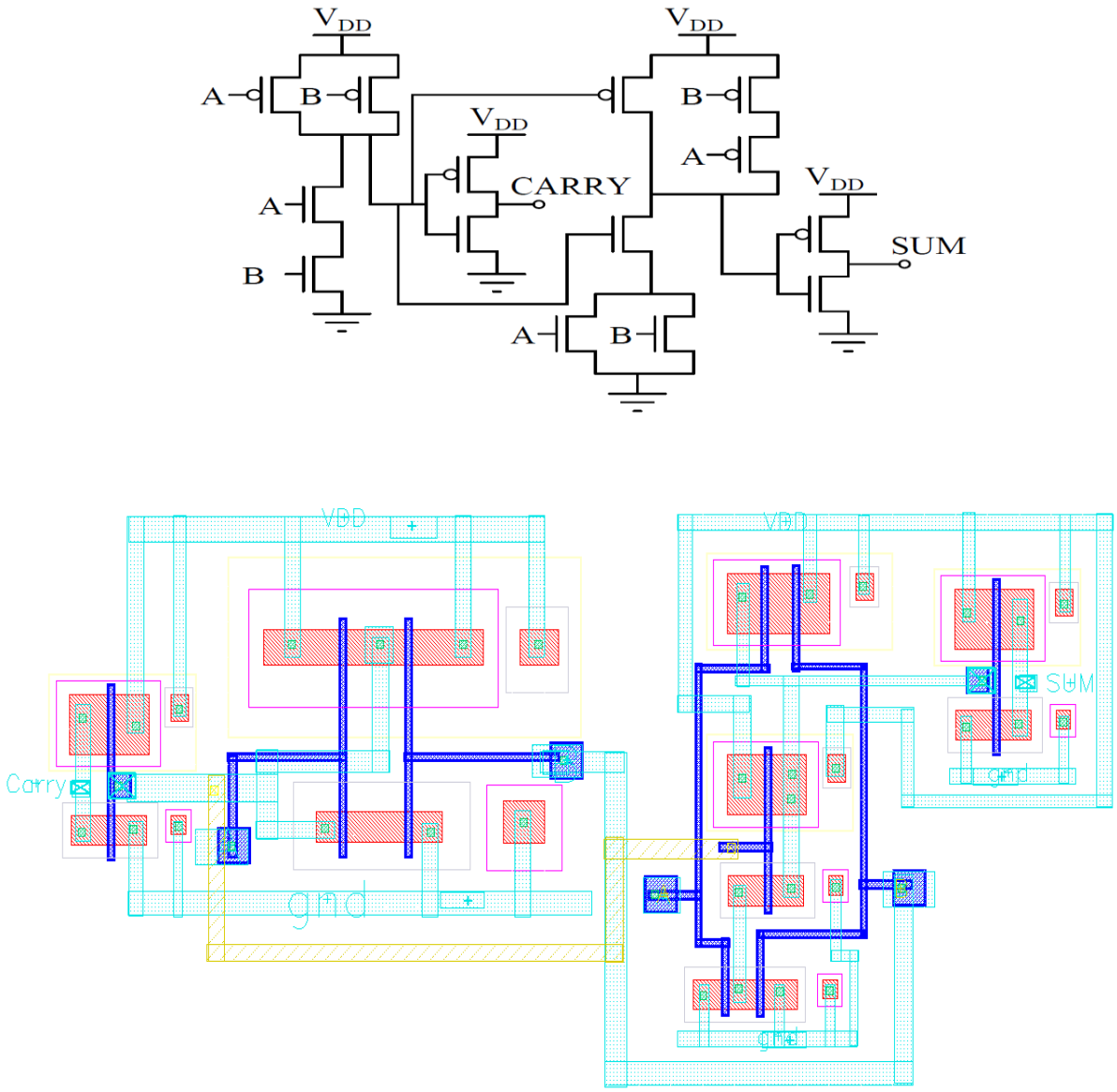


Figure 4.9: Schematic and layout of 2-2 LOC using Static-CMOS logic

ii. The 3-2 LOC is used in partial product accumulation module to reduce the number of partial product elements in the particular column. Figure 4.10 shows the schematic diagram of 3-2 LOC using Static-CMOS logic style [20][21][22].

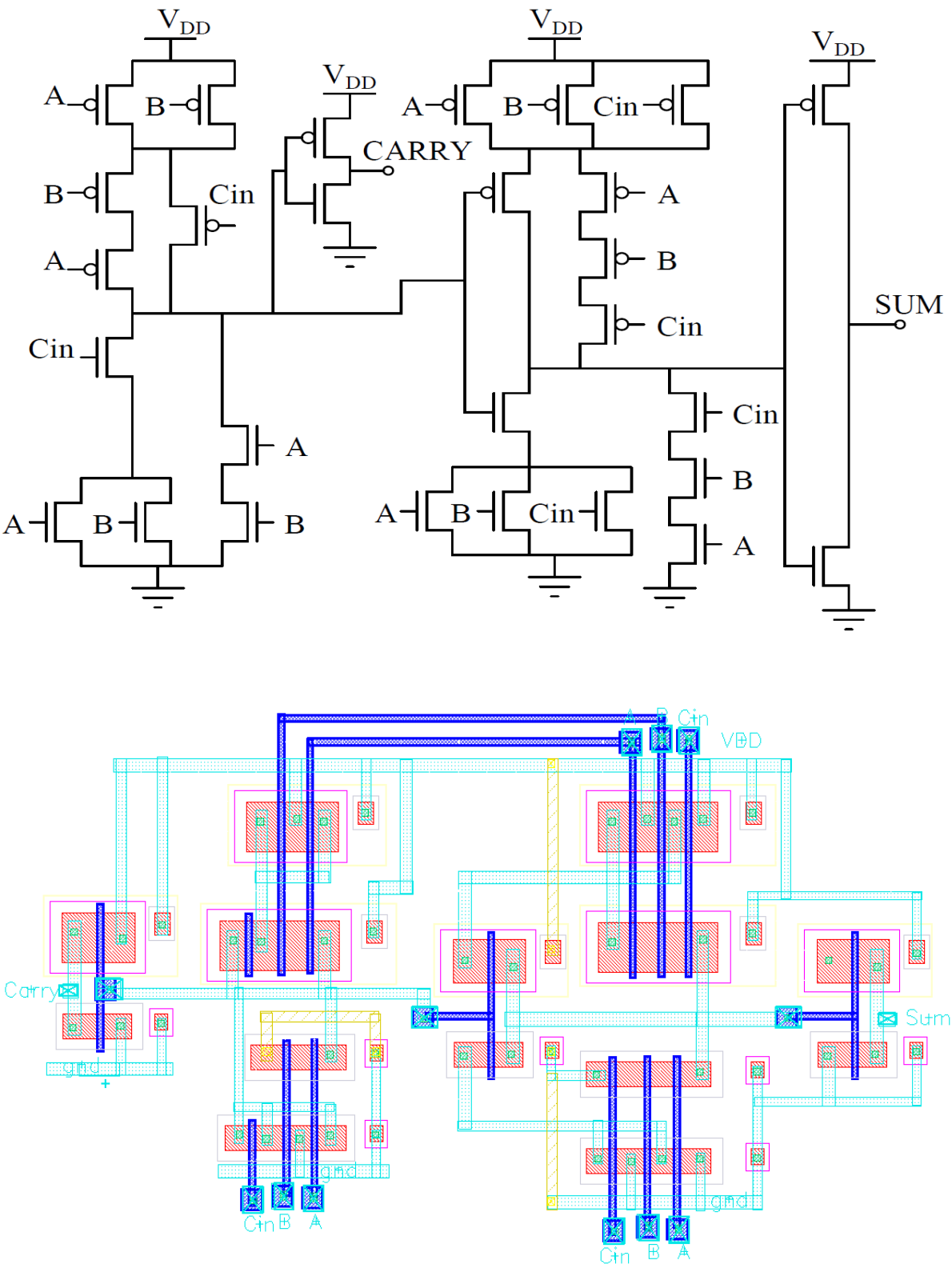


Figure 4.10: Schematics and Layouts of 3-2 LOC using Static-CMOS logic

4.5.3. LOC Design using HYB-TG Logic

LOC cells are the combinations of 2:1 MUX and 4:1 MUX using HYB-TG logic design style. The internal circuit's implementation of 2:1 MUX and 4:1 MUX using HYB-TG logic with their layouts are shown in Figures 4.11 and 4.12 respectively.

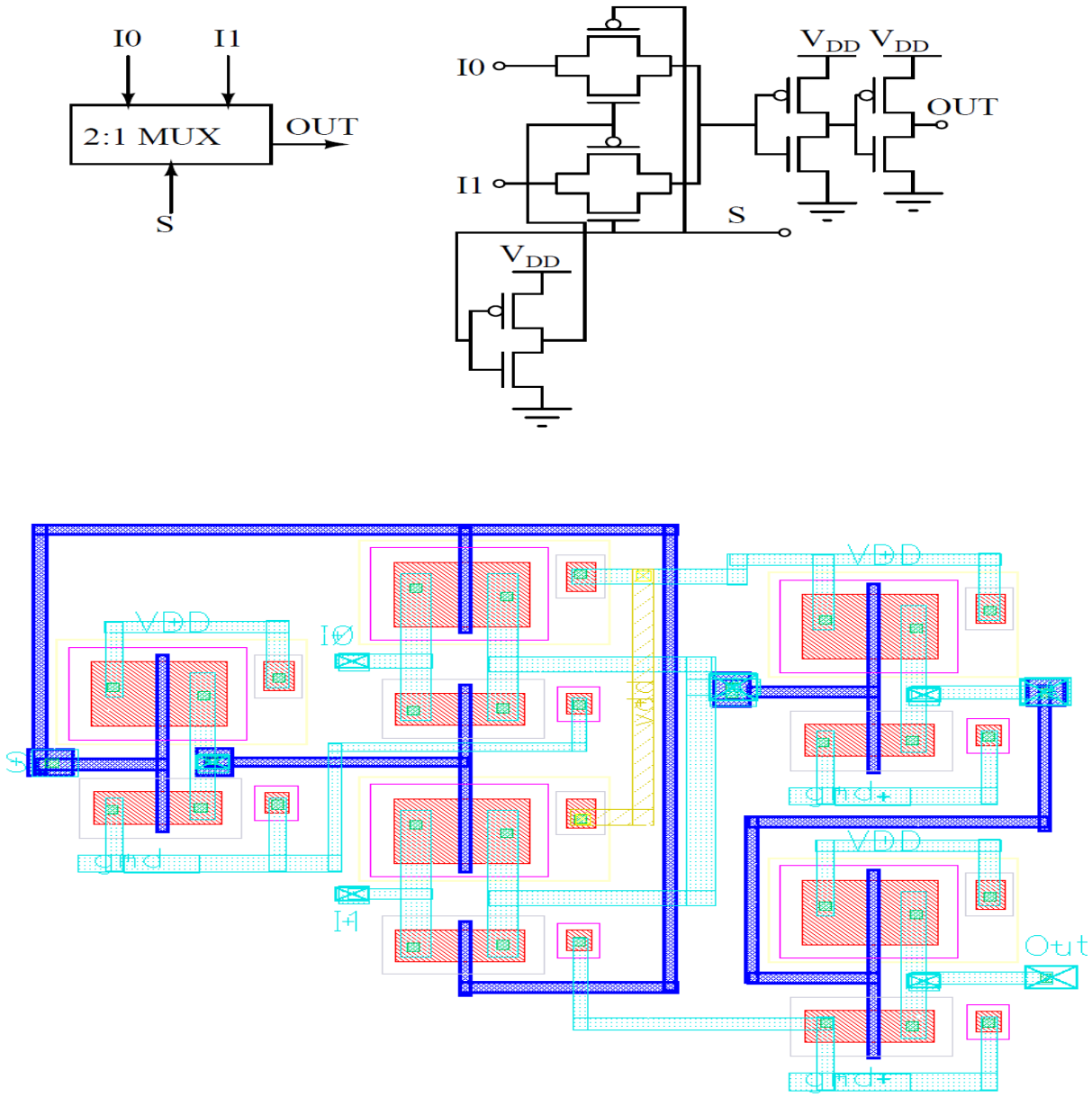


Figure 4.11: Schematic and layout of 2:1MUX using HYB-TG logic

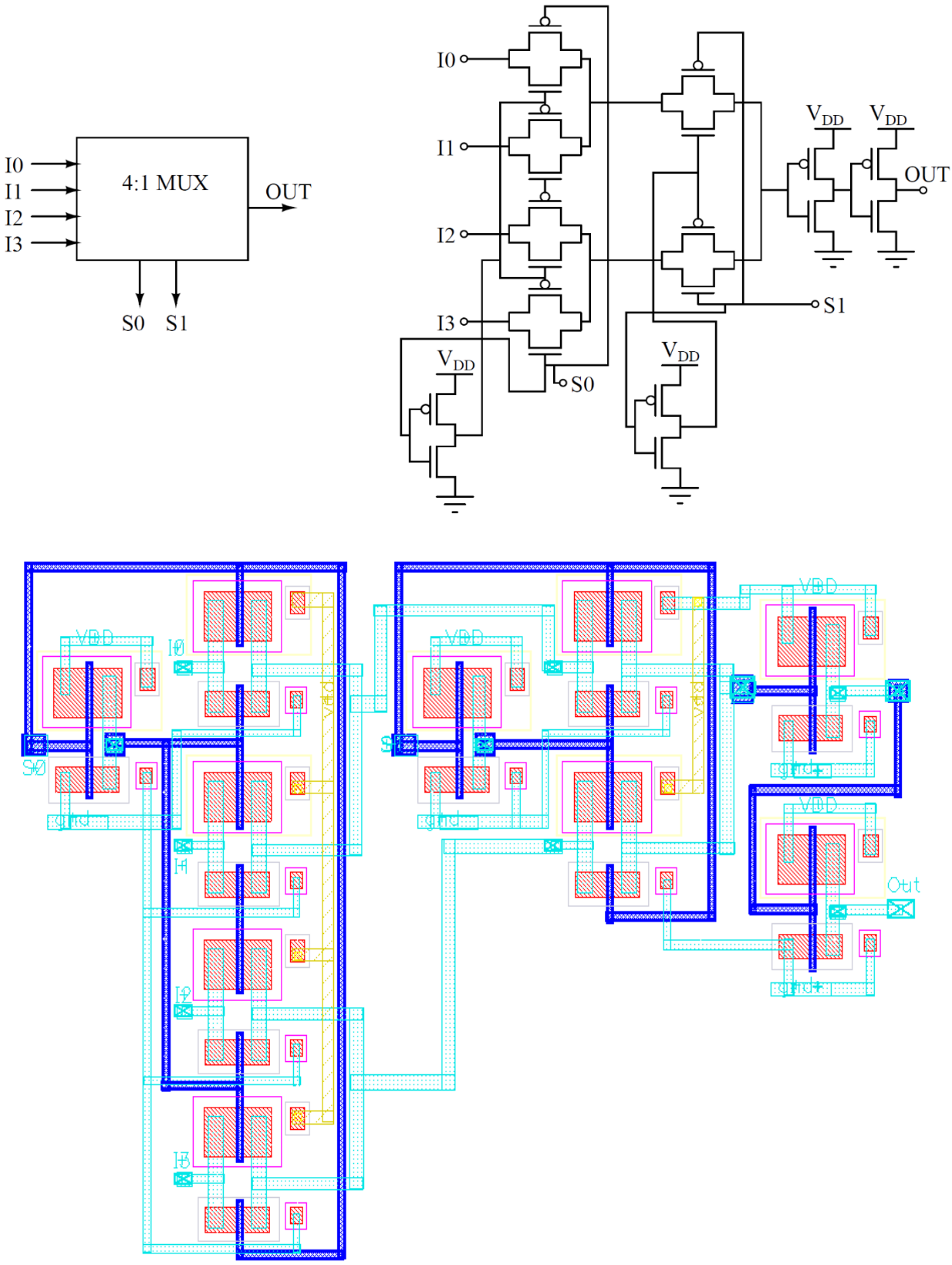


Figure 4.12: Schematic and layout of 4:1 MUX using HYB-TG logic

i. The 2-2 LOC cell using HYB-TG logic design style, takes two inputs X1, X2 and generates two outputs Sum and Carry. The internal transistor level schematic diagram and its layout of 2-2 compressor using HYB-TG logic is shown in Figure 4.13.

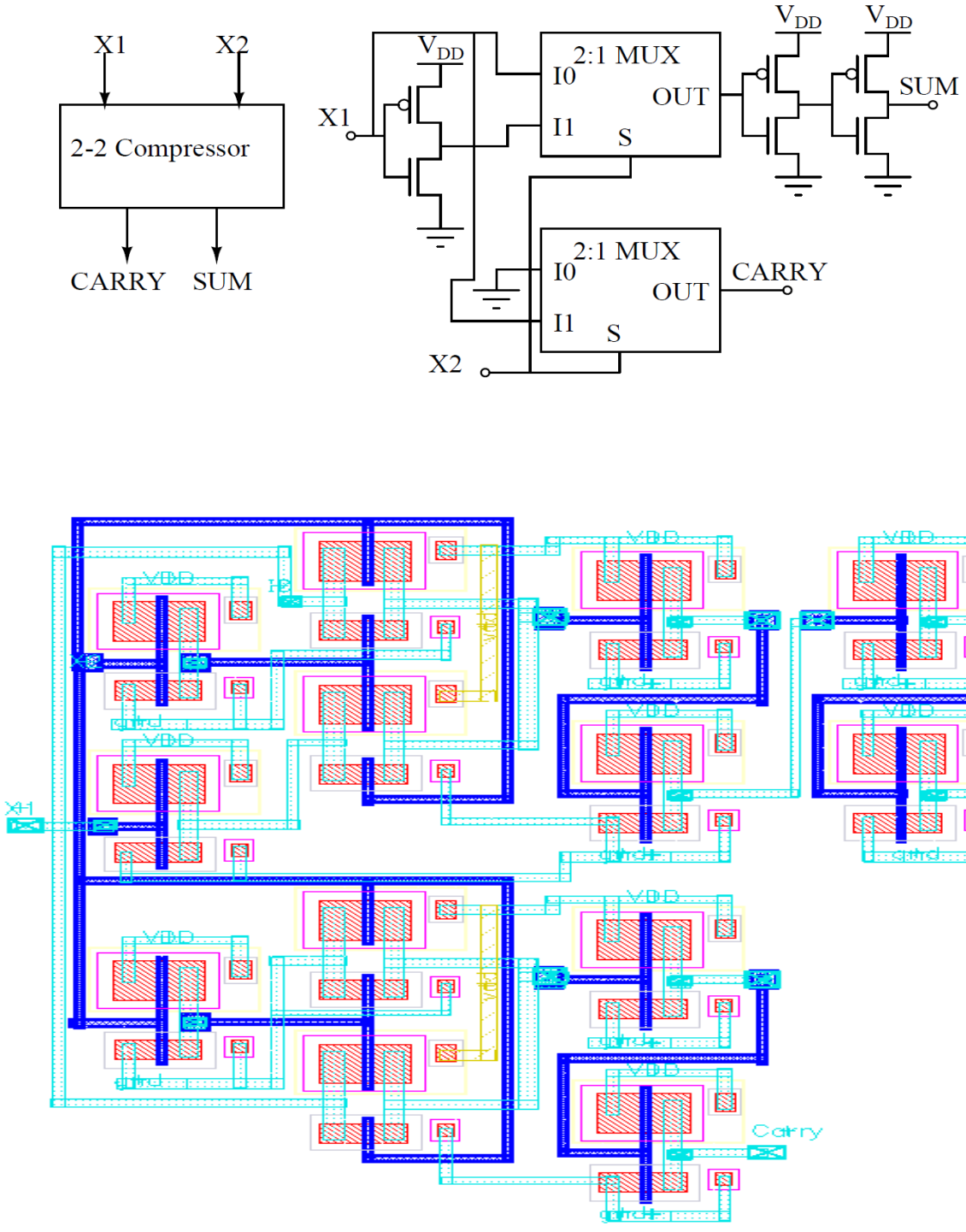


Figure 4.13: Schematic and layout of 2-2 LOC using HYB-TG logic

ii. The 3-2 LOC cell using HYB-TG logic design style, takes three inputs X1, X2, X3 and generates two outputs Sum and Carry. The internal transistor level schematic diagram and its layout of 3-2 LOC using HYB-TG logic is shown in Figure 4.14.

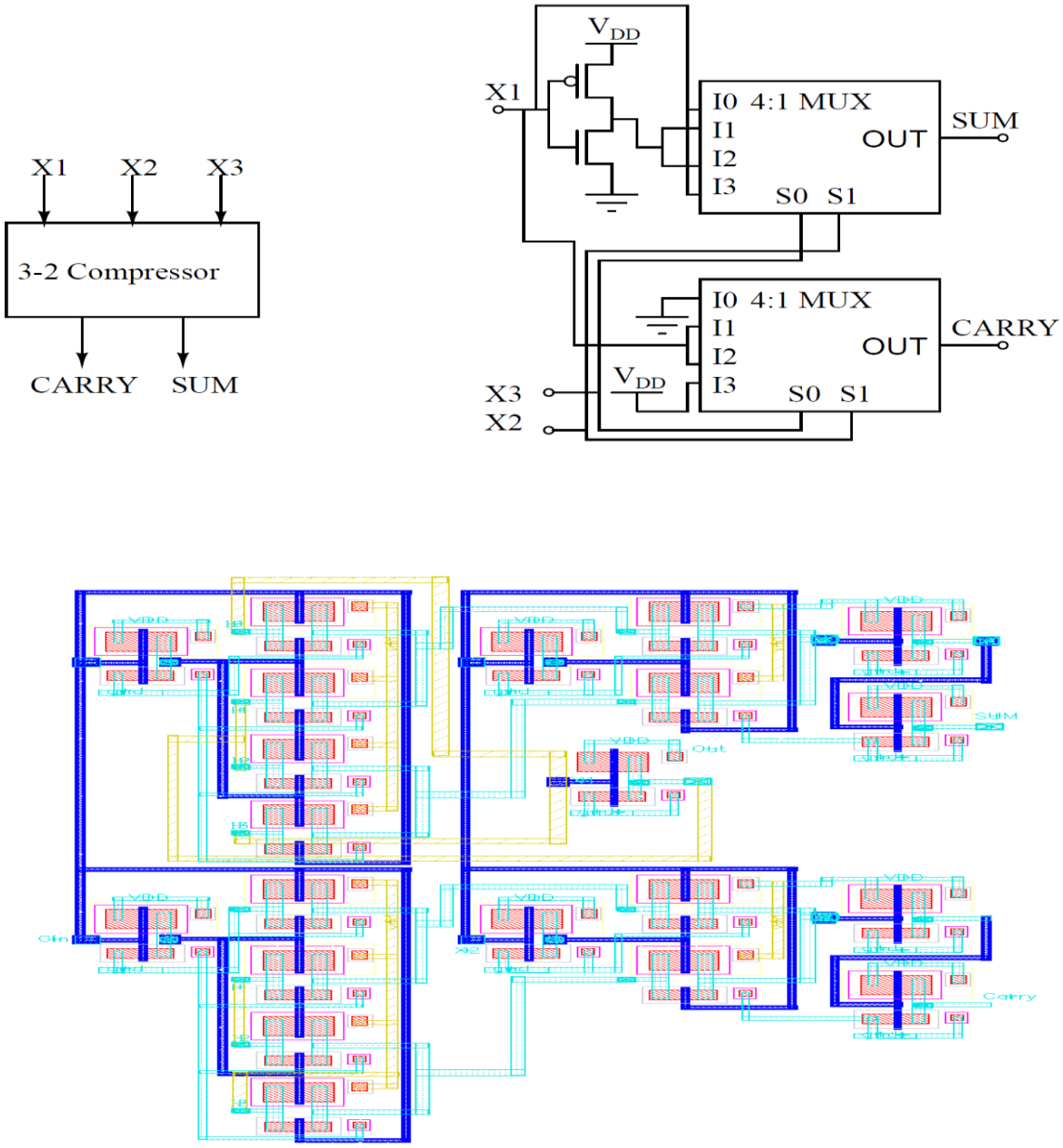


Figure 4.14: Schematic and layout of 3-2 LOC using HYB-TG logic

4.5.4. Higher Order Compressors (HOC)

For higher order multiplication, HOC's (4-2, 5-2, 6-2, and 7-2) are used to compress the bits [23][24]. The HOC's can be derived using a single bit adder circuit. It has four/five/six/seven inputs and three outputs.

The HOC cells (4-2, 5-2, 6-2 and 7-2) can be implemented in many different logic structures [25][26]. However, in general, it comprises of three main modules. The first module is required to generate XOR/XNOR function, the second module is used to generate sum and the last module is used to produce the carry output.

Conventionally, the implementations of compressors are composed of serially connected full adders and MUX. At gate level, HOC's are anatomized into XOR gates and carry generators are normally implemented by MUX. Therefore, different designs can be classified based on the critical path delay, in terms of the number of primitive gates. There are several designs of the XOR and MUXs, which have already been proposed using different logic styles [27] [28]. In [29][30][31], 4-2, 5-2, 6-2 and 7-2 compressors have been designed using different circuit techniques to achieve the improvement in terms of both delay and power.

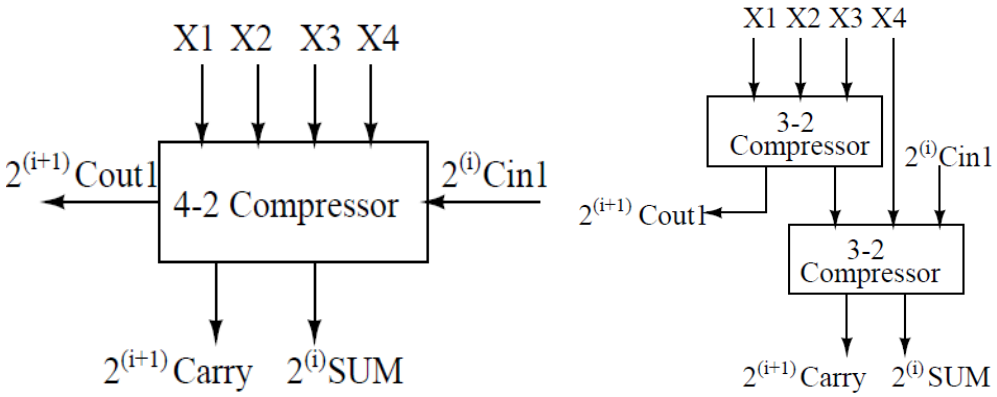
In this proposed work, compressors utilize the standard hierarchical design approach, where the HOC's are built using 2-2 and 3-2 compressor cells. Input combinations and the corresponding decimal counts of all compressors and their functionalities are shown in Table 4.1.

Table 4.1: Truth table of different Compressors (2-2, 3-2, 4-2, 5-2, 6-2, and 7-2)

(Decimal count)	**Input Conditions**	**2-2 Outputs (C,S)**	**3-2 Outputs (C,S)**	**4-2 Outputs (C2,C1,S)**	**5-2 Outputs (C2,C1,S)**	**6-2 Outputs (C2,C1,S)**	**7-2 Outputs (C2,C1,S)**
0	All the inputs are zero	(0,0)	(0,0)	(0,0,0)	(0,0,0)	(0,0,0)	(0,0,0)
1	Any one input is one	(0,1)	(0,1)	(0,0,1)	(0,0,1)	(0,0,1)	(0,0,1)
2	Any two inputs are one	---	(1,0)	(0,1,0)	(0,1,0)	(0,1,0)	(0,1,0)
3	Any three inputs are one	---	---	(0,1,1)	(0,1,1)	(0,1,1)	(0,1,1)
4	Any four inputs are one	---	---	---	(1,0,0)	(1,0,0)	(1,0,0)
5	Any five inputs are one	---	---	---	---	(1,0,1)	(1,0,1)
6	Any six inputs are one	---	---	---	---	---	(1,1,0)
7	All the inputs are one	(1,0)	(1,1)	(1,0,0)	(1,0,1)	(1,1,0)	(1,1,1)
Note: *C, C1, C2 are the carry bits, S is the Sum bit of compressors. C2 is the most significant bit and S is the least significant bit.*							

4.5.4.1. Conventional and Modified Architecture of 4-2 Compressor

i. Conventional architecture of 4-2 compressor [25][26]: Figure 4.15 shows the conventional architecture of 4-2 compressor.



(a) (b)

Figure 4.15: The conventional architecture of 4-2 compressor

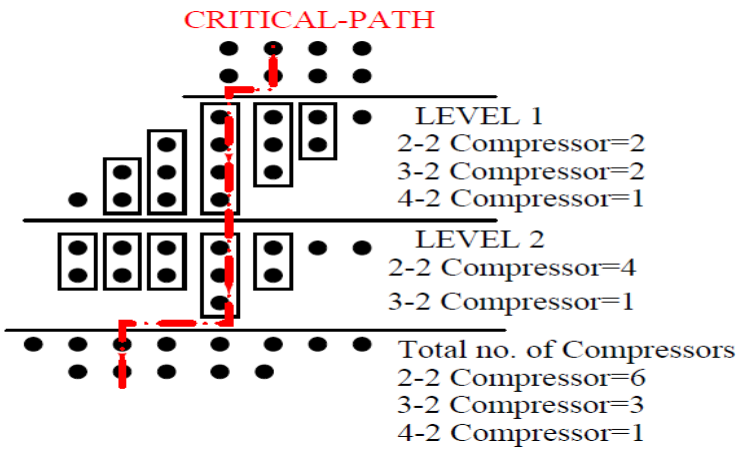
Figure 4.15(a) shows the block diagram of conventional architecture of 4-2 compressor.

Figure 4.15 (b) shows that a conventional 4-2 compressor consists of two serially connected 3-2 compressors and involves a critical path delay of 4 XOR/MUXs. It has the five input bits (X1, X2, X3 and X4) at i^{th} position including a carry-in (Cin1) from the neighboring cell at $(i-1)^{th}$ position. It has three outputs SUM at i^{th} position, Carry and carry-out (Cout1) at $i+1^{th}$ position.

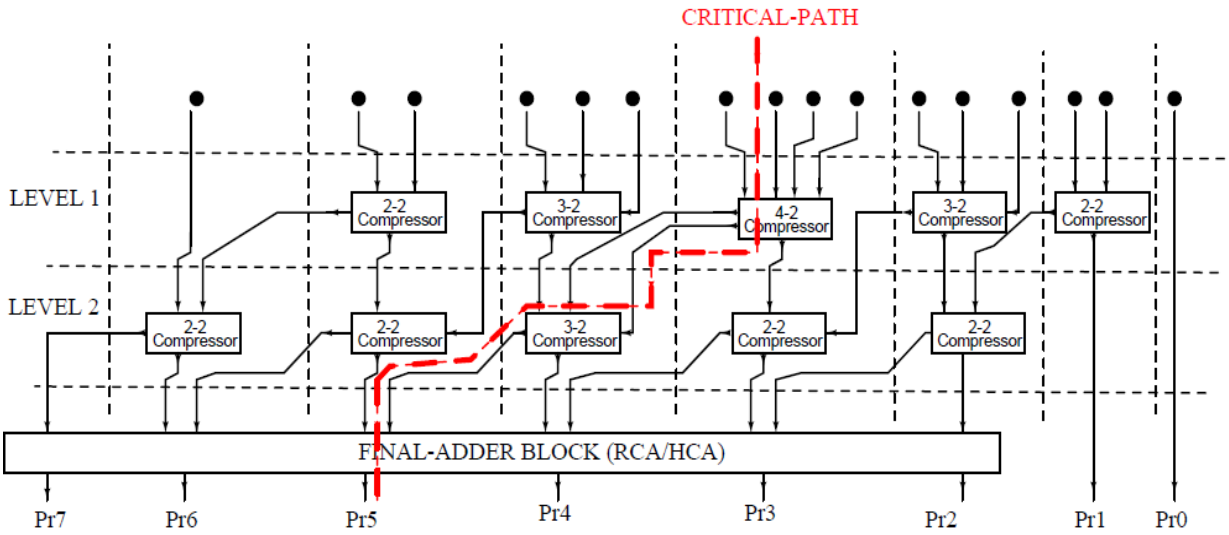
The conventional 4-*2* compressor abides by the fundamental equation as given in Eq. (4.1)

$$X0 + X1 + X2 + X3 + Cin1 = 2^{i}SUM + 2^{i+1}.(Carry + Cout1) \quad (4.1)$$

The operation and implementation of 4x4-bit Wallace tree multiplier using conventional architecture of compressors is shown in Figure 4.16.



(a)



(b)

Figure 4.16: The conventional architecture of compressors used in 4x4-bit Wallace tree multiplier

Figure 4.16 (a) shows the operation using dot diagram of conventional compressors based 4x4-bit Wallace tree multiplier. It utilizes total ten numbers of compressors which includes six 2-2 compressors, three 3-2 compressors and one 4-2 compressor cell.

Figure 4.16 (b) shows the implementation and signal flow in its critical delay path. The critical delay path utilizes following number of gates

Critical Path $_{Conventional}$ = (One 4-2 Compressor + One 3-2 Compressor)

= {(Four XOR, Two MUX's) + (Two XOR and One MUX's)}

ii. Modified architecture of 4-2 compressor: Figure 4.17 shows the modified architecture of 4-2 compressor.

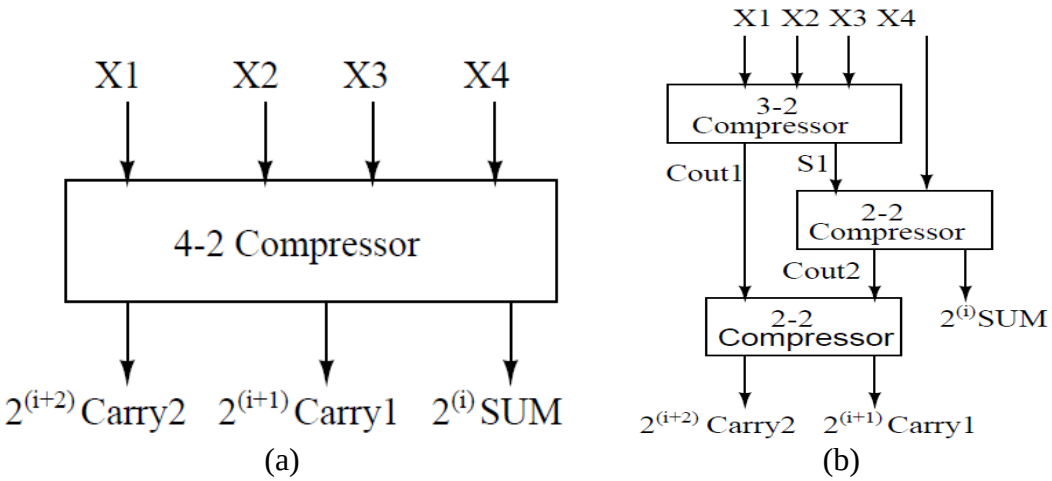


Figure 4.17: The modified architecture of 4-2 compressor

Figure 4.17 (a) shows the block diagram of modified architecture of 4-2 compressor.

Figure 4.17 (b) shows that in contrast to the conventional design, the modified 4-2 compressor cell is composed of serially connected one 3-2 compressor and two 2-2 compressors. It has the four input bits (X1, X2, X3 and X4) at i^{th} position. It has three outputs final SUM at i^{th} position, Carry1 at $i+1^{th}$ and Carry2 at $i+2^{th}$ position. The modified 4-2 compressor cell does not include a carry-in (Cin1) bit from the neighboring cell.

The modified 4-2 compressor abides by the fundamental equation as given in Eq. (4.2)

$$X0 + X1 + X2 + X3 = 2^{i}SUM + 2^{i+1}Carry1 + 2^{i+2}Carry2 \quad (4.2)$$

The operation and implementation of 4x4-bit Wallace tree multiplier using modified architecture of compressors is shown in Figure 4.18.

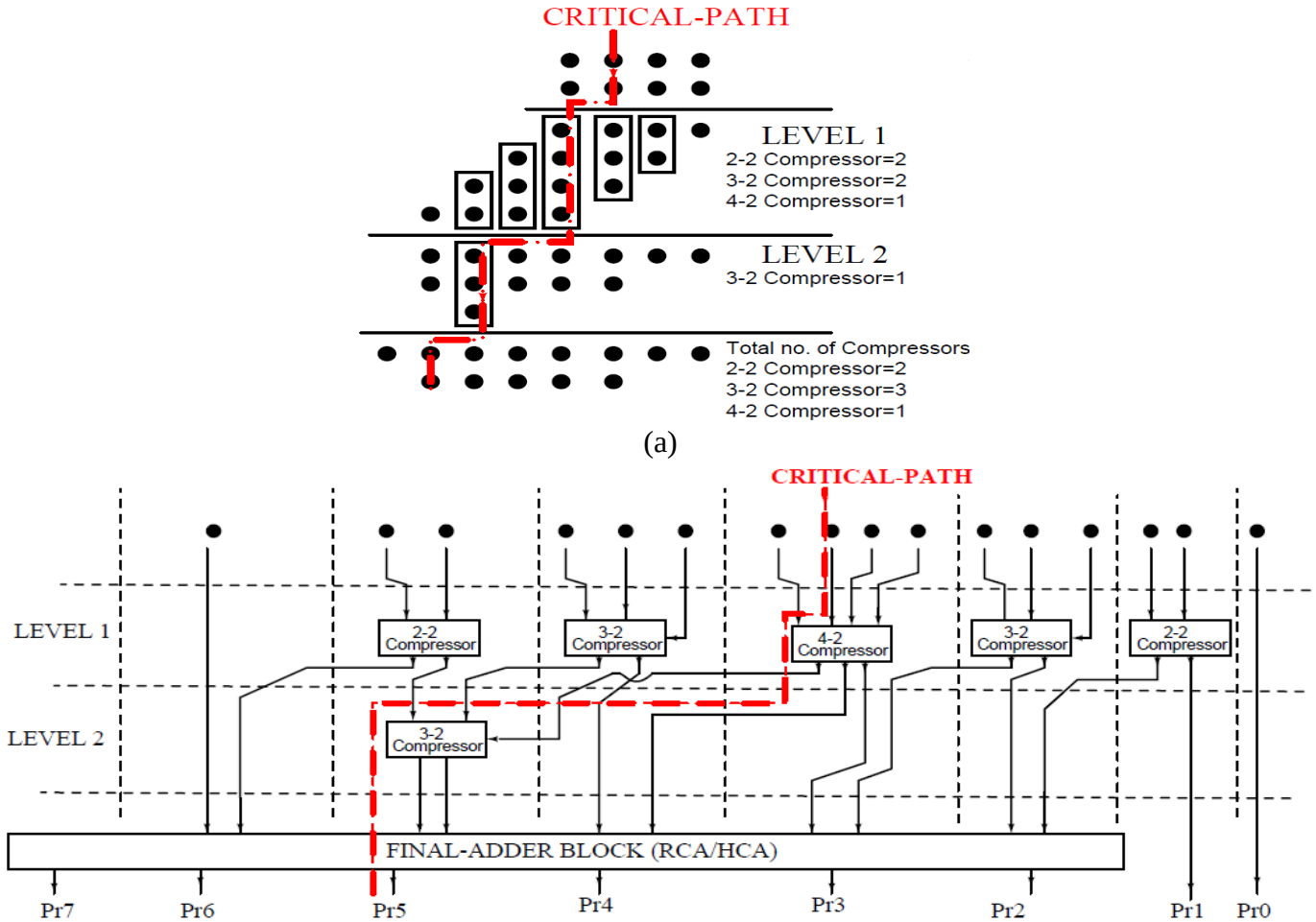


Figure 4.18: The modified architecture of compressors used in 4x4-bit Wallace tree multiplier

Figure 4.18 (a) shows the operation using the dot diagram of modified compressors based 4x4-bit Wallace tree multiplier. It utilizes total six numbers of modified compressors which combine two 2-2 compressors, three modified 3-2 compressors and one 4-2 compressor cell.

Figure 4.18 (b) shows the implementation and signal flow in its critical delay path. The critical delay path utilizes following number of gates:

Critical Path $_{Modified}$ = (One 4-2 Compressor + One 3-2 Compressor)

= {(Six MUX's) + (Two MUX's)}

Therefore, in contrast to conventional compressor cells based 4x4-bit Wallace tree multiplier, the modified compressor cells based multiplier reduces the total number of compressor cell which reduces the overall area of the multiplier.

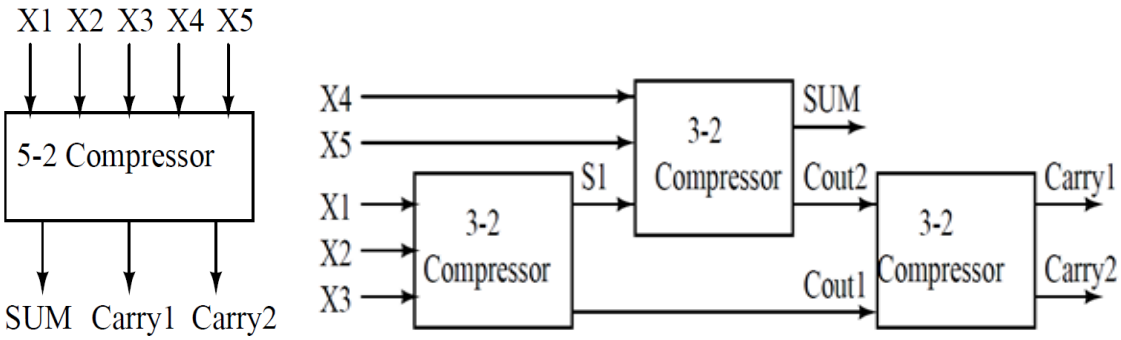
Hence, in this work, based on less hardware requirement, modified compressor cells are used for implementation of partial product accumulation stage of multipliers.

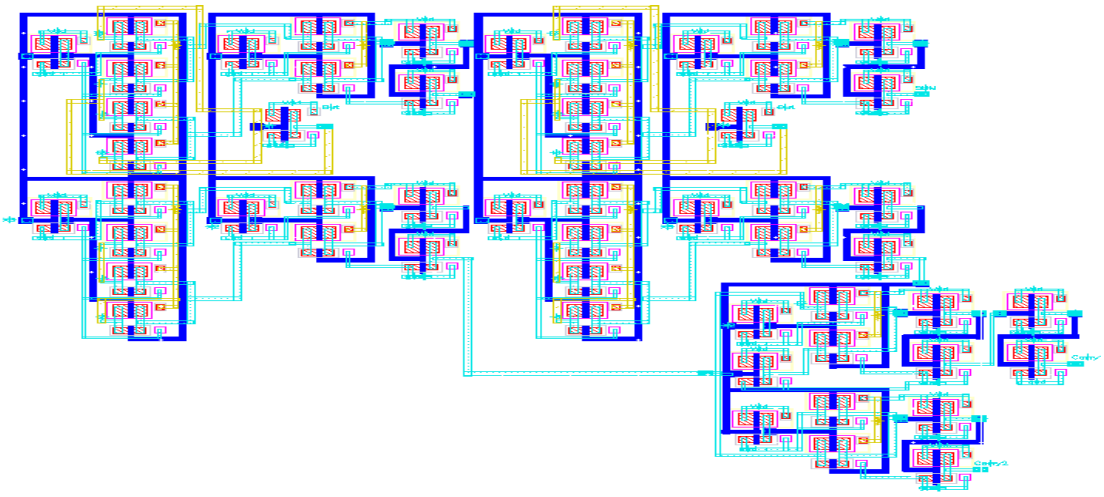
4.5.4.2. Design Implementation of Modified HOC's (5-2, 6-2 and 7-2)

All modified HOC cells (5-2, 6-2 and 7-2) are implemented by using two different logic style (Static-CMOS and HYB-TG cell). The internal transistor level diagram of 2-2 and 3-2 compressors using Static-CMOS design style and using HYB-TG cell have been given in Sections 4.5.2 and 4.5.3.

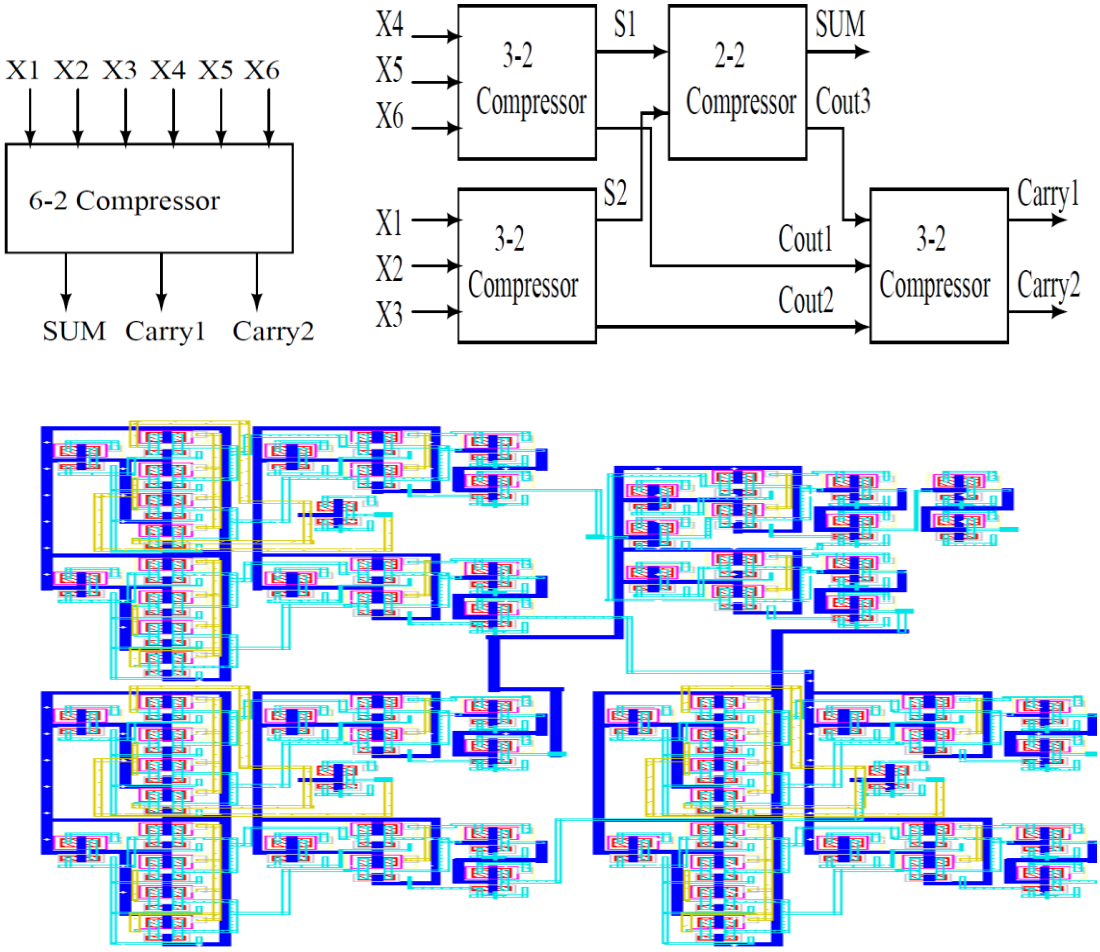
In the modified HOC's (5-2, 6-2 and 7-2), the internal signals (Cout1, Cout2 and Cout3) from one of the internal blocks acts as the carry input to succeeding block and finally generates one SUM and two carry (Carry1, Carry2) outputs as shown in Figure 4.19.

The internal blocks and designs of the compressors cell is discussed below

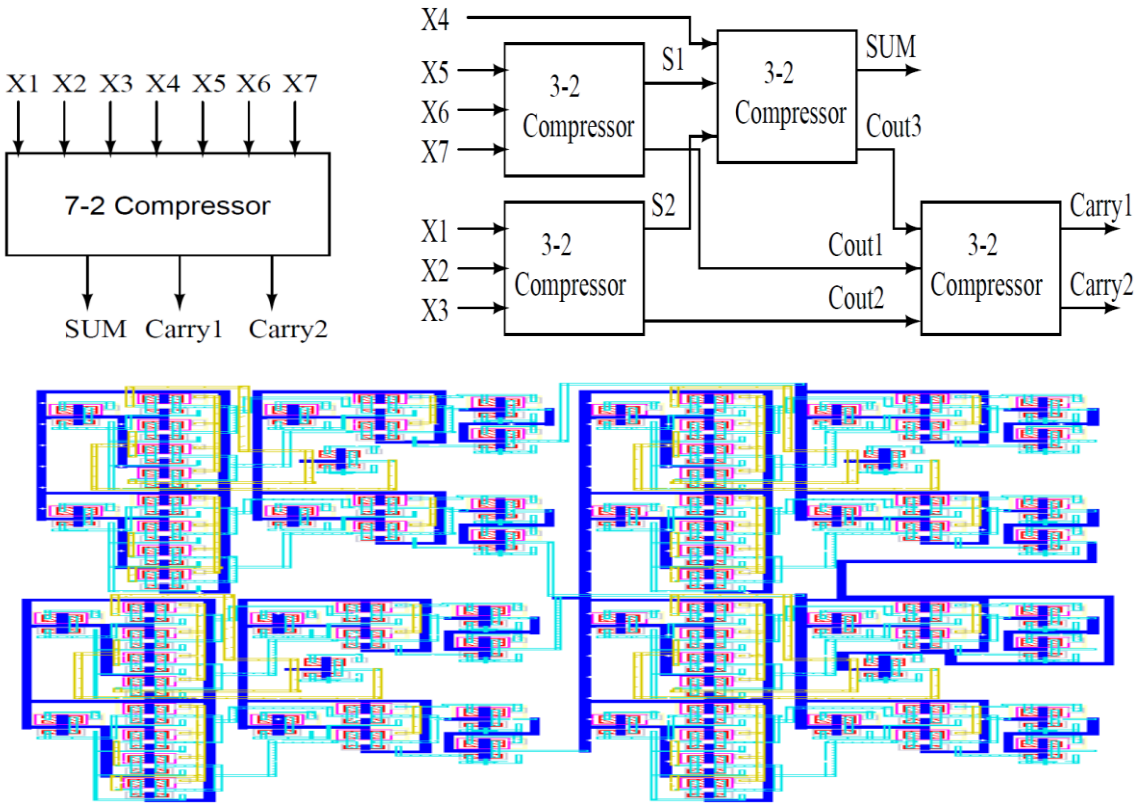




(a) Modified 5-2 compressor



(b) Modified 6-2 compressor



(c) Modified 7-2 compressor

Figure 4.19: The schematics and layouts of modified HOC's

4.5.5. Performance Analysis of Compressor Designs using Different Logic Design Styles for Sub-Threshold Operation

This section gives the performance analysis of compressors designs for partial product accumulation using different selected (Static-MOS and HYB-TG) logic design styles.

Table 4.2 gives the measured power, delay and power-delay product of all compressors design using Static-CMOS and HYB-TG logic design styles.

The simulated results show that all the modules are properly functional in sub-threshold region at supply voltage as low as 0.4 V. The schematic and layouts are designed and simulated using two different technologies (45 nm / 180 nm). The designs are characterized in terms of power, delay and power-delay product. For minimum power-delay product, the W/L's of all MOS transistors are chosen to keep the pull up to pull down network ratio as 2:1 in all designed logic modules [8].

Table 4.2: Simulation results of LOC and modified HOC Designs

Module name	Logic style	Number of transistors	Power (nW)		Delay (ns)		Power-Delay Product (watt*sec10^{-18})	
			45 nm	180 nm	45 nm	180 nm	45 nm	180 nm
LOC DESIGNS								
2-2	Static-CMOS	14	**1.815**	**0.531**	0.268	52.690	**0.486**	**027.978**
	HYB-TG	26	4.819	0.947	**0.209**	**47.575**	2.866	045.053
3-2	Static-CMOS	28	**2.608**	**1.550**	1.362	71.655	**3.552**	**111.065**
	HYB-TG	42	8.438	5.262	**0.902**	**62.575**	7.611	329.200
MODIFIED HOC DESIGNS								
			Power (nW)		**Delay (ns)**		**Power-Delay Product (watt*sec10^{-15})**	
4-2	Static-CMOS	56	**14.782**	**9.770**	8.747	374.410	0.129	03.657
	HYB-TG	94	21.150	19.860	**2.953**	**154.891**	**0.624**	**03.076**
5-2	Static-CMOS	70	**28.410**	**22.420**	15.341	411.870	0.435	09.234
	HYB-TG	110	34.750	30.231	**3.435**	**257.790**	**0.119**	**07.792**
6-2	Static-CMOS	98	**38.980**	**34.740**	21.210	552.310	0.826	19.187
	HYB-TG	152	44.260	39.990	**4.358**	**326.540**	**0.192**	**13.058**
7-2	Static-CMOS	112	**47.440**	**41.040**	33.740	614.110	1.600	25.184
	HYB-TG	168	52.371	46.730	**5.633**	**412.370**	**0.295**	**19.270**

For the comparative analysis of the modified and published compressor designs under same simulation settings, we have taken the conventional architectures from referred publications and implemented them using the same technology and supply voltage.

The architecture of conventional 2-2, 3-2, 4-2, 5-2, 6-2 and 7-2 compressors and their design parameters are taken from references [8][11][32][33][34].

Table 4.3 and Table 4.4 show comparative simulation results of LOC and modified HOC compressors with designs of published references at 0.4V power supply using 45 nm / 180 nm technology.

Here only best results of LOC and modified HOC compressors obtained from Table 4.2 are compared.

Table 4.3: Comparative results of proposed modified compressor with designs of published references at 45 nm technology

References	Design style	Module name	Power (nW)	Delay (ns)	Power-Delay Product (watt*sec 10^{-18})
Ref [32]	CPL	2-2 Compressor	06.32	28.87	182.4
Ref [33]	DPL	3-2 Compressor	12.78	61.12	781.1
LOC Designs (proposed)	Static-CMOS	2-2 Compressor	**01.81**	**0.26**	**0.486**
		3-2 Compressor	**02.60**	**1.36**	**3.552**
Ref [8]	CPL and DPL	4-2 Compressor	**18.48**	27.70	511.8
Ref [8]	CPL and DPL	5-2 Compressor	**25.55**	87.21	2,228
Ref [34]	Static-CMOS	6-2 Compressor	**28.13**	184.50	5,189
Ref [33]	DPL	7-2 Compressor	**43.78**	135.90	5,949
Modified HOC Designs (proposed)	HYB-TG	4-2 Compressor	21.15	**2.95**	**62.45**
		5-2 Compressor	34.75	**3.43**	**119.36**
		6-2 Compressor	44.26	**4.35**	**192.88**
		7-2 Compressor	52.37	**5.63**	**295.00**

Table 4.4: Comparative results of proposed LOC and modified HOC compressors with designs of published references at 180 nm technology

References	Design style	Module name	Power (nW)	Delay (µs)	Power-Delay Product (watt*sec 10^{-15})
Ref [32]	CPL	2-2 Compressor	0.441	0.357	0.157
Ref [33]	DPL	3-2 Compressor	3.417	0.787	2.689
LOC Designs (proposed)	Static-CMOS	2-2 Compressor	**0.531**	**0.052**	**0.027**
		3-2 Compressor	**1.550**	**0.071**	**0.111**
Ref [8]	CPL and DPL	4-2 Compressor	**15.47**	1.474	22.802
Ref [8]	CPL and DPL	5-2 Compressor	**19.74**	2.470	48.757
Ref [34]	Static-CMOS	6-2 Compressor	**23.31**	4.311	100.48
Ref [33]	DPL	7-2 Compressor	**40.88**	3.235	132.24
Modified HOC Designs (proposed)	HYB-TG	4-2 Compressor	19.86	**0.154**	**03.076**
		5-2 Compressor	30.23	**0.257**	**07.792**
		6-2 Compressor	39.99	**0.326**	**13.058**
		7-2 Compressor	46.73	**0.412**	**19.270**

The overall propagation delay and power-delay product results of the all LOC and modified HOC cells are less in comparison to existing published results of conventional compressor cells. However, modified HOC's have 23.9% (29.2%) in average higher power consumption at 45 nm (180 nm) technology.

Key Points: The results of the modified Compressor designs show that

- For LOC designs, Static-CMOS logic design style provides lesser power-delay product at both technologies in sub-threshold region.
- For Modified HOC designs, HYB-TG logic design style provides lesser power-delay product at both technologies in sub-threshold region
- At 45 nm, for all designs of LOC and modified HOC designs, the propagation delay is smaller, power consumption is higher and power-delay product is smaller in comparison to 180 nm technology.
- The overall power-delay product of the LOC and modified HOC designs is lesser than designs of published references at 0.4V supply voltage at both technologies.

Outcome: Based on above results, Static-CMOS logic family is used for the final implementation of multipliers using LOC's. Similarly, HYB-TG logic family is used for the final implementation of multipliers using modified HOC's.

4.6. DESIGN AND ANALYSIS OF WALLACE TREE AND DADDA MULTIPLIERS

In this section, design and analysis of multipliers using two architectures (Wallace tree and Dadda) in two different partial product accumulation schemes is given. These schemes are given below:

- Using LOC
- Using Mixed L/H

An example of operation of 8×8 multiplier shown in Figure 4.20 is used to explain the partial product accumulation schemes using Wallace tree and Dadda compression tree.

Here, X0, X1, X2….X7 are multiplicand bits; Y0, Y1, Y2…...Y7 are multiplier bits. PXY is the partial-product of X, Y, Prn is the final n^{th} product of the multiplier.

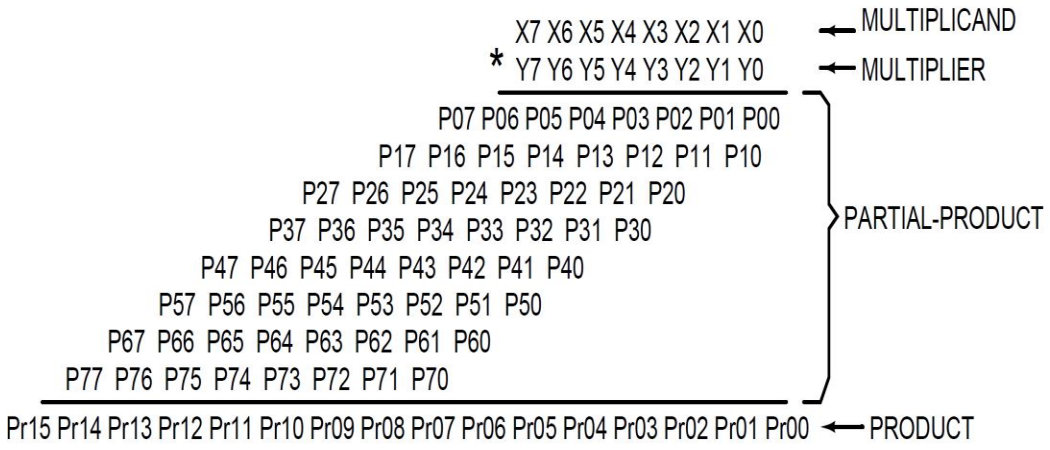


Figure 4.20: Multiplication of 8x8-bit multiplier

The internal architecture of 8x8-bit multipliers using Wallace tree and Dadda and their circuit implementations are given below.

4.6.1. Design Implementation of Wallace tree multiplier

In Wallace tree's scheme, the partial products are reduced as soon as possible. The internal architecture of Wallace tree using LOC and Mixed L/H are shown in Figure 4.21 and Figure 4.22 respectively. The circuit level diagrams of blocks for partial-product generation, partial-product accumulation and final adder addition are given in section 4.3, 4.5 and 4.4 respectively.

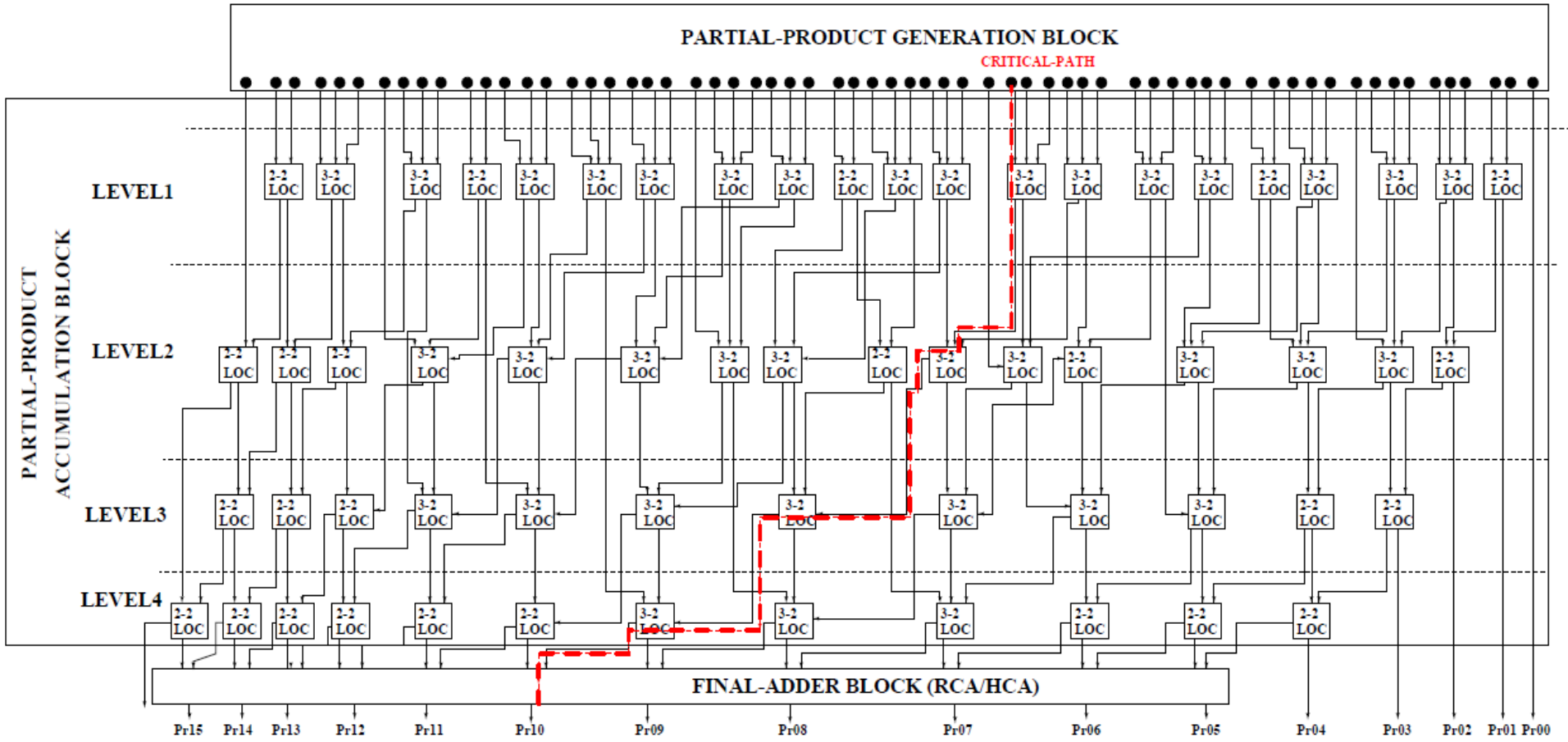


Figure 4.21: Block diagram of Wallace tree using LOC

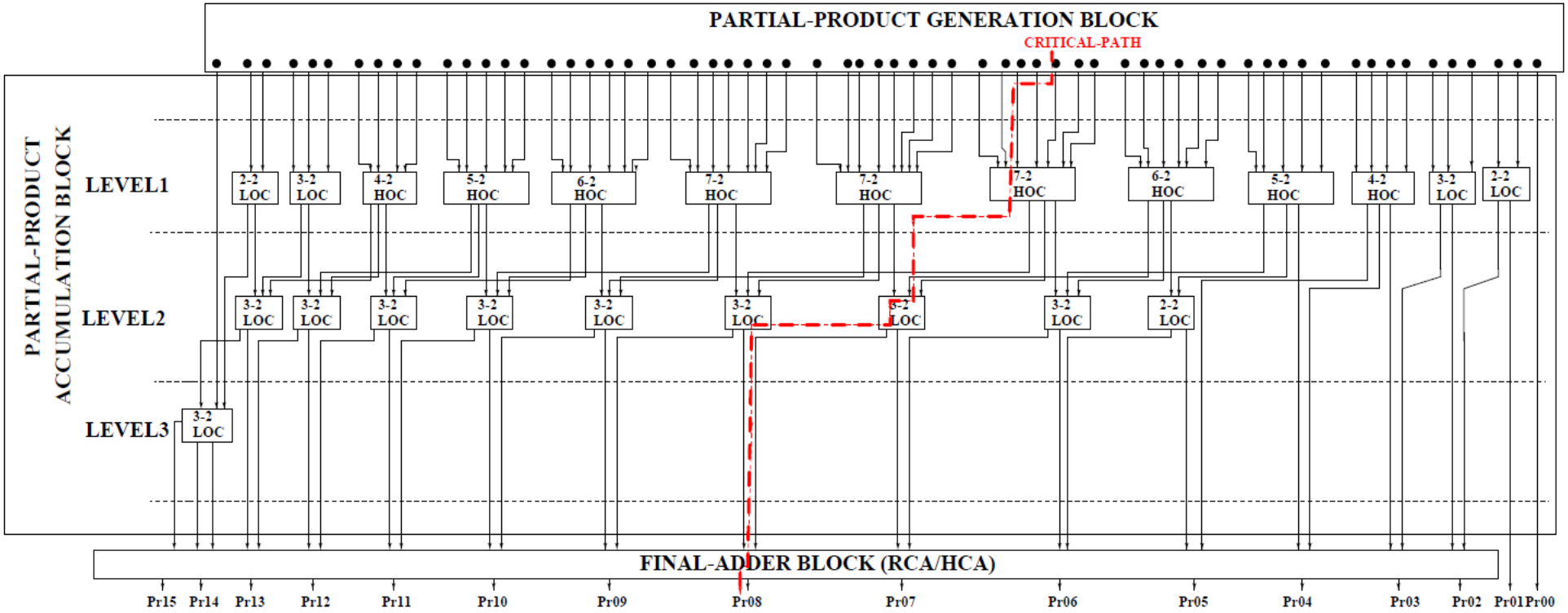


Figure 4.22: Block diagram of Wallace tree using Mixed L/H

4.6.2. Simulation Methodology and Results of Wallace tree Multipliers

To obtain the simulation results for the Wallace tree multipliers in sub-threshold region, the following methodology is followed:

The 4×4-bit and 8×8-bit Wallace tree multiplier using LOC and Mixed L/H cells are designed in Cadence Virtuoso (Schematic and Layout). Two different technology nodes i.e. 45 nm / 180 nm technologies have been considered in implementation and simulated using the BSIM3 (V3.24) model, at a supply voltage of 0.4 V. For both technology nodes, transient simulations have been done by applying input pulses having rise and fall times of 1 pico-second, pulse width (ON time) of 1 micro-second and pulse period of 5 micro-second and power, delay and power-delay product values are evaluated. Total eight designs of Wallace tree multipliers are implemented using different combinations of partial accumulation modules (LOC, Mixed L/H) and final stage adders (RCA, HCA) at two different technology nodes (45 nm, 180 nm).

In this thesis, the following nomenclature as shown in Table 4.5, is used to represent the proposed designs of multiplier:

Architecture (**Wallace tree**) - technology (**45/ 180**) - compressor LOC (**L**) / Mixed L/H (**L/H**)- final adder (**RCA/ HCA**)

Table 4.5: Nomenclature used for the proposed designs of Wallace tree multiplier

S. No.	Multiplier Design Descriptions	Nomenclature
1	Wallace tree multiplier at 45 nm using LOC based accumulation scheme with final addition through RCA	Wallace tree-45-L-RCA.
2	Wallace tree multiplier at 45 nm using LOC based accumulation scheme with final addition through HCA	Wallace tree-45-L-HCA
3	Wallace tree multiplier at 45 nm using Mixed L/H based accumulation scheme with final addition through RCA	Wallace tree-45-L/H-RCA.
4	Wallace tree multiplier at 45 nm using Mixed L/H based accumulation scheme with final addition through HCA	Wallace tree-45-L/H-HCA.
5	Wallace tree multiplier at 180 nm using LOC based accumulation scheme with final addition through RCA	Wallace tree-180-L-RCA.
6	Wallace tree multiplier at 180 nm using LOC based accumulation scheme with final addition through HCA	Wallace tree-180-L-HCA.
7	Wallace tree multiplier at 180 nm using Mixed L/H based accumulation scheme with final addition through RCA	Wallace tree-180-L/H-RCA.
8	Wallace tree multiplier at 180 nm using Mixed L/H based accumulation scheme with final addition through HCA	Wallace tree-180-L/H-HCA.

Table 4.6 and Table 4.7 show power, delay and power-delay product of Wallace tree multipliers using 45 nm / 180 nm technology.

Table 4.6: Simulation results of Wallace tree multipliers using 45 nm technology at V_{DD}=0.4V

Module Name	Size (in bits)	Power (µW)	Delay (ns)	Power-Delay Product (watt*sec10^{-15})	Area (µm^2)
Wallace tree-45-L-RCA	4x4	**0.397**	13.410	05.323	**0167.2**
	8x8	**0.613**	34.250	20.990	**0638.3**
Wallace tree-45-L-HCA	4x4	0.412	10.470	04.313	0314.7
	8x8	0.631	30.450	19.210	0807.1
Wallace tree-45-L/H-RCA	4x4	0.472	05.171	02.441	0255.9
	8x8	3.131	06.041	18.910	0957.4
Wallace tree-45-L/H-HCA	4x4	0.478	**04.821**	**02.304**	0411.3
	8x8	3.457	**05.011**	**17.320**	1072.4

Table 4.7: Simulation results of Wallace tree multipliers uisng 180 nm technology at V_{DD}=0.4V

Module Name	Size (in bits)	Power (µW)	Delay (ns)	Power-Delay Product (watt*sec10^{-15})	Area (µm^2)
Wallace tree-180-L-RCA	4x4	**0.071**	778.70	055.280	**0334.7**
	8x8	**0.115**	997.10	114.660	**1174.7**
Wallace tree-180-L-HCA	4x4	0.073	721.50	052.660	0674.4
	8x8	0.123	811.50	099.810	1551.1
Wallace tree-180-L/H-RCA	4x4	0.131	295.70	038.736	0497.2
	8x8	0.244	390.40	095.257	1874.4
Wallace tree-180-L/H-HCA	4x4	0.150	**245.10**	**036.765**	0788.8
	8x8	0.289	**311.23**	**089.945**	2041.7

Key Points: The results of the Wallace tree multiplier show that

- Wallace tree multiplier operates down to 0.4V power supply for selected logic design styles at both technology nodes in sub-threshold region.
- The simulation results show that power, delay and power-delay product of the Wallace tree multipliers increases with the increase in operand size as expected.
- The Wallace tree multiplier using Mixed L/H based accumulation scheme exhibits the least power-delay product at both technologies.
- Wallace tree multiplier with HCA gives less delay and power-delay product as compared to Wallace tree multiplier with RCA.
- In comparison to 180 nm technology, for 45 nm, the propagation delay is smaller, power consumption is higher (due to increased leakage currents) and power-delay product is smaller for all designs of Wallace tree multiplier.

The overall power consumption, propagation delay and power-delay product graphs of Wallace tree multipliers at 45 nm / 180 nm technology using different accumulation scheme is shown in Figure 4.23.

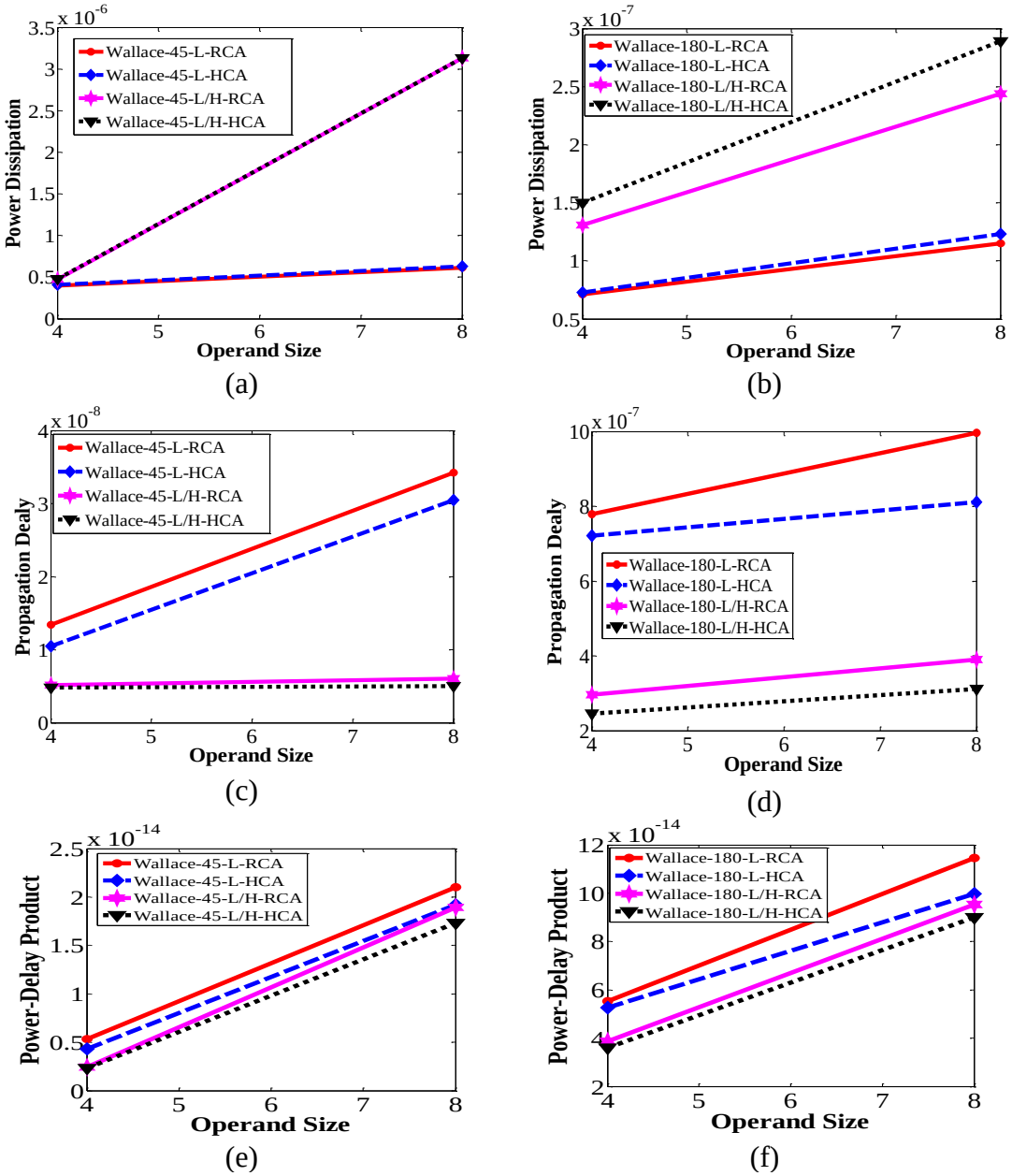


Figure 4.23: The overall power consumption, propagation delay and power-delay product graphs of Wallace tree multipliers at 45 nm / 180 nm technology

4.6.3. Design Implementation of Dadda Multiplier

In Dadda's method, at each level the partial products does minimum necessary reduction. The internal architecture of Dadda using LOC and Mixed L/H are shown in Figure 4.24 and Figure 4.25 respectively. The circuit level diagrams of all these blocks (partial-product generation, partial-product accumulation, and final adder addition) are given in section 4.3, 4.5 and 4.4 respectively.

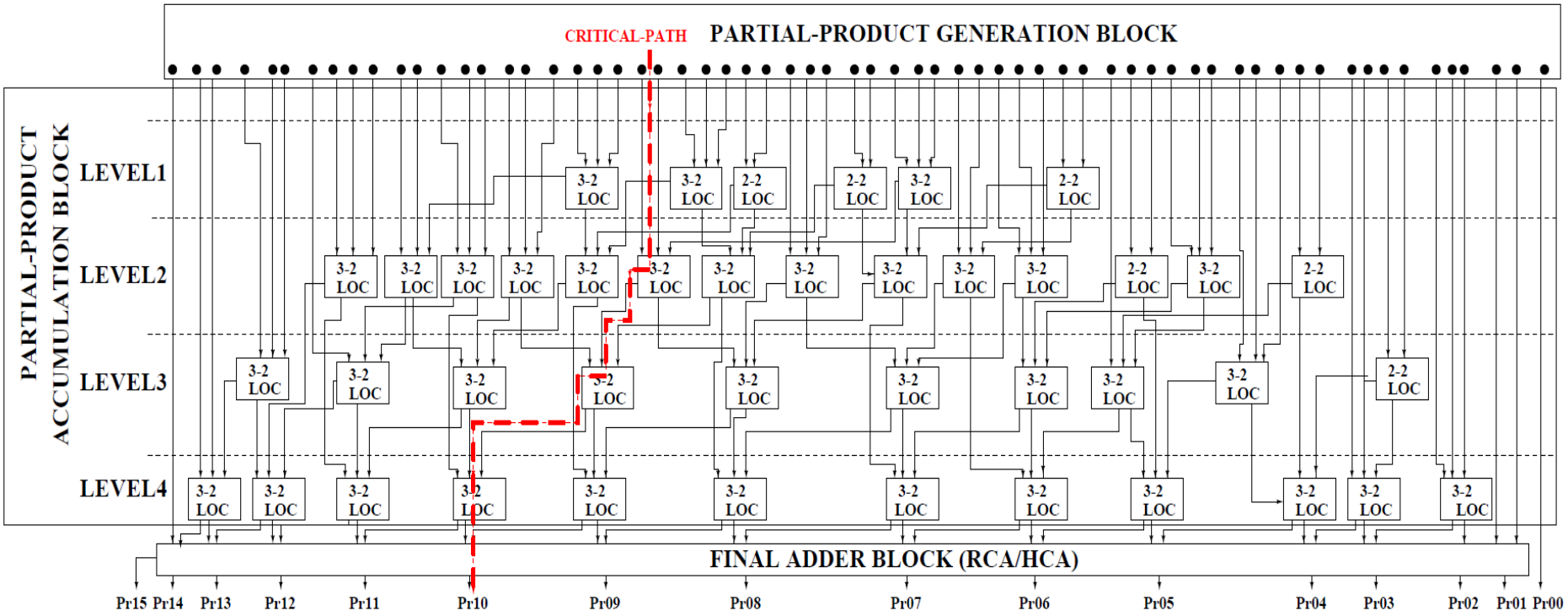


Figure 4.24: Block diagram of Dadda multiplier using LOC

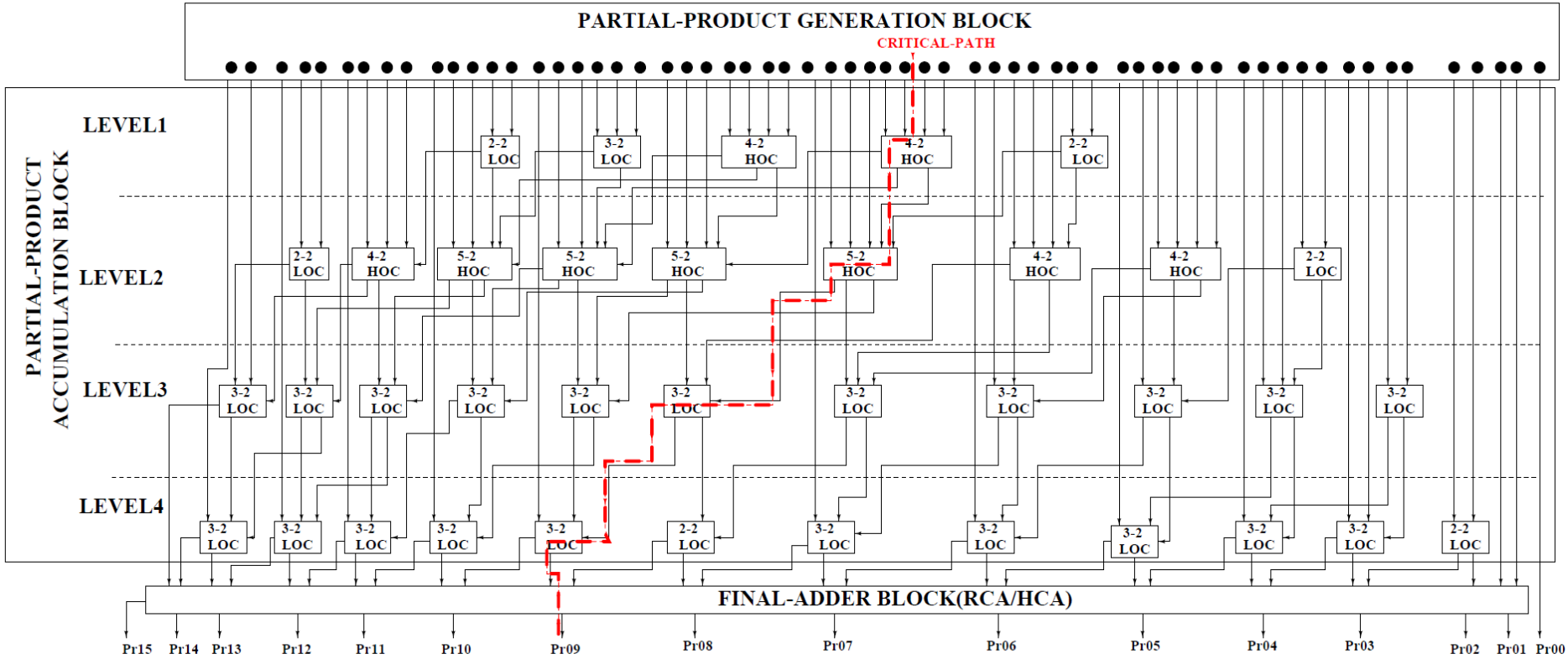


Figure 4.25: Block diagram of Dadda multiplier using Mixed L/H

4.6.4. Simulation Methodology and Results of Dadda Multipliers

The methodology followed for simulation of Dadda multipliers in sub-threshold region is same as given in Section 4.6.2.

Total eight designs of Dadda multipliers are implemented using different combinations of partial accumulation modules (LOC, Mixed L/H) and final stage adders (RCA, HCA) at two different technology nodes (45 nm, 180 nm).

In this thesis, the following nomenclature as shown in Table 4.8, is used to represent the designs of multiplier:

Architecture (**Dadda tree**) - technology (**45/ 180**) - compressor LOC (**L**) / Mixed L/H (**L/H**)- final adder (**RCA/ HCA**).

Table 4.8: Nomenclature used for the proposed designs of Dadda multiplier

S. No.	Multiplier Design Descriptions	Nomenclature
1	Dadda multiplier at 45 nm using LOC based accumulation scheme with final addition through RCA	Dadda-45-L-RCA.
2	Dadda multiplier at 45 nm using LOC based accumulation scheme with final addition through HCA	Dadda-45-L-HCA
3	Dadda multiplier at 45 nm using Mixed L/H based accumulation scheme with final addition through RCA	Dadda-45-L/H-RCA.
4	Dadda multiplier at 45 nm using Mixed L/H based accumulation scheme with final addition through HCA	Dadda-45-L/H-HCA.
5	Dadda multiplier at 180 nm using LOC based accumulation scheme with final addition through RCA	Dadda-180-L-RCA.
6	Dadda multiplier at 180 nm using LOC based accumulation scheme with final addition through HCA	Dadda-180-L-HCA.
7	Dadda multiplier at 180 nm using Mixed L/H based accumulation scheme with final addition through RCA	Dadda-180-L/H-RCA.
8	Dadda multiplier at 180 nm using Mixed L/H based accumulation scheme with final addition through HCA	Dadda-180-L/H-HCA.

Table 4.9 and Table 4.10 show power, delay and power-delay product of proposed Dadda multipliers using 45 nm / 180 nm technology.

Table 4.9: Simulation results of Dadda multipliers using 45 nm technology at V_{DD}=0.4V

Module Name	Size (in bits)	Power (µW)	Delay (ns)	Power-Delay Product (watt*sec10^{-15})	Area (µm^2)
Dadda-45-L-RCA	4x4	**0.274**	10.73	02.940	**122.7**
	8x8	**0.465**	30.63	14.240	**588.5**
Dadda-45-L-HCA	4x4	0.294	07.44	02.187	224.9
	8x8	0.484	28.22	13.650	704.8
Dadda-45-L/H-RCA	4x4	0.303	04.14	01.254	187.6
	8x8	2.457	05.01	12.280	880.4
Dadda-45-L/H-HCA	4x4	0.310	**03.79**	**01.175**	369.9
	8x8	2.939	**04.03**	**11.850**	988.1

Table 4.10: Simulation results of Dadda multipliers using 180 nm technology at V_{DD}=0.4V

Module Name	Size (in bits)	Power (µW)	Delay (ns)	Power-Delay Product (watt*sec10^{-15})	Area (µm^2)
Dadda-180-L-RCA	4x4	**0.065**	771.4	050.140	**0287.4**
	8x8	**0.113**	989.1	111.760	**1078.6**
Dadda-180-L-HCA	4x4	0.070	705.3	049.370	0578.2
	8x8	0.121	802.7	097.120	1478.3
Dadda-180-L/H-RCA	4x4	0.114	289.2	032.960	0411.4
	8x8	0.234	384.1	089.870	1774.2
Dadda-180-L/H-HCA	4x4	0.131	**222.8**	**029.186**	0668.4
	8x8	0.284	**307.7**	**087.386**	1878.4

Key Points: The results of the Dadda multipliers show that

- Dadda multipliers operate down to 0.4V power supply for selected logic design styles at both technology nodes in sub-threshold region.
- The simulation results show that power, delay and power-delay product of the Dadda multipliers increases with the increase in operand size as expected.
- The Dadda multiplier using Mixed L/H based accumulation scheme exhibits the least power-delay product at both technologies.
- Dadda multiplier with HCA gives less delay and power-delay product as compared to Dadda multiplier with RCA.
- At 45 nm, the propagation delay is smaller, power consumption is higher (due to increased leakage current) and power-delay product is smaller for all designs of Dadda multiplier in comparison to 180 nm technology.

The power consumption, propagation delay and power-delay product graphs of Dadda multipliers at 45 nm / 180 nm technology using different accumulation scheme is shown in Figure 4.26.

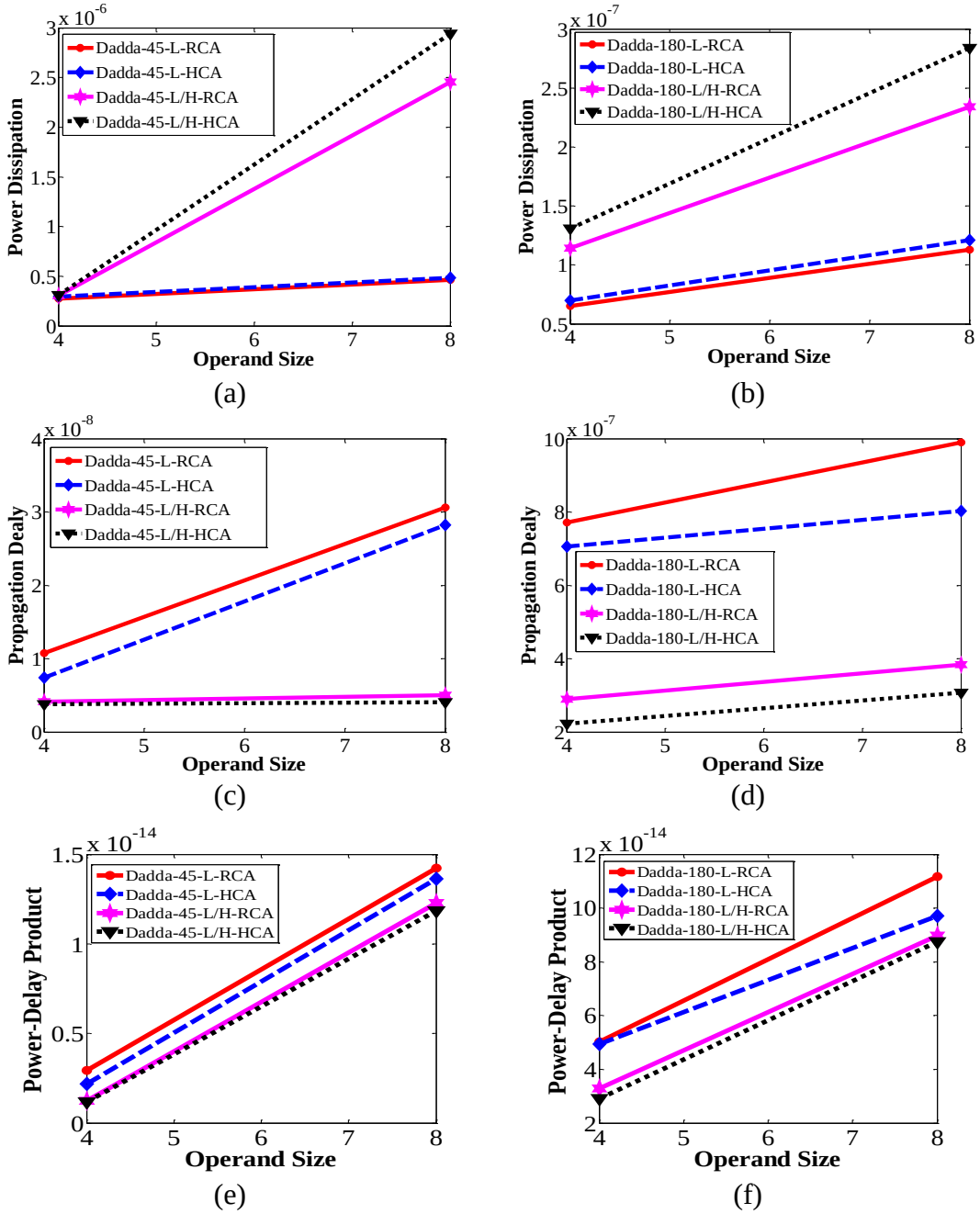


Figure 4.26: The overall power consumption, propagation delay and power-delay product graphs of Dadda multipliers at 45 nm / 180 nm technology

4.7. FINAL RESULTS AND DISCUSSION

Comparison of proposed Wallace tree and Dadda multiplier designs with results of published architectures

This section presents the comparative analysis of 4×4-bit and 8×8-bit of Wallace tree and Dadda multipliers with referenced architectures operated in sub-threshold region at 45nm / 180 nm technology for 0.4V supply voltage at same frequency of operation (200 KHz).

Here, for comparison, the 4x4-bit and 8x8-bit Wallace tree and Dadda multipliers of the referenced architectures [17][18][35][36] are designed to obtain their results in the same simulation setup for sub-threshold operation.

Whereas, all proposed designs show minimum power-delay product as compared to referenced architectures at both technology nodes, but Table 4.11 and 4.12 show comparisons with only best–proposed multiplier designs *i.e* with minimum power-delay product, (as per results obtained from Table 4.6, 4.7, 4.9 and 4.10) with the referenced architectures in sub-threshold region.

Table 4.11: Comparative results between proposed and referenced multiplier designs at 45 nm

Referenced/ Proposed designs	Module name	Size (in bits)	Power (µW)	Delay (ns)	Power-Delay Product (Watt*Sec 10^{-15})	% reduction in Power-Delay Product
Ref [35]	Wallace tree	4x4	0.723	25.910	018.732	(4x4 size) -87.7% (8x8 size) - 90.2%
		8x8	**2.423**	73.010	176.903	
Wallace tree-45-L/H-HCA (best)	Wallace tree	4x4	**0.478**	**04.821**	**002.304**	
		8x8	3.457	**05.011**	**017.323**	
Ref [36]	Dadda	4x4	0.562	10.721	006.023	(4x4 size) - 80.5% (8x8 size) -79.9%
		8x8	**1.901**	31.110	059.140	
Dadda-45-L/H-HCA (best)	Dadda	4x4	**0.310**	**03.791**	**001.175**	
		8x8	2.939	**04.033**	**011.852**	

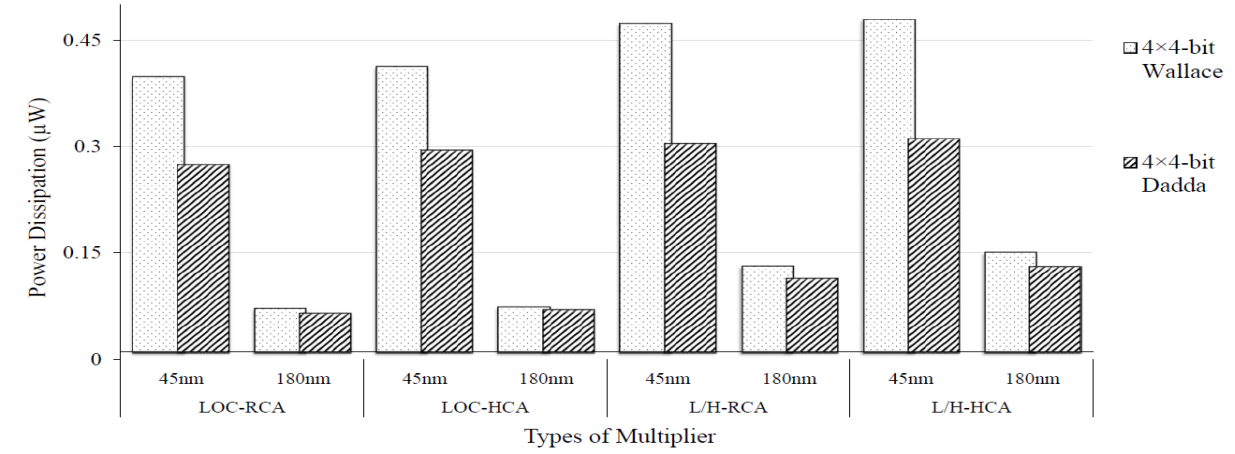
Table 4.12: Comparative table between proposed and referenced multiplier designs at 180 nm

Referenced/ Proposed designs	Module name	Size (in bits)	Power (µW)	Delay (µs)	Power-Delay Product (Watt*Sec 10^{-12})	% reduction in Power-Delay Product
Ref [17]	Wallace tree	4x4	0.194	1.857	0.3602	(4x4 size) - 89.8% (8x8 size) - 87.6%
		8x8	**0.282**	2.586	0.7292	
Wallace tree-180-L/H-HCA (best)	Wallace tree	4x4	**0.150**	**0.245**	**0.0367**	
		8x8	0.289	**0.311**	**0.0899**	
Ref [18]	Dadda	4x4	0.187	0.849	0.1587	(4x4 size) - 81.7% (8x8 size) -82.1%
		8x8	**0.274**	1.784	0.4888	
Dadda-180-L/H-HCA (best)	Dadda	4x4	**0.131**	**0.222**	**0.0291**	
		8x8	0.284	**0.307**	**0.0873**	

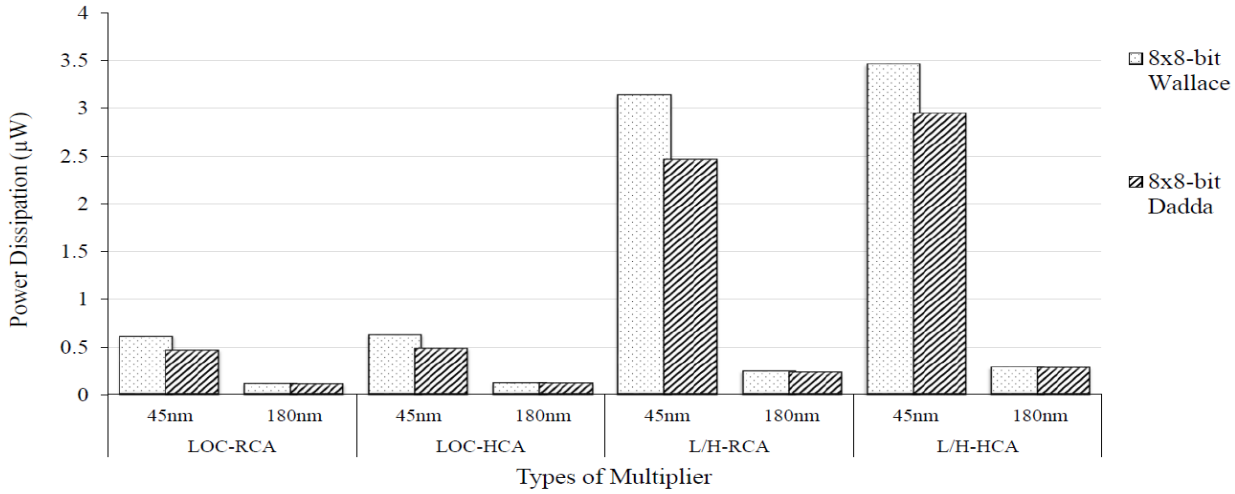
Comparison of results of proposed Wallace and Dadda multiplier designs among themselves

All proposed designs show minimum power-delay product as compared to published referenced architectures. Thus, a comparison of these designs, among themselves, is done to obtain the best design in terms of overall power-delay product at both technologies.

For comparison purpose, Figure 4.27, Figure 4.28 and Figure 4.29 show the power consumption, propagation delay and power-delay product histograms of all proposed sixteen designs.

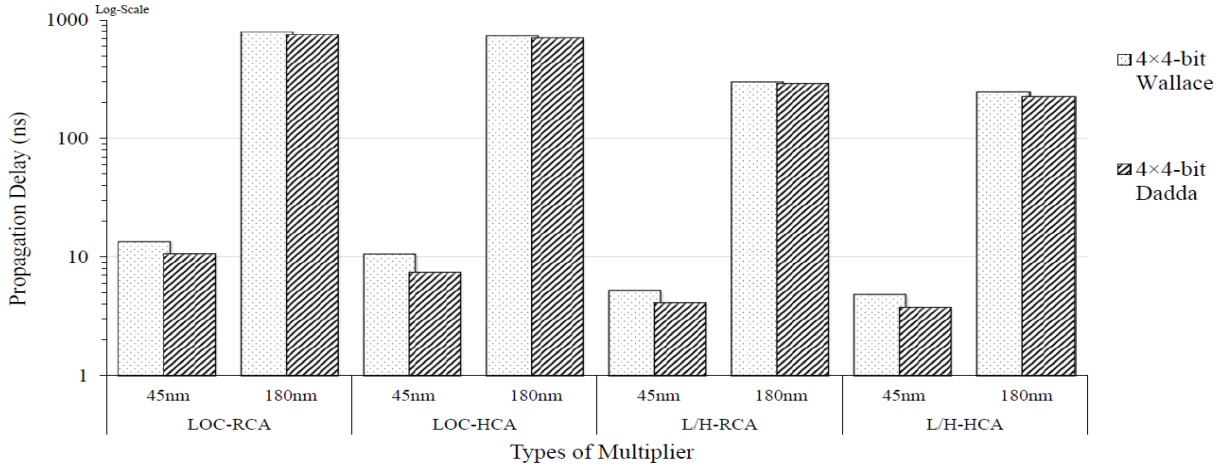


(a)

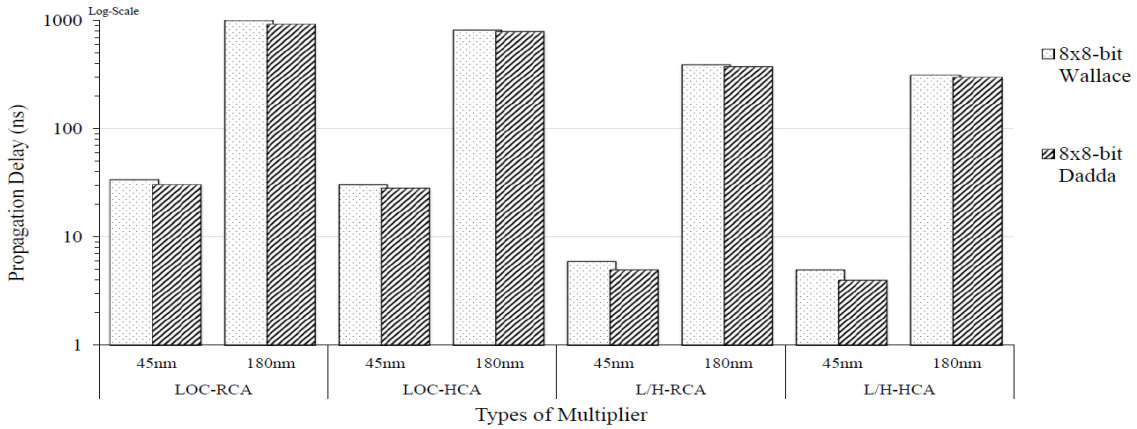


(b)

Figure 4.27: The comparative power consumption graph between Wallace tree and Dadda multipliers for (a) 4x4-bit (b) 8x8-bit

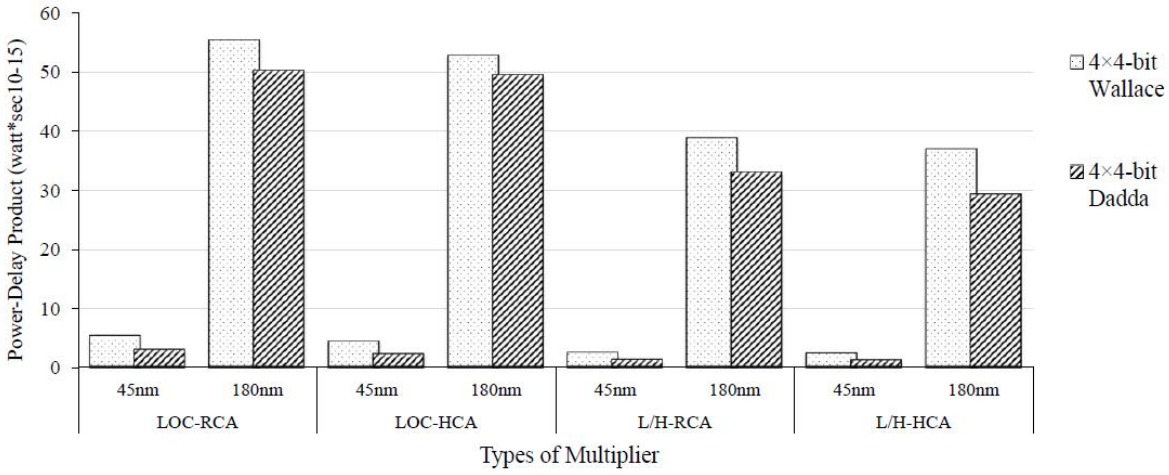


(a)

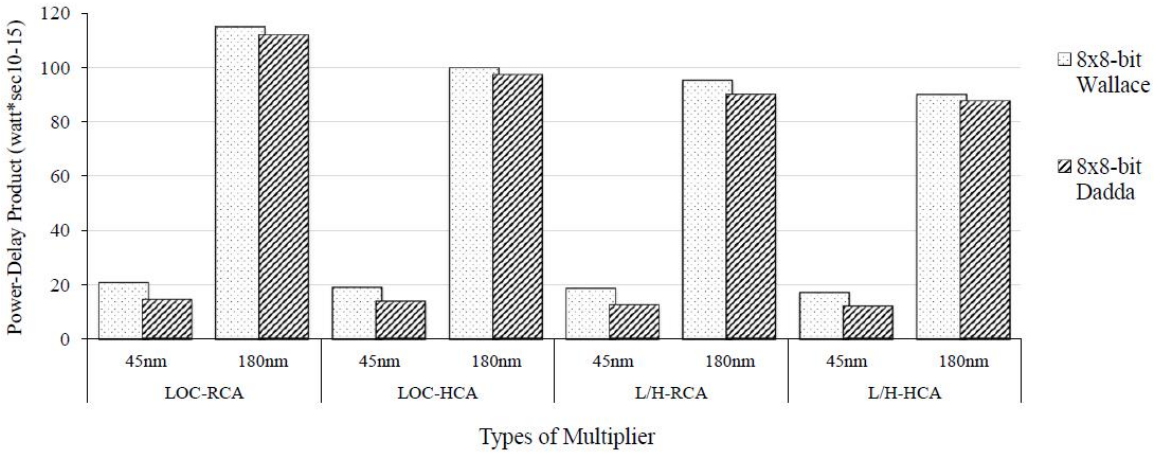


(b)

Figure 4.28: The comparative propagation delay graph between Wallace tree and Dadda multipliers for (a) 4x4-bit (b) 8x8-bit



(a)



(b)

Figure 4.29: The comparative power-delay product graph between Wallace tree and Dadda multipliers for (a) 4x4-bit (b) 8x8-bit

Observations

The comparative results of the Wallace tree and Dadda multiplier show that in sub-threshold region:

- In selected logic design styles (Static-CMOS and HYB-TG), both multiplier architectures operate down to 0.4V with correct functionality using all four different combinations of partial-product accumulation scheme and final adder (LOC-RCA, LOC-HCA, L/H-RCA and L/H-HCA).
- The power, delay and power-delay product of both the multiplier designs increase with the increase in operand size.

(i) Effect of Logic Design Style:

- Static-CMOS logic gives lowest power consumption because of simpler logic cells using LOC based accumulation scheme at both technology nodes.
- HYB-TG logic gives lowest propagation delay because of shorter critical paths using Mixed L/H based accumulation scheme at both technology nodes.

(ii) Effect of Technology Scaling:

- At same frequency of operation, at 45 nm, the propagation delay is smaller, power consumption is higher (due to increased leakage current as supply voltage is kept same at 0.4V) and power-delay product is smaller for all different implemented combinations of multipliers in comparison to 180 nm technology.

(iii) Effect of Multiplier Architecture:

- Dadda multiplier is the most power efficient, high performance architecture for all different implemented combinations as compared to Wallace tree multiplier at both technology nodes.
- Both the multipliers with Mixed L/H based partial-product accumulation scheme shows reduced power-delay product as compared to LOC based partial-product accumulation scheme.

  In both technologies, multipliers with HCA provide lower propagation delay and lesser power-delay product but higher power consumption because of its complex architecture as compared to multipliers with RCA.

4.8. CONCLUSIONS

The overall results of the Wallace tree and Dadda multipliers show following conclusions at 45 nm / 180 nm technology nodes:

(i) Power Consumption

Comparison of proposed multipliers with referenced designs [35][36] at 45 nm, [17][18] at 180 nm

- For LOC based proposed Wallace tree and Dadda multipliers:

At 45 nm: For 4x4-bit and 8x8-bit, the proposed designs give lesser power consumption with respect to referenced designs. The range of reduction in power consumption varies from 43.1% to 74.5%.

At 180 nm: For 4x4-bit and 8x8-bit, the proposed designs give lesser power consumption with respect to referenced designs. The range of reduction in power consumption varies from 55.8% to 62.5%.

- Mixed L/H based proposed Wallace tree and Dadda multipliers:

At 45 nm: For 4x4-bit, the proposed designs give lesser power consumption, varying from 33.8% to 44.8%. Whereas for 8x8-bit, the proposed designs give more power consumption, varying from 42.6% to 54.6% with respect to referenced designs.

At 180 nm: For 4x4-bit, the proposed designs have lesser power consumption, varying from 63.3% to 74.1%. Whereas for 8x8-bit, the proposed designs give more power consumption, varying from 2.4% to 3.5% with respect to referenced designs.

Comparison of all proposed Wallace tree and Dadda multiplier designs among themselves

- For LOC based architectures:

For both technology nodes, **Dadda multiplier (based designs)** has the least power consumption in comparison to corresponding Wallace tree multiplier as given below:

At 45 nm: For 4x4-bit, the lesser power consumption varying from 28.6% to 30.9%. Whereas, for 8x8-bit, they consume lesser power consumption, varying from 23.2% to 24.1%.

At 180 nm: For 4x4-bit, they consume lesser power consumption varying from 4.1% to 8.4%. Whereas, for 8x8-bit, they consume lesser power consumption, varying from 1.6% to 1.7%

- For Mixed L/H based architectures:

For both technology nodes, **Dadda multiplier (based designs)** has the least power consumption as compared to corresponding Wallace tree multiplier based designs as given below:

At 45 nm: For 4x4-bit, they have lesser power consumption varying from 35.1% to 35.8%. Whereas, for 8x8-bit, they consume lesser power consumption, varying from 14.9% to 21.5% as compared to Wallace tree multipliers.

At 180 nm: For 4x4-bit, they consume lesser power consumption varying from 12.6% to 12.9%. Whereas, for 8x8-bit, they consume lesser power consumption, varying from 1.7% to 4.1%.

- At 45 nm, for both sizes (4x4-bit and 8x8-bit), among all eight (LOC as well Mixed L/H based) proposed multipliers implemented, **Dadda-45-L-RCA** is the most power efficient architecture.

  It consumes 42.6% (for 4x4-bit), and 86.5 % (for 8x8-bit) less power in comparison to highest power consuming design which is Wallace tree-45-L/H-HCA.

- At 180 nm, for both sizes, **Dadda-180-L-RCA** is the most power efficient architecture among all eight proposed designs.

  It has 56.6% (for 4x4-bit) and 60.8% (for 8x8-bit) less power consumption less power in comparison to highest power consuming design which is Wallace tree-180-L/H-HCA.

(ii) Propagation Delay

Comparison of proposed multipliers with referenced designs [17][18][35][36]

- For LOC based proposed Wallace tree and Dadda multipliers:

At 45 nm: For 4x4-bit and 8x8-bit, the proposed designs give a lesser propagation delay varying from 9.28% to 59.5 %.

At 180 nm: For 4x4-bit and 8x8-bit, the proposed designs give a lesser propagation delay varying from 16.9% to 68.6 %.

- Mixed L/H based proposed Wallace tree and Dadda multipliers:

At 45 nm: For 4x4-bit and 8x8-bit, the proposed designs give a lesser propagation delay varying from 64.6% to 87.1%.

At 180 nm: For 4x4-bit and 8x8-bit, the proposed designs give a lesser propagation delay varying from 73.7% to 87.9 %.

Comparison of all proposed Wallace tree and Dadda multipliers among themselves

- For LOC based architectures:

Dadda multiplier (based designs) has the least propagation delay at both technology nodes in comparison to corresponding Wallace tree multiplier designs as given below:

At 45 nm: For 4x4-bit, **Dadda multipliers** give lesser propagation delay varying from 19.9% to 28.9%. Whereas for 8x8-bit, they give lesser propagation delay varying from 7.3% to 10.5% as compared to Wallace tree multipliers.

At 180 nm: For 4x4-bit, **Dadda multipliers** give lesser propagation delay varying from 0.9% to 2.2%. Whereas for 8x8-bit, they give lesser propagation delay varying from 0.8% to 1.1% as compared to Wallace tree multipliers.

- For Mixed L/H based architectures:

Dadda multiplier (based designs) have the least propagation delay at both technology nodes in comparison to corresponding Wallace tree multiplier designs as given below.

At 45 nm: For 4x4-bit, Dadda multipliers give lesser propagation delay varying from 19.9 % to 21.3%. Whereas, for 8x8-bit, they give lesser propagation delay varying from 17.2% to 19.5% as compared to Wallace tree multipliers.

At 180 nm: For 4x4-bit, the Dadda multipliers give lesser propagation delay varying from 2.1% to 9.1%. Whereas, for 8x8-bit, they give lesser propagation delay varying from 1.1% to 1.6% as compared to Wallace tree multipliers.

- Among all eight (LOC as well Mixed L/H based) proposed multipliers implemented at 45 nm, **Dadda-45-L/H-HCA** has the least propagation delay. It has 71.7% (for 4x4-bit), and 88.2% (for 8x8-bit) lesser propagation delay in comparison to most delay intensive design which is Wallace tree-45-L/H-HCA.
- Similarly, at 180 nm, **Dadda-180-L/H-HCA** has the least propagation delay. It has 71.3% (for 4x4-bit) and 69.1% (for 8x8-bit) less propagation delay in comparison to most delay intensive design which is Wallace tree-180-L/H-HCA.

(iii) Power-Delay Product

Comparison of proposed multipliers with referenced designs [17][18][35][36]

- LOC based proposed Wallace tree and Dadda multipliers:

At 45 nm: For 4x4-bit and 8x8-bit, the proposed designs give lesser power-delay product varying from 63.6% to 89.1%.
At 180 nm: For 4x4-bit and 8x8-bit, the proposed designs give lesser power-delay product varying from 68.8% to 86.3 %.

- Mixed L/H based proposed Wallace tree and Dadda multipliers:

At 45 nm: For 4x4-bit and 8x8-bit, the proposed designs give lesser power-delay product varying from 70.4% to 90.2%.
At 180 nm: For 4x4-bit and 8x8-bit, the proposed designs give lesser power-delay product varying from 81.6% to 89.7 %.

Comparison of proposed Wallace tree and Dadda multipliers among themselves

- For LOC based architectures:

At 45 nm: For 4x4-bit, the **Dadda multipliers** give lesser power-delay product varying from 44.7% to 49.2%. Whereas, for 8x8-bit, they give lesser power-delay product varying from 28.9% to 32.1% as compared to corresponding Wallace tree multipliers.
At 180 nm: For 4x4-bit, the **Dadda multipliers** give lesser power-delay product varying from 6.2% to 9.2%. Whereas, for 8x8-bit, they give lesser power-delay product varying from 2.5% to 2.6% as compared to corresponding Wallace tree multipliers.

- For Mixed L/H based architectures:

At 45 nm: For 4x4-bit, the Dadda multipliers give lesser power-delay product varying from 48.6 % to 49%. Whereas, for 8x8-bit, they give lesser power-delay product varying from a 31.5% to 35.1% as compared to corresponding Wallace tree multipliers.

At 180 nm: For 4x4-bit, the Dadda multipliers give lesser power-delay product varying from 14.9% to 20.6%. Whereas, for 8x8-bit, they give lesser power-delay product varying from a 2.8% to 5.6% as compared to corresponding Wallace tree multipliers.

- Among all eight (LOC as well Mixed L/H based) proposed multipliers implemented at 45 nm, **Dadda-45-L/H-HCA** has the least power-delay product. It has 49% (for 4x4-bit), and 31.5% (for 8x8-bit) lesser power-delay product in comparison to Wallace tree-45-L/H-HCA having highest power-delay product.
- Similarly, at 180 nm, **Dadda-180-L/H-HCA** has the least power-delay product. It has 20.6% (for 4x4-bit), and 2.5% (for 8x8-bit) lesser power-delay product in comparison to Wallace tree-180-L/H-HCA having highest power-delay product.
- Static-CMOS logic and HYB-TG design style are most power-delay product efficient design style for LOC and Mixed L/H based Wallace tree and Dadda multipliers respectively.

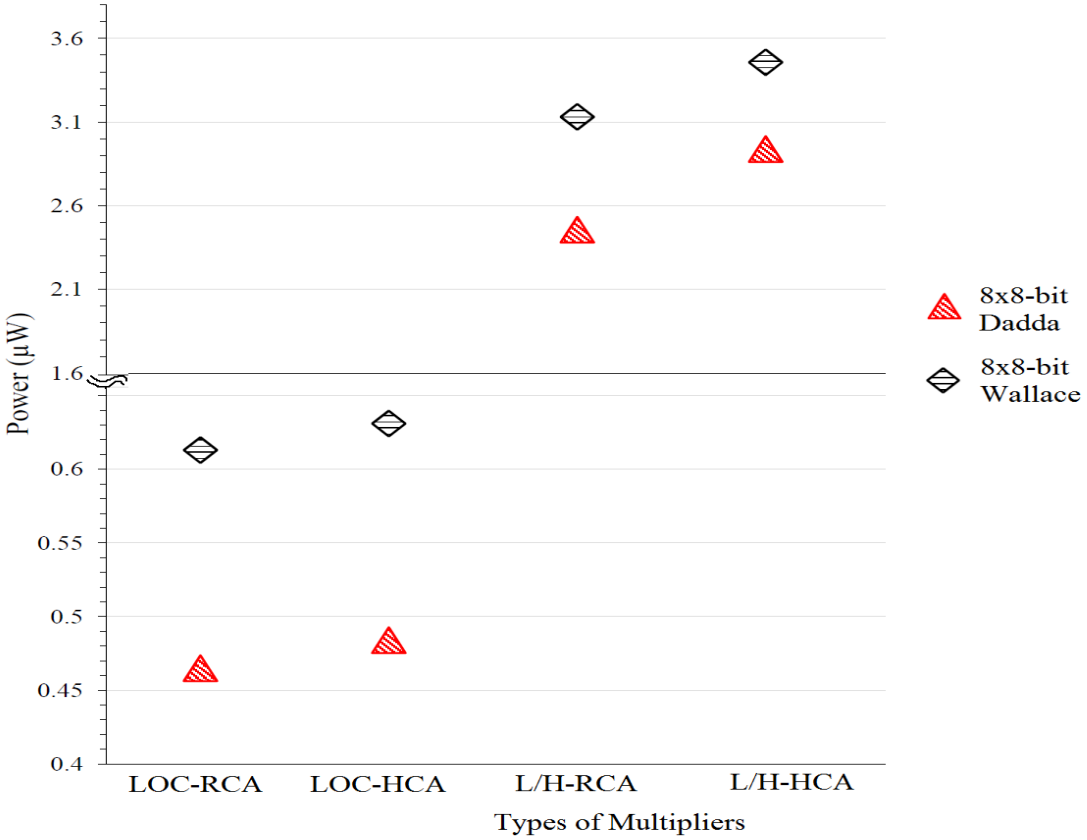
(iv) Effect of Technology Scaling

At same frequency of operation, at 45 nm, the propagation delay is smaller, power consumption is higher (due to increased leakage current since supply voltage is kept same at 0.4V) and power-delay product is smaller for all different implemented combinations of multipliers in comparison to 180 nm technology.

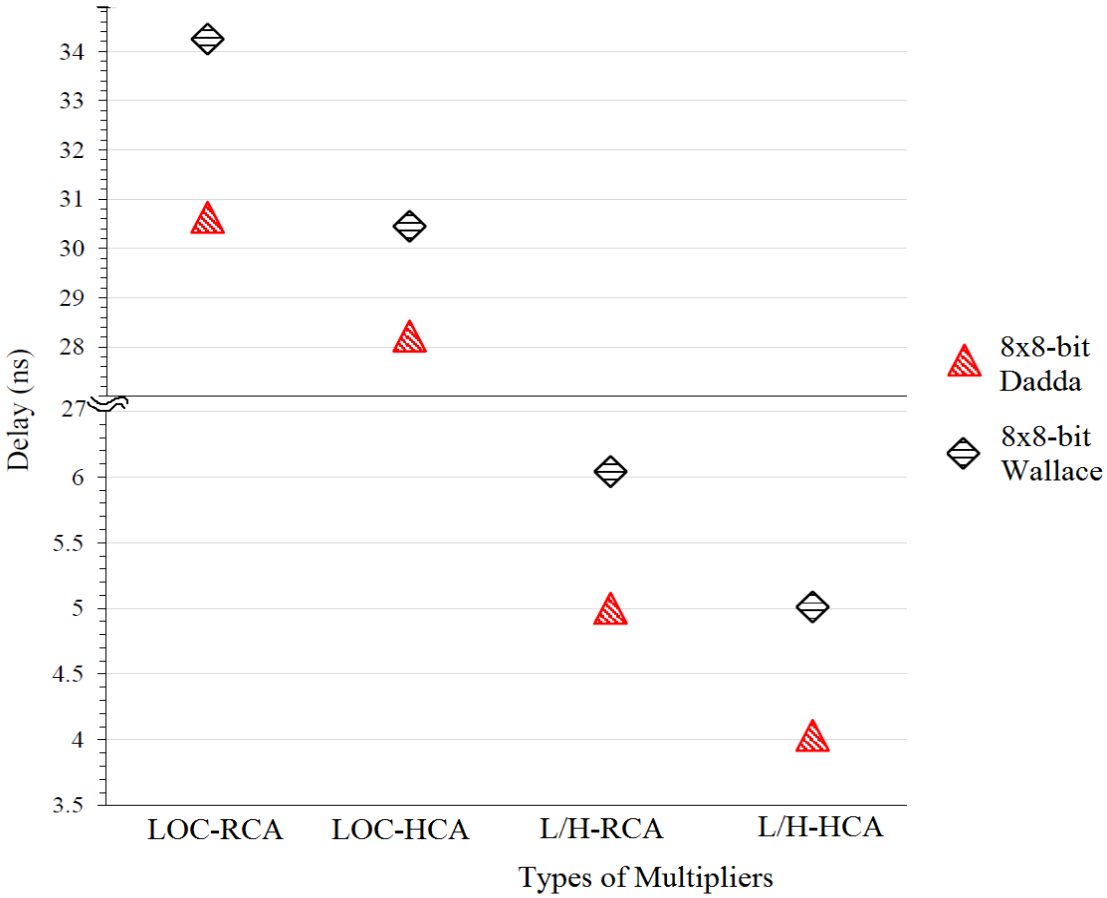
Figure 4.30 shows the Design Space Exploration (DSE) chart of all proposed 8x8-bit Wallace tree and Dadda multipliers at 45 technology nodes in sub-threshold region.

In Figure 4.30, a change of scale on y-axis is shown with a kink (~) to show the histograms for power and delay for all types of multipliers in its entire range. This is done to show the comparisons of power and delay for all types of multipliers in same figure.

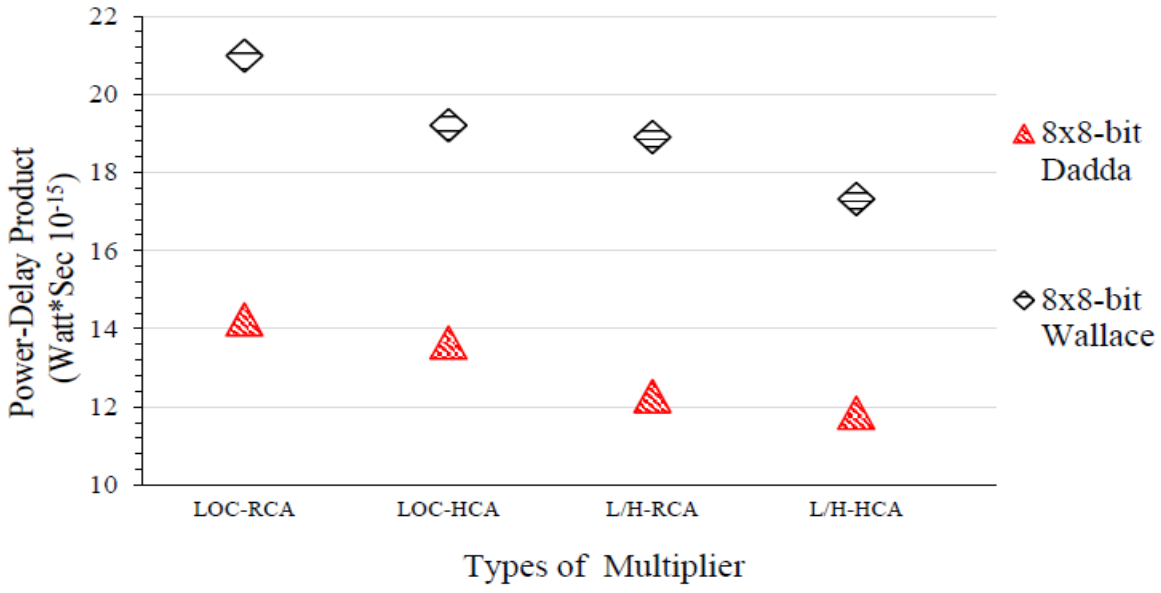
The same distribution pattern of power, delay and power-delay product of both the multipliers are found at 180 nm technology.


3.6
3.1
2.6
2.1
1.6
0.6
0.55
0.5
0.45
0.4
Power (µW)
LOC-RCA
LOC-HCA
L/H-RCA
L/H-HCA
Types of Multipliers
8x8-bit Dadda
8x8-bit Wallace

(a)


34
33
32
31
30
29
28
27
6
5.5
5
4.5
4
3.5
Delay (ns)
LOC-RCA
LOC-HCA
L/H-RCA
L/H-HCA
Types of Multipliers
8x8-bit Dadda
8x8-bit Wallace

(b)



(c)

Figure 4.30: DSE chart of all published referenced and proposed 8x8-bit Wallace tree and Dadda multipliers (a) power (b) delay (c) power-delay product

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CHAPTER 5

STATIC RANDOM ACCESS MEMORY (SRAM)

5.1. INTRODUCTION

In this era of system on chips (SoC), embedded SRAM is an essential component in the memory hierarchy of modern computing systems [1][2][3]. SRAM comprises 20% to 80% of the total chip transistor count on an average which consumes a large amount of power in SoC [4]. As a result, SRAM's area, power, performance and leakage have become significant deciding factors in overall budgeting of SoC. To satisfy the low power requirement of the SRAM cells, sub-threshold design technique is being introduced. Typical application of a sub-threshold based SRAM cell is in low power 16-bit RISC general processor in 130nm IBM CMOS process which can be used for wireless sensor node applications [5].

Sub-threshold memory designs demand low leakage currents which involves scaling the power supply voltage below the device threshold [6]. Data retention of the SRAM cell, both in standby (hold) mode and during a read access, is an important functional constraint in nanometer technology nodes. The cell becomes less stable with lower supply voltage, increasing leakage currents and increasing variability, all resulting from technology scaling. Hence, the low supply voltage reduces the performance of the memory cell which makes it necessary to develop new designs with improved performance.

Further, to achieve stable read and successful write operation, static noise margin (SNM), a critical metric for SRAM bit-cell stability, should be as high as possible under various temperature and voltage condition. As SRAM is scaled with lower supply voltage (V_{DD}) and technology, sufficient SNM becomes difficult to maintain in the conventional 6T SRAM cell (C6T). This difficulty occurs due to increase in inter-die statistical variation in the process parameters (threshold voltage (V_{th}), channel length (L), channel width (W) of transistors) [7]. These inter-die parameter variations may lead to destructive read (i.e., flipping of the stored data in a cell while reading) and unsuccessful write (inability to write to a cell) in a SRAM cell, thereby, degrading the memory design yield in nanometer technologies [8].

To overcome these problems several technologies, such as FinFET, CNTFET, SOI, 3D designs, nano computing etc. have become very attractive area in research but these are very

expensive, less reliable under low voltage or temperature gradients [9]. This drawback necessitates improvement in the design of SRAM cells with the current CMOS technology.

Further, the impact of scaling on the SRAM cell performance needs to be investigated. So, in this thesis work, scaling impact has been observed by studying designs performance at above and below nanometer range i.e. 180 nm, and 45 nm technology nodes.

Through literature survey, it is observed that while few papers are published at 45 nm technology, but a good research has already been carried out on designing ultra-low power SRAM cells, with number of transistors varying from 4 to 12, at 180 nm, and 0.4 V supply in sub-threshold region [10][11][12][13][14][15][16][17]. The focus is mainly on to improve certain typical important parameters like hold power, read delay, write delay, and read SNM (RSNM). Thus, new designs are not created at 180nm technology in present work.

The results of above published references at 180 nm technology node have been studied and summarized in Table 5.1(a). It is observed that for these referenced designs, either the aspect ratios of transistors are different from each other or the different 45 nm libraries are used for simulation. Thus, for the sake of uniformity, the RSNM, WSNM, read delay, write delay, and leakage power consumption values have been re-evaluated for all at 180 nm technology, in our simulation set up, keeping the schematic of the referenced cells same as given in original references.

Table 5.1(a): Comparison of various SRAM cells at 180 nm technology at 0.4 V

Types of SRAM cells	References	Leakage Power in Hold mode (W)	RSNM (mV)	Read Delay (s)	WSNM (mV)	Write Delay (s)
4T	[12]	7.79E-10	28.0	200E-9	32.4	100E-9
	[12]	7.79E-10	18.0	120E-9	22.1	20.0E-9
5T	[10]	03.60E-6	21.4	65.0E-9	35.7	1.30E-9
	[12]	3.42E-10	22.0	5.00E-9	41.0	5.00E-9
	[12]	5.65E-10	20.1	10.0E-9	47.7	10.0E-9
6T	[16]	81.00E-6	19.4	8.50E-9	32.4	6.00E-9
	[18]	05.44E-6	140	7.84E-9	28.4	4.74E-9
	[10]	131.0E-6	15.2	0.47E-9	27.8	0.96E-9
	[12]	9.29E-10	22.4	5.00E-9	55.7	1.00E-9
	[12]	1.56E-10	20.1	41.0E-9	47.7	35.4E-9
	[14]	152E-06	40.2	2.24E-9	22.1	8.44E-9
7T	[10]	6.64E-09	26.7	127E-9	38	210E-9
8T	[13]	3.89E-09	59.6	8.27E-9	70.2	7.50E-9
9T	[10]	5.09E-09	23.4	65.0E-9	44.8	2.00E-9
12T	[15]	4.77E-09	32	110E-9	68.5	81.1E-9

For ultra-low power SRAM cells, with number of transistors varying from 4 to 12, only those configurations are considered for further comparison for which leakage power in hold mode is less in Table 5.1(a). Additional performance metrics from N curve analysis are also estimated for them. Table 5.1(b) shows all performance parameter values of selected referenced SRAM cells.

Table 5.1(b): Comparison of low power SRAM cells at 180 nm technology at 0.4 V

SRAM cell	WSNM (mV)	|WTI| (µA)	WTV (mV)	RSNM (mV)	SVNM (mV)	SINM (µA)	Leakage Power in Hold mode (W)	Write Delay (s)	Read Delay (s)
4T[12]	22.1	84.0	230	18.0	170	32.1	7.79E-10	20.0E-9	120.0E-9
5T[12]	41.0	55.2	220	22.0	180	60.1	3.42E-10	5.00E-9	005.0E-9
6T[12]	47.7	32.3	250	20.1	150	26.9	1.56E-10	35.4E-9	041.0E-9
7T[10]	38.0	64.1	230	26.7	170	14.8	6.11E-09	210E-9	127.0E-9
8T[13]	70.2	13.0	220	59.6	180	73	3.89E-09	7.50E-9	8.27E-9
9T[10]	44.8	23.1	200	23.4	200	38.4	5.09E-09	2.00E-9	65.00E-9
12T[15]	68.5	25.5	190	32.0	210	65.4	4.77E-09	81.1E-9	110.0E-9

The results summarized in Table 5.1(b) are used to study & obtain performance trends, comparison, and effect of technology scaling (i.e. 180 nm to 45 nm) on the performance metrics while drawing conclusions.

At 45 nm technology, a major problem is that NMOS as well as PMOS transistors do not turn off completely. A high current through channel in OFF state (termed as 'leakage current' in this thesis) leads to either improper operation or reduced SNM during read, write operation. Thus, new designs need to be created for proper functional output.

For super-threshold operation, negative bit-line (BL) scheme, cell-V_{DD} (CV_{DD}) adjustment (1 extra control line), differential CVSS (2 extra control line), dual-rail supply scheme, and write back (4 extra control lines) schemes have been devised [18][19]. However, these designs can only operate at supply voltage in 0.45 V to 0.7 V range.

Few reported works at 45 nm technology, for sub-threshold region, have developed various read or write assist methods to enhance the write margin and read stability for various SRAM cells for ultra-low power operation. These schemes include cell virtual-ground (CVSS) bias (1 extra control line), and boosted or reduced word-line (WL) voltage (2 extra control line) [20].

Reducing the supply voltage further is desirable to achieve very low power consuming memory design.

A comprehensive analysis of sub-threshold based SRAM cells and combined effects of all design metrics (read stability, write ability, hold stability, read/write access time and leakage power consumption) have not been reported so far at sub-nanometer technology.

Thus, this chapter focuses on proposal of new functional SRAM cell designs with a comprehensive study, and analysis of their all design metrics (read stability, write ability, hold stability, read/write access time and leakage power consumption) at 45 nm technology in sub-threshold region along with performance comparison with published designs at 45 and 180 nm technology.

In this chapter,

- Results of published research papers at 180 nm technology node have been studied and summarized in Table 5.1. The design trends have been analyzed and conclusions are drawn in Section 5.6 and Section 5.7 respectively.
- New five ultra-low power, low voltage SRAM cells are implemented and their thorough performance parameter analysis is carried out and compared with C6T in sub-threshold region at 45 nm technology.

  All these five proposed SRAM cells are designed by inserting additional transistors to increase the node currents for stability improvement. This is done without inserting an additional control line to switch the data inside/outside the memory cells thereby saving overall area of the memory cells.

The proposed five SRAM cell designs are

i. Modified 7T SRAM cell (named as M7T)

ii. Modified PMOS pass transistor logic (PTL)-based eight transistors SRAM cell, (named as MPT8T)

iii. Modified eight transistors SRAM cell (named as M8T)

iv. Modified 9T SRAM cell (named as M9T)

v. Modified inverter based twelve transistors SRAM cell (named as MI-12T)

The rest of the chapter is organized as follows:

Section 5.2 presents the architecture of C6T with their functional read, write and hold operation. Section 5.3 present the architecture of proposed M7T, MPT8T, M8T, M9T, and MI-12T SRAM cells with their functional read, write and hold operation. Section 5.4 describes the simulation methodology and overall post layout simulation results of the all proposed designs. Section 5.5 presents analytical model of all C6T and proposed SRAM cells to obtain the read/write and hold SNM values mathematically and also verifies the simulated results. Section 5.6 describes the final results and discussion of SRAM cells and Section 5.7 presents the summary of the chapter and the concluding remarks.

5.2. DESIGN AND OPERATION OF C6T

The conventional structure of SRAM cell consists of two cross coupled inverters to store one-bit information inside the cell and two nodes (Q and QB) of the inverters are connected to two separate bit-lines, BL and BLB via two switches (left and right of the cell). Both the bits lines BL /BLB participate in read and write operations [20].

The two switches in Figure 5.1 are used to communicate one-bit information with the outside of the cell. These two switches are replaced by different kinds of pass transistor (acts as a switch) which are controlled by a word-line (WL). As long as the switches are turned off, the cell keeps one of its two possible steady states either ‘logic 0’ or ‘logic 1’. During the read and write operations, common WL controls accessibility to the cell nodes Q and QB through these two switches.

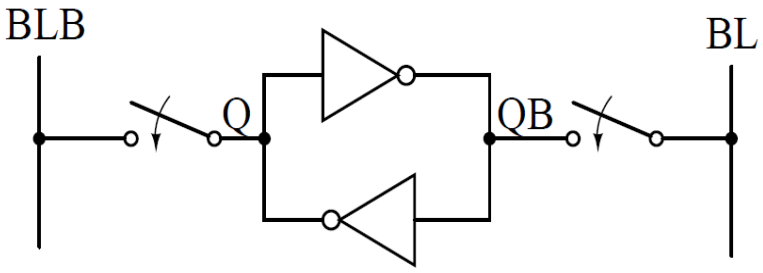


Figure 5.1: Basic SRAM cell

During read operation, the data contents of a memory word are read out (nondestructively), and during write operation, data is stored in a memory word, replacing any data that was previously stored there.

- During ‘read’ operation, the bit-lines (BL/BLB) start pre-charging to reference voltage usually close to the positive supply and the WL is activated. The SRAM cell starts to

discharge one of the bit lines (the one connected to the cell node storing logic 0). The minimum acceptable differential voltage across the bit-line pair directly governs the read access time of the memory and therefore its speed. A larger bit line differential voltage is advantageous for reliable sensing but the cell takes longer to develop that differential voltage. The sense amplifier (SA) circuit is used to sense values at BL and BLB lines during the read operation. It detects the difference of voltages between BL and BLB.

An optimum exists between time taken by the cell to develop the bit line differential (usually 100mV [21]) and SA to amplify the input data to full swing CMOS signal levels [22][23].

- During 'write' operation, the write data is transferred to the desired columns by driving the data onto the bit-line pair by grounding either the bit line or its complement. If the cell data is different from the write data, then the logic '1' is discharged when the access transistor connect it to the discharged bit-line, thus causing the cell to be written with the bit-line value.

The schematic and layout of C6T is shown in Figure 5.2 [24]. The internal architecture of this cell consists of cross-coupled inverter pair (MP1/MN1) and (MP2/MN2) to store one-bit information inside the cell. The access transistors (MN5 and MN6) are used to communicate one-bit information with the outside of the cell. These two NMOS pass transistor are controlled by WL. As long as the MN5 and MN6 transistors are turned off, the cell keeps one of its two possible steady states either logic '0' or logic '1'.

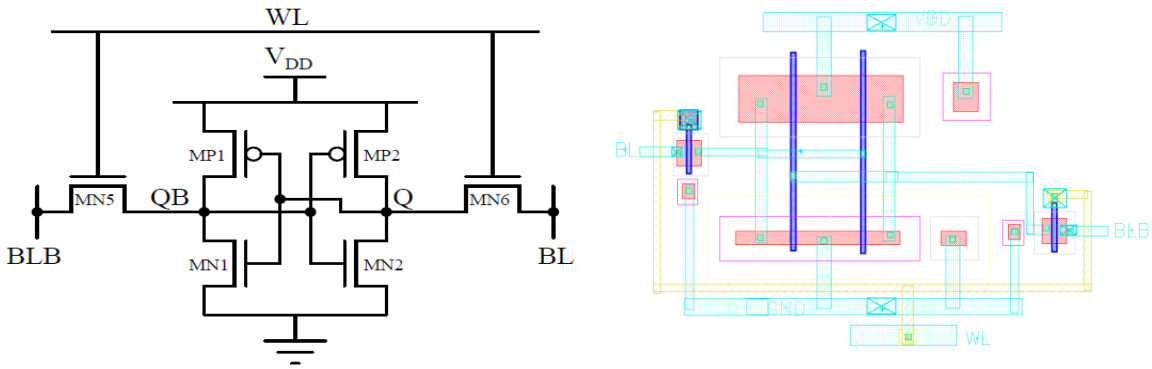


Figure 5.2: Schematic and layout of C6T

Transistor sizing i.e. cell ratio (CR) and pull up ratio (PR), is an important factor which decides stable read and writes operation for an SRAM cell that is indicated by a high RSNM and WSNM (figure of merits). CR is the ratio between sizes of the pull-down transistor to the access transistor ($=W_{pull\ down}/W_{access}$) keeping L same for both transistors, during the read

operation. Similarly, PR is a ratio between sizes of the pull up transistor to the access transistor ($=W_{pull\ up}/W_{access}$) keeping L same for both transistors, during write operation.

Typically, to obtain an maximum value for both in C6T, the CR and PR is kept in the range of 1.2 to 3 and ≤ 1.8 respectively [25][26]. For 45 nm technology, mobility ratio of NMOS to PMOS transistor is $\mu_n/\mu_p = 2.25$, $V_{th,n}=0.422V$, $|V_{th,p}|=0.412V$. Accordingly, CR and PR ratio is selected by equating transistor currents under steady state conditions during read and write operations.

(i) Read operation of C6T: Circuit set up for read operation of C6T is shown in Figure 5.3. Assuming that logic '0' is stored in the cell initially. Thus, internal node voltages are Q = 0 V and QB = 1 V and access transistors (MN5 and MN6) are turned OFF. The transistors MP2 and MN1 are turned OFF, while the transistors MP1 and MN2 operate in linear mode.

During read operation, the bit-lines (BL/BLB) are pre-charged to a high level (V_{DD}) and WL is enabled (pulsed to a high level) which turns-on the access transistors MN5 and MN6 [27].

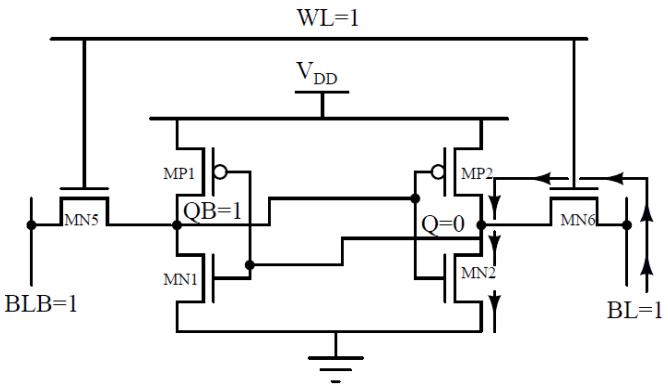


Figure 5.3: Test circuit for read operation of C6T

The voltage at BLB will not have a significant variation in voltage as no current flows through MN5 due to BLB & QB ='1' at both end. On the other hand, transistors MN6 and MN2 conduct and the voltage level of BL line will begin to drop slightly, so that a differential voltage develops between the bit-lines which are sensed by sense amplifier. For successful read operation, the node voltage at Q should remain below the threshold voltage of MN1 to prevent false turn ON of transistor MN1.

Thus, CR is the critical parameter of the SRAM cell during the read operation which is here selected as 3 to keep the node voltage Q less than the threshold voltage of MN1.

The high value of CR is desirable to prevent tripping of the cell due to noise at Q, thereby increasing read stability (i.e. RSNM) but at the cost of increased cell area.

(ii) Write operation of C6T: Circuit set up for write operation of C6T is shown in Figure 5.4. The node voltage QB always remains below the threshold voltage of MN2, since MN1 and MN5 are designed according to CR ratio. So, it is not sufficient to turn ON MN2.

To change the stored information, i.e. to force QB = V_{DD}, the node voltage at Q must be reduced below the threshold voltage of MN1 to turn it OFF.

So, consider a write '0' operation at node Q. Thus, internal node voltages are Q = '1' and QB = '0' before WL is enabled (i.e. pulsed to a high level). The transistors MP1 and MN2 are turned OFF, while the transistors MN1 and MP2 operate in linear mode.

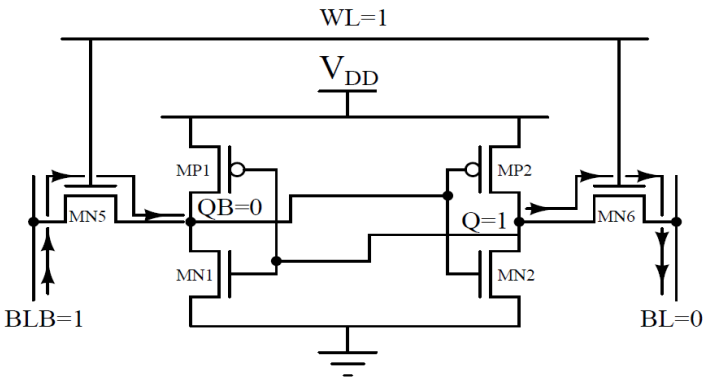


Figure 5.4: Test circuit for write operation of C6T

During write operation, the bit-lines BLB is at high level (V_{DD}) and BL is pulled down to low level (logic '0') , WL is enabled which turns on the access transistors MN5 and MN6. For successful write '0' operation, the node voltage Q discharges through MN6 to a low voltage below the threshold voltage of MN1. This turns OFF MN1 and turns ON MP1. The current through MP1, pulls up the voltage at QB to logic '1'.

The critical part of the circuit is the voltage divider formed by the pull up and access transistor. So, PR is an important parameter in write mode which is here selected as PR= 2.6.

The strength of the pull-up transistor determines the ease/difficulty of writing data '0' (i.e. flipping the state of cell from '1' to '0'). With small PR, it is easier to pull the node Q to GND thereby increasing write ability of the cell.

(iii) Hold Operation of C6T: One of the primary performance metric in nano-scale SRAM design is data retention ability which is analyzed by computing SNM in hold mode. This hold SNM metric, first defined by Seevinck et al. [28], measures the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the stored bit. A higher SNM indicates better stability of the cell. Conceptual test circuit for measuring the hold SNM of C6T is shown in Figure 5.5.

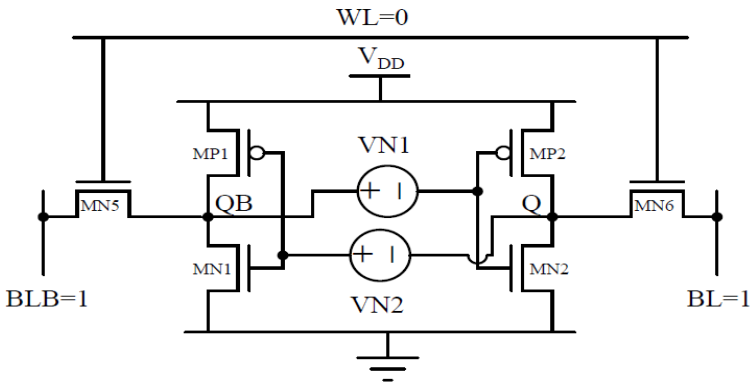


Figure 5.5: Test circuit for measurement of hold SNM of C6T

The hold operation is performed by lowering WL to logic '0' , switching OFF the MN5 and MN6 access transistors and bit line pair (BL/BLB) is at high voltage. This disconnects the cell nodes QB and Q from both the bit-lines. Two equal dc voltage sources, VN1 and VN2 are placed between inverters indicating the dc noise sources. These two voltage sources are swept from 0 to V_{DD} to obtain voltage transfer curves.

Then voltage transfer curve (VTC) of inverter (MP1, MN1) and the mirrored voltage transfer curve (VTC^{-1}), of second inverter (MP2, MN2) are plotted on same axis. The resultant curve is referred as 'butterfly curve'. The side length of the largest square that can be embedded inside the lobes of the butterfly curve represents the hold SNM of the cell of the C6T [29]. The pull up to pull down transistor ratio is critical for stability during hold operation which is here selected as 0.8. Figures showing transient waveform of Q, QB during read, write, and hold mode are included in Appendix B.

5.3. DESIGN AND OPERATION OF PROPOSED SRAM CELLS AT 45 NM

In C6T, due to high leakage current in OFF state, NMOS access transistors do not turn OFF completely leading to degraded output at nodes Q and QB in both ON and OFF state (as shown in Table 5.2) which is high compared to 0 V in sub-threshold region. This causes degradation in stability of stored logic due to high OFF STATE leakage currents in cross coupled inverter pair. Therefore, modification is required in C6T for its proper operation.

The C6T design is modified by using following three techniques:

I. Modification in design of access transistor.
II. Modification in design of cross coupled inverter pair.
III. Modification in connection of WL signal to access transistors to generate clock feed-through effect.

This section presents the design and analysis of all five proposed M7T, MPT8T, M8T, M9T and MI-12T SRAM cells using above techniques.

I. Technique I: Modification in design of access transistor

Figure 5.6 shows designs of possible ten different transistor- transistor combinations N, P, NP, PP, PN, NN, NN-parallel, NP-parallel, PP-parallel and PN-parallel that can replace NMOS access transistor i.e. MN5 (MN6) of C6T in Figure 5.2.

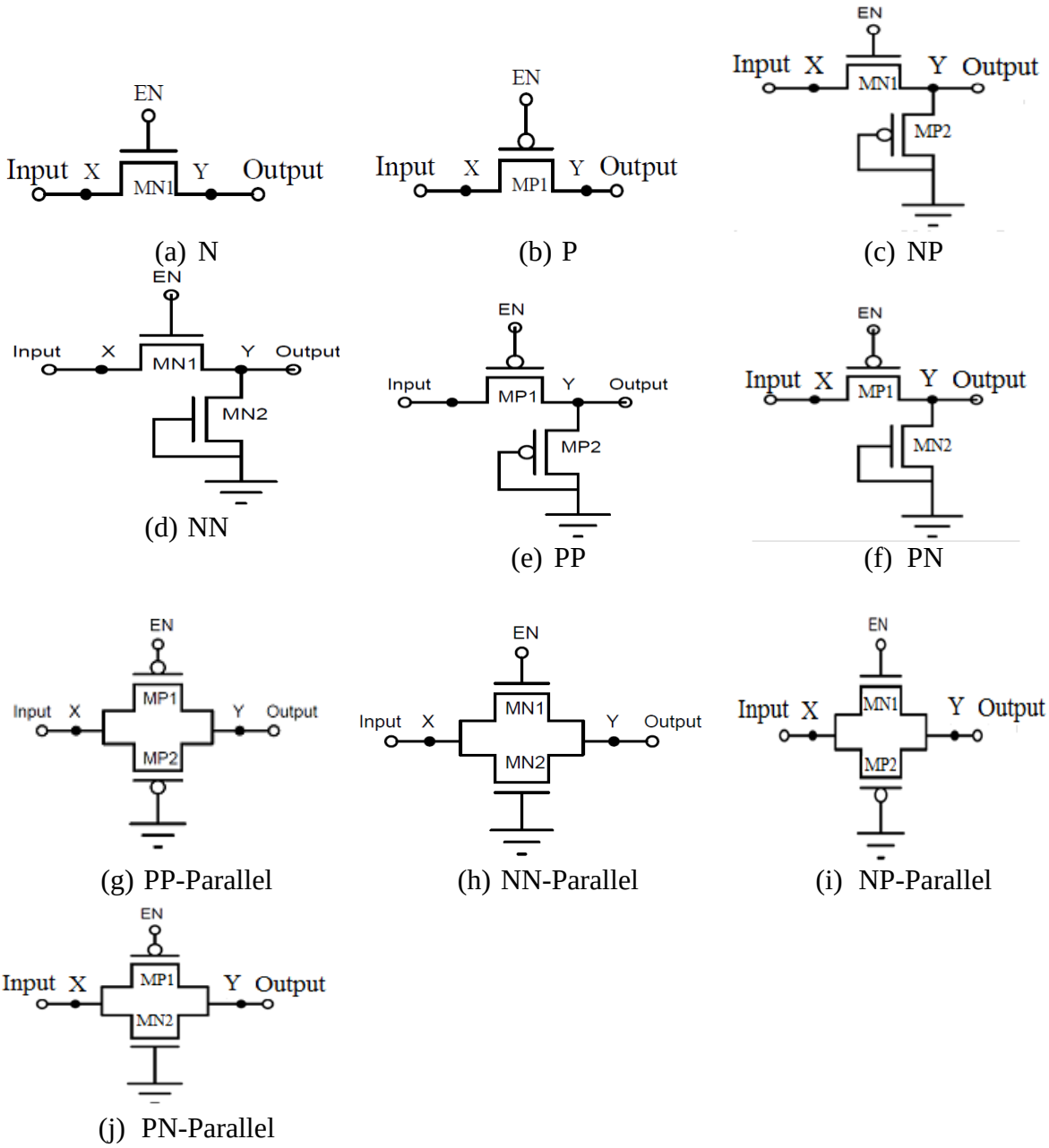


Figure 5.6: Schematics of access transistor pairs

Each configuration, given above, is checked for functionality through simulation at 0.4V supply for 45 nm. For simulation, aspect ratio of transistor (either MN1 or MP1) in each configuration is taken (W/L) = 75 nm/ 55nm=1.5. Aspect ratio of additional transistor (i.e. either MN2 or MP2) in each configuration is kept constant at (W/L) = 65/45 nm=1.4. If this value is increased above 1.4, the function of all modified configurations does not show any improvement in observed output. The simulation results of these ten combinations are given in Table 5.2 and the graph are shown in Figure 5.7. These show the ON/OFF transient state analysis of these access transistor pairs.

Table 5.2: Results of conventional and modified access transistor (P, NP, PP, PN and NN) at 0.4V supply for 45 nm

Access Transistor Type	**Enable [EN=1 for NMOS = 0 for PMOS] (ON Condition)**		**Enable [EN=0 for NMOS = 1 for PMOS] (OFF Condition)**		**Operation**	
	Input given at node X (V)	**Output at node Y (V)**	**Input at node X (V)**	**Output at node Y (V)**	**Turn ON**	**Turn OFF**
N (MN5/MN6)	**0.4**	**0.239**	**0.4**	**0.073**	**Degraded**	**Degraded**
P	0.4	0.400	0.4	0.336	Proper	Faulty output
NP	0.4	0.396	0.4	0.400	Proper	Faulty output
PP	0.4	0.400	0.4	0.321	Proper	Faulty output
PN	**0.4**	**0.400**	**0.4**	**0.000**	**Proper**	**Proper**
NN	0.4	0.038	0.4	0.000	Faulty output	Proper
NN-parallel	**0.4**	**0.400**	**0.4**	**0.078**	**Proper**	**Degraded**
NP-parallel	**0.4**	**0.219**	**0.4**	**0.078**	**Degraded**	**Degraded**
PN-parallel	0.4	0.400	0.4	**0.400**	Proper	Faulty output
PP-parallel	0.4	0.400	0.4	**0.400**	Proper	Faulty output

The results indicate that:

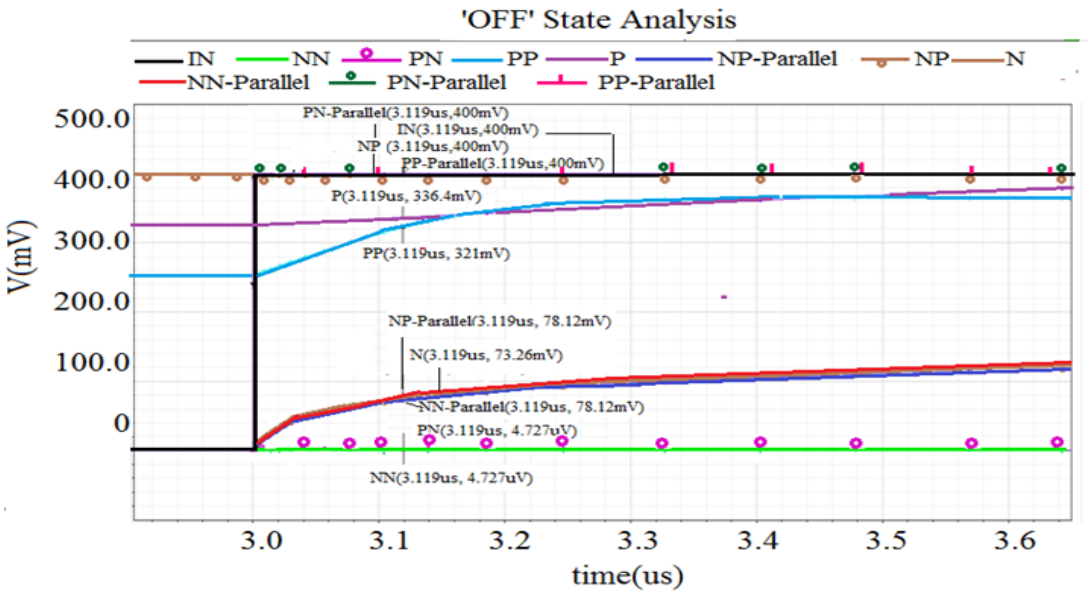
- An N (NMOS) transistor, in Figure 5.6, does not properly turn OFF with a voltage of 0.073 V at its output which is high as compared 0 V. This is due to high off state leakage current. This causes degradation in logic '0'. N also shows degradation of logic ‘1’ in turn ON state due to low sub-threshold conduction current at low power supply voltage of 0.4V.
- P (PMOS) transistor also has a turn OFF problem and does not pass a proper 0 V at its output.

Both N and P access transistors (described above) have been modified by adding an extra transistor at its output. The purpose of adding this additional transistor is to discharge the

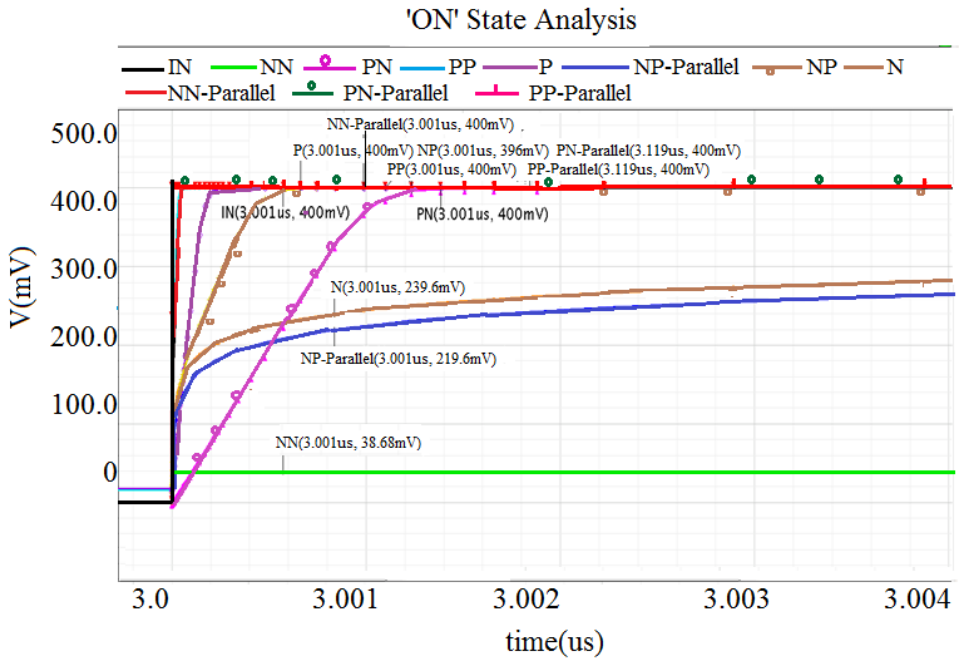
output node (Y) to 0 V. The gate terminal of additional transistor is connected to ground for the ease of layout so that no additional control line is required for gate voltage. The performance of modified designs is discussed below:

- The resulting NP and PP combinations have shown a turn OFF problem as output remains in charged stage always due to insufficient discharge current provided by additional transistor.
- NN, also, has a turn ON problem as output remains in discharged stage always. Sizing of transistors also have not yield proper operation.
- PN shows proper operation. Here, transistors are carefully sized so that they are strong enough to allow data to be changed at the storage nodes during writing but weak enough not to flip the state of the cell during reading.
- NN-parallel does not properly turn OFF with a voltage of 0.078 V at its output which is high as compared 0 V. This causes degradation in logic '0'.
- NP-parallel combination shows degraded output at both ON/OFF condition. Its performance is poorer than N.
- PP-parallel, PN-parallel combination shows faulty result at OFF condition.

The graphs in Figure 5.7 show the ON/OFF performance of above ten access transistor combinations obtained through transient simulation.



(a)



(b)

Figure 5.7: ON/OFF state analysis of access transistors

- The plotted graph shows that only PN combination performs perfect operation for both turn ON and OFF state.
- The access transistor (N, NN-parallel and NP-parallel) show degraded output (i.e. V_{OL} is low but greater than 0V and V_{OH} is high but less than 0.4V) in ON/OFF state with NP parallel performance poorer than N.
- The access transistor combinations (P, NP, PP, NN, PP-parallel and PN-parallel) show faulty output in either ON or OFF state. Hence, these cannot be used as access transistors in SRAM cells.

Based on above analysis, two new designs of SRAM cell are created by modification in design of access transistor which are discussed in Sections 5.3.1 and 5.3.2.

5.3.1. Design of Proposed MPT8T using PN Access Transistor

The proposed MPT8T SRAM cell comprises of eight transistors as shown in Figure 5.8. The internal architecture of proposed 8T-SRAM cell consists of a cross-coupled inverter pair (MP1/MN1 and MP2/MN2) similar to C6T to store one-bit information.

Modification: The access transistors (MN5, MN6) of 6T are replaced by MP3-MN3 pair and MP4-MN4 pair respectively, thereby making it an 8T SRAM cell [30]. The additional NMOS transistors (MN3/ MN4) are always in OFF state for both read/write operations. During hold

operation off state leakage current of MN3/MN4 helps in maintaining '0' at node QB/Q. Also, they do not require additional control line to turn them ON/ OFF. For CR and PR calculation, aspect ratio of additional transistor (i.e. either MN3 or MN4) in each configuration is kept constant at (W/L) = 65/45 nm=1.4.

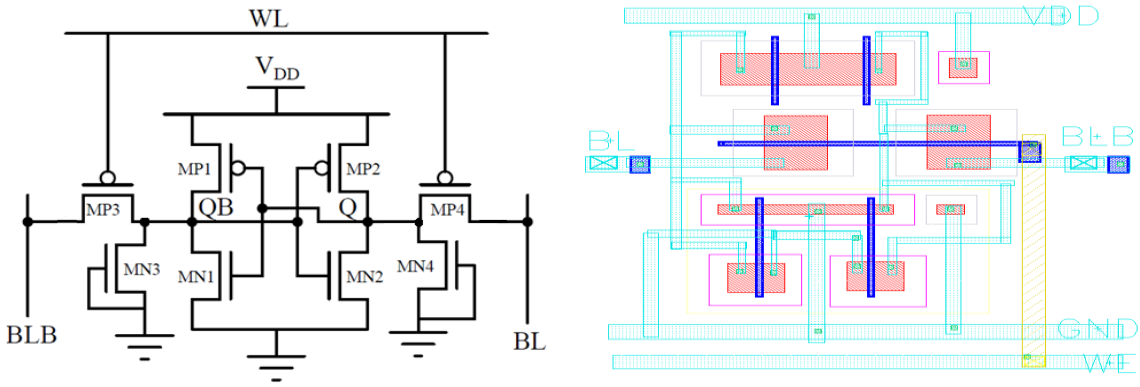


Figure 5.8: Schematic and layout of MPT8T

(i) Read operation of MPT8T: Circuit set up for read operation of MPT8T is shown in Figure 5.9. Assuming that logic '0' is stored in the cell initially. Thus, internal node voltages are Q = 0 V and QB = 1 V and the access transistors (MP3 and MP4) are OFF. The transistors MP2 and MN1 are turned OFF, while the transistors MP1 and MN2 operate in linear mode.

During read operation, the bit-lines (BL/BLB) are pre-charged to V_{DD} and WL is enabled (pulsed to a low level) which turns-on the MP3 and MP4 transistors of each access transistor pair.

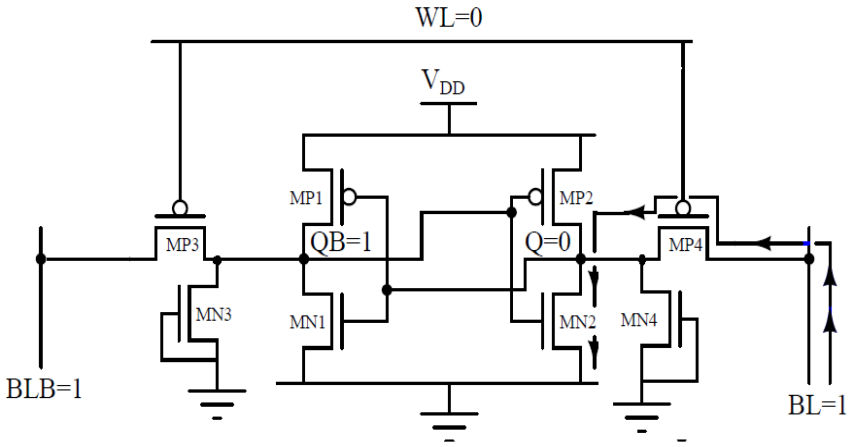


Figure 5.9: Test circuit for read operation of MPT8T

After the access transistors MP3 and MP4 are switched ON, the voltage at BLB will not have any change in voltage level as no current flows through MP3 due to BLB & QB ='1' at both

end. On the other hand, transistors MP4 and MN2 conduct and the voltage level of BL line will begin to drop slightly, so that a differential voltage develops between the bit-lines which are sensed by sense amplifier. The read operation would be stable provided the node voltage Q, which tends to rise, does not exceed the threshold voltage of MN1.

For maximum RSNM in MPT8T, the CR has been checked through simulation and chosen to be 3.

(ii) Write operation of MPT8T: Circuit set up for write operation of MPT8T is shown in Figure 5.10. Assuming logic'1' is stored in the SRAM cell initially, the transistors MP1 and MN2 are turned off, while the transistors MN1 and MP2 operate in linear mode. Thus, internal node voltages are Q = '1' and QB = '0'.

During write '0' operation, the bit-lines BLB is pre-charged to a high level (V_{DD}) and BL is pre-(dis) charged to low level (logic '0') and WL is enabled (pulsed to a low voltage) which turns on the PMOS transistors (MP3 and MP4) of the corresponding access transistor pairs. The voltages at Q/ QB nodes fall/ rise respectively to reach logic 0/ 1.

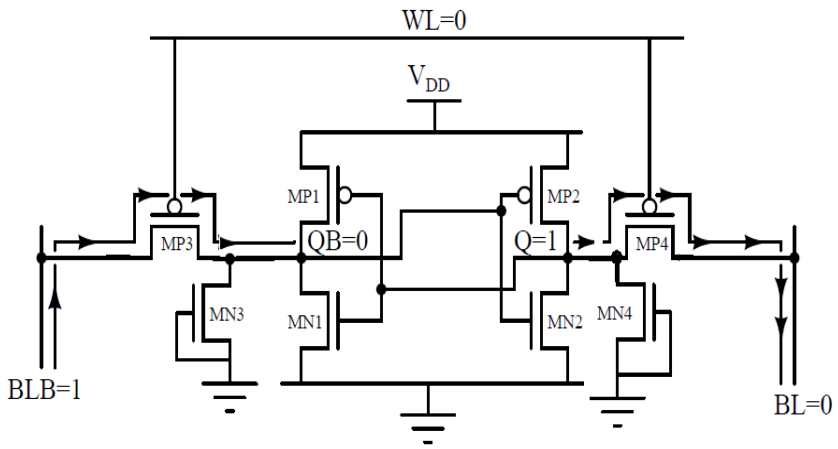


Figure 5.10: Test circuit for write operation of MPT8T

For successful write '0' operation the node voltage Q should remain below the threshold voltage of MN1. For this, the aspect ratios of the transistors (MP4, MN2) and (MP3, MN1) have to be computed accurately. For maximum WSNM in MPT8T, the PR has been obtained through simulation as 1.8.

(iii) Hold Operation of MPT8T: Conceptual test circuit for measuring the hold SNM of MPT8T is shown in Figure 5.11.

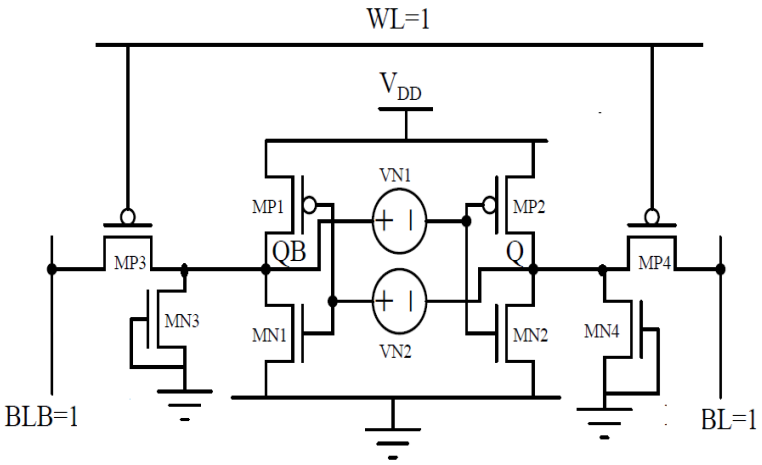


Figure 5.11: Test circuit for hold SNM of MPT8T

The hold operation is performed by pre-charging bit line pair (BL/BLB) to high voltage (V_{DD}). WL is disabled (biased at logic '1'), thus, switching OFF the MP3 and MP4 access transistors. This disconnects the cell nodes QB and Q from both the bit-lines.

The pull up to pull down transistor ratio is critical for stability during hold operation which is here selected as 0.6. Then similar methodology is followed for calculating the hold SNM of the MPT8T in sub-threshold region as given in Section 5.2. Figures showing transient waveform of Q, QB during read, write, and hold mode are included in Appendix B.

5.3.2. Design of Proposed M8T using NN-Parallel Access Transistor

The proposed M8T SRAM cell comprises of eight transistors as shown in Figure 5.12. The internal architecture of proposed 8T-SRAM cell consists of cross-coupled inverter pair (MP1/MN1 and MP2/MN2) with NN-parallel type access transistor i.e. MN5-MN3 (or MN6-MN4).

Modification: Here, in NN-parallel type access transistor pair, MN3 and MN4 always operate in off state and provide additional current (their off-state leakage current) to nodes Q/QB which decreases delay of the memory cell and improves the SNM characteristics. Another advantage is that no additional control lines are required to control gate voltage of MN3 and MN4. For CR and PR calculation, aspect ratio of additional transistor (i.e. either MN3 or MN4) in each configuration is kept constant at (W/L) = 65/ 45nm =1.4.

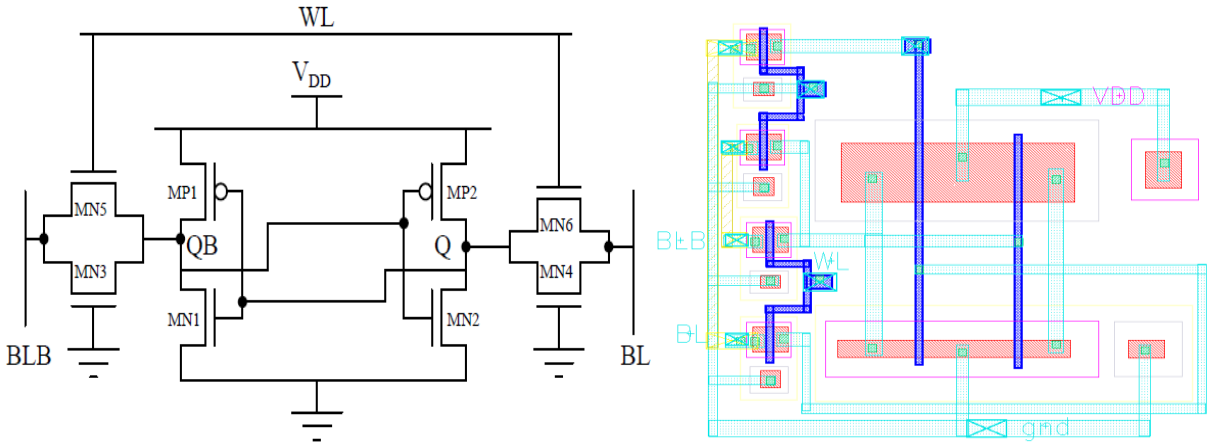


Figure 5.12: Schematic and layout of M8T

(i) Read operation of M8T: Circuit set up for read operation of M8T is shown in Figure 5.13. Assuming that logic '0' is stored in the cell initially. Thus, internal node voltages are Q = 0 V and QB = 1 V. The access transistors (MN5 and MN6) are turned OFF. The transistors MP2 and MN1 are turned OFF, while the transistors MP1 and MN2 operate in linear mode. The additional two NMOS transistors (MN3 and MN4) operate in cut off region (OFF state).

During read operation, the bit-lines (BL/BLB) are pre-charged to V_{DD} and WL is enabled (pulsed to a high level) which turns-ON the access transistors MN5 and MN6.

After the access transistors are switched ON, the voltage at BLB will not have a significant variation in voltage as no current flows through MN5 due to BLB & QB ='1' at both end.

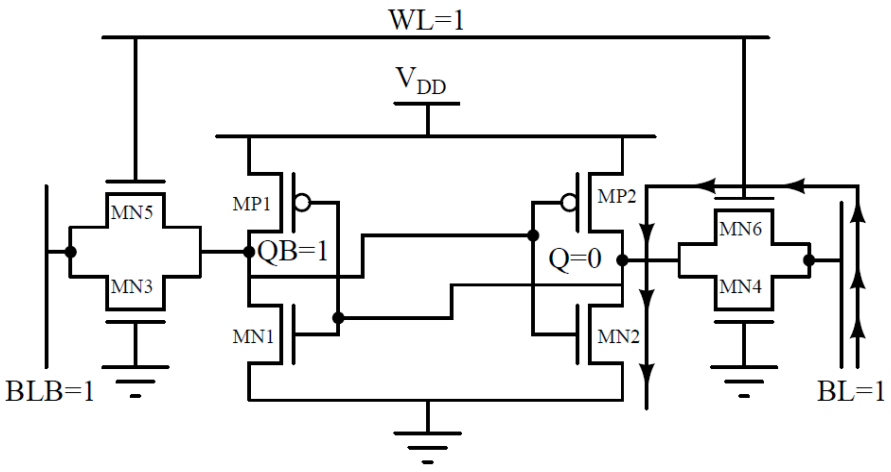


Figure 5.13: Test circuit for read operation of M8T

On the other hand, transistors MN6 and MN2 conduct and the voltage level of BL line will begin to drop slightly, so that a differential voltage develops between the bit-lines which are

sensed by sense amplifier. For successful read operation, the node voltage at Q should remain below the threshold voltage of MN1 to prevent false turn ON of transistor MN1. Thus, CR is the critical parameter of the SRAM cell during the read operation. For maximum RSNM, the CR has been obtained through simulation as 2.7.

(ii) Write operation of M8T: Circuit set up for write operation of M8T is shown in Figure 5.14. Consider a write '0' operation at node Q. Thus, internal node voltages are Q = '1' and QB = '0' before WL is enabled (i.e. pulsed to a high level). The transistors MP1 and MN2 are turned OFF, while the transistors MN1 and MP2 operate in linear mode.

During write operation, the bit-lines BLB is at high level (V_{DD}) and BL is pulled down to low level (logic '0') , WL is enabled which turns on the access transistors MN5 and MN6. For successful write '0' operation, the node voltage Q discharges through MN6 to a low voltage below the threshold voltage of MN1.

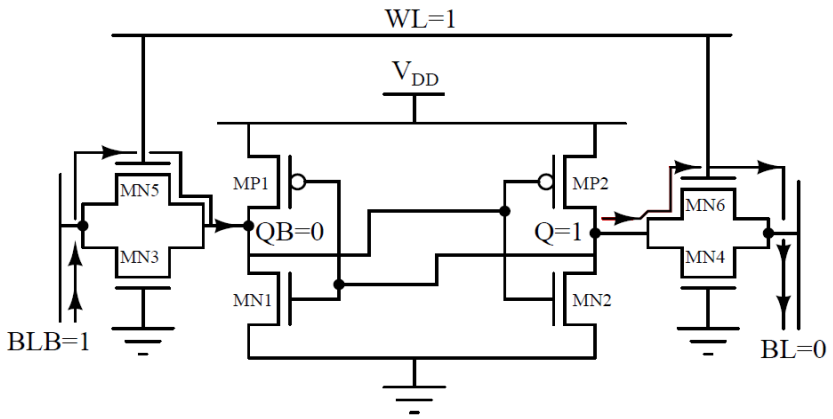


Figure 5.14: Test circuit for write operation of M8T

The critical part of the circuit is the voltage divider formed by the pull up and access transistor. For maximum WSNM, the PR has been obtained through simulation as 2.5.

(iii) Hold Operation of M8T: Test circuit for measurement of hold SNM of M8T is shown in Figure 5.15.

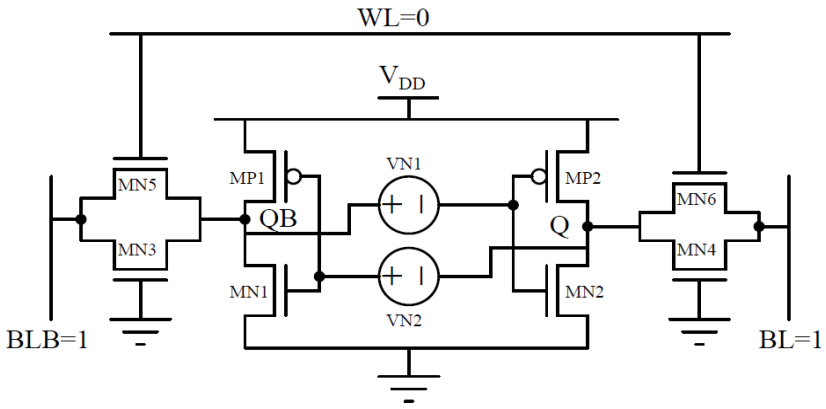


Figure 5.15: Test circuit for measurement of hold SNM of M8T

The hold operation is performed by lowering WL biased to logic '0', switching OFF the MN5 and MN6 access transistors and bit line pair (BL/BLB) is at high voltage. This disconnects the cell nodes QB and Q from both the bit-lines. The pull up to pull down transistor ratio is critical for stability during hold operation which is here selected as 0.9. Then similar methodology is followed for calculating the hold SNM of the M8T in sub-threshold region as given in Section 5.2. Figures showing transient waveform of Q, QB during read, write, and hold mode are included in Appendix B.

II. Technique II: Modification in design of cross coupled inverter pair

Section 5.3.3 discusses the new design where modification is done in design of cross coupled inverter pair.

5.3.3. Design of Proposed MI-12T

The proposed MI-12T SRAM cell comprises of twelve transistors as shown in Figure 5.16. The internal architecture of proposed MI-12T consists of N type access transistors (MN5, MN6) and a modified cross-coupled inverter pair (MP1/MN1 and MP2/MN2).

Modification: Here, cross-coupled inverter pair is modified by adding an ON-OFF logic composed of PMOS & NMOS transistor (MP3-MN3-MN7 and MP4-MN4-MN8) in order to minimize the OFF-state leakage current during hold mode [31]. Transistors (MN3, MN1) and (MN4, MN2) form a stacked path. Due to body bias effect, MN3 & MN1 have an increased threshold voltage thereby reducing the OFF-state leakage current through MN1 even with logic '0' at node Q.

Further, the ON-OFF logic transistor MN3 isolates MN1 from node QB. In the case of voltage increasing at Q (due to destructive read operation), which may cause false turn on of MN1, as MN3 remains off causing QB to remain high. This stops the positive feedback through the

cross coupled inverter path which otherwise could cause switch ON of the MP2 transistor and could change the stored logic '0' in the cell at Q node.

The gate voltage of (MN3, MN4) is generated by (MP3, MP4) for, both, logic '0' / '1' at QB/Q node as per Table 5.2. Thus, for QB = '0', node a ='1' so MN3 turn ON and vice versa. MN3 transistor (in the cross coupled inverter logic) operate in the linear region for QB= '0', and cut off region for QB = '1', of the SRAM cell. Same is valid for node Q as well.

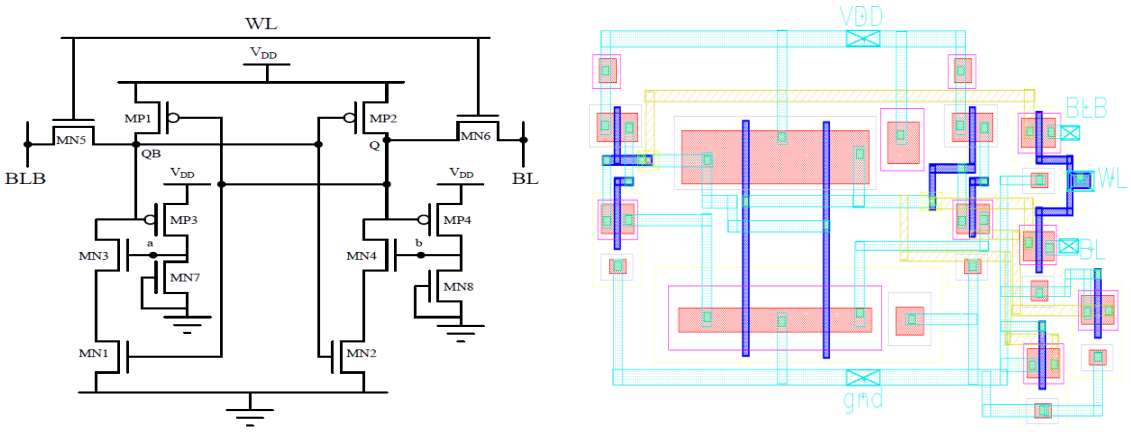


Figure 5.16: Proposed modified inverter based 12T SRAM cell MI-12T

(i) Read operation of MI-12T: Circuit set up for read operation of MI-12T is shown in Figure 5.17. Assuming that logic '0' is stored in the cell initially. Thus, internal node voltages are Q = 0 V and QB = 1 V and the access transistors (MN5 and MN6) are OFF. The transistors MP2 and MN1 are turned OFF, while the transistors MP1 and MN2 operate in linear mode. One of the transistors (MN4) in ON-OFF logic is turned ON, and transistor in the other ON-OFF logic is in the OFF state. During read operation, the bit-lines (BL/BLB) are pre-charged to V_{DD} and WL is enabled (pulsed to a high level) which turns-ON the access transistors.

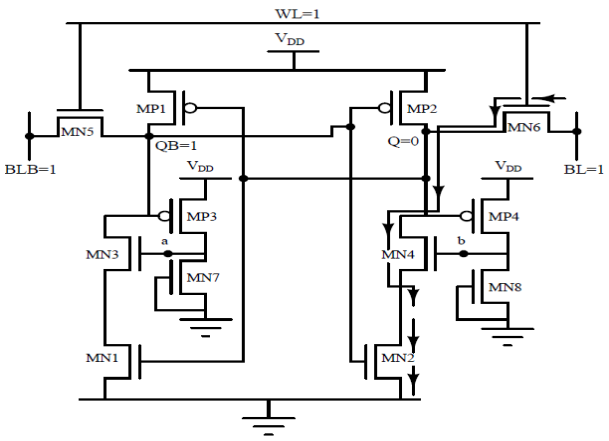


Figure 5.17: Test circuit for read operation of MI-12T

The voltage at BLB will not have a significant change in voltage level as no current flows through MN5 due to BLB & QB ='1' at both end. On the other hand, MN6, MP4, MN4 and MN2 will conduct and the voltage level of BL line will begin to drop slightly, so that a differential voltage develops between the bit-lines which are sensed by sense amplifier. The read operation would be stable provided the node voltage Q does not exceed the threshold voltage of MN1.

For proper read operation, the aspect ratios of the transistors (MN6, MN4, MN2) and (MN5, MN3, MN1) have to be computed accurately. For maximum RSNM, the CR has been obtained through simulation as 2.9.

The ON-OFF logic transistor of MN3 isolates MN1 from node QB. In the case of voltage increasing at Q (destructive read), which may cause false turn on of MN1, MN3 remains OFF as QB is high. This stops the positive feedback through the cross coupled inverter path which otherwise could cause false switch ON of the MP2 transistor and could change the stored logic '0' in the cell at Q node.

(ii) Write operation of MI-12T: Circuit set up for write operation of MI-12T is shown in Figure 5.18. Consider a write '0'operation, assuming logic'1' is stored in the SRAM cell initially. Internal node voltages are Q = '1' and QB = '0' and the access transistors (MN5 and MN6) are in off state. The transistors MP1 and MN2 are turned off, while the transistors MN1 and MP2 operate in linear mode. In ON-OFF logic pairs, transistor MN3 will be ON and MN4 will be OFF.

During write operation, the bit-line BLB is pre-charged to a high level (V_{DD}) and BL is pre-charged to low level (logic '0') . WL is enabled (pulsed to a high level) which turns on access transistors. The access transistors, MN5 and MN6, conduct causing voltages at Q & QB to decrease and increase respectively. This leads to (MN1 & MP2) turn OFF and (MN2 & MP1) to turn ON.

For successful write operation, the aspect ratios of the transistors (MN6, MP2) and (MN5, MP1) have to be computed accurately. For maximum WSNM in MI-12T, the PR has been obtained through simulation as 1.8.

Due to stack of MN4/ MN2 at Q (increased resistance of pull down path), for getting optimum CR, transistor widths need to be increased.

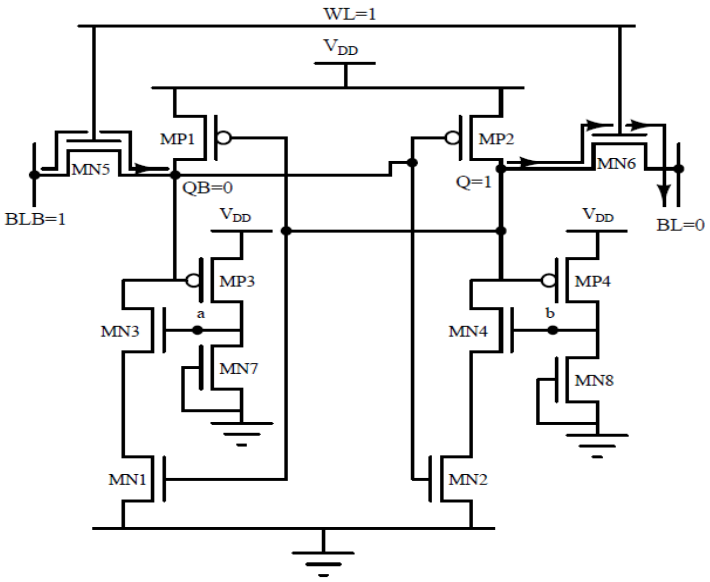


Figure 5.18: Test circuit for write operation of MI-12T

(iii) Hold operation of MI-12T: Test circuit for measurement of hold SNM of MI-12T is shown in Figure 5.19.

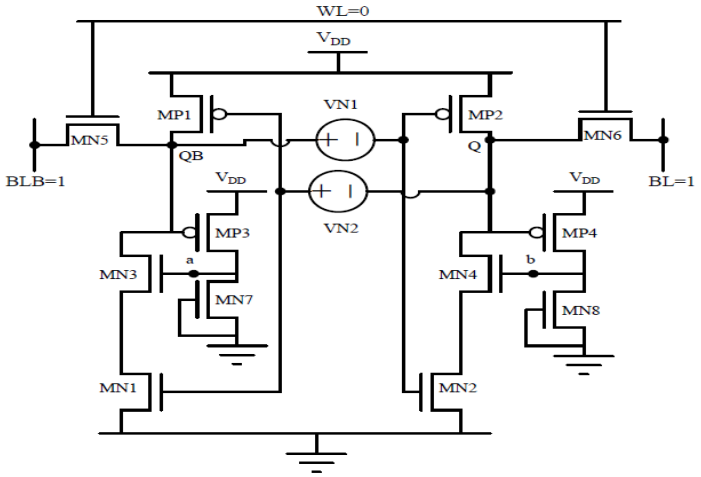


Figure 5.19: Test circuit for measurement of hold SNM of MI-12T

The hold operation is performed by disabling WL (at logic '0') , switching OFF the MN5 and MN6 access transistors and bit line pair (BL/BLB) is pre-charged to high voltage (V_{DD}). This disconnects the cell nodes QB and Q from both the bit-lines.

The ON-OFF logic forms stack of MN3 and MN1. This increase the threshold voltage of MN3 thereby reducing the OFF-state leakage current through the stacked transistor path. This reduces the rate at which charge stored at QB (or Q) leaks through this path which improves hold SNM. Figure 5.20 shows comparison of OFF state leakage current through pull down

path (MN1) of MI-12T and C6T during hold operation. The value of leakage current is less in MI-12T thereby confirming stacking effect.

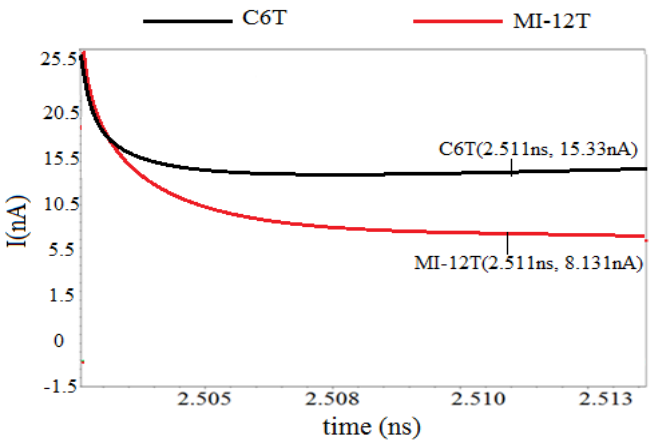


Figure 5.20: Pull down currents plot for MI-12T and C6T during hold operation

The pull up to pull down transistor ratio is critical for stability during hold operation which is here selected as 0.62. Then similar methodology is followed for calculating the hold SNM of the M8T in sub-threshold region as given in Section 5.2. Figures showing transient waveform of Q, QB during read, write, and hold mode are included in Appendix B.

III. Technique III: Modification in connection of WL signal to access transistors to generate clock feed-through effect

Section 5.3.4 discusses the two new designs where modification is done in connection of WL signal to access transistors to generate clock feed-through effect.

5.3.4. Design of Proposed M7T

The proposed M7T SRAM cell is very much similar to C6T with addition of an extra transistor. It comprises of seven transistors as shown in Figure 5.21. The internal architecture of proposed M7T consists of access transistors (MN5, MN6) and cross-coupled inverter pair (MP1/MN1) and (MP2/MN2) to store one-bit information inside the cell.

Modification: An extra PMOS transistor (MP3) whose gate terminal is controlled by WL is added. Its source and drain terminals are connected to gate of access transistors (MP5/MN6). The voltage generated by clock feed-through effect through parasitic capacitances of MP3, MN5, and MN6 is used in two ways:

- To turn ON/ OFF MN5/MN6 transistors

- To generate a negative voltage at node Q, when WL is disabled, due to clock feed through effect (through parasitic capacitances of MP3, MN5, and MN6). This negative voltage reduces the net voltage at node Q during read operation. Hence, voltage at node Q does not exceed the threshold voltage of MN1. This increases the RSNM of M7T in comparison to C6T. Similar analysis is valid for node QB.

Generation of gate voltage for MN5/MN6 transistors to turn ON/ OFF:

As MP3, does not turn off properly at 45 nm technology (as shown in Table 5.2), it always remains ON and node X and node Y gets coupled through it leading to same final voltage (either low or high) at gate terminals of MN5 and MN6.

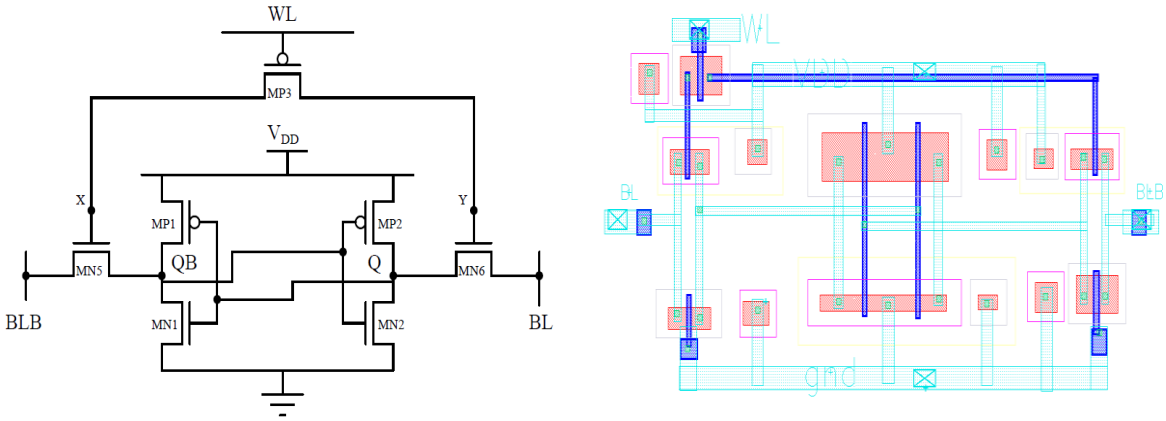


Figure 5.21: Schematic and layout of M7T

The transistor MP3 acts as a switch between the two access transistors. When WL is enabled (logic 1), the source/drain voltage of MP3 is generated due to due to clock feed-through effect through coupling of parasitic capacitances of MP3 and access transistors (MN5/MN6) as shown in Figure 5.22. Figure 5.23 shows the model of circuit, with parasitic capacitances only, for estimation of voltage node X and Y during clock feed-through event. Transistors MP1 and MN2 are modeled as closed ideal switch.

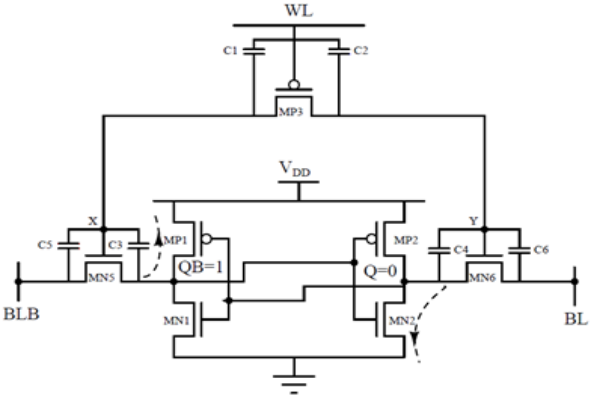


Figure 5.22: Coupling of parasitic capacitances in M7T during clock feed-through event

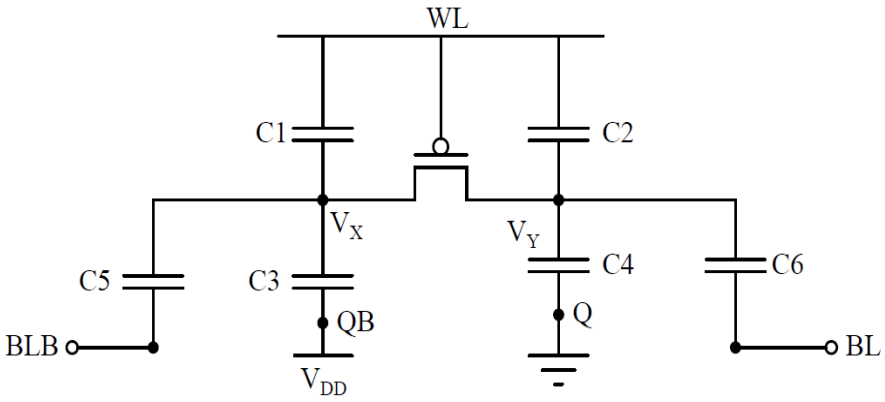


Figure 5.23: Model for estimation of voltage at node X and Y during clock feed-through event

Here

C1/C2 is the gate-source/gate-drain capacitance of MP3 (or vice versa) respectively;

C3/C5 is the gate-source/ gate-drain capacitance of MN5 respectively;

C4/C6 is the gate-source/ gate-drain capacitance of MN6 respectively;

Other capacitances show negligible values during simulation, hence they are neglected.

Read Operation: Here WL = increases from 0 to V_{DD}, BL= BLB= pre-charged to V_{DD}, Q= 0, QB=V_{DD}. Through simulation, values of parasitic capacitances are obtained as: C1 = C2 = 0.41pF, C5 = C6 = 0.0001 pF, C3= 0.002pF, and C4= 0.008 pF.

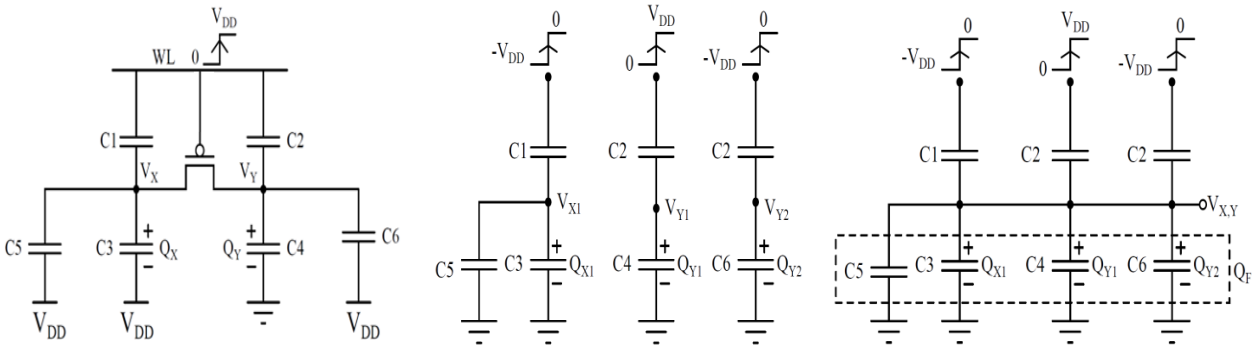


Figure 5.24: Read circuit set up for estimation of charge at different nodes during clock feed-through event

Figure 5.24 (a) shows the model of Figure 5.23 with node voltage of read operation.

Figure 5.24 (b) shows the equivalent circuit of Figure 5.24 (a) for each capacitive path shown separately for estimation of instantaneous charge stored across them.

Figure 5.24 (c) shows the equivalent circuit for estimation of voltage $V_{X,Y}$ obtained under steady state condition.

The expressions for voltage/charge at different nodes in Figure 5.24 (b) are given below:

Expression for charge Q_{X1}: Voltage V_{X1} is generated at node X1 due to clock feed-through effect through C1, C3 and C5 capacitive path.

$$V_{X1} = (V_{DD})\left(\frac{C1}{C1 + (C3 + C5)}\right)$$

Therefore, the final expression for charge Q_{X1} (=(C5+C3).V_{X1}) is define as

$$Q_{X1} = (V_{DD})(C3 + C5)\left(\frac{C1}{C1 + (C3 + C5)}\right) \quad (5.1)$$

Expression for charge Q_{Y1} : Voltage V_{Y1} is generated at node Y1 due to clock feed-through effect through C2, C4 capacitive path.

$$V_{Y1} = (V_{DD})\left(\frac{C2}{C2 + C4}\right)$$

Therefore, the final expression for charge Q_{Y1} (=C4.V_{Y1}) is define as

$$Q_{Y1} = (V_{DD})(C4)\left(\frac{C2}{C2 + C4}\right) \quad (5.2)$$

Expression for charge Q_{Y2}: Voltage V_{Y2} is generated at node Y2 due to clock feed-through effect through C2, C6 capacitive path.

$$V_{Y2} = (V_{DD})\left(\frac{C2}{C2 + C6}\right)$$

Therefore, the expression for charge Q_{Y2} (=C6.V_{Y2}) is define as

$$Q_{Y2} = (V_{DD})(C6)\left(\frac{C2}{C2 + C6}\right) \quad (5.3)$$

From Figure 5.24 (c), the expression of final charge (Q_F) is obtained as :

$$Q_F = (V_{X,Y})(C3 + C4 + C5 + C6)$$

Final steady state voltage $V_{X,Y}$ (=V_X =V_Y) using charge conservation theorem when MP3 is on (modeled as closed switch)

$$Q_F = Q_{X1} + Q_{Y1} + Q_{Y2}$$

$$V_{X,Y} = \frac{(Q_{X1} + Q_{Y1} + Q_{Y2})}{C3 + C4 + C5 + C6} \tag{5.4}$$

Write Operation: Here, WL= increases from 0 to V_{DD}, BL= 0, BLB=V_{DD}, Q= V_{DD}, QB=0. Through simulation, values of parasitic capacitances are obtained as: C1 = C2 =0.0062pF, C5 = C6= 0.0001pF, C3=0.002pF and C4=0.008pF.

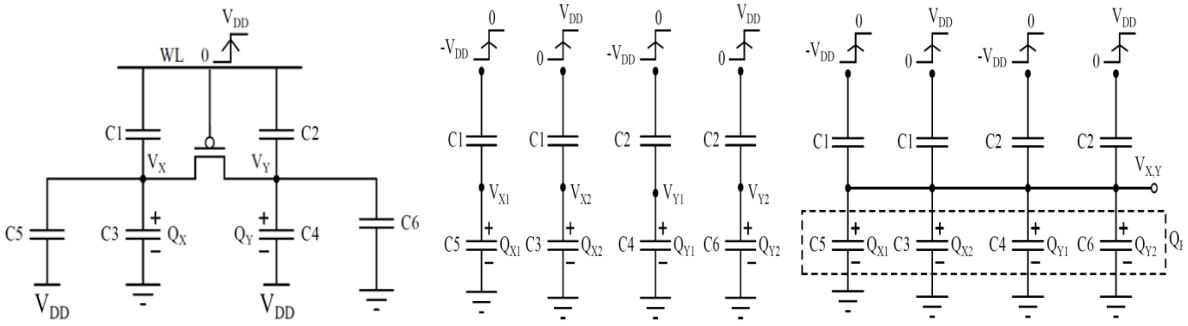


Figure 5.25: Write circuit set up for estimation of charge at different nodes during clock feed-through event

Figure 5.25 (a) shows the model of Figure 5.23 with node voltage of write operation.

Figure 5.25 (b) shows the equivalent circuit of Figure 5.25 (a) for each capacitive path shown separately for estimation of instantaneous charge stored across them.

Figure 5.25 (c) shows the equivalent circuit for estimation of voltage $V_{X,Y}$ obtained under steady state condition.

The expressions for voltage/charge at different nodes in Figure 5.25 (b) is given below:

Expression for voltage Q_{X1}: Voltage V_{X1} generated due to clock feed-through effect through C1, C5 capacitive path

$$V_{X1} = (V_{DD})\left(\frac{C1}{C5 + C1}\right)$$

Therefore, the final expression for charge Q_{X1} (=C5.V_{X1}) is define as

$$Q_{X1} = (V_{DD})(C5)\left(\frac{C1}{C5 + C1}\right) \tag{5.5}$$

Expression for voltage Q_{X2}: Voltage V_{X2} generated due to clock feed-through effect through C1, C3 capacitive path

$$V_{X2} = (V_{DD})\left(\frac{C1}{C1+C3}\right)$$

Therefore, the final expression for charge Q_{X1} (=C3.V_{X2}) is define as

$$Q_{X2} = (V_{DD})(C3)\left(\frac{C1}{C1+C3}\right) \tag{5.6}$$

Expression for charge Q_{Y1} : Voltage V_{Y1} is generated at node Y1 due to clock feed-through effect through C2 and C4 capacitive path.

$$V_{Y1} = (V_{DD})\left(\frac{C2}{C2+C4}\right)$$

Therefore, the final expression for charge Q_{Y1} (=C4.V_{Y1}) is define as

$$Q_{Y1} = (V_{DD})(C4)\left(\frac{C2}{C2+C4}\right) \tag{5.7}$$

Expression for charge Q_{Y2}: Voltage V_{Y2} is generated at node Y2 due to clock feed-through effect through C2 and C6 capacitive path.

$$V_{Y2} = (V_{DD})\left(\frac{C2}{C2+C6}\right)$$

Therefore, the final expression for charge Q_{Y2} (=C6.V_{Y2}) is define as

$$Q_{Y2} = (V_{DD})(C6)\left(\frac{C2}{C2+C6}\right) \tag{5.8}$$

From Figure 5.25(c), the expression of final charge (Q_F) is obtained as :

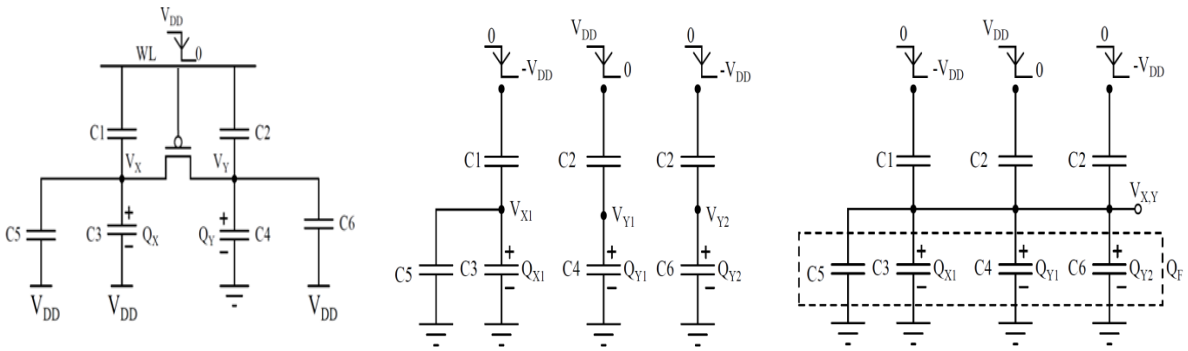
$$Q_F = (V_{X,Y})(C3+C4+C5+C6)$$

Final steady state voltage $V_{X,Y}$ (=V_X =V_Y) using charge conservation theorem when MP3 is on (modeled as closed switch)

$$Q_F = Q_{X1} + Q_{Y1} + Q_{Y2}$$

$$V_{X,Y} = \frac{(Q_{X1} + Q_{Y1} + Q_{Y2})}{C3+C4+C5+C6} \tag{5.9}$$

Hold Operation: Here, WL=decreases from V_{DD} to 0, BL= V_{DD}, BLB=V_{DD}, Q= 0, QB=V_{DD}. Through simulation, values of parasitic capacitances are obtained as: C1= C2 =0.41pF, C5 = C6= 0.001pF, C3=0.002pF and C4=0.008pF.



(a) (b) (c)

Figure 5.26: Hold circuit set up for estimation of charge at different nodes during clock feed-through event

Figure 5.26 (a) shows the model of Figure 5.23 with node voltage of hold operation.

Figure 5.26 (b) shows the equivalent circuit of Figure 5.26 (a) for each capacitive path shown separately for estimation of instantaneous charge stored across them.

Figure 5.26 (c) shows the equivalent circuit for estimation of voltage $V_{X,Y}$ obtained under steady state condition.

The expressions for voltage/charge at different nodes in Figure 5.26 (b) is given below:

Expression for voltage Q_{X1}: Voltage V_{X1} generated due to clock feed-through effect through C1, C3 and C5 capacitive path

$$V_{X1} = (-V_{DD})\left(\frac{C1}{C1 + (C5 + C3)}\right)$$

Therefore, the final expression for charge Q_{X1} (=(C5+C3).V_{X1}) is define as

$$Q_{X1} = (-V_{DD})(C3 + C5)\left(\frac{C1}{C1 + (C3 + C5)}\right) \qquad (5.10)$$

Expression for charge Q_{Y1} : Voltage V_{Y1} is generated at node Y1 due to clock feed-through effect through C2 and C4 capacitive path.

$$V_{Y1} = (-V_{DD})\left(\frac{C2}{C2 + C4}\right)$$

Therefore, the final expression for charge Q_{Y1} (=C4.V_{Y1}) is define as

$$Q_{Y1} = (-V_{DD})(C4)\left(\frac{C2}{C2 + C4}\right) \qquad (5.11)$$

Expression for charge Q_{Y2}: Voltage V_{Y2} is generated at node Y2 due to clock feed-through effect through C2 and C6 capacitive path.

$$V_{Y2} = (-V_{DD})\left(\frac{C2}{C2+C6}\right)$$

Therefore, the final expression for charge Q_{Y2} (=C6.V_{Y2}) is define as

$$Q_{Y2} = (-V_{DD})(C6)\left(\frac{C2}{C2+C6}\right) \quad (5.12)$$

From Figure 5.26(c), the expression of final charge (Q_F) is obtained as :

$$Q_F = (V_{X,Y})(C3+C4+C5+C6)$$

Final steady state voltage $V_{X,Y}$ (=V_X =V_Y) using charge conservation theorem when MP3 is on (modeled as closed switch)

$$Q_F = Q_{X1} + Q_{Y1} + Q_{Y2}$$

$$V_{X,Y} = \frac{(Q_{X1} + Q_{Y1} + Q_{Y2})}{C3+C4+C5+C6} \quad (5.13)$$

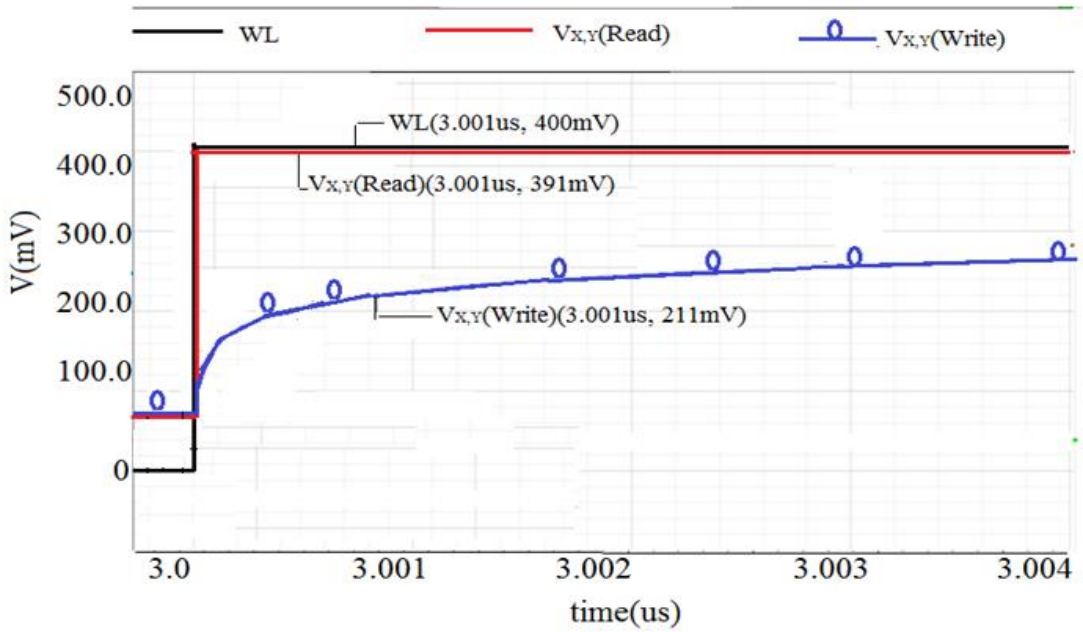
Therefore, the final gate voltage develops at access transistors (MN5/MN6), when PMOS is enabled:

The estimated values of voltages at node X and node Y, using equations (5.1) - (5.13), in read, writes and hold operation is given in Table 5.3. The results show close matching between estimated and simulated values. This confirms the proposition that access transistors function properly in M7T.

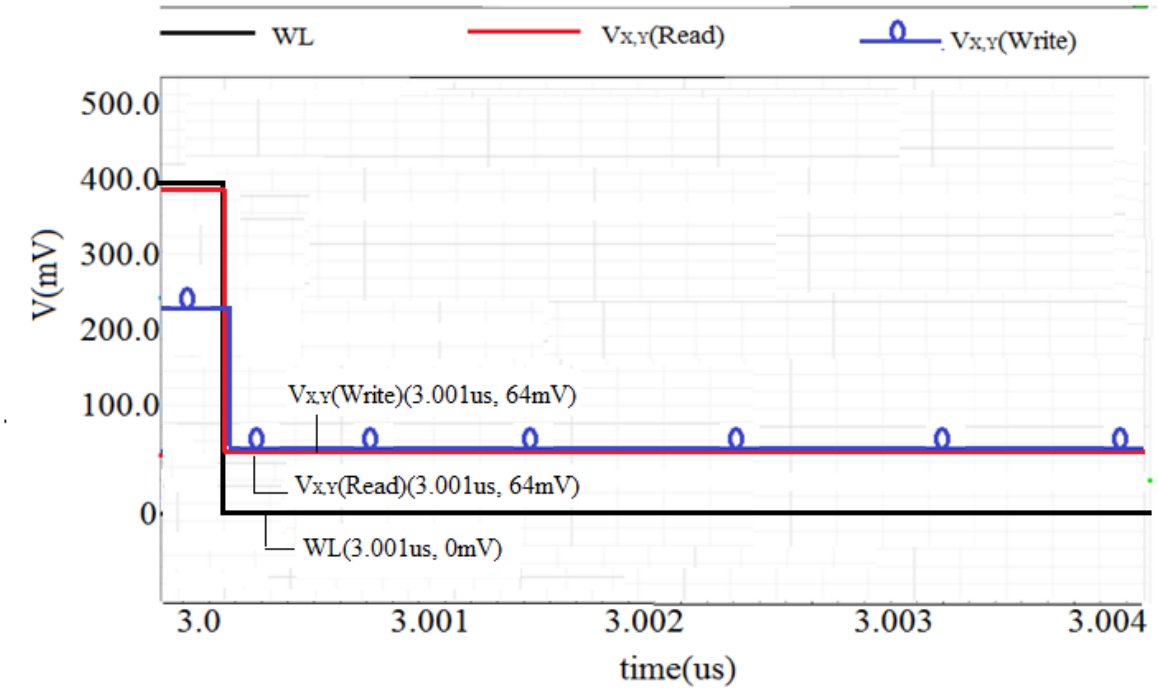
Table 5.3: Generation of Voltages at node X and node Y in write, read, and hold operation

WL	**State of MP3** (as per Table 5.2)	**Simulated values**	**Estimated value through expressions (5.1)-(5.13)**
		$V_{X,Y}$ (write/ read) (in V)	**$V_{X,Y}$ (in V)**
ON (Logic '1') Write/ Read Operation MN3 = MN5 = ON	MP3 = ON	0.211/ 0.391	0.203/ 0.374
OFF (Logic '0') Hold Operation MN3 = MN5= OFF	MP3 = ON	0.064	-0.374

Figure 5.27 shows the transient waveforms at nodes X and Y obtained through simulations.



(a)



(b)

Figure 5.27: Waveforms at nodes X and Y during (a) read/ write (b) hold operation

(i) Read operation of M7T: Circuit set up for read operation of M7T is shown in Figure 5.28. Assuming that logic '0' is stored in the cell initially. Thus, internal node voltages are Q = 0 V and QB = 1 V before the access transistors (MN5 and MN6) are turned ON. The

transistors MP2 and MN1 are turned OFF, while the transistors MP1 and MN2 operate in linear mode. During read operation, the bit-lines (BL/BLB) are pre-charged to V_{DD} and WL is enabled (pulsed to a high level) which turns-ON MP3 (it does not turn off properly due to faulty operation). The access transistors then turn ON due to their gate voltage generated through clock feed through effect.

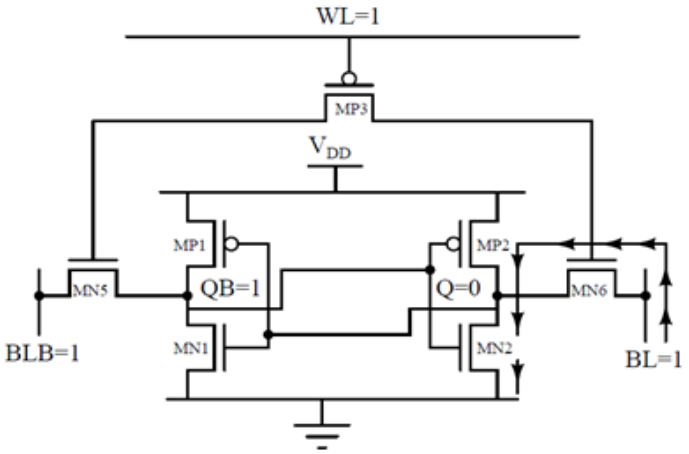


Figure 5.28: Test circuit for read operation of M7T

The voltage at BLB will not have a significant change in voltage as no current flows through MN5 due to BLB & QB ='1' at both end. On the other hand, transistors MN6 and MN2 conduct and the voltage level of BL line will begin to drop slightly, so that a differential voltage develops between the bit-lines which are sensed by sense amplifier. During this process, the voltage at Q/QB nodes falls to '0'/ rises to '1' respectively.

Here clock feed through effect helps in stability of stored data. Because of clock feed through effect through parasitic capacitances, a negative transient voltage is developed at node Q which reduces the net voltage at node Q thereby decreasing its probability to exceed the threshold voltage of MN1. This increases the RSNM of M7T. For successful read operation, the node voltage at Q should remain below the threshold voltage of MN1 to prevent false turn ON of transistor MN1.

For maximum RSNM, the CR has been obtained through simulation as 2.2.

Figure 5.29 shows the transient waveforms at nodes Q and QB obtained through simulation. The figure shows that net voltage at Q and QB node in M7T is less than corresponding value in C6T.

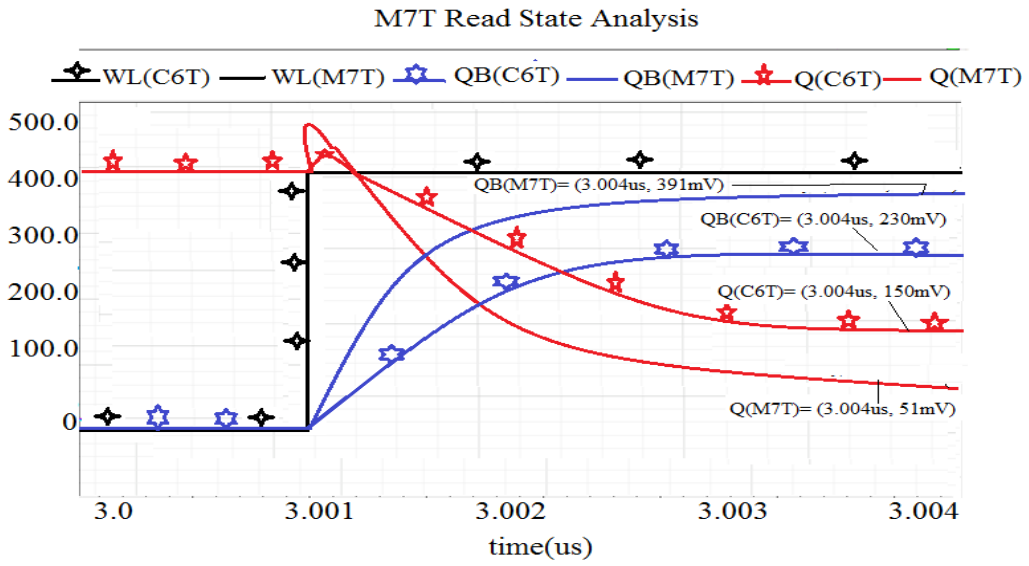


Figure 5.29: Waveforms at nodes Q and QB during read mode

(ii) Write operation of M7T: Circuit set up for write operation of M7T is shown in Figure 5.30. Consider a write '0' operation at node Q. Thus, internal node voltages are Q = '1' and QB = '0' before WL is enabled (i.e. pulsed to a high level). The transistors MP1 and MN2 are turned OFF, while the transistors MN1 and MP2 operate in linear mode.

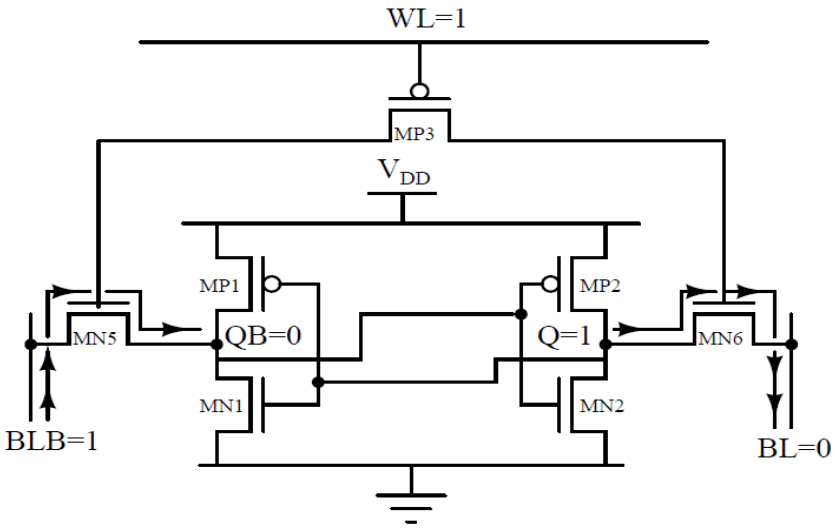


Figure 5.30: Test circuit for write operation of M7T

During write operation, the bit-lines BLB is pre-charged to a high level (V_{DD}) and BL is pulled down to low level (logic '0'), WL is enabled which turns-on the PMOS transistor (MP3 does not turn off properly due to faulty operation) as well as the access transistors MN5 and MN6. After the pass transistors MN5 and MN6 are switched ON, the voltage at node QB should not

rise above the threshold voltage of MN2 to change the stored information i.e. forcing node Q =’0’ and QB =’1’.

For successful write ‘0’ operation, the node voltage Q discharges through MN6 to a low voltage below the threshold voltage of MN1.

In addition to setting aspect ratio, clock feed through effect also helps in ensuring node voltage Q to remain below the threshold voltage of MN1. Because of clock feed through effect through parasitic capacitances, a negative transient voltage is developed at node Q which reduces the net voltage at node Q thereby decreasing its probability to exceed the threshold voltage of MN1. This increases the WSNM of M7T.

The critical part of the circuit is the voltage divider formed by the pull up and access transistor. So, PR is an important parameter in write mode. For maximum WSNM, the PR has been obtained through simulation as 2.1.

Figure 5.31 shows the transient waveforms at nodes Q and QB obtained through simulation. The figure shows that net voltage at Q and QB node in M7T is less than corresponding value in C6T.

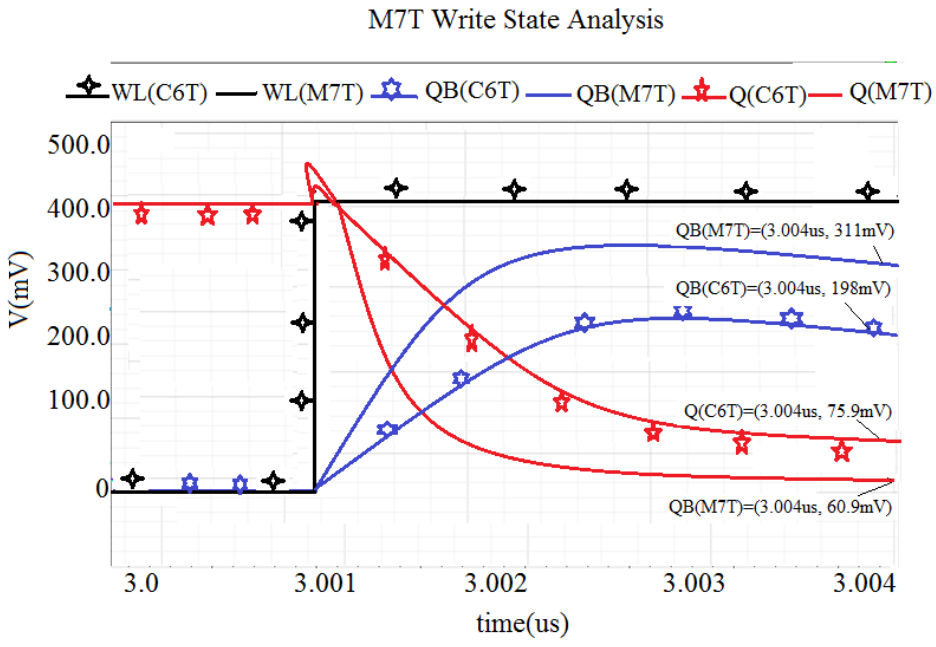


Figure 5.31: Waveforms at nodes Q and QB during write mode

(iii) Hold Operation of M7T: Conceptual test circuit for measuring the hold SNM of M7T is shown in Figure 5.32.

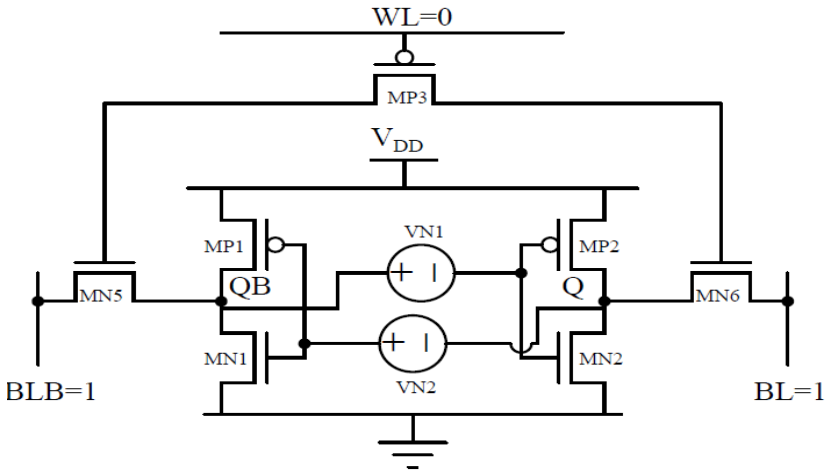


Figure 5.32: Test circuit for measurement of hold SNM of M7T

During hold operation, WL is disabled (goes low), and MP3 turns ON. Voltages at node X and node Y decreases to 0 V due to clock feed-through effect through parasitic capacitances of MP3, MP5, and MN6. This switches OFF the MN5 and MN6 access transistors. Bit line pair (BL/BLB) is pre-charged to high voltage (V_{DD}). This disconnects the cell nodes QB and Q from both the bit-lines.

The pull up to pull down transistor ratio is critical for stability during hold operation which is here selected as 0.95. Then similar methodology is followed for calculating the hold SNM of the M7T in sub-threshold region as given in Section 5.2.

Figure 5.33 shows the transient waveforms at nodes Q and QB obtained through simulations. The figure shows that net voltage at Q / QB node in M7T is less/ more than corresponding value in C6T.

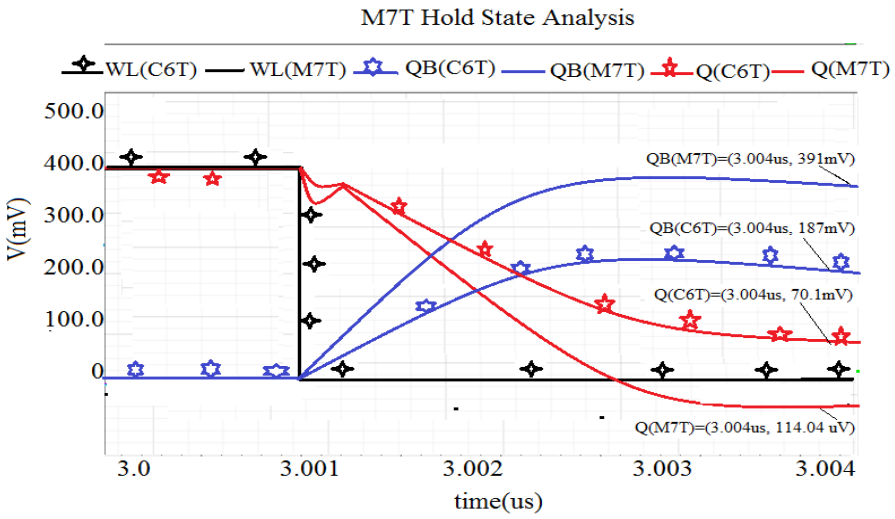


Figure 5.33: Waveforms at nodes Q and QB during hold mode

5.3.5. DESIGN OF PROPOSED M9T

The proposed M9T SRAM cell comprises of nine transistors as shown in Figure 5.34. This design is the modified version of TG-based fully differential 8T SRAM bit cell [32]. The internal architecture of this cell consists of cross-coupled inverter pair (MP1/MN1 and MP2/MN2) with NN-parallel type access transistor i.e. MN5-MN3 (or MN6-MN4) to store one bit information.

As explained in Section 5.3.4, an extra PMOS transistor (MP3) whose gate terminal is controlled by WL is added. Its source and drain terminals are connected to gate of access transistors (MP5/MN6). The voltage generated by clock feed-through effect through parasitic capacitances of MP3, MN5, and MN6 is used to turn ON/ OFF MN5/MN6 transistors and to generate a negative voltage at node Q, when WL is disabled, due to clock feed through effect (through parasitic capacitances of MP3, MN5, and MN6).

Modification: The access transistors are implemented with NN parallel type access transistor combination (i.e. MN5/MN3 and MN6/MN4). The ON/ OFF operation of (MN5, MN6) is controlled by an extra added PMOS transistor (MP3). For CR and PR calculation, aspect ratio of additional transistor (i.e. either MN3 or MN4) in each configuration is kept constant at (W/L) = 65nm/45nm=1.4.

The same design methodology is followed for designing the M9T in sub-threshold region as for configuration M7T given in Section 5.3.4.

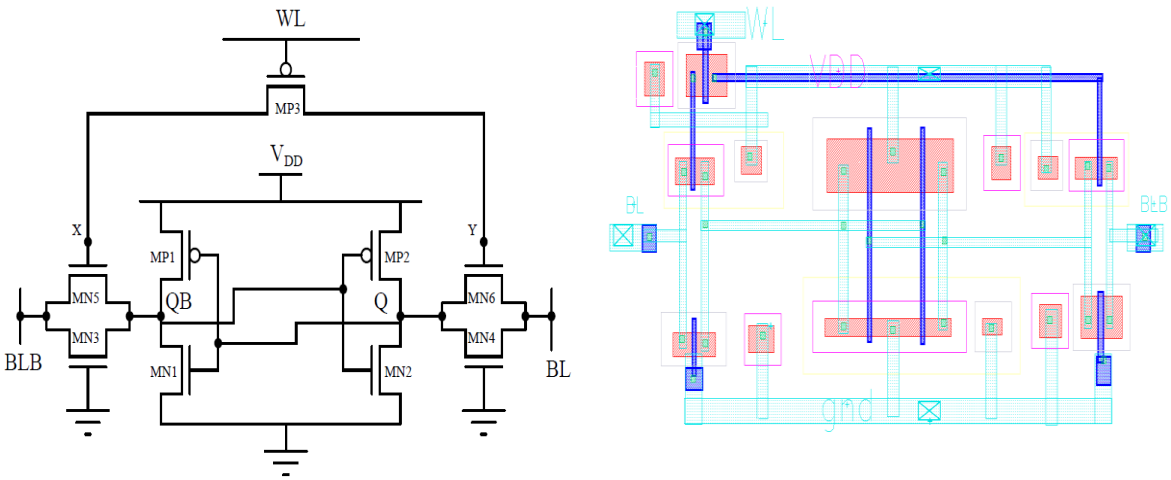


Figure 5.34: Schematic and layout of M9T

(i) Read operation of M9T: Circuit set up for read operation of M9T is shown in Figure 5.35. Assuming that logic '0' is stored in the cell initially. Thus, internal node voltages are Q = 0 V and QB = 1 V before the access transistors (MN5 and MN6) are turned ON. The

transistors MP2 and MN1 are turned OFF, while the transistors MP1 and MN2 operate in linear mode. The additional two NMOS transistors (MN3 and MN4) operate in cut off region (OFF state).

During read operation, the bit-lines (BL/BLB) are pre-charged to V_{DD} and WL is enabled (pulsed to a high level) which turns-ON MP3 (it does not turn off properly due to faulty operation). The access transistors then turn ON due to their gate voltage generated through clock feed through effect.

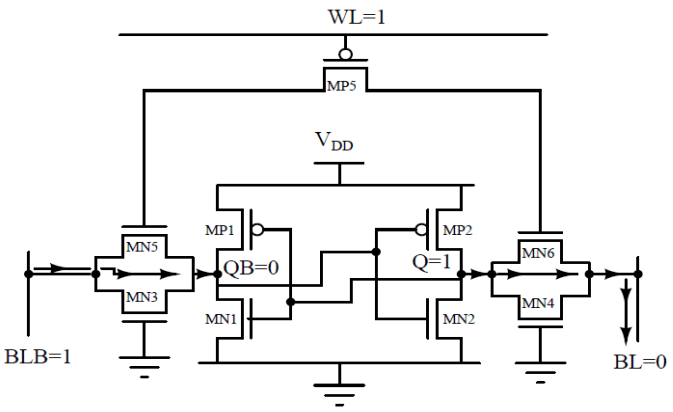


Figure 5.35: Test circuit for read operation of M9T

The voltage at BLB will not have a significant change in voltage as no current flows through MN5 due to BLB & QB ='1' at both end. On the other hand, transistors MN6 and MN2 conduct and the voltage level of BL line will begin to drop slightly, so that a differential voltage develops between the bit-lines which are sensed by sense amplifier. Here clock feed through effect helps in stability of stored data. Because of clock feed through effect through parasitic capacitances, a negative transient voltage is developed at node Q which reduces the net voltage at node Q thereby decreasing its probability to exceed the threshold voltage of MN1

Thus, CR is the critical parameter of the SRAM cell during the read operation. For maximum RSNM, the CR has been obtained through simulation as 2.9.

(ii) Write operation of M9T: Circuit set up for write operation of M9T is shown in Figure 5.36. The node voltage QB always remains below the threshold voltage of MN2, since MN1 and MN5 are designed according to CR ratio. So, it is not sufficient to turn ON MN2. To change the stored information, i.e. to force QB = V_{DD}, the node voltage at Q must be reduced below the threshold voltage of MN1 to turn it OFF. So, consider a write '0' operation at node Q. Thus, internal node voltages are Q = '1' and QB = '0' before WL is enabled (i.e. pulsed to a high level). The transistors MP1 and MN2 are turned OFF, while the transistors MN1 and MP2 operate in linear mode.

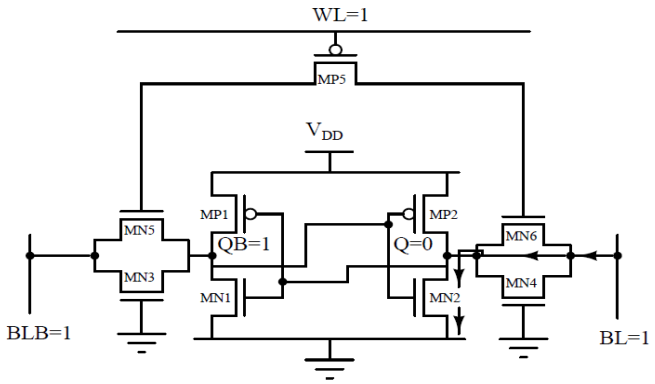


Figure 5.36: Test circuit for write operation of M9T

During write operation, the bit-lines BLB is pre-charged to a high level (V_{DD}) and BL is pulled down to low level (logic '0'), WL is enabled which turns-on the PMOS transistor (MP3 does not turn off properly due to faulty operation) as well as the access transistors MN5 and MN6. For successful write '0' operation, the node voltage Q discharges through MN6 to a low voltage below the threshold voltage of MN1.

In addition to setting aspect ratio, clock feed through effect also helps in ensuring node voltage Q to remain below the threshold voltage of MN1. Because of clock feed through effect through parasitic capacitances, a negative transient voltage is developed at node Q which reduces the net voltage at node Q thereby decreasing its probability to exceed the threshold voltage of MN1. This increases the WSNM of M9T. For maximum WSNM, the PR has been obtained through simulation as 2.3.

(iii) Hold Operation of M9T: Test circuit for measurement of hold SNM of M9T is shown in Figure 5.37.

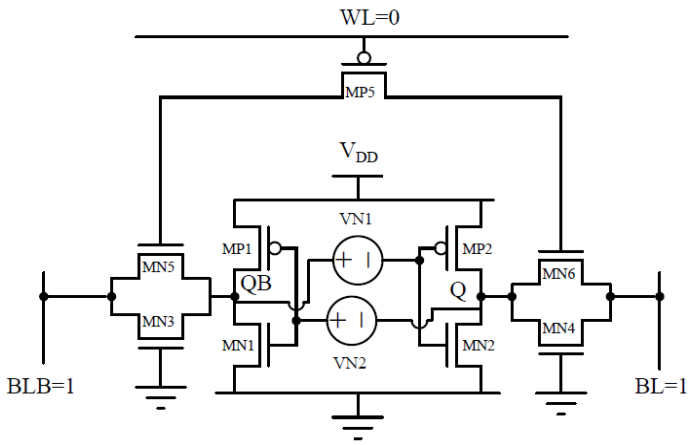


Figure 5.37: Test circuit for measurement of hold SNM of M9T

The hold operation is performed by lowering WL to logic '0', switching OFF the MN5 and MN6 access transistors and bit line pair (BL/BLB) is at high voltage. This disconnects the cell nodes QB and Q from both the bit-lines. The pull up to pull down transistor ratio is critical for stability during hold operation which is here selected as 0.79. Then similar methodology is followed for calculating the hold SNM of the M9T in sub-threshold region as given in Section 5.2.

5.4. SIMULATION RESULTS AND DISCUSSION AT 45 nm

Static noise margin metrics have long been the standard for measuring stability and estimating the yield of SRAM arrays. However, in nanometer technologies, under scaled supply voltages, these traditional metrics are no longer sufficient. Alternatively, cell stability based on the N-curve uses additional performance metrics like static voltage noise margin (SVNM), static current noise margin (SINM), write trip current (WTI), write trip voltage (WTV) to overcome some of the limitations of static noise margin metrics [36].

However, dynamic stability metrics [47] which capture the inherent dynamic behavior of SRAM cell and access operations have not been considered in present work for stability analysis of SRAM cells. Further this work does not focus on stability degradation of SRAM cell due to process variation. Hence these issues are included in the future scope of this chapter.

This section presents comparative analysis of proposed SRAM cells using design metrics like Hold SNM, RSNM, WSNM, SINM, SVNM, WTI, WTV, read access time (T_{RA}), and write access time (T_{RA}**),** leakage Power Consumption of the C6T, M7T, MPT8T, M8T, M9T and MI-12T SRAM cells. Impacts of process variations is studied in terms of mean and standard deviation of read delay and write delay for C6T and the proposed SRAM cells. These design metrics are estimated using 45 nm technology libraries in sub-threshold region.

Simulation setup:

The butterfly curves of SNM during hold, read/write mode, and NCM curves are extracted among the data stored through simulations using MATLAB script for both C6T and proposed SRAM cells.

Monte Carlo analysis was performed on both C6T and the proposed SRAM cells to find the mean and standard deviation of read and write delay only. For Monte Carlo simulation, we have created a design file which includes device models for 45 nm technology that are assigned statistically varying parameter values.

In Monte Carlo (MC) simulation set up, the V_{th} is assumed to have independent Gaussian distributions with ±3 sigma (σ) variation of 30%. Expected variation in V_{DD} is 10% in the future technology generations such as 45 nm, hence, design metrics (read and write delay) are measured by varying the supply voltage by ±10% around the nominal V_{DD} of 0.4 V [32]. Design metrics in this work are estimated with 1500 MC run at 25 ˚C temperatures to achieve high accuracy for all process corners. The simulation set-up has been performed in Cadence ADE XL window using statistical (.scs) files.

5.4.1. SRAM Standby Stability Analysis (Hold Stability)

The primary metric in nano-scale SRAM design is stability (data retention in the cell) which is analyzed by computing SNM in hold mode. Hold SNM is the smaller of the two squares that can be fitted between the SRAM cell dc voltage transfers characteristics (VTCs) with the WL disabled. A higher SNM indicates better stability of the cell (discussed in Section 5.2). Figure 5.38 shows combined 'butterfly curve' (i.e. VTC's) of C6T, M7T, MPT8T, M8T and M9T during hold operation.

The five curves are overlapped into each other as expected since cross coupled inverter pair designs are same for all these SRAM cells.

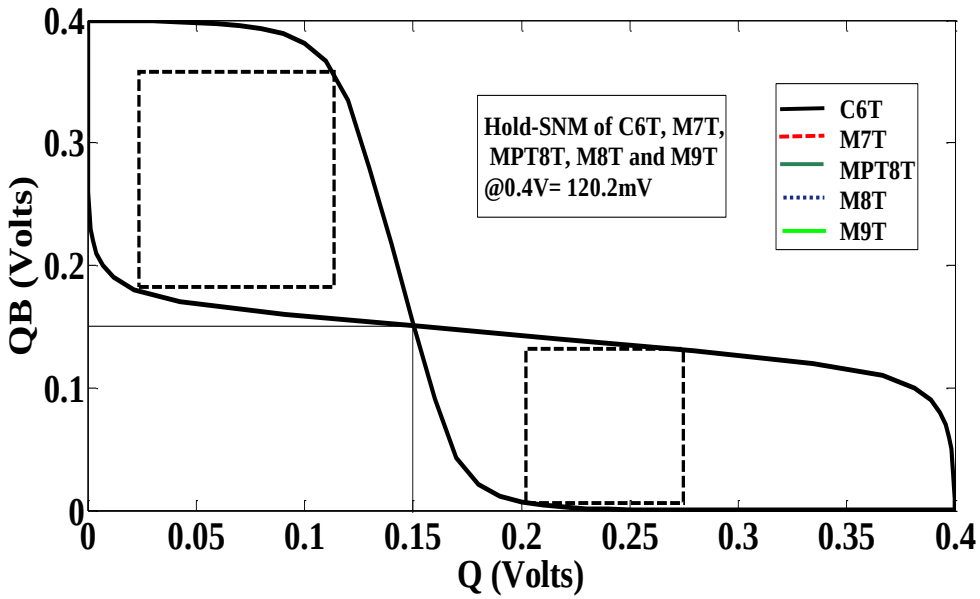


Figure 5.38: Overlapped VTC's of C6T, M7T, MPT8T, M8T and M9T during hold operation

SNM of C6T, M7T, MPT8T, M8T and M9T in hold mode is 120.2mV at nominal supply voltage of V_{DD} = 0.4V. It is observed that there are three intersection points of the hold state

VTC (VQ, VQB) = (0.4, 0) V, (0, 0.4) V, and (0.150, 0.150) V. The stable states are corresponding to intersection points (0.4, 0) V and (0, 0.4) V, whereas the cell's state corresponding to (0.150, 0.150) V is unstable.

The hold SNM for all (C6T, M7T, MPT8T, M8T and M9T) are 120.2 mV, minimum of side of the two largest squares that can be fitted inside the lobes of the "butterfly" curve [33]) indicating that all designs are equally stable in hold mode.

In proposed MI-12T, the modification has been done in the cross-couple inverter pair (see Figure 5.16). Therefore, the hold SNM is evaluated separately and is found to be more as compared to others.

Figure 5.39 shows the VTC of MI-12T. SNM of MI-12T is 170 mV at nominal supply voltage of V_{DD} = 0.4V.

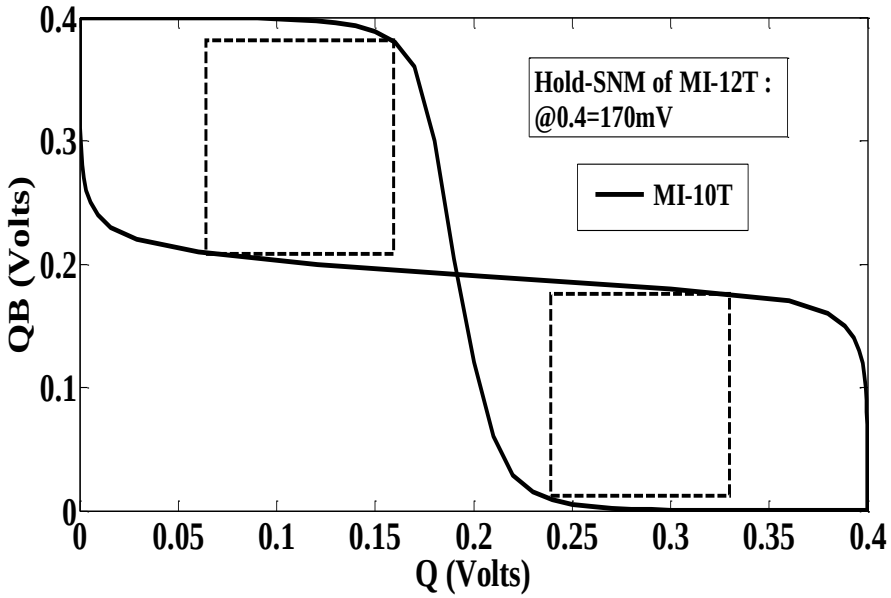


Figure 5.39: VTC of MI-12T during hold operation

Effect of variation in Supply Voltage on Hold Stability:

Figure 5.40 shows VTC's of C6T, M7T, MPT8T, M8T and M9T during hold operation, on same axis, at V_{DD} varying form 0.4 V to 0.2 V.

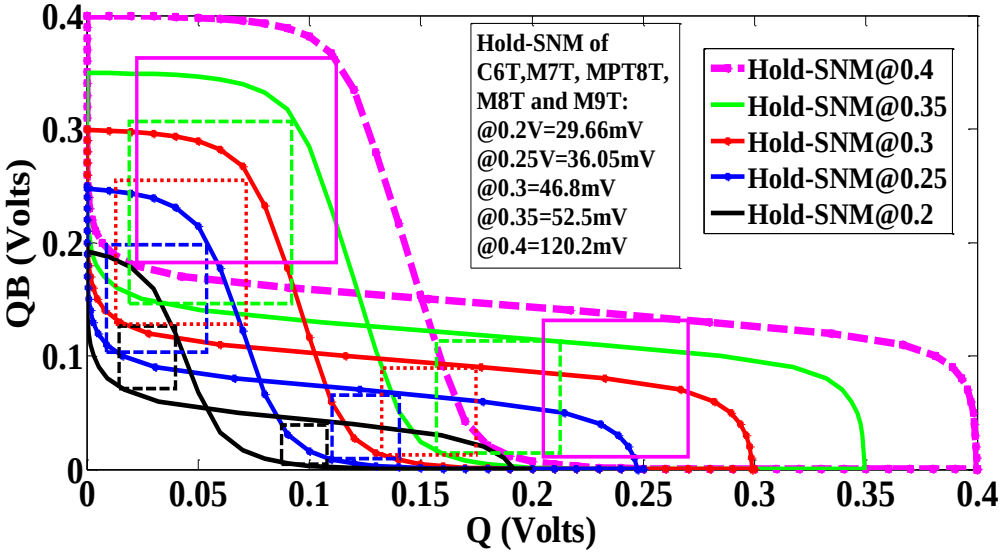


Figure 5.40: Combined VTC's of C6T, M7T, MPT8T, M8T and M9T during hold operation at varying V_{DD}

Figure 5.41 shows VTC's of MI-12T during hold operation at varying V_{DD} form 0.4 V to 0.2 V.

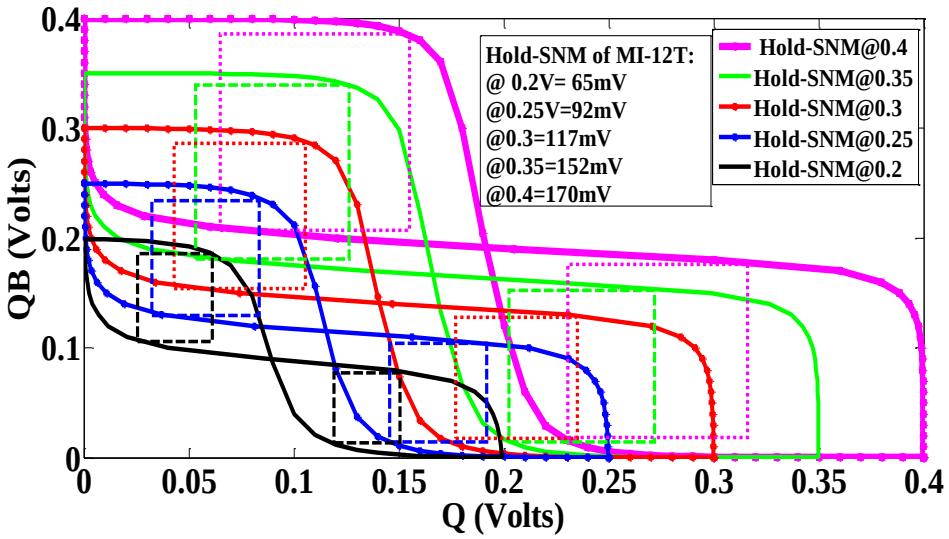


Figure 5.41: VTC's of MI-12T during hold operation at varying V_{DD}

From the Figure 5.40 and Figure 5.41**,** it is observed that all SRAM cells are able to hold the stored information down to 0.2 V power supply voltage although reduction in supply voltage leads to reduction in hold SNM.

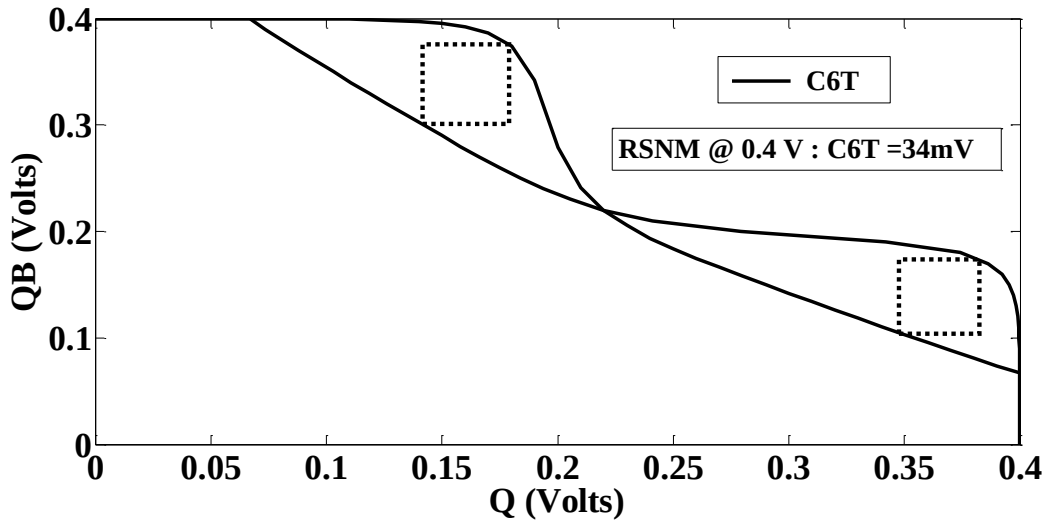
Also, the proposed MI-12T cell exhibits (2.09×) improvements in average hold SNM as compared to C6T, M7T, MPT8T, M8T and M9T cells due to reduced leakage current because of stacked pull down path.

5.4.2. SRAM Read Stability Analysis

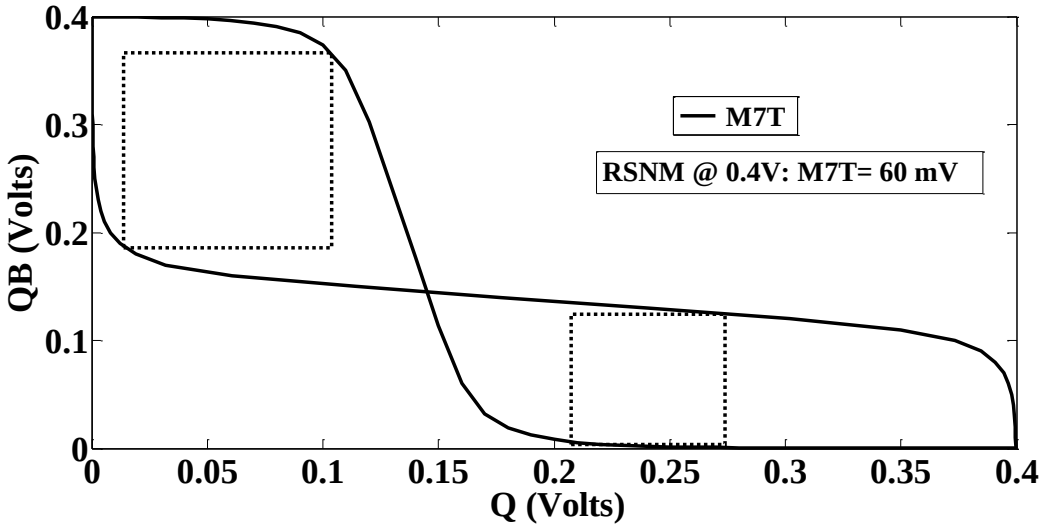
Read stability, analyzed by RSNM, is an important design metric of SRAM cell. Measurements of RSNM is carried out in a similar fashion as done for hold SNM with BL/BLB pre-charged to V_{DD} and WL is biased in enable state (discussed in Section 5.2 and 5.3).

RSNM is the smaller of the two squares that can be fitted between the SRAM cell dc voltage transfers characteristics (VTCs) with the WL enabled.

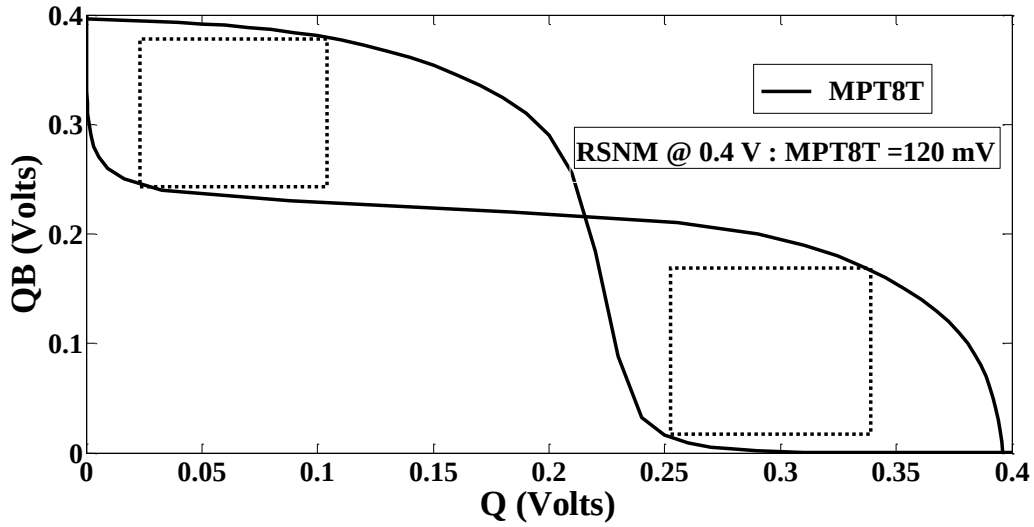
Figure 5.42 represents RSNM 'butterfly curve' for C6T, M7T, MPT8T, M8T, M9T and MI-12T SRAM cells.



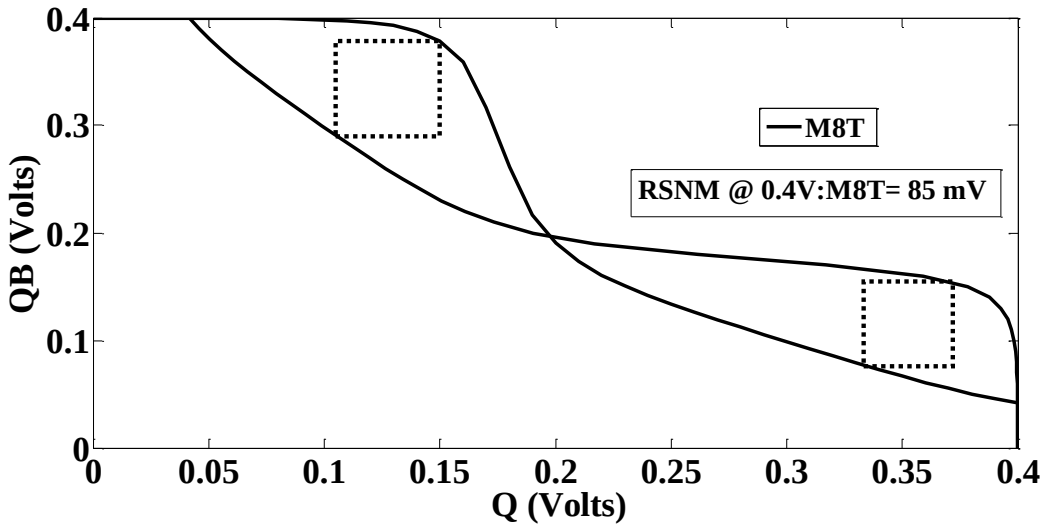
(a)



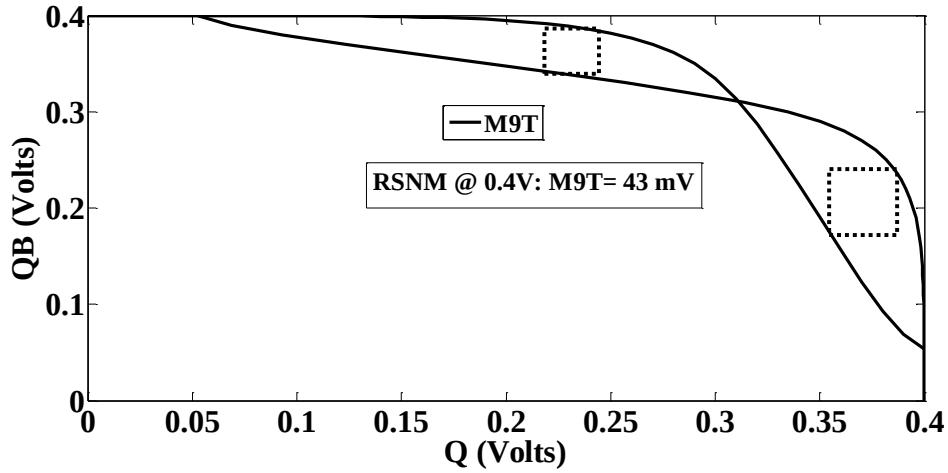
(b)


MPT8T
RSNM @ 0.4 V : MPT8T =120 mV
QB (Volts)
Q (Volts)
0.4
0.3
0.2
0.1
0
0.05
0.15
0.25
0.35

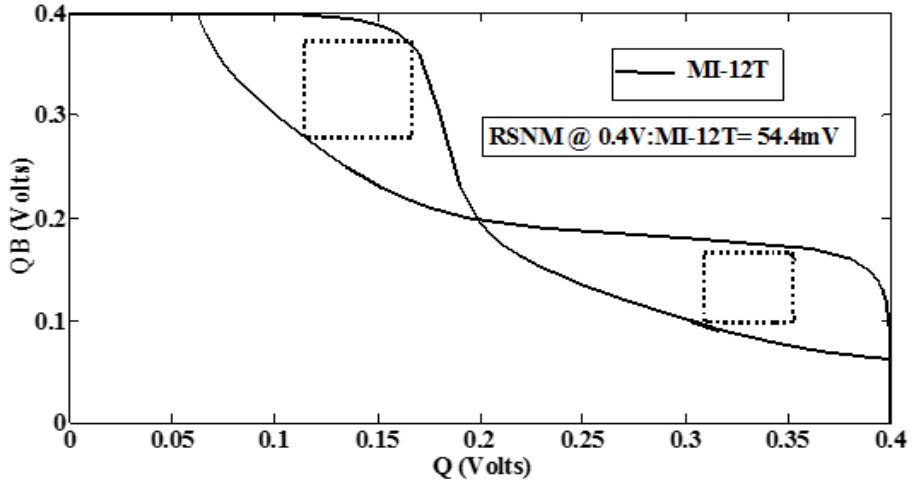
(c)


M8T
RSNM @ 0.4V:M8T= 85 mV
QB (Volts)
Q (Volts)
0.4
0.3
0.2
0.1
0
0.05
0.15
0.25
0.35

(d)


M9T
RSNM @ 0.4V: M9T= 43 mV
QB (Volts)
Q (Volts)
0.4
0.3
0.2
0.1
0
0.05
0.15
0.25
0.35

(e)



(f)

Figure 5.42: RSNM 'butterfly curve' of (a) C6T (b) M7T (c) MPT8T (d) M8T (e) M9T (f) MI-12T

From the Figure 5.42 and Table 5.4, it is observed that the proposed SRAM cells have higher RSNM as compared to the C6T.

Since the M7T, MPT8T, M8T, M9T and MI-12T consume more area compared to the C6T, it is worthwhile to compare these cells under 'iso-area' condition. For iso-area condition, the CR in the C6T is increased for all SRAM cells i.e. M7T, MPT8T, M8T, M9T and MI-12T so as to have same area to analyze the impact of increasing CR value.

Table 5.4 also shows the comparative analysis of RSNM under iso-area condition. Results show that RSNM of all proposed SRAM cells and C6T show only marginal increment with increased CR value which are in confirmation with the result published in [34].

Table 5.4: Comparative analysis of RSNM, at 0.4V

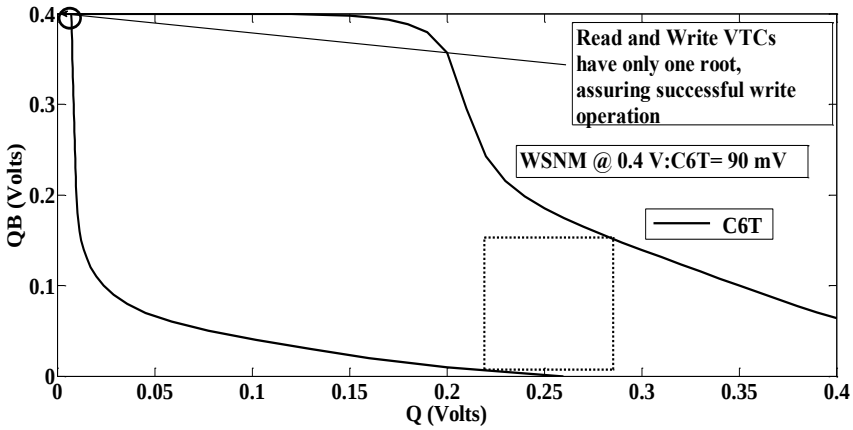
Types of SRAM cells	**RSNM (mV)**	**% Increment w.r.t. C6T**	**Layout Area (μm^2)**	**RSNM(mV) For Iso (Layout) Area = 7.705 μm^2**
C6T	034.0	--	**3.824**	37.0
M7T	060.0	43.33%	4.874	67.0
MPT8T	**120.0**	**71.60%**	5.986	123.0
M8T	085.0	60.00%	6.281	88.0
M9T	043.0	20.93%	6.634	49.0
MI-12T	054.4	37.50%	7.705	54.4

5.4.3. SRAM Write Ability Analysis

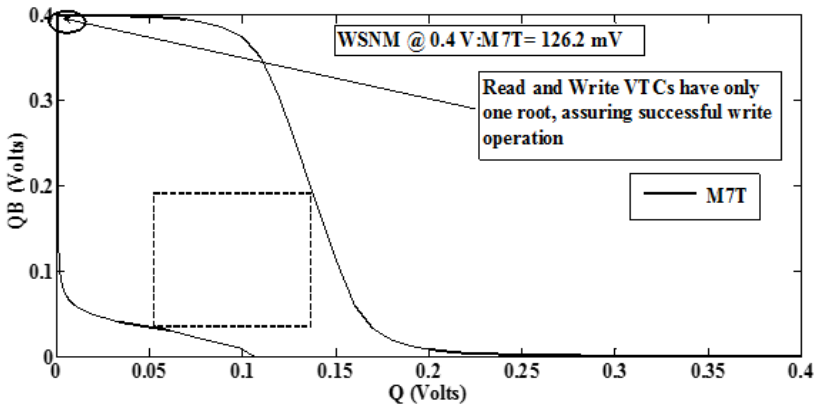
Write ability, analyzed by WSNM, is the minimum voltage necessary to drive the bit cell into a mono-stable state during a write '0' operation. Measurement of WSNM is carried out with BL/BLB line at '0'/ '1' (or vice versa) and WL of the cell is enabled (logic '1' as discussed in Section 5.2). During write operation, the bit-line pair directly connects to the node Q and QB and forces the nodes Q and QB (the stored information) to obtain required voltage levels. On completion of change in state, WL signal is asserted low, and cross coupled inverter pair stores the written one-bit information. WSNM is defined as the minimum bit-line dc voltage below V_{DD} needed to write the opposite value into the cell [35]. For a successful write, only one cross point should be found on the butterfly curves, indicating that the cell is mono-stable.

WSNM for writing '1' is the width of the smallest square that can be nested between the Write '0' and Write '1' static characteristics. A cell with lower WSNM implies poor write ability of SRAM cell.

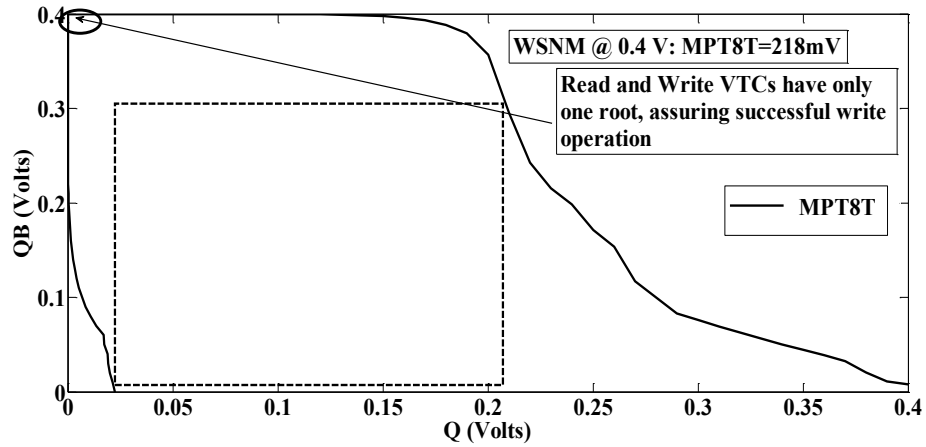
Figure 5.43 shows estimation of WSNM from VTC curves of both inverters (of cross coupled inverter pair of SRAM cell) for of C6T, M7T, MPT8T, M8T, M9T and MI-12T SRAM cells.



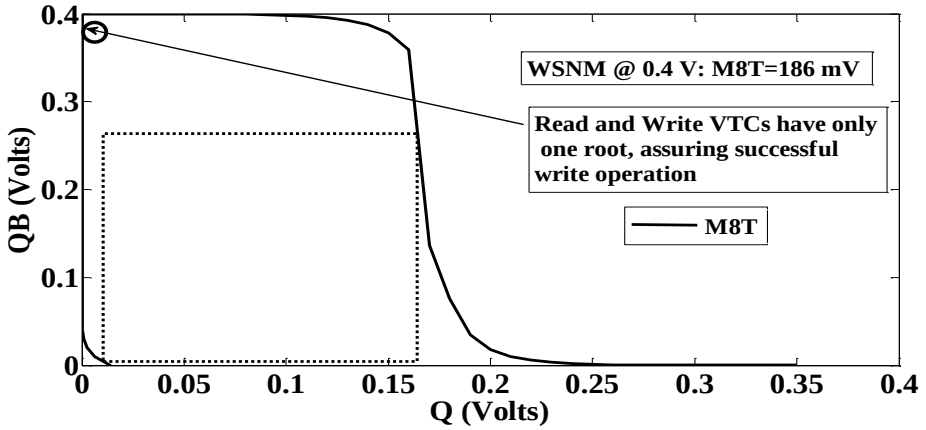
(a)



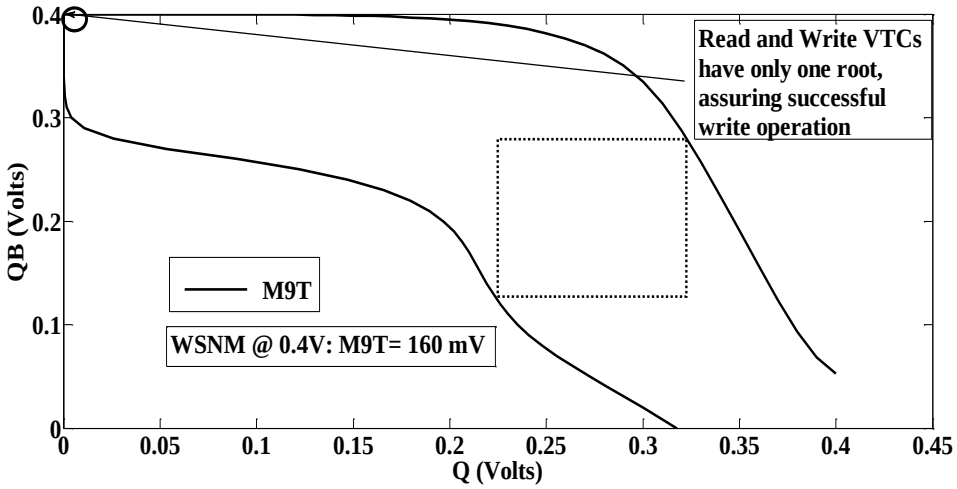
(b)


WSNM @ 0.4 V: MPT8T=218mV
Read and Write VTCs have only one root, assuring successful write operation
MPT8T
QB (Volts)
Q (Volts)
0
0.1
0.2
0.3
0.4
0.05
0.15
0.25
0.35

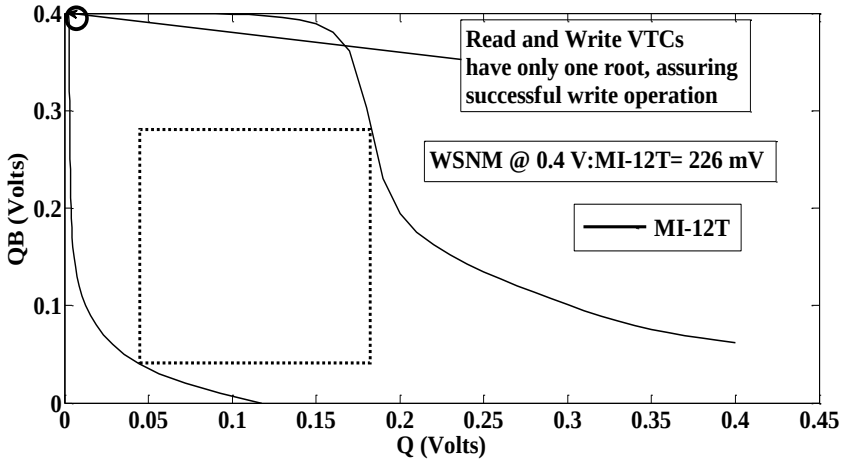
(c)


WSNM @ 0.4 V: M8T=186 mV
Read and Write VTCs have only one root, assuring successful write operation
M8T
QB (Volts)
Q (Volts)
0
0.1
0.2
0.3
0.4
0.05
0.15
0.25
0.35

(d)


Read and Write VTCs have only one root, assuring successful write operation
M9T
WSNM @ 0.4V: M9T= 160 mV
QB (Volts)
Q (Volts)
0
0.1
0.2
0.3
0.4
0.05
0.15
0.25
0.35
0.45

(e)



(f)

Figure 5.43: WSNM 'butterfly curve' of (a) C6T (b) M7T (c) MPT8T (d) M8T (e) M9T (f) MI-12T

As observed from Figure 5.43, there is only one intersection point found on the butterfly curves of VTC curves for all SRAM cells.

This indicates the single stable point which signifies the successful write operation and functionality of the cross coupled inverters of the cell as mono-stable circuit.

Table 5.5 shows the comparative analysis of WSNM for all SRAM cells given above; it is observed that the proposed SRAM cells have higher WSNM as compared to the C6T.

Table 5.5: Comparative analysis of WSNM of all SRAM cells, at 0.4V

Types of SRAM cells	**WSNM (mV)**	**% Increment w.r.t. C6T**
C6T	090.0	--
M7T	126.2	28.6%
MPT8T	218.0	58.7%
M8T	186.0	51.6%
M9T	160.0	43.7%
MI-12T	**226.0**	**60.1%**

5.4.4. ALTERNATIVE NOISE MARGINS

Analysis based on N-curve metrics (NCM) of the cell is used for the further evaluation of robustness of the SRAM cell in terms of additional performance parameters like; SVNM, SINM, WTV, and WTI. N-curve contains information both on the read stability and on the write ability, thus allowing a complete functional analysis of the SRAM cell with only one N-curve. [36]

Figure 5.44 shows the test circuit for extracting NCM of C6T during read mode. Bit-line pair is pre-charged to V_{DD}, WL is pre-charged at logic '1' (ON state), QB ='0', and Q='1' for the NCM analysis [37].

An external voltage source (V_{IN}) is applied at the input storage node 'QB'. V_{IN} is swept from 0 V to V_{DD} and corresponding input current (I_{IN}) produces the NCM characteristics.

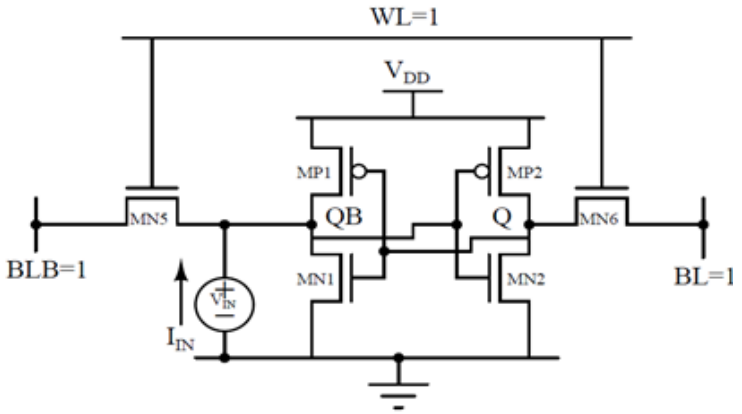
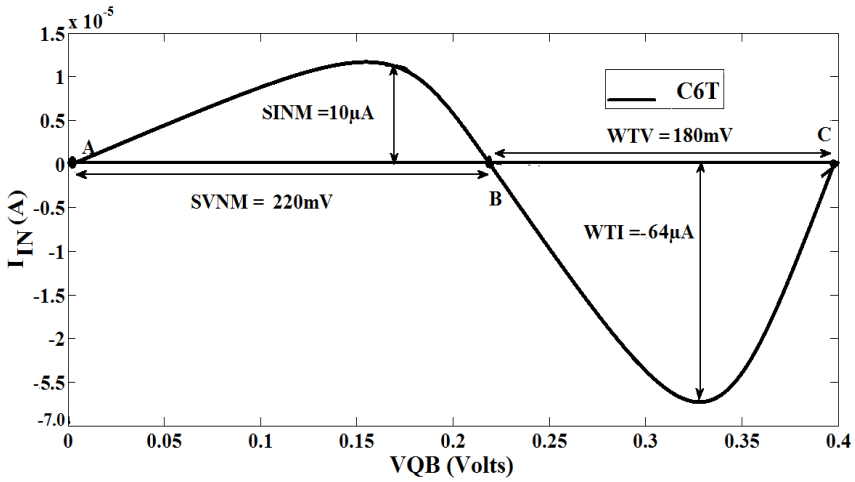
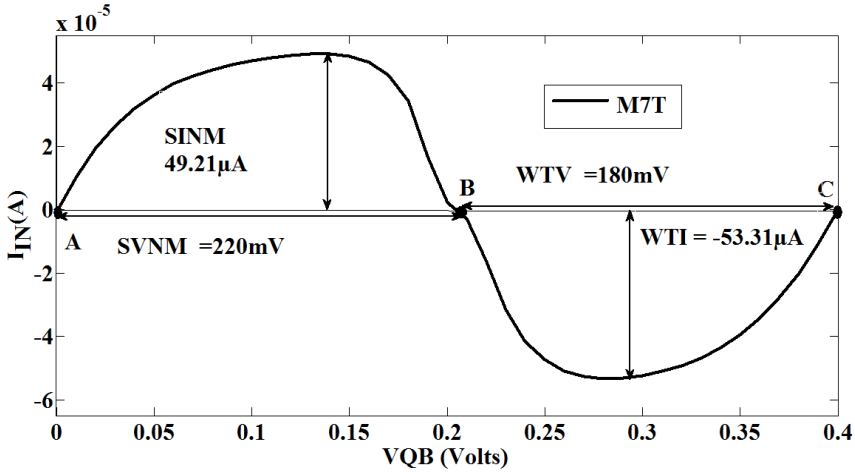


Figure 5.44: Test circuit for extracting N-curve of C6T during read mode

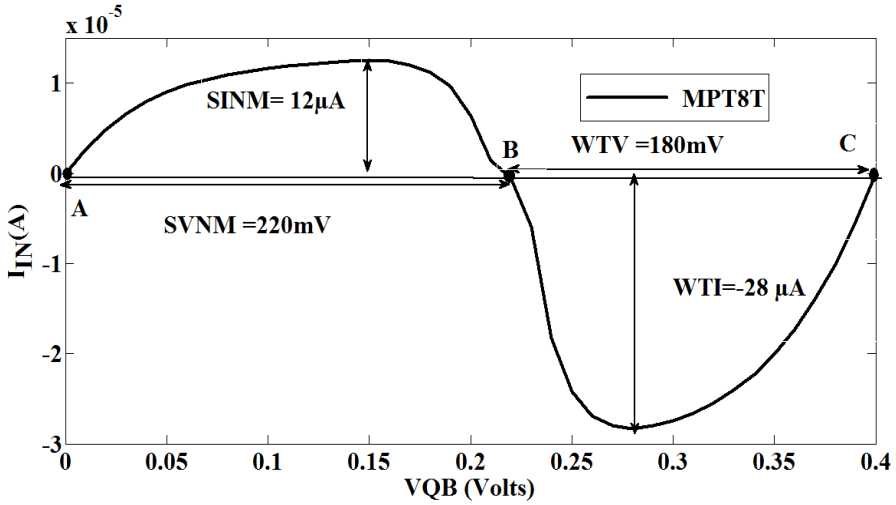
Figure 5.45 shows the NCM characteristics of C6T, M7T, MPT8T, M8T, M9T and MI-12T respectively.



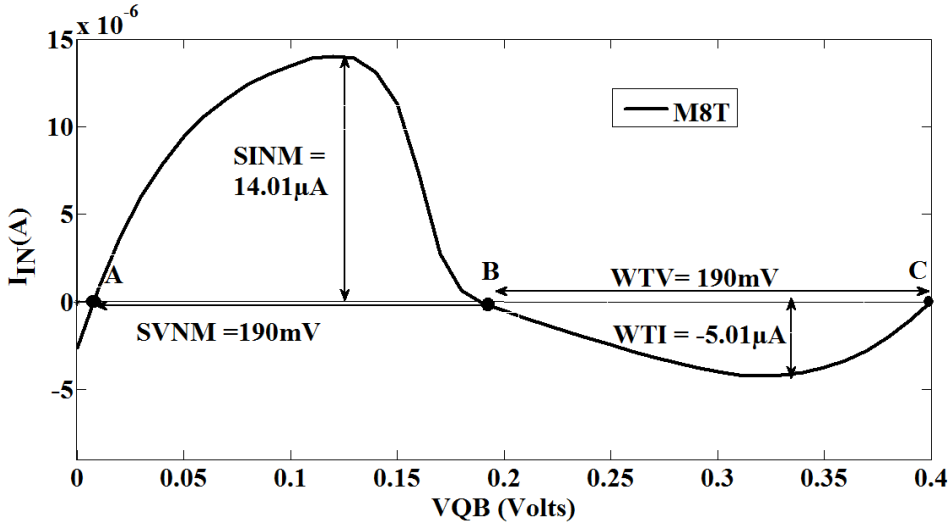
(a)


x 10^-5
M7T
SINM
49.21µA
WTV =180mV
B
C
A
SVNM =220mV
WTI = -53.31µA
I_IN(A)
VQB (Volts)

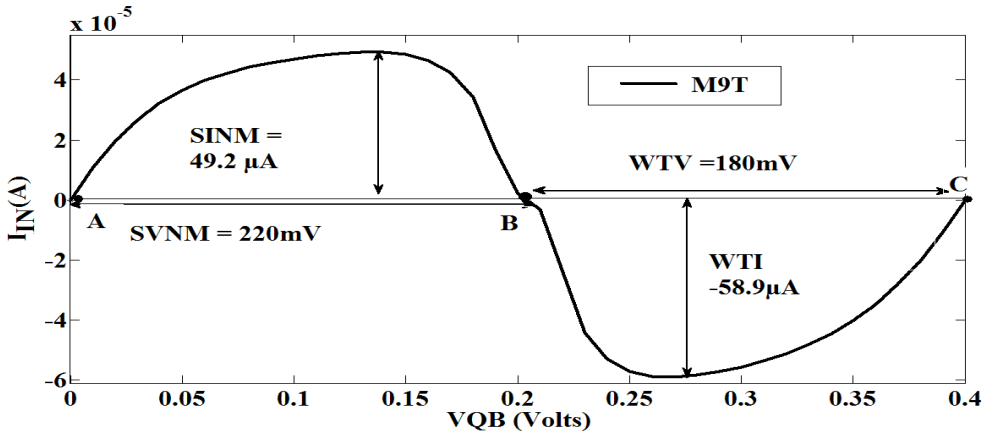
(b)


x 10^-5
MPT8T
SINM= 12µA
B
WTV =180mV
C
A
SVNM =220mV
WTI=-28 µA
I_IN(A)
VQB (Volts)

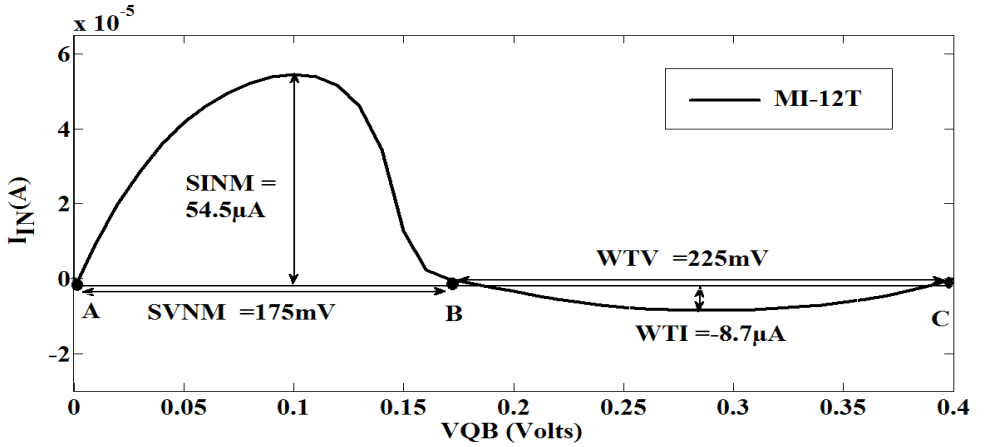
(c)


x 10^-6
M8T
SINM =
14.01µA
A
B
WTV= 190mV
C
SVNM =190mV
WTI = -5.01µA
I_IN(A)
VQB (Volts)

(d)



(e)



(f)

Figure 5.45: N-curve characteristics of (a) C6T (b) M7T (c) MPT8T (d) M8T (e) M9T (f) MI-12T

The curve is analyzed at the three points (A, B and C), where it crosses zero. Point A and C are the two stable points, while B is a meta-stable point.

The voltage in A is determined by the pull down (MN2) to access transistor (MN6) ratio or cell ratio CR.

The voltage in B is related to the pull down (MN2) to pull up (MP2) ratio and access transistor (MN6) of the cell.

The voltage in C is defined by the pull up (MP2) to access transistor (MN6) ratio or the pull up ratio (PR) of the cell.

The performance metrics SVNM, SINM and WTI are defined as:

- SVNM: The voltage difference between A and B gives SVNM which indicates the maximum tolerable dc noise voltage at the internal node 'QB'. When points A and B coincide, the cell is at the edge of stability and a destructive read can easily occur.

- SINM: The positive peak current between A and B indicates the stability of the cell, characterized as SINM which indicates the maximum injected dc current in the SRAM cell required to flip the content.
- WTI: The third metrics WTI is the amount of current needed to write the cell when both bit-lines are kept at V_{DD}. The negative current peak between point B and C gives WTI. This is the current margin of the cell for which its content changes.
- WTV: The voltage difference between point C and B. WTV is the voltage drop needed to flip the internal node '1' of the cell with both the bit-lines clamped at $V_{DD.}$

Table 5.6 shows the comparative analysis of SVNM, SINM and WTI for all SRAM cells. It is observed that that the proposed SRAM cells have higher SINM and WTI values (thus more robust) as compared to the C6T.

Table 5.6: Comparative analysis of SVNM, SINM, WTI and WTV at 0.4V

Types of SRAM cells	**SVNM(mV)**		**SINM (µA)**		**WTI (µA)**		**WTV (mV)**	
	Values	**% Decrement w.r.t. C6T**	**Values**	**% Increment w.r.t. C6T**	**|Values|**	**% Decrement w.r.t. C6T**	**Values**	**% Increment w.r.t. C6T**
C6T	**220**	--	10.00	--	64.00	--	**180**	--
M7T	**220**	0%	49.21	79.6%	53.31	16.7%	**180**	0%
MPT8T	**220**	0%	12.00	16.6%	28.00	56.2%	**180**	0%
M8T	190	13.6%	14.01	28.6%	**05.01**	92.1%	190	5.2%
M9T	**220**	0%	49.20	79.6%	58.90	07.9%	**180**	0%
MI-12T	175	20.4%	**54.50**	81.6%	08.70	86.4%	225	20%

Table 5.7 and Table 5.8 show the comparison of WTV, WTI with WSNM and comparison of SVNM, SINM, with RSNM respectively.

Table 5.7: Comparison of WTV, WTI with WSNM

Types of SRAM cells	**|WTI| (µA)**	**WTV (mV)**	**WSNM (mV)**
C6T	64.00	**180**	090.0
M7T	53.31	**180**	126.2
MPT8T	28.00	**180**	218.0
M8T	**05.01**	190	186.0
M9T	58.90	**180**	160.0
MI-12T	08.70	225	**226.0**

Performance order from best to worst:

WSNM in decreasing order: MI-12T > MPT8T > M8T > M9T > M7T > C6T

WTI in increasing order: M8T < MI-12T << MPT8T < M7T < M9T < C6T

WTV in increasing order: MPT8T = M7T= M9T = C6T < M8T< MI-12T

Table 5.8: Comparison of SVNM, SINM, with RSNM

Types of SRAM cells	SVNM (mV)	SINM (µA)	RSNM (mV)
C6T	**220**	10.00	37.0
M7T	**220**	49.21	60.0
MPT8T	**220**	12.00	**123.0**
M8T	190	14.01	88.0
M9T	**220**	49.20	43.0
MI-12T	175	**54.50**	54.4

Performance order from best to worst:

RSNM in decreasing order: MPT8T > M8T > M7T > MI-12T > M9T > C6T

SINM in decreasing order: MI-12T> M7T= M9T >>M8T > MPT8T > C6T

SVNM in decreasing order: C6T= M7T = MPT8T=M9T > M8T >MI-12T

5.4.5. Read Access Time (T_{RA}) with Variability

Read delay or T_{RA} is measured from the point when WL reaches to its 50% point from its initial low level to the point when bit line differential voltage is developed from its initial high level.

The designed architecture of sense amplifier can detect the differential voltage greater than equal to 50 mV between bit-line pair (BL and BLB) without generating any read error [38] for sub-micron technology. Standard deviation is a measure that is used to quantify the amount of variation (or dispersion) of a set of data values.

A low standard deviation indicates that the data points tend to be close to the average value of the data, while a high standard deviation indicates that the data points are spread out over a wider range of values.

Variability is defined as standard deviation (σ) to mean (µ) ratio of a design metric. In this section, variability is calculated for read (& write) access time for varying supply voltages.

Figure 5.46 show the read delay and its variability of C6T, M7T, MPT8T, M8T, M9T and MI-12T at varying supply voltage from 0.2 V to 0.4V.

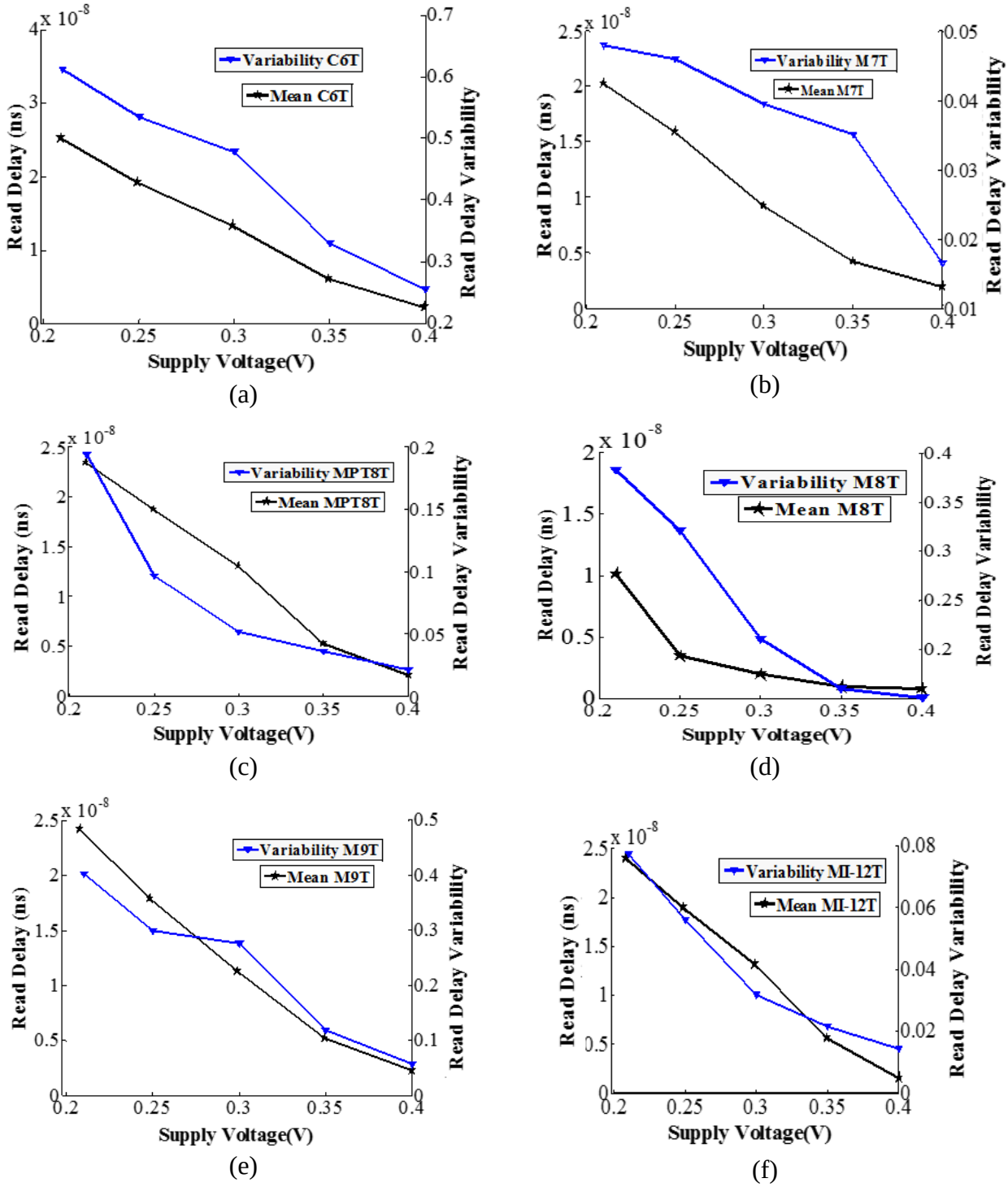


Figure 5.46. Read delay and its variability of (a) C6T (b) M7T (c) MPT8T (d) M8T (e) M9T (f) MI-12T

From the Figure 5.46, it is observed that the M7T, MPT8T, M8T, M9T and MI-12T have less range of variability around mean value at supply voltage varying from 0.2 V to 0.4 V as compared to C6T.

Table 5.9 shows the comparative analysis of average read delay and its variability for all proposed SRAM cells with C6T. Where σ is standard deviation and μ is the mean value of the read delay.

Average read delay in increasing order: M8T<<M7T< M9T< MPT8T< MI-12T< C6T

For M7T, read delay value is 3× more than M8T.

Read delay its and variability reduces with reduction in power supply voltage.

Table 5.9: Comparative analysis of read delay and its variability for all proposed SRAM cells with C6T

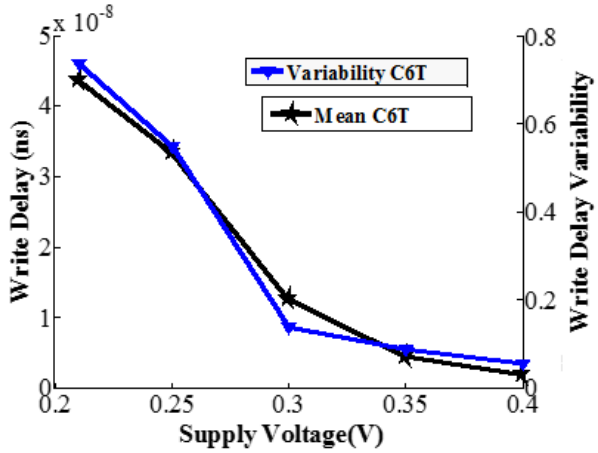
Types of SRAM cells	**Average READ delay [T_{RA} (ns)]**		**Variability (σ/μ)**
	Values	**% decrement w.r.t. C6T**	**Range (for V_{DD} varying from 0.2V to 0.4V)**
C6T	13.20	--	0.25 to 0.61
M7T	11.00	16.6%	**0.01 to 0.04**
MPT8T	12.50	05.3%	0.02 to 0.19
M8T	03.45	**73.8%**	0.15 to 0.38
M9T	12.20	07.5%	0.05 to 0.40
MI-12T	12.60	04.5%	0.01 to 0.07

5.4.6. Write Access Time (T_{WA}) with Variability

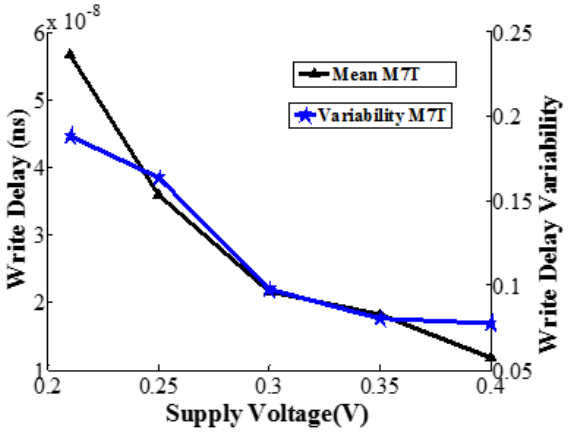
Write delay is the estimated time required to flip the cell contents at WL='1' during write operation. It is measured as the time required for writing '0' or '1' at storage nodes, when WL reaches 50% of its full swing (from its initial low level) to the point when storage nodes falls or rises to 10% or 90% of its full swing from its initial high or low level. This leads to successful write operation without any errors.

An improvement in T_{WA} is observed in M7T, MPT8T, M8T, M9T and MI-12T compared to C6T.

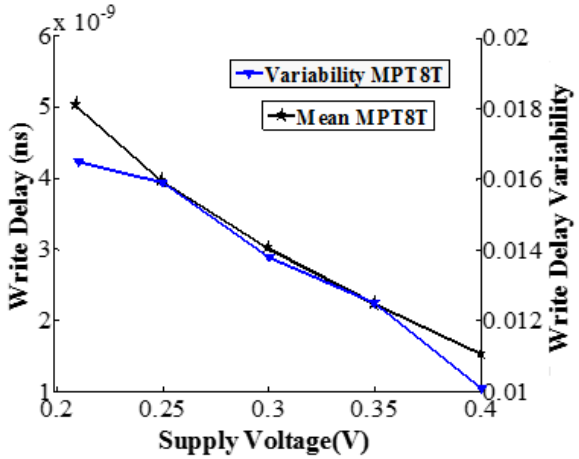
Figure 5.47 show the write delay and its variability of C6T, M7T, MPT8T, M8T, M9T and MI-12T at varying supply voltage from 0.2 V to 0.4V.



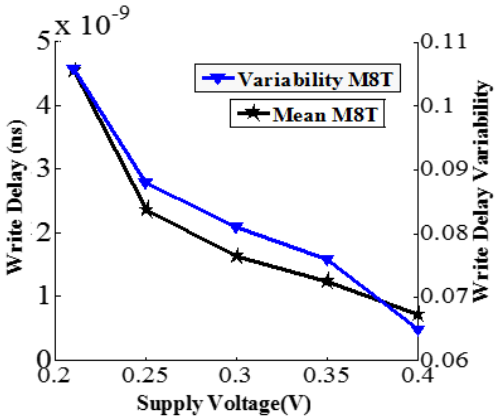
(a)



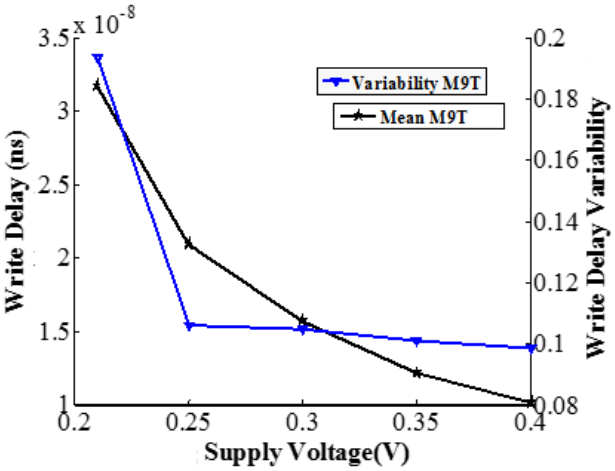
(b)



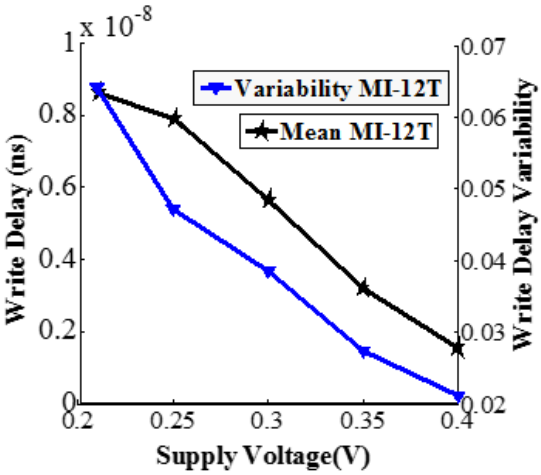
(c)



(d)



(e)



(f)

Figure 5.47: Write delay and its variability of (a) C6T (b) M7T (c) MPT8T (d) M8T (e) M9T (f) MI-12T

From the Figure 5.47, it is observed that the M7T, MPT8T, M8T, M9T and MI-12T have less range of variability around mean value at supply voltage varying from 0.2 V to 0.4 V as

compared to C6T. Table 5.10 shows the comparative analysis of average write delay and its variability for all proposed SRAM cells with C6T.

Average write delay in increasing order: M8T< MPT8T< MI-12T< M7T<< M9T< C6T

For M9T, write delay value is 3× more than M7T.

Write delay and its variability reduces with reduction in power supply voltage.

Table 5.10: Comparative analysis of write delay and its variability for all proposed SRAM cells with C6T

Types of SRAM cells	Average WRITE delay [$T_{WA\ (ns)}$]		Variability (σ/μ)
	Values	% decrement w.r.t. C6T	Range (for V_{DD} varying from 0.2V to 0.4V)
C6T	19.20	--	0.05 to 0.730
M7T	05.85	69.5%	0.07 to 0.180
MPT8T	03.15	83.5%	**0.01 to 0.016**
M8T	**02.09**	**89.1%**	0.06 to 0.100
M9T	18.11	05.6%	0.09 to 0.190
MI-12T	05.37	72.0%	0.02 to 0.060

5.4.7. Leakage Power Consumption in Hold mode

The major leakage components of C6T and proposed cells during hold mode are discussed and given in Appendix C. A comparison of leakage power consumption in hold mode of C6T, M7T, MPT8T, M8T, M9T and MI-12T cells at supply voltage varying from 0.2V to 0.4V is shown in Figure 5.48.

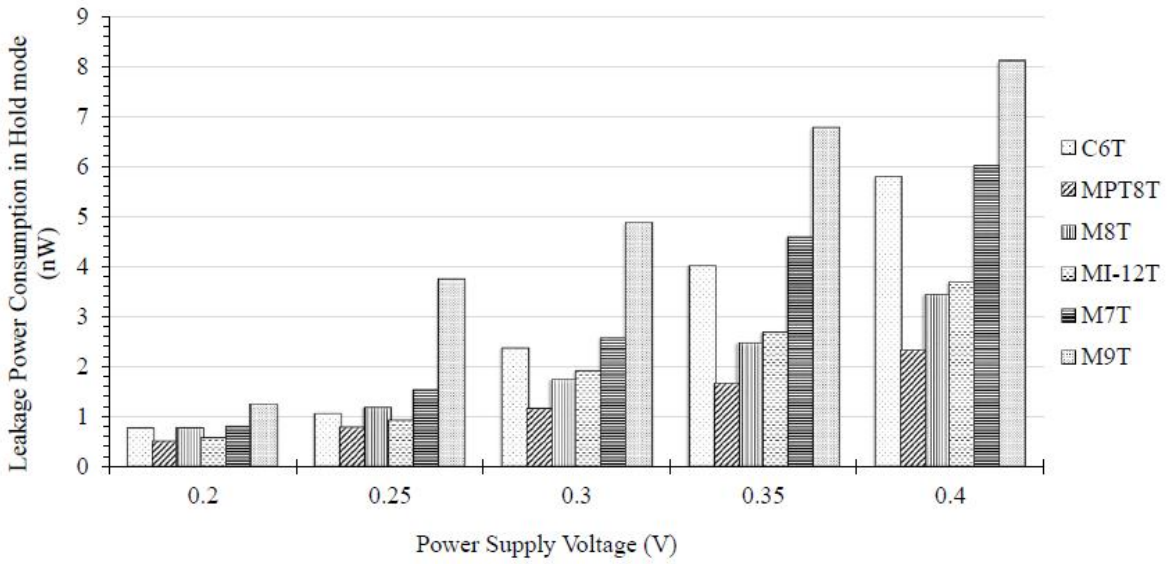


Figure 5.48: Leakage power consumptions in hold mode versus supply voltage

From Figure 5.48, the analyzed results show that for supply voltage value 0.3V onwards, C6T has significant increase in leakage power consumption in hold mode as compared to the MPT8T, M8T and MI-12T. Whereas M9T followed by M7T show high leakage power consumption for all supply voltages.

Table 5.11 shows the comparative analysis of leakage power consumption for all SRAM cells in hold mode.

Leakage power consumption in hold mode in increasing order is given below:

MPT8T < M8T < MI-12T < C6T < M7T < M9T

Table 5.11: Comparative analyses of leakage power consumptions in hold mode at 0.4 V supply

Types of SRAM cells	**Leakage Power Consumption (nW)**	**% less power consumption w.r.t. C6T**
C6T	5.76	--
M7T	6.01	10.7 % more
MPT8T	**2.31**	**54.6%**
M8T	3.14	32.1%
M9T	8.10	76.4% more
MI-12T	3.67	30.7%

5.5. ANALYTICAL EXPRESSIONS FOR HOLD SNM, RSNM & WSNM OF SRAM CELLS

Stability parameters can be expressed as a function of aspect ratio and supply voltage. Hence these expressions can be directly utilized to determine transistor sizes for a desired value of stability parameters (hold SNM, RSNM and WSNM) or vice versa.

The derivations of these expressions and comparison of value thus obtained with simulated results are given in this section.

For analysis, following sub-threshold drain current equation is used and its parameters are taken from 45 nm BSIM model library [39][40]:

$$I_{D,SUB} = I_S \exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right)\left(1 - \exp\left(\frac{V_{DS}}{V_T}\right)\right)$$

Where,

$$I_{S,NMOS} = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left(\frac{kT}{q}\right)^2 \left(1 - e^{1.8}\right)$$

$$I_{S,PMOS} = \mu_p C_{ox} \left(\frac{W}{L}\right)_p \left(\frac{kT}{q}\right)^2 \left(1 - e^{1.8}\right)$$

$$\left(C_{ox}\right)_p = \frac{\varepsilon_{ox}}{(t_{ox})_p} \quad \text{and} \quad \left(C_{ox}\right)_n = \frac{\varepsilon_{ox}}{(t_{ox})_n}$$

Following parameter values are taken from 45 nm BSIM model library

$$(V_{th})_n = 0.4226V$$
$$(V_{th})_p = -0.412642V$$
$$(t_{ox})_p = 1.26 \times 10^{-9}\,m$$
$$(t_{ox})_n = 1.14 \times 10^{-9}\,m$$
$$\mu_n = 0.045 cm^2/V\text{-}s$$
$$\mu_p = 0.02 cm^2/V\text{-}s$$
$$n_n = n_p = 1.5$$

Constant values for calculating the analytical expressions:

$$V_T = \frac{kT}{q} = 0.025V$$
$$\varepsilon_{ox} = 3.97\varepsilon_o$$
$$\varepsilon_o = 8.85 \times 10^{-12}\,F/m$$

Using the above-mentioned values and formulas, following parameters have been computed

$$\left(C_{ox}\right)_p = 0.027$$
$$\left(C_{ox}\right)_n = 0.0308$$
$$I_{S,NMOS} = 4.37 \times 10^{-6}\left(\frac{W}{L}\right)_n$$
$$I_{S,PMOS} = 1.76 \times 10^{-6}\left(\frac{W}{L}\right)_p$$

5.5.1. Analytical Expressions for Hold SNM of C6T, M7T, MPT8T, M8T, M9T and MI-12T SRAM cells

Figure 5.49 show a part of schematics of C6T, M7T, MPT8T, M8T, M9T and MI-12T (full description given in Section 5.2 and Section 5.3) during hold operation when QB is low and Q is high (i.e. V_{QB}=low, V_Q=high). Crossed/Uncrossed transistors represent OFF/ON state respectively.

Pull-up, pull-down and access transistor current analysis during hold mode for C6T and proposed SRAM cells are given in Appendix D.

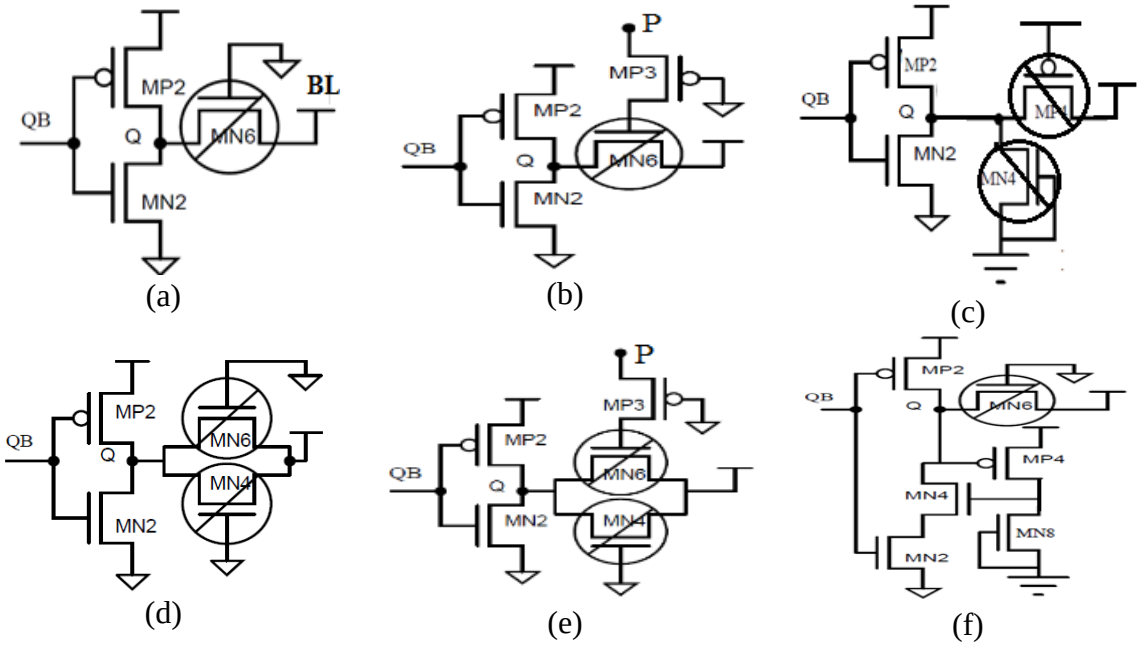


Figure 5.49: Half part of SRAM cells during hold operation (a) C6T (b) M7T (c) MPT8T (d) M8T (e) M9T (f) MI-12T

a) The cross coupled inverter pair designs are same for C6T, M7T, MPT8T, M8T and M9T. Therefore, the analytical expressions for C6T, M7T, MPT8T, M8T and M9T during hold operation are same.

During hold operation, in Figure 5.49 (a),

- Voltage conditions taken are: V_Q is high, V_{QB} is low, BL=V_{DD},
- Transistors MN6 is OFF,

For the proper logic operation in sub-threshold region under steady state, assuming I_{MN6} =0, applying KCL at node Q gives I_{n2}=I_{p2} which leads to following expression;

$$I_{S,n2}\exp\left(\frac{V_Q - V_{th,n2}}{n_{n2}\cdot V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right) = I_{S,p2}\exp\left(\frac{V_{DD}-V_Q-V_{th,p2}}{n_{p2}\cdot V_T}\right)\left(1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q and V_{QB} gives:

$$V_Q = \frac{n_{n2}\cdot n_{p2}\cdot V_T}{n_{n2}+n_{p2}}\left[\ln\left(\frac{I_{S,p2}}{I_{S,n2}}\right)+\ln\left(\frac{1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)}{1-\exp\left(\frac{-V_{QB}}{V_T}\right)}\right)\right] + \frac{n_{n2}\cdot V_{DD}}{n_{p2}+n_{n2}} + \frac{n_{p2}\cdot n_{n2}}{n_{p2}+n_{n2}}\left(\frac{V_{th,p2}}{n_{p2}}+\frac{V_{th,n2}}{n_{n2}}\right). \quad (5.14)$$

For 45 nm technology, choosing L=45nm, (W_{p2}/ W_{n2}) = 51nm/85nm = 0.6, this equation is used to generate butterfly curves for different values of V_{DD} (in range-0.2 to 0.4). Then Hold SNM is calculated for each supply value.

The relationship between Hold SNM and supply voltage is modeled, with the help of linear regression (least squares estimation) applied to this data set. The following regression equation has been obtained for C6T,

$$V_{\text{Hold SNM,C6T}} = -0.0112 + 0.375 * V_{DD} \quad (5.15)$$

For V_{DD} = 0.4V, value of Hold SNM is obtained from equation 5.15 as;

$$V_{\text{Hold SNM, C6T,LP7T,MPT8T,M8T,M9T}} = 0.138V$$

Same procedure is repeated for other proposed M7T, MPT8T, M8T and M9T cells. The results are found to be similar as the structure of cross coupled inverter is identical.

b) The analytical expression for MI-12T SRAM cell with stacked transistors based cross coupled invertors configuration during hold operation is done separately and is given below.

During hold operation, in Figure 5.49 (f),

- Voltage conditions taken are V_Q is high, V_{QB} is low, BL=V_{DD},
- Transistors MN6 is OFF,

For the proper logic operation in sub-threshold region under steady state, assuming I_{MN6} =0, applying KCL at node Q gives I_{p2}=I_{n2} (or I_{n4}) which leads to following expression;

$$I_{S,n2}\exp\left(\frac{V_Q - V_{th,n2}}{n_{n2}\cdot V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right) = I_{S,p2}\exp\left(\frac{V_{DD}-V_Q-V_{th,p2}}{n_{p2}\cdot V_T}\right)\left(1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q and V_{QB} gives:

$$V_Q = \frac{n_{n2}\cdot n_{p2}\cdot V_T}{n_{n2}+n_{p2}}\left[\ln\left(\frac{I_{S,p2}}{I_{S,n2}}\right)+\ln\left(\frac{1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)}{1-\exp\left(\frac{-V_{QB}}{V_T}\right)}\right)\right]$$
$$+\frac{n_{n2}\cdot V_{DD}}{n_{p2}+n_{n2}}+\frac{n_{p2}\cdot n_{n2}}{n_{p2}+n_{n2}}\left(\frac{V_{th,p2}}{n_{p2}}+\frac{V_{th,n2}}{n_{n2}}\right).$$

(5.16)

For 45 nm technology, choosing L=45nm, (W_{p2}/ W_{n2}) = 51nm/85nm = 0.6, this equation is used to generate butterfly curves for different values of V_{DD} (in range-0.2 to 0.4). Then Hold SNM is calculated for each supply value.

The relationship between Hold SNM and supply voltage is modeled, with the help of linear regression (least squares estimation) applied to this data set. The following regression equation has been obtained for MI-12T,

$$\boxed{V_{\text{Hold SNM, MI-12T}} = -0.0129 + 0.480 * V_{DD}} \qquad (5.17)$$

At V_{DD} = 0.4V; value of Hold SNM is obtained from equation 5.17 as;

$$\boxed{V_{\text{Hold SNM, MI-12T}} = 0.179V}$$

Comparison of values of Hold SNM between simulated and estimated values through analytical and regression equation at 0.4V is done in Table 5.12.

Table 5.12: Comparison of hold SNM between simulated and estimated values through analytical and regression equation at 0.4V

Types of SRAM cells	Hold SNM (mV) Simulated values	Hold SNM (mV) Estimated through analytical equation using butterfly curve	Hold SNM (mV) Estimated through regression equation
C6T	120.2	125	138
M7T	120.2	125	138
MPT8T	120.2	125	138
M8T	120.2	125	138
M9T	120.2	125	138
MI-12T	170	177	179

The value of Hold SNM estimated from analytical equations is within (3.84% to 3.9%) to those that are observed with simulated values. The value of Hold SNM estimated from regression equations is within (5% to 12.8%) to those that are observed with simulated values.

5.5.2. Analytical Expressions for RSNM of C6T, M7T, MPT8T, M8T, M9T and MI-12T SRAM cells

Figure 5.50 show a part of schematics of C6T, M7T, MPT8T, M8T, M9T and MI-12T (full description given in Section 5.2 and Section 5.3) during read '0' operation for V_Q is low, V_{QB} is high. Crossed/Uncrossed transistors show OFF/ON state respectively. Pull-up, pull-down and access transistor current analysis during read mode for C6T and proposed SRAM cells are given in Appendix D.

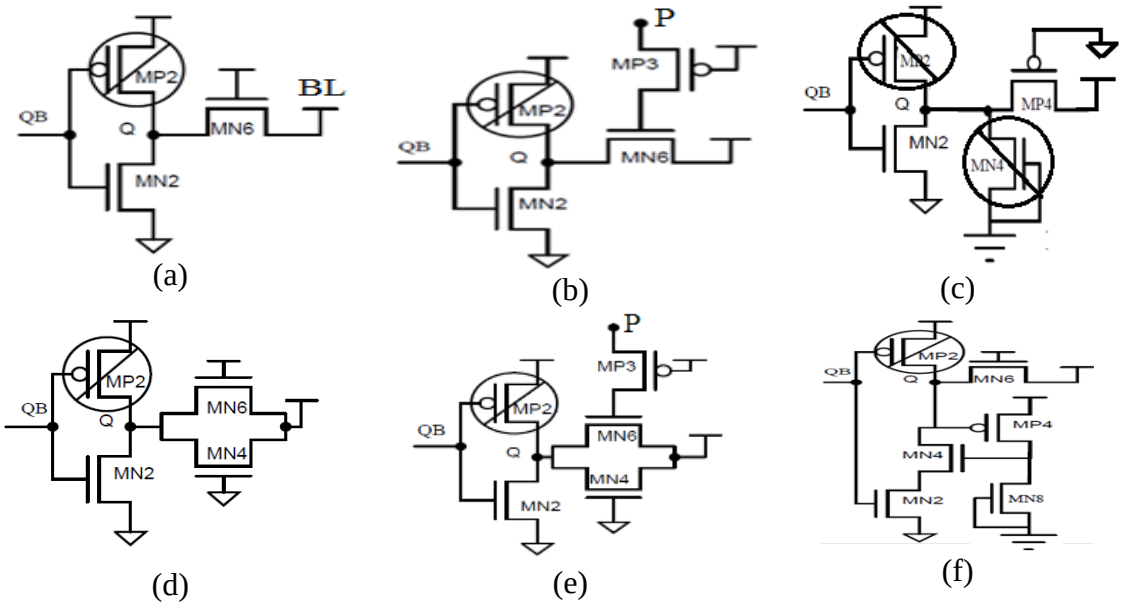


Figure 5.50: Half part of SRAM cells during read operation (a) C6T (b) M7T (c) MPT8T (d) M8T (e) M9T (f) MI-12T

a) The analytical expression for C6T during read '0' operation is given below:

During read operation, in Figure 5.50 (a),

- Voltage conditions taken are: V_{QB} is high, V_Q is low, BL=V_{DD},
- Transistor MP2 is turned OFF with I_{MP2}=0,
- Transistors MN6 and MN2 are ON,

For the proper logic operation in sub-threshold region under steady state, applying KCL at node Q gives I_{n2}=I_{n6} which leads to following expression;

$$I_{S,n2}\exp\left(\frac{V_Q - V_{th,n2}}{n_{n2}V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right) = I_{S,n6}\exp\left(\frac{V_{DD} - V_{QB} - V_{th,n6}}{n_{n6}V_T}\right)\left(1-\exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q gives:

$$V_Q = n_{n2}\cdot V_T \ln\left(\frac{I_{S,n6}}{I_{S,n2}}\right) + n_{n2}\cdot V_T \ln\left(\frac{1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)}{1-\exp\left(\frac{-V_{QB}}{V_T}\right)}\right) + V_{th,n2}$$

$$+\frac{n_{n2}}{n_{n6}}\left(V_{DD} + V_{th,n6} - V_{QB}\right) \qquad (5.18)$$

For 45 nm technology, choosing L_{n2}= L_{n6}= 45nm, (W_{n2}/ W_{n6}) = 180nm/60nm = 3. This equation is used to generate butterfly curves for different values of V_{DD} (in range-0.2 V to 0.4V) and different values of (W_{n2}/ W_{n6}) (in range-3 to 5). Then RSNM is calculated for each supply value.

The relationship between RSNM, CR, and supply voltage is modeled with the help of multiple linear regressions applied to this data set (i.e. RSNM vs. V_{DD}). The following regression equation has been obtained for C6T;

$$V_{SNM,Read,C6T} = 0.0375\times\ln\left(\frac{W_{n2}/L_{n2}}{W_{n6}/L_{n6}}\right) + 0.829V_{DD} - 0.318 \qquad (5.19)$$

For 45 nm technology, choosing V_{DD} = 0.4V, L_{n2}= L_{n6}= 45nm, (W_{n2}/W_{n6}) = 180nm/60nm = 3 (CR ratio chosen as discussed in Section 5.3), value of RSNM is obtained from equation 5.19 as;

$$\boxed{V_{RSNM,C6T} = 0.054V}$$

b) The analytical expression for M7T during read '0' operation is given below:

During read operation, in Figure 5.50 (b),

- Voltage conditions taken are; V_{QB} is high, V_Q is low, BL=V_{DD},
- Transistor MP2 is turned OFF with I_{MP2}=0,
- Transistors MP3, MN6 and MN2 are ON,

For the proper logic operation in sub-threshold region under steady state, Applying KCL at node Q gives I_{n2}=I_{n6} which leads to following expression;

$$I_{S,n2}\exp\left(\frac{V_Q - V_{th,n2}}{n_{n2}V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right) = I_{S,n6}\exp\left(\frac{V_{DD} - V_{QB} - V_{th,n6}}{n_{n6}V_T}\right)\left(1-\exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q gives:

$$V_Q = n_{n2}\cdot V_T \ln\left(\frac{I_{S,n6}}{I_{S,n2}}\right) + n_{n2}\cdot V_T \ln\left(\frac{1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)}{1-\exp\left(\frac{-V_{QB}}{V_T}\right)}\right) + V_{th,n2} \qquad (5.20)$$

$$+\frac{n_{n2}}{n_{n6}}\left(V_{DD} + V_{th,n6} - V_{QB}\right)$$

Using the procedure as described in Section 5.5.2 (a), the following regression equation has been obtained for M7T;

$$V_{SNM,Read,M7T} = 0.0375\times\ln\left(\frac{W_{n2}/L_{n2}}{W_{n6}/L_{n6}}\right) + 0.962V_{DD} - 0.356 \qquad (5.21)$$

For 45 nm technology, choosing V_{DD} = 0.4V, L_{n2}= L_{n6}= 45nm, (W_{n2}/W_{n6}) = 180nm/60nm =3 (CR ratio chosen as discussed in Section 5.3), value of RSNM is obtained from equation 5.21 as;

$$\boxed{V_{RSNM,M7T} = 0.069V}$$

c) The analytical expression for MPT8T during read '0'operation is given below:

During read operation, in Figure 5.50 (c),

- Voltage conditions taken are; V_{QB} is high, V_Q is low, BL=V_{DD},
- Transistors MP2 and MN4 are turned OFF with I_{MP2} = I_{MN4} = 0,

- Transistors MN6 and MN2 are ON,

For the proper logic operation in sub-threshold region under steady state, applying KCL at node Q gives $I_{n2}=I_{p4}$ which leads to following expression;

$$I_{S,n2}\exp\left(\frac{V_Q-V_{th,n2}}{n_{n2}\cdot V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right)=I_{S,p4}\exp\left(\frac{V_{DD}-V_Q-V_{th,p4}}{n_{p4}\cdot V_T}\right)\left(1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q gives:

$$V_Q=\frac{n_{n2}\cdot n_{p4}\cdot V_T}{n_{n2}+n_{p4}}\left[\ln\left(\frac{I_{S,p4}}{I_{S,n2}}\right)+\ln\left(\frac{1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)}{1-\exp\left(\frac{-V_{QB}}{V_T}\right)}\right)\right]$$
$$+\frac{n_{n2}\cdot V_{DD}}{n_{p4}+n_{n2}}+\frac{n_{p4}\cdot n_{n2}}{n_{p4}+n_{n2}}\left(\frac{V_{th,p4}}{n_{p4}}+\frac{V_{th,n2}}{n_{n2}}\right). \quad (5.22)$$

Using the procedure as described in Section 5.5.2 (a), the following regression equation has been obtained for MPT8T;

$$V_{SNM,Read,MPT8T}=0.0375\times\ln\left(\frac{W_{n2}/L_{n2}}{W_{p4}/L_{p4}}\right)+0.812V_{DD}-0.231 \quad (5.23)$$

For 45 nm technology, choosing V_{DD} = 0.4V, L_{n2}= L_{p4}= 45nm, (W_{n2}/W_{p4}) = 180nm/60nm = 3 (CR ratio chosen as discussed in Section 5.3), value of RSNM is obtained from equation 5.23 as;

$$\boxed{V_{RSNM,MPT8T}=0.134V}$$

d) The analytical expression for M8T during read '0' operation is given below:

During read operation, in Figure 5.50 (d),

- Voltage conditions taken are V_{QB} is high, V_Q is low, BL=V_{DD},
- Transistor MP2 is turned OFF with I_{MP2} = 0,
- Transistors MN6 and MN2 are ON, MN4 provides extra OFF state current to the nodes

For the proper logic operation in sub-threshold region under steady state, applying KCL at node Q gives $I_{n2}=I_{n6}+ I_{n4}$ which leads to following expression;

$$I_{S,n2}\exp\left(\frac{V_Q - V_{th,n2}}{n_{n2}\cdot V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right) = I_{S,n6}\exp\left(\frac{V_{DD} - V_{QB} - V_{th,n6}}{n_{n6}\cdot V_T}\right)\left(1-\exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)\right)$$
$$+ I_{S,n4}\exp\left(\frac{V_{DD} - V_{QB} - V_{th,n4}}{n_{n4}\cdot V_T}\right)\left(1-\exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q gives:

$$V_Q = n_{n2}\cdot V_T \ln\left(\frac{I_{S,n6} + I_{S,n4}}{I_{S,n2}}\right) + n_{n2}\cdot V_T \ln\left(\frac{1-\exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)}{1-\exp\left(\frac{-V_{QB}}{V_T}\right)}\right) + V_{th,n2} \quad (5.24)$$
$$+ \frac{n_{n2}}{n_{n6} + n_{n4}}\left(V_{DD} - (V_{th,n6} + V_{th,n4}) + V_{QB}\right)$$

Using the procedure as described in Section 5.5.2 (a), the following regression equation has been obtained for M8T by taking fixed W_{n4}/L_{n4} = 65nm/45nm = 1.4;

$$V_{SNM,Read,M8T} = 0.0375\times \ln\left(\frac{W_{n2}/L_{n2}}{W_{n6}/L_{n6}}\right) + 1.23V_{DD} - 0.427 \quad (5.25)$$

For 45 nm technology, choosing V_{DD} = 0.4V, L_{n2}= L_{n6}= 45nm, (W_{n2}/W_{n6}) = 162nm/60nm = 2.7 (CR ratio chosen as discussed in Section 5.3), value of RSNM is obtained from equation 5.25 as;

$$\boxed{V_{RSNM,M8T} = 0.102V}$$

e) The analytical expression for M9T during read '0' operation is given below:

During read operation, in Figure 5.50 (e),

- Voltage conditions taken are V_{QB} is high, V_Q is low, BL=V_{DD},
- Transistor MP2 is turned OFF with I_{MP2} = 0,
- Transistors MP3, MN6 and MN2 are ON, MN4 provides extra OFF state current to the nodes

For the proper logic operation in sub-threshold region under steady state, Applying KCL at node Q gives I_{n2}=I_{n6}+ I_{n4} which leads to following expression;

$$I_{S,n2}\exp\left(\frac{V_Q - V_{th,n2}}{n_{n2}\cdot V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right) = I_{S,n6}\exp\left(\frac{V_{DD} - V_{QB} - V_{th,n6}}{n_{n6}\cdot V_T}\right)\left(1-\exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)\right)$$
$$+ I_{S,n4}\exp\left(\frac{V_{DD} - V_{QB} - V_{th,n4}}{n_{n4}\cdot V_T}\right)\left(1-\exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q gives:

$$V_Q = n_{n2}\cdot V_T \ln\left(\frac{I_{S,n6} + I_{S,n4}}{I_{S,n2}}\right) + n_{n2}\cdot V_T \ln\left(\frac{1-\exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)}{1-\exp\left(\frac{-V_{QB}}{V_T}\right)}\right) + V_{th,n2} \qquad (5.26)$$
$$+ \frac{n_{n2}}{n_{n6} + n_{n4}}\left(V_{DD} - (V_{th,n6} + V_{th,n4}) + V_{QB}\right)$$

Using the procedure as described in Section 5.5.2 (a), the following regression equation has been obtained for M9T by taking fixed W_{n4}/L_{n4} = 65nm/45nm = 1.4;

$$V_{SNM,Read,M9T} = 0.0375\times\ln\left(\frac{W_{n2}/L_{n2}}{W_{n6}/L_{n6}}\right) + 1.43V_{DD} - 0.551 \qquad (5.27)$$

For 45 nm technology, choosing V_{DD} = 0.4V, L_{n2}= L_{n6}= 45nm, (W_{n2}/W_{n6}) = 174nm/60nm = 2.9 (CR ratio chosen as discussed in Section 5.3), value of RSNM is obtained from equation 5.27 as;

$$\boxed{V_{RSNM,M9T} = 0.060V}$$

f) The analytical expression for MI-12T during read '0' operation is given below:
During read operation, in Figure 5.50 (f),

- Voltage conditions taken are; V_{QB} is high, V_Q is low, BL=V_{DD},
- Transistor MP2 is turned OFF with I_{MP2} = 0,
- Transistors MN6, MN4, MP4 and MN2 are ON,

For the proper logic operation in sub-threshold region under steady state, applying KCL at node Q gives I_{n2}=I_{n6} which leads to following expression;

$$I_{S,n2}\exp\left(\frac{V_Q - V_{th,n2}}{n_{n2}\cdot V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right) = I_{S,n6}\exp\left(\frac{V_{DD} - V_{QB} - V_{th,n6}}{n_{n6}\cdot V_T}\right)\left(1-\exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q gives:

$$V_Q = n_{n2} \cdot V_T \ln\left(\frac{I_{S,n6}}{I_{S,n2}}\right) + n_{n2} \cdot V_T \ln\left(\frac{1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)}{1-\exp\left(\frac{-V_{QB}}{V_T}\right)}\right) + V_{th,n2}$$

$$+ \frac{n_{n2}}{n_{n6}}\left(V_{DD} + V_{th,n6} - V_{QB}\right) \tag{5.28}$$

Using the procedure as described in Section 5.5.2 (a), the following regression equation has been obtained for MI-12T;

$$V_{SNM,Read,MI\text{-}12T} = 0.0375 \times \ln\left(\frac{W_{n2}/L_{n2}}{W_{n6}/L_{n6}}\right) + 1.43V_{DD} - 0.554 \tag{5.29}$$

For 45 nm technology, choosing V_{DD} = 0.4V, L_{n2}= L_{n6}= 45nm, (W_{n2}/W_{n6}) = 174nm/60nm= 2.9 (CR ratio chosen as discussed in Section 5.3), value of RSNM is obtained from equation 5.29 as;

$$\boxed{V_{RSNM,MI\text{-}12T} = 0.067}$$

Comparison of values of RSNM between simulated and estimated values through analytical and regression equation at 0.4V is shown in Table 5.13.

Table 5.13: Comparison of RSNM between simulated and estimated values through analytical and regression equation at 0.4V

Types of SRAM cells	**RSNM(mV)** Simulated values	**RSNM(mV)** Estimated through analytical equation using butterfly curve	**RSNM(mV)** Estimated through regression equation
C6T	034.0	042	053
M7T	060.0	065	069
MPT8T	120.0	129	134
M8T	085.0	097	102
M9T	043.0	057	060
MI-12T	054.4	062	067

The value of RSNM estimated from analytical equations is within (6.9% to 24.5%) to those that are observed with simulated values. The value of RSNM estimated from regression equations is within (10.4% to 34.8%) to those that are observed with simulated values.

5.5.3. Analytical Expressions for WSNM of C6T, M7T, MPT8T, M8T, M9T and MI-12T SRAM cells

Figure 5.51 show a part of schematics of C6T, M7T, MPT8T, M8T, M9T and MI-12T (full description given in Section 5.2 and Section 5.3) during write '0' operation for V_Q is high, V_{QB} is low. Crossed/Uncrossed transistors show OFF/ON state respectively. Pull-up, pull-down and access transistor current analysis during write mode for C6T and proposed SRAM cells are given in Appendix D.

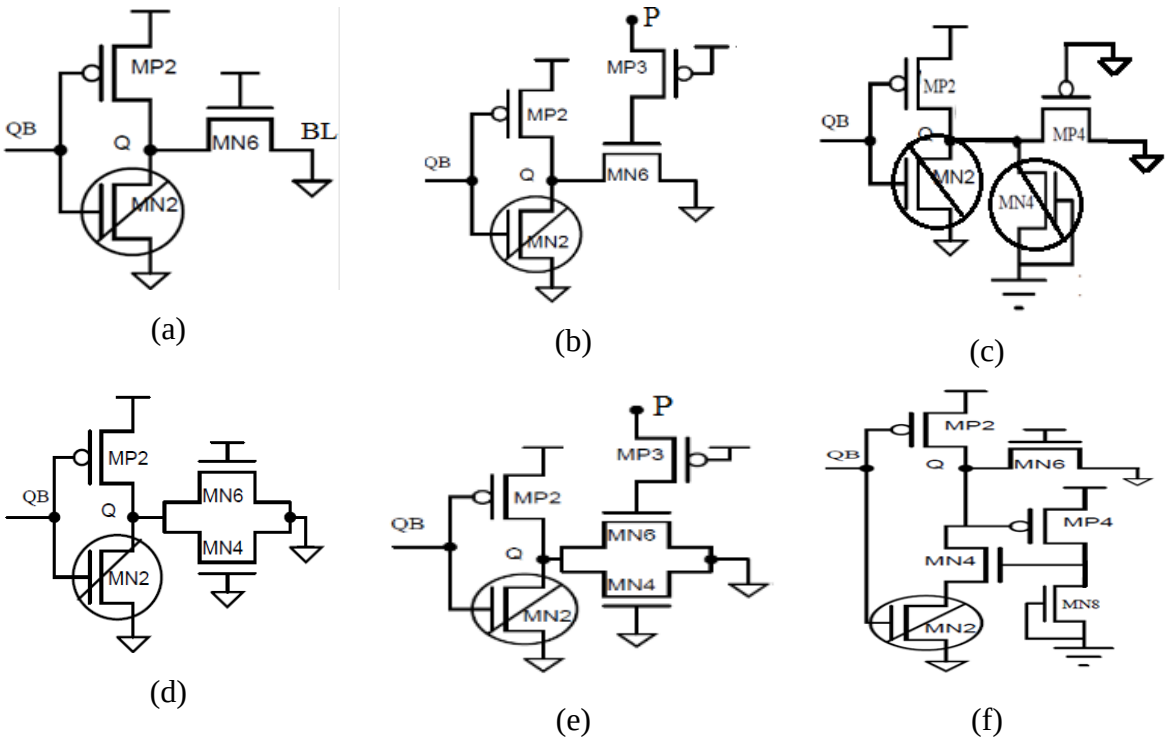


Figure 5.51: Half part of SRAM cells during write operation (a) C6T (b) M7T (c) MPT8T (d) M8T (e) M9T (f) MI-12T

a) The analytical expression for C6T during write '0' operation is given below:

During write operation, in Figure 5.51 (a),

- Voltage conditions taken are; V_{QB} is low, V_Q is high, BL = low (GND),
- Transistor MN2 is turned OFF,
- Transistors MN6 and MP2 are ON,

For the proper logic operation in sub-threshold region under steady state, applying KCL at node Q, gives $I_{n6} = I_{p2}$ which leads to following expression;

$$I_{n6}\exp\left(\frac{V_Q - V_{th,n6}}{n_{n6}\cdot V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right) = I_{p2}\exp\left(\frac{V_{DD} - V_Q - V_{th,p2}}{n_{p2}\cdot V_T}\right)\left(1-\exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q gives

$$V_Q = n_{p2}\cdot V_T \ln\left(\frac{I_{S,n6}}{I_{S,p2}}\right) + n_{p2}V_T \ln\left(\frac{1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)}{1-\exp\left(\frac{-V_{QB}}{V_T}\right)}\right) \qquad (5.30)$$

$$+V_{th,p2} + \frac{n_{p2}}{n_{n6}}\left(V_{DD} + V_{th,n6} - V_{QB}\right)$$

For 45 nm technology, choosing L_{p2}= L_{n6}= 45nm, (W_{n6}/ W_{p2}) = 143nm/55nm = 2.6. This equation is used to generate butterfly curves for different values of V_{DD} (in range-0.2 to 0.4V) and (W_{n6}/ W_{p2}) (in range-2.6 to 5). Then WSNM is calculated for each supply value.

The relationship between WSNM, PR, and supply voltage is modeled with the help of multiple linear regressions applied to this data set (i.e. WSNM vs. V_{DD}). The following regression equation has been obtained for C6T;

$$V_{WSNM,C6T} = 0.0931\times\ln\left(\frac{W_{n6}/L_{n6}}{W_{p2}/L_{p2}}\right) + 0.962V_{DD} - 0.319 \qquad (5.31)$$

For 45 nm technology, choosing V_{DD} = 0.4V, L_{p2}= L_{n6}= 45nm, (W_{n6}/ W_{p2}) = 143nm/55nm = 2.6 (PR ratio chosen as discussed in Section 5.3), value of RSNM is obtained from equation 5.31 as;

$$\boxed{V_{WSNM,C6T} = 0.154V}$$

b) The analytical expression for M7T during write '0' operation is given below:

For M7T, during write operation, in Figure 5.51 (b),

- voltage conditions taken are V_{QB} is low, V_Q is high, BL= low (GND),
- Transistor MN2 is turned OFF,
- Transistors MN6, MP3 and MP2 are ON,

For the proper logic operation in sub-threshold region under steady state, Applying KCL at node Q gives $I_{n6} = I_{p2}$ which leads to following expression;

$$I_{n6}\exp\left(\frac{V_Q - V_{th,n6}}{n_{n6}\cdot V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right) = I_{p2}\exp\left(\frac{V_{DD}-V_Q-V_{th,p2}}{n_{p2}\cdot V_T}\right)\left(1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q gives

$$V_Q = n_{p2}\cdot V_T \ln\left(\frac{I_{S,n6}}{I_{S,p2}}\right) + n_{p2}V_T \ln\left(\frac{1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)}{1-\exp\left(\frac{-V_{QB}}{V_T}\right)}\right) \qquad (5.32)$$

$$+V_{th,p2} + \frac{n_{p2}}{n_{n6}}\left(V_{DD}+V_{th,n6}-V_{QB}\right)$$

Using the procedure as described in Section 5.5.3 (a), the following regression equation has been obtained for M7T;

$$V_{SNM,\,Write,M7T} = 0.0931\times\ln\left(\frac{W_{n6}/L_{n6}}{W_{p2}/L_{p2}}\right) + 0.962V_{DD} - 0.274 \qquad (5.33)$$

For 45 nm technology, choosing V_{DD} = 0.4V, L_{p2}= L_{n6}= 45nm, (W_{n6}/W_{p2}) = 126nm/26nm = 2.1 (PR ratio chosen as discussed in Section 5.3), value of WSNM is obtained from equation 5.33 as;

$$\boxed{V_{WSNM,M7T} = 0.179V}$$

c) The analytical expression for MPT8T during write '0' operation is given below:

For MPT8T, during write operation, in Figure 5.51 (c),

- Voltage conditions taken are V_{QB} is low, V_Q is high, BL= low (GND),
- Transistor MN2 and MN4 are turned OFF,
- Transistors MP4 and MP2 are ON,

For the proper logic operation in sub-threshold region under steady state, Applying KCL at node Q gives $I_{p4} = I_{p2}$ which leads to following expression;

$$I_{p4}\exp\left(\frac{V_{DD}-V_Q-V_{th,p4}}{n_{p4}\cdot V_T}\right)\left(1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)\right) = I_{p2}\exp\left(\frac{V_{DD}-V_Q-V_{th,p2}}{n_{p2}\cdot V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q gives

$$V_Q = n_{p2} \cdot V_T \ln\left(\frac{I_{S,p4}}{I_{S,p2}}\right) + n_{p2} V_T \ln\left(\frac{1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)}{1-\exp\left(\frac{-V_{QB}}{V_T}\right)}\right) \quad (5.34)$$

$$+ V_{th,p2} + \frac{n_{p2}}{n_{p4}}\left(V_{DD} + V_{th,p4} - V_{QB}\right)$$

Using the procedure as described in Section 5.5.3 (a), the following regression equation has been obtained for MPT8T;

$$V_{WSNM,MPT8T} = 0.0375 \times \ln\left(\frac{W_{P4}/L_{p4}}{W_{p2}/L_{p2}}\right) + 0.962 V_{DD} - 0.120 \quad (5.35)$$

For 45 nm technology, choosing V_{DD} = 0.4V, L_{p2}= L_{p4}= 45nm, (W_{p4}/W_{p2}) =108nm/60nm = 1.8 (PR ratio chosen as discussed in Section 5.3), value of WSNM is obtained from equation 5.35 as;

$$\boxed{V_{WSNM,MPT8T} = 0.286V}$$

d) The analytical expression for M8T during write '0' operation is given below:

For M8T, during write operation, in Figure 5.51 (d),

- Voltage conditions taken are; V_{QB} is low, V_Q is high, BL= low (GND),
- Transistor MN2 is turned OFF,
- Transistors MN6 and MP2 are ON, MN4 provides extra OFF state current to the nodes.

For the proper logic operation in sub-threshold region under steady state, Applying KCL at node Q gives I_{n6}+ I_{n4} = I_{p2} which leads to following expression;

$$I_{n6}\exp\left(\frac{V_Q - V_{th,n6}}{n_{n6} \cdot V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right) + I_{n4}\exp\left(\frac{V_Q - V_{th,n4}}{n_{n4} \cdot V_T}\right)\left(1-\exp\left(\frac{-V_{QB}}{V_T}\right)\right)$$

$$= I_{p2}\exp\left(\frac{V_{DD} - V_Q - V_{th,p2}}{n_{p2} \cdot V_T}\right)\left(1-\exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q gives

$$V_Q = n_{p2} \cdot V_T \ln\left(\frac{I_{S,n6} + I_{S,n4}}{I_{S,p2}}\right) + n_{p2} V_T \ln\left(\frac{1 - \exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)}{1 - \exp\left(\frac{-V_{QB}}{V_T}\right)}\right) \tag{5.36}$$

$$+ V_{th,p2} + \frac{n_{p2}}{n_{n6} + n_{n4}}\left(V_{DD} + (V_{th,n6} + V_{th,n4}) - V_{QB}\right)$$

Using the procedure as described in Section 5.5.3 (a), the following regression equation has been obtained for M8T by taking fixed W_{n4}/L_{n4} = 65nm/45nm = 1.4;

$$V_{WSNM,M8T} = 0.093 \times \ln\left(\frac{W_{n6}/L_{n6}}{W_{p2}/L_{P2}}\right) + 0.963 V_{DD} - 0.223 \tag{5.37}$$

For 45 nm technology, choosing V_{DD} = 0.4V, L_{p2}= L_{n6}= 45nm, (W_{n6}/W_{p2}) =150nm/60nm = 2.5 (PR ratio chosen as discussed in Section 5.3), value of WSNM is obtained from equation 5.37 as;

$$\boxed{V_{WSNM,M8T} = 0.247V}$$

e) The analytical expression for M9T during write '0' operation is given below:

For M9T, during write operation, in Figure 5.51 (e),

- Voltage conditions taken are V_{QB} is low, V_Q is high, BL= low (GND),
- Transistor MN2 is turned OFF,
- Transistors MN6, MP3 and MP2 are ON, MN4 provides extra OFF state current to the nodes.

For the proper logic operation in sub-threshold region under steady state, Applying KCL at node Q gives I_{n6}+ I_{n4} = I_{p2} which leads to following expression;

$$I_{n6} \exp\left(\frac{V_Q - V_{th,n6}}{n_{n6} \cdot V_T}\right)\left(1 - \exp\left(\frac{-V_{QB}}{V_T}\right)\right) + I_{n4} \exp\left(\frac{V_Q - V_{th,n4}}{n_{n4} \cdot V_T}\right)\left(1 - \exp\left(\frac{-V_{QB}}{V_T}\right)\right)$$

$$= I_{p2} \exp\left(\frac{V_{DD} - V_Q - V_{th,p2}}{n_{p2} \cdot V_T}\right)\left(1 - \exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q gives

$$V_Q = n_{p2} \cdot V_T \ln\left(\frac{I_{S,n6} + I_{S,n4}}{I_{S,p2}}\right) + n_{p2} V_T \ln\left(\frac{1 - \exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)}{1 - \exp\left(\frac{-V_{QB}}{V_T}\right)}\right) \quad (5.38)$$

$$+ V_{th,p2} + \frac{n_{p2}}{n_{n6} + n_{n4}}\left(V_{DD} + (V_{th,n6} + V_{th,n4}) - V_{QB}\right)$$

Using the procedure as described in Section 5.5.3 (a), the following regression equation has been obtained for M9T by taking fixed W_{n4}/L_{n4} = 65nm/45nm = 1.4;

$$V_{WSNM,M9T} = 0.093 \times \ln\left(\frac{W_{n6}/L_{n6}}{W_{p2}/L_{P2}}\right) + 0.573 V_{DD} - 0.106 \quad (5.39)$$

For 45 nm technology, choosing V_{DD} = 0.4V, L_{p2}= L_{n6}= 45nm, (W_{n6}/W_{p2}) =138nm/60nm = 2.3 (PR ratio chosen as discussed in Section 5.3), value of WSNM is obtained from equation 5.39 as;

$$\boxed{V_{WSNM,M9T} = 0.200V}$$

f) The analytical expression for MI-12T during write '0' operation is given below:

For MI-12T, during write operation, in Figure 5.51 (f),

- Voltage conditions taken are V_{QB} is low, V_Q is high, BL= low (GND),
- Transistor MN2 is OFF,
- Transistors MN6, MP4, MN4 and MP2 are ON,

For the proper logic operation in sub-threshold region under steady state, Applying KCL at node Q gives $I_{n6} = I_{p2}$ which leads to following expression;

$$I_{n6} \exp\left(\frac{V_Q - V_{th,n6}}{n_{n6} \cdot V_T}\right)\left(1 - \exp\left(\frac{-V_{QB}}{V_T}\right)\right) = I_{p2} \exp\left(\frac{V_{DD} - V_Q - V_{th,p2}}{n_{p2} \cdot V_T}\right)\left(1 - \exp\left(\frac{V_{QB} - V_{DD}}{V_T}\right)\right)$$

Using the method given in [41][42], solving above expression for V_Q gives

$$V_Q = n_{p2} \cdot V_T \ln\left(\frac{I_{S,n6}}{I_{S,p2}}\right) + n_{p2} V_T \ln\left(\frac{1-\exp\left(\frac{V_{QB}-V_{DD}}{V_T}\right)}{1-\exp\left(\frac{-V_{QB}}{V_T}\right)}\right) \quad (5.40)$$

$$+ V_{th,p2} + \frac{n_{p2}}{n_{n6}}\left(V_{DD} + V_{th,n6} - V_{QB}\right)$$

Using the procedure as described in Section 5.5.3 (a), the following regression equation has been obtained for MI-12T;

$$\mathrm{V_{WSNM,MI\text{-}12T}} = 0.0931 \times \ln\left(\frac{W_{n6}/L_{n6}}{W_{p2}/L_{p2}}\right) + 0.962 V_{DD} - 0.174 \quad (5.41)$$

For 45 nm technology, choosing V_{DD} = 0.4V, L_{p2}= L_{n6}= 45nm, (W_{n6}/W_{p2}) = 108nm/60nm = 1.8 (PR ratio chosen as discussed in Section 5.3), value of WSNM is obtained from equation 5.41 as;

$$\boxed{\mathrm{V_{WSNM,MI\text{-}12T}} = 0.265\mathrm{V}}$$

Comparison of values of WSNM between simulated and estimated values through analytical and regression equation at 0.4V is shown in Table 5.14.

Table 5.14: Comparison of WSNM between simulated and estimated values through analytical and regression equation at 0.4V

Types of SRAM cells	**WSNM (mV)** Simulated values	**WSNM (mV)** Estimated through analytical equation using butterfly curve	**WSNM (mV)** Estimated through regression equation
C6T	090.0	102	154
M7T	126.2	143	179
MPT8T	218.0	237	286
M8T	186.0	200	247
M9T	160.0	183	200
MI-12T	**226.0**	239	265

Note: The value of WSNM estimated from analytical equations is within (5.4% to 11.7%) to those that are observed with simulated values. The value of WSNM estimated from regression equations is within (14.7% to 41.7%) to those that are observed with simulated values. This is high in comparison to Hold SNM, and RSNM calculations due to the following reason:

Unlike for the hold and read margin case, using the sub-V_T approximation for I_{MN6} and I_{MP2} does not yield an accurate solution of V_Q as given in [43]. This may be because the exponential behavior of I_D (V_{GS}) is accurate only for V_{GS}< 200mV [43].

This error yields significantly different result for V_Q, when applied to the drive fight between I_{MN6} and I_{MP2} at V_{QB}=0. Thus, finding an accurate value of V_Q depends on accurately modeling current in the moderate-V_T region which is included in future scope at the end of this chapter.

5.6. FINAL RESULTS AND DISCUSSIONS

This section presents the comparative analysis of proposed designs of SRAM cell at 45nm with referenced architectures. Also, a comparison of published results is done at 180nm technology. Then impact of scaling is obtained from 180nm to 45 nm on performance of SRAM cell.

- **At 45 nm**

All five proposed designs of SRAM cell (M7T, MPT8T, M8T, M9T and MI-12T) designs are compared with referenced cells, with similar transistor numbers, operated in sub-threshold region at 45 nm for 0.4V supply voltage. Here, for comparison 6T, 7T, 8T and 12T SRAM cells of the referenced architectures [44][32][45][46] are also designed to obtain their results in the same simulation setup for sub-threshold operation to maintain uniformity of simulation environment.

The values of parameters like RSNM, WSNM, SINM, SVNM, WTI, WTV, read delay, write delay and leakage power consumption in hold mode for different proposed and referenced SRAM cells (with same number of transistor count) are shown in Table 5.15 for comparison.

Figure 5.52 (a) shows histogram comparison of results of proposed SRAM designs, along with C6T, in terms of RSNM, WSNM, and read/write delay and leakage power in hold mode. Figure 5.52 (b) shows the histogram comparison of WTI, WTV, SINM and SVNM of all C6T and proposed SRAM cells at 45 nm technologies.

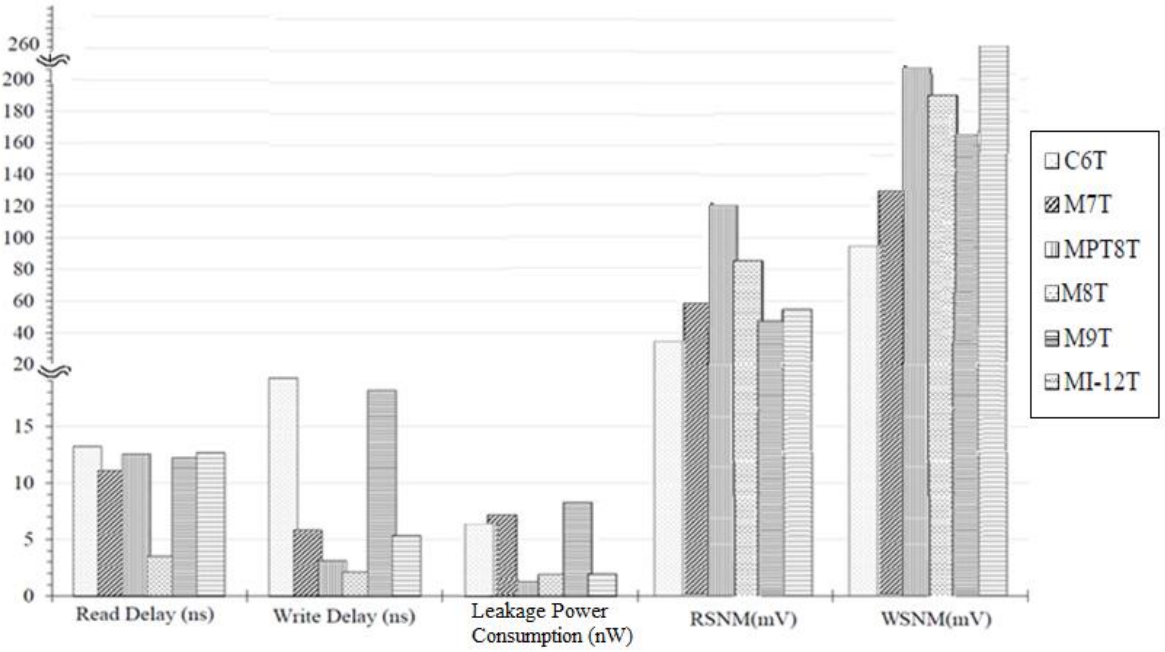
Table 5.16 and Table 5.17 shows the write ability and read stability performance of all proposed SRAM cells at 45 nm respectively.

Table 5.18 shows the comparison of all proposed SRAM cells with C6T at 45 nm.

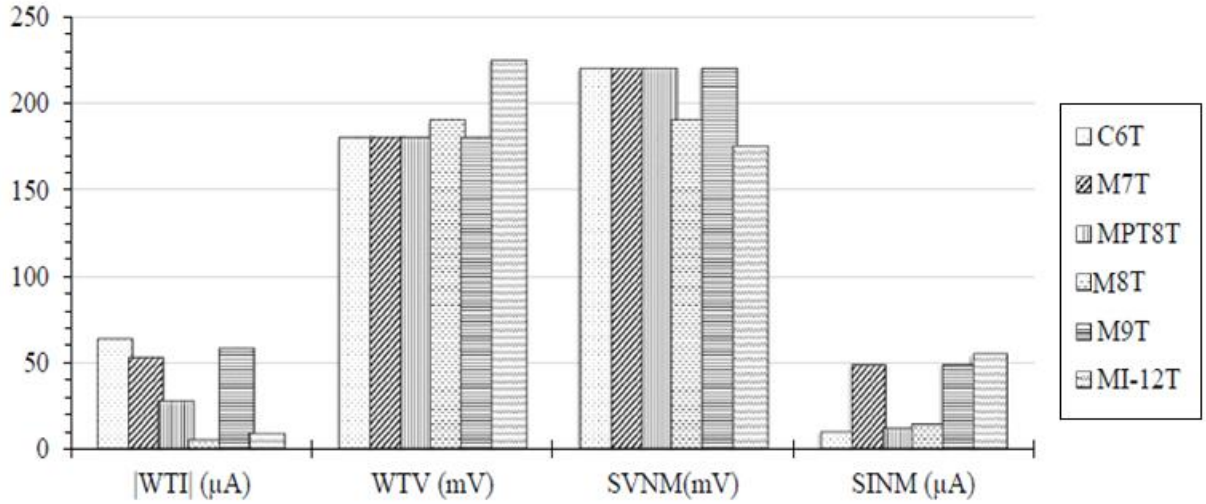
These designs are also compared with published designs at 180 nm technology to get impact of technology scaling.

Table 5.15: Comparison of proposed with referenced SRAM cells (for 7T, 8T, 9T and 12T configurations) at 45 nm technology, V_{DD}= 0.4V

References / Proposed SRAM cells	Types of SRAM cell	RSNM		WSNM		Read Delay		Write Delay		Leakage Power Consumption in Hold mode	
		RSNM (mV)	% increment in RSNM in proposed cells	WSNM (mV)	% increment in WSNM in proposed cells	Read Delay (ns)	% decrement in Read Delay in proposed cells	Write Delay (ns)	% decrement in write Delay in proposed cells	Hold-Power (nW)	% less power dissipation in proposed cells
Ref. [44]	7T	042		102.7		15.87		03.74		5.29	
Proposed	**M7T**	060	**30.0%**	126.2	**18.6%**	11.70	**26.2%**	01.15	**69.2%**	6.01	11.9% **(more)**
Ref. [32]	8T	040		154		05.87		04.41		4.70	
Proposed	**MPT8T**	120	**66.6%**	218	**29.3%**	02.11	**64.0%**	01.53	**65.3%**	2.31	**50.8%**
Proposed	**M8T**	085	**52.9%**	186	**17.2%**	00.74	**87.3%**	00.71	**83.9%**	3.14	**33.1%**
Ref. [46]	9T	035		147		06.58		13.11		7.44	
Proposed	**M9T**	043	**18.6%**	160	**8.1%**	02.28	**65.3%**	10.10	**22.9%**	8.10	8.1% (more)
Ref. [45]	12T	50.1		158		03.33		06.54		6.82	
Proposed	**MI-12T**	54.4	**32.7%**	226	**30.1%**	01.54	**53.7%**	01.51	**76.9%**	3.67	**46.1%**



(a)



(b)

Figure 5.52: The comparative histograms of SRAM cells at 45 nm

In Figure 5.52 (a), a change of scale on y-axis is shown with a kink (~) to show the histograms for RSNM in its entire range. This is done to show the comparisons of RSNM, WSNM, read delay, write delay, and leakage power consumption in hold mode on same axis.

Robustness of write operation is given by WSNM, WTI, and WTV which are independent of each other as indicated by performance order, from best to worst, given below;

WSNM in decreasing order: MI-12T > MPT8T > M8T > M9T > M7T > C6T

WTI in increasing order: M8T < MI-12T << MPT8T < M7T < M9T < C6T

WTV in increasing order: MPT8T = M7T = M9T = C6T < M8T< MI-12T

It is observed that none of the proposed cell has best value for all three-metrics related to write ability (i.e. highest WSNM, least WTI, and least WTV). For example, MI-12T has highest WSNM and lower WTI, and a highest WTV. Similarly, C6T has least WSNM and WTI, but a highest WTV. Concluding the write ability metric by mere observation of above performance order (of WSNM, WTI, and WTV) may lead to a wrong outcome.

Thus, we need to estimate a performance index value for write ability metric for each proposed SRAM cell through multi criteria decision analysis taking all three metrics i.e. WSNM, WTI, and WTV into account. Table 5.16 shows the write ability index for all proposed SRAM cells.

Table 5.16: Write ability metric of proposed SRAM cells at 45 nm

SRAM cells	**|WTI| (µA) X1**	**D1= max-X1**	**I1=D1/R1**	**WTV (mV) X2**	**D2= max-X2**	**I2=D2/R2**	**WSNM (mV) X3**	**D3= X3-min**	**I3=D3/R3**	**INDEX (I) =11+12+13**
C6T	64.00 *max*	00.00	0.00	180	45	1.00	090.0 *min*	00.0	0.00	1.00
M7T	53.31	10.69	0.18	180	45	1.00	126.2	036.2	0.26	1.44
MPT8T	28.00	36.00	0.61	180	45	1.00	218.0	128.0	0.94	2.55
M8T	05.01	58.99	1.00	190	35	0.77	186.0	096.0	0.70	2.47
M9T	58.90	05.10	0.08	180	45	1.00	160.0	070.0	0.51	1.59
MI-12T	08.70	55.30	0.93	225 *max*	00	0.00	226.0	136.0	1.00	1.93
Range››	R1= 58.9			R2=45			R3=136			
Range (R) of a performance metric (WSNM, WTI, and WTV) = maximum value – minimum value										

From Table 5.16, write ability performance order (in decreasing order according to Index I) from best to worst: **MPT8T> M8T > MI-12T > M9T > M7T > C6T**

Robustness of read operation is given by RSNM, SINM, and SVNM which are independent of each other as indicated by performance order, from best to worst, given below;

RSNM in decreasing order: MPT8T > M8T > M7T > MI-12T > M9T > C6T

SINM in decreasing order: MI-12T > M7T > M9T >> M8T > MPT8T > C6T

SVNM in decreasing order: C6T = M7T = MPT8T=M9T > M8T > MI-12T

It is observed that none of the proposed cell has best value for all three-metrics related to read stability (i.e. highest RSNM, highest SINM, and highest SVNM). For example, MPT8T has highest RSNM and SVNM, but a lower SINM. Similarly, C6T has least RSNM and SINM, but a higher SVNM

Thus, we need to estimate a performance index value for read stability metric for each proposed SRAM cell through multi criteria decision analysis taking all three metrics i.e. RSNM, SINM, and SVNM into account.

Table 5.17 shows the read stability index for all proposed SRAM cells.

Table 5.17: Read stability metric of proposed SRAM cells at 45 nm

SRAM cells	**SVNM (mV)** **X1**	**D1= X1-min**	**I1=D1/ R1**	**SINM (µA)** **X2**	**D2= X2-min**	**I2=D2 /R2**	**RSNM (mV)** **X3**	**D3= X3-min**	**I3=D3 / R3**	**INDEX (I) =11+12+13**
C6T	220	45.00	1.00	10.00 *min*	00.00	0.00	037.0 *min*	00.00	0.00	1.00
M7T	220	45.00	1.00	49.21	39.21	0.88	060.0	23.00	0.26	2.14
MPT8T	220	45.00	1.00	12.00	02.00	0.04	123.0	86.00	1.00	2.04
M8T	190	15.00	0.33	14.01	04.01	0.09	088.0	51.00	0.59	1.01
M9T	220	45.00	1.00	49.20	39.20	0.88	043.0	06.00	0.07	1.95
MI-12T	175 *min*	00.00	0.00	54.50	44.50	1.00	054.4	17.40	0.20	1.20
Range››	R1= 45			R2=44.5			R3=86			
Range (R) of a performance metric (RSNM, SINM, and SVNM) = maximum value - minimum value										

From Table 5.18, read stability performance order (in decreasing order according to Index I) from best to worst: **M7T> MPT8T> M9T> MI-12T> M8T> C6T**

Evaluation of read stability and write ability performance order through observation is shown in Appendix F for both 45 nm / 180 nm technology nodes.

Table 5.18 shows the comparison of all proposed SRAM cells with C6T at 45 nm

Table 5.18: Percentage comparison of all proposed SRAM cells with C6T at 45 nm

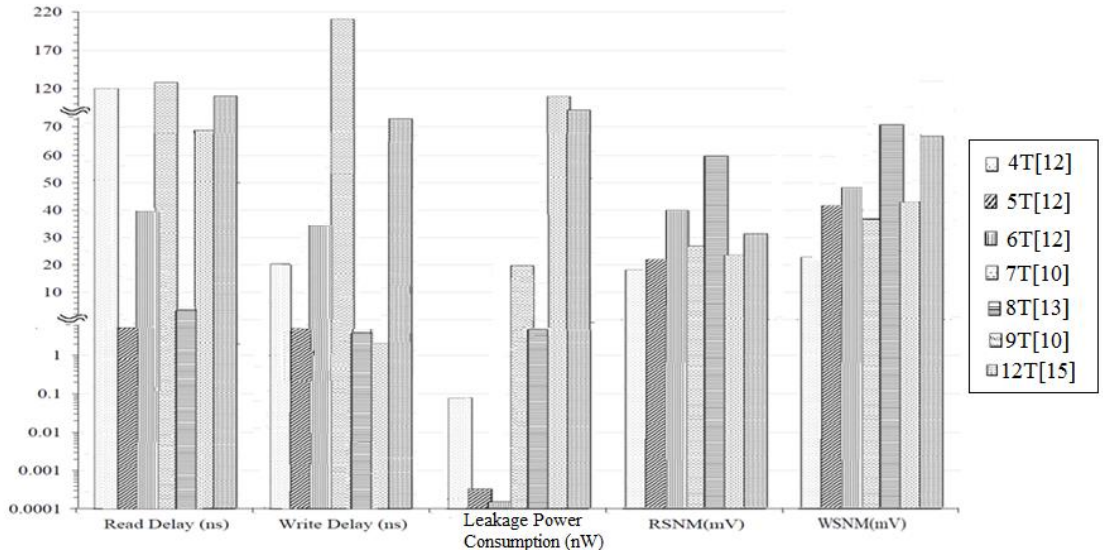
Types of SRAM cells / Parameters	M7T	MPT8T	M8T	M9T	MI-12T
% increment in Hold SNM	Same value as C6T	Same value as C6T	Same value as C6T	Same value as C6T	29.2%
% increment in RSNM	43.3%	**71.6%**	60.0%	20.9%	37.5%
% increment in SVNM	Same value as C6T	Same value as C6T	13.6%	Same value as C6T	20.4%
% increment in SINM	**79.6%**	16.6%	28.6%,	79.6%	81.9%
% increment in WSNM	28.6%	58.7%	51.6%	43.7%	**60.1%**
% decrement in WTI	16.7%	56.2%	**92.1%**	07.9%	86.4%
% decrement in WTV	Same value as C6T	Same value as C6T	5.2% (more)	Same value as C6T	20% (more)
% decrement in Read Delay	16.6%	05.3%,	**73.8%,**	07.5%	04.5%
% decrement in Write Delay	69.6%	83.5%,	**89.1%,**	05.6%	72.0%
% less leakage Power Consumption in hold mode	10.7% (more power consumption here)	**54.6%**	32.1%	76.4% (more power consumption here)	30.7%

- **At 180 nm**

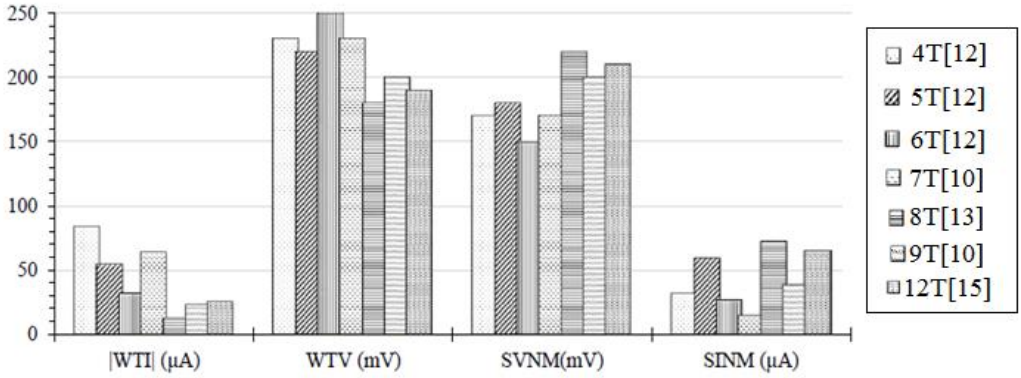
For 180 nm technology, a literature survey of SRAM cells with 4, 5, 6, 7, 8, 9, 12 transistor counts have been done. These referenced designs were simulated in the same simulation setup for sub-threshold operation to maintain uniformity of simulation environment and their RSNM, read/write delay and leakage power consumption in hold mode have been obtained. This data has been compiled in Table 5.1(b) and is presented in Figure 5.53 for the sake of comparison.

Figure 5.53 shows comparison of results of only those referenced SRAM designs which show the best results (out of all designs that were studied for a fixed transistor count configuration) in Table 5.1(a)) in terms of leakage power.

In Figure 5.53 (a), a change of scale on y-axis is shown with a kink (~) to show the performance metrics in their entire range. This is done to show the comparisons of RSNM, WSNM, read delay, write delay, and leakage power consumption in hold mode on same axis.



(a)



(b)

Figure 5.53: The comparative histograms of SRAM cells at 180 nm

Robustness of write operation is given by WSNM, WTI, and WTV which are independent of each other as indicated by performance order, from best to worst, given below;

WSNM in decreasing order: 8T[13]>12T[15] > 6T[12] > 9T[10] > 7T[10] > 5T[12] > 4T[12]

WTI in increasing order: 8T[13] < 9T[10] < 12T[15] < 6T[12] < 5T[12] < 7T[10] < 4T[12]

WTV in increasing order: 6T[12] < 7T[10] = 4T[12] < 5T[12] < 9T[10] < 12T[15] < 8T[13]

It is observed that none of the cell has best value for all three-metrics related to write ability (i.e. highest WSNM, least WTI, and least WTV). For example, 8T[13] has highest WSNM and lower WTI, but a highest WTV. Similarly, 4T[12] has least WSNM and least WTI, but a moderate WTV.

Thus, we need to estimate a performance index value for write ability metric for each SRAM cell through multi criteria decision analysis taking all three metrics i.e. WSNM, WTI, and WTV into account. Table 5.19 shows the write ability index for all SRAM cells.

Table 5.19: Write ability metric of SRAM cells at 180 nm

SRAM cells	**WSNM (mV)** **X1**	**D1= X1-min**	**I1=D1/ R1**	**|WTI| (µA)** **X2**	**D2= max-X2**	**I2=D2 /R2**	**WTV (mV)** **X3**	**D3= max-X3**	**I3=D3 / R3**	**INDEX (I) =11+12+ 13**
4T[12]	22.1 *min*	00.00	0.00	84.0 *max*	00.00	0.00	230	20.00	0.33	0.33
5T[12]	41.0	18.90	0.39	55.2	28.80	0.40	220	30.00	0.50	1.29
6T[12]	47.7	25.60	0.53	32.3	51.70	0.72	250 *max*	00.00	0.00	1.25
7T[10]	38.0	15.90	0.34	64.1	19.90	0.28	230	20.00	0.33	0.95
8T[13]	70.2	48.10	1.00	13.0	71.00	1.00	220	30.00	0.50	2.50
9T[10]	44.8	22.70	0.47	23.1	60.90	0.85	200	50.00	0.83	2.15
12T[15]	68.5	46.40	0.96	25.5	58.50	0.82	190	60.00	1.00	2.78
Range››	R1=48.1			R2=71.0			R3=60			
Range (R) of a performance metric (WSNM, WTI, and WTV) = maximum value - minimum value										

From Table 5.19, write ability performance order (in decreasing order according to Index I) from best to worst:

12T[15]> 8T[13]> 9T[10]> 5T[12]> 6T[12]> 7T[10]> 4T[12]

Robustness of read operation is given by RSNM, SINM, and SVNM which are independent of each other as indicated by performance order, from best to worst, given below;

RSNM in decreasing order: 8T[13] > 12T[15] > 7T[10] > 9T [10] > 5T[12] > 6T[12] > 4T[12]

SINM in decreasing order: 8T[13] > 12T[15] > 5T[12] > 9T[10] > 4T[12] > 6T[12] > 7T[10]

SVNM in decreasing order: 12T[15] < 9T[10] < 8T[13] = 5T[12] < 7T[10] = 4T[12] < 6T [12]

It is observed that none of the proposed cell has best value for all three-metrics related to read stability (i.e. highest RSNM, highest SINM, and highest SVNM). For example, 8T[13] has highest RSNM and SINM, but a lower SVNM. Similarly, 4T[12] has least RSNM and lower SVNM, but moderate SINM. Thus, we need to estimate a performance index value for read stability metric for each SRAM cell through multi criteria decision analysis taking all three metrics i.e. RSNM, SINM, and SVNM into account. Table 5.20 shows the read stability index for all SRAM cells.

Table 5.20: Read stability metric of SRAM cells at 180 nm

SRAM cells	RSNM (mV) X1	D1= X1-min	I1=D1/ R1	SVNM (mV) X2	D2= X2-min	I2=D2/ R2	SINM (µA) X3	D3= X3-min	I3=D3/ R3	INDEX (I)= 11+12+13
4T[12]	18 *min*	00.00	0.00	170	20.00	0.33	32.1	17.30	0.30	0.63
5T[12]	22.0	04.00	0.09	180	30.00	0.50	60.1	45.30	0.77	1.36
6T[12]	20.1	02.10	0.05	150 *min*	00.00	0.00	26.9	12.10	0.21	0.26
7T[10]	26.7	08.70	0.21	170	20.00	0.33	14.8 *min*	00.00	0.00	0.54
8T[13]	59.6	41.60	1.00	180	30.00	0.50	73.0	58.20	1.00	2.50
9T[10]	23.4	05.40	0.12	200	50.00	0.84	38.4	23.60	0.41	1.37
12T[15]	32.0	14.00	0.33	210	60.00	1.00	65.4	50.60	0.87	2.20
Range››	R1= 41.6			R2=60			R3=58.2			
Range (R) of a performance metric (RSNM, SINM, and SVNM) = maximum value - minimum value										

From Table 5.20, read stability performance order (in decreasing order according to Index I) from best to worst:

8T[13]> 12T[15]> 9T[10]> 5T[12]> 4T[12]> 7T[10] > 6T [12]

Observations:

(i) Comparison of Results of Proposed Designs at 45 nm

Table 5.15 show that, in comparison to referenced designs, proposed SRAM designs have higher RSNM, lower read / write delay and less leakage power consumption (except M7T and M9T) in hold mode.

Figures 5.52 show that in sub-threshold region at 0.4V supply:

- **Write Ability of SRAM Cell:** Based on index value, performance in the decreasing write ability is given as MPT8T> M8T > MI-12T > M9T > M7T > C6T as per Table 5.16.
- **Read Stability of SRAM Cell:** Based on index value, performance in the decreasing read stability is given as M7T> MPT8T> M9T> MI-12T> M8T> C6T as per Table 5.17.
- **Read Delay of SRAM Cell:** M8T shows least average read delay. Average read delay performance in the decreasing order is given as: M8T<<M7T< M9T< MPT8T< MI-12T< C6T. Variability of all proposed cell is observed to be ranging from 0.04 to 0.40 at supply voltage

of 0.4V with M7T having the least value. Read delay and its variability reduces with reduction in power supply voltage.

- **Write Delay of SRAM Cell:** M8T shows least average write delay at supply voltage of 0.4V. Average write delay performance in the decreasing order is given as: M8T< MPT8T< MI-12T< M7T<< M9T< C6T. Variability of all proposed cell is observed to be ranging from 0.016 to 0.19 at supply voltage of 0.4V with MPT8T having the least value. Write delay its and variability reduces with reduction in power supply voltage.

- **Leakage Power Consumption in Hold Mode:** MPT8T is most power efficient design. Leakage power consumption in the increasing order is given as: MPT8T < M8T < MI-12T < C6T < M7T < M9T.

(ii) Comparison of Proposed SRAM Cells with C6T at 45 nm

The comparative analysis in Table 5.18 exhibit that **M8T, MPT8T** and **MI-12T** designs have low leakage power consumption along with improved design parameters like achieving high read stability, high write ability, fast read & write operation.

M7T and M9T are also achieving high read stability, high write ability, fast read and write operation but leakage power consumption is increasing (10.7%, and 76.4% respectively) in comparison to C6T.

(iii) Comparison of Results of Referenced Designs At 180 nm Technology Among Themselves

Figures 5.53 show that in sub-threshold region:

- **Write Ability of SRAM Cell:** Based on index value performance in the decreasing write ability is given as 12T[15] > 8T[13] > 9T[10] > 5T[12] > 6T[12] > 7T[10] > 4T[12] as per Table 5.19.

Read Stability of SRAM Cell: Based on index value, performance in the decreasing read stability is given as 8T [13] > 12T [15] > 9T [10] > 5T [12] > 4T [12] > 7T [10] > 6T [12] as per Table 5.20.

- **Read Delay of SRAM Cell:** 5T[12] SRAM cell has least value of read delay.

- **Write Delay of SRAM Cell:** 9T[10] SRAM cell has least value of write delay.

- **Leakage Power Consumption in Hold Mode of SRAM Cell:** 6T [12] is most power efficient SRAM cell with least leakage power consumption in hold mode.

(iv) Effect of Technology Scaling

At 45 nm technology nodes, all proposed designs show increased value of RSNM and WSNM, reduced values of read/write delay and increased values of leakage power consumption in hold mode as compared to all SRAM cells implemented at 180 nm. For few cells like 7T, 8T, and 12T, leakage power consumption reduces due to different cell design. Appendix E contains table of percentage change in all performance metrics of SRAM cells (with same transistor count) at 45 nm in comparison to 180nm technology.

5.7. CONCLUSIONS

This chapter explores the design space of proposed M7T, MPT8T, M8T, M9T and MI-12T SRAM cells implemented at 45 nm technology node which are suitable for sub-threshold operation. The thorough analyses on the impacts of read stability, write ability, average write delay, average read delay and leakage power consumption in hold mode, have been done. The proposed memory cells exhibit improvement in performance over C6T.

Here, at 45 nm, comparison of proposed SRAM cells with referenced designs [32][44][45][46] and with each other are done. At 180 nm, performance parameters of low power referenced designs are compiled in Table 5.1(b), and used for comparison.

The overall results of the SRAM cells show following conclusions at 45 nm and 180 nm technology nodes:

(i) Comparison of Results of Proposed Designs with Respective Referenced Designs at 45nm Technology

- RSNM- Proposed designs show an RSNM increment ranging from 30% to 66.6 %.
- WSNM- Proposed designs show an WSNM increment ranging from 8.1% to 30.1 %.
- Average Read Delay- Proposed designs show an RSNM decrement ranging from 26.2% to 87.3 %.
- Average Write Delay- Proposed designs show an RSNM decrement ranging from 22.9% to 83.9 %.
- Leakage Power Consumption in hold mode- Proposed designs show an RSNM decrement ranging from 16.8% to 50.8 % except M7T and M9T which consumes 11.9% and 8.1% more leakage power respectively.

(ii) Comparison of Results of Proposed Designs Among Themselves at 45nm Technology

- **Impact of Design Configuration on RSNM of SRAM Cell:** Among all proposed SRAM cells, MPT8T has highest RSNM of 120mV. The increased RSNM values in MPT8T and M8T are due to addition of extra transistor in parallel to access transistor which helps in maintaining proper logic '0' at internal storage node. Also, this overcomes the voltage degradation at BLB/BL nodes i.e. increase the node voltage for logic '1' stored.

- **Impact of Design Configuration on WSNM of SRAM Cell:** Among all proposed SRAM cells, MI-12T has highest WSNM of 226mV. This is due to removal of positive feedback in bi-stable element in write operation due to stacking of pull down path.

- **Impact of Design Configuration on Average Read Delay of SRAM Cell:** Among all proposed SRAM cells, M8T has minimum read delay of 0.74 ns. This is due to extra current driven by extra added transistor in parallel to access transistor which consequently decreases the charging/ discharging time of the internal node of SRAM cell, hence decreases the read delay. Variability of all proposed cell is observed to be ranging from 0.04 to 0.40 at supply voltage of 0.4V with M7T having the least value making it less sensitive to process variation. Read delay and its variability reduces with reduction in power supply voltage.

- **Impact of Design Configuration on Average Write Delay of SRAM Cell:** Among all proposed SRAM cells, M8T has minimum write delay of 0.71 ns. This is due to extra current driven by extra added transistor in parallel to access transistor which consequently decreases the charging/ discharging time of the of the internal node of SRAM cell, hence decreases the write delay. Variability of all proposed cell is observed to be ranging from 0.016 to 0.19 at supply voltage of 0.4V with MPT8T having the least value making it less sensitive to process variation. Write delay its and variability reduces with reduction in power supply voltage.

- **Impact of Design Configuration on Leakage Power Consumption in Hold Mode:** Among all proposed SRAM cells, MPT8T has least leakage power consumption (in hold mode) of 2.31 nW. This is due to proper logic '0' and logic '1' at internal storage nodes (Q, and QB). This causes full turn OFF of pull up and pull down transistors in bi-stable element of MPT8T thereby reducing the leakage current during hold mode.

(iii) Comparison of All Proposed SRAM Cells with C6T at 45 nm:

The comparative analysis exhibit that **M8T, MPT8T** and **MI-12T** designs have low leakage power consumption along with other improved design parameters like achieving high read stability, high write ability, fast read & write operation. Thus, these designs can be an attractive choice for low power based application in scaled technology. Whereas M7T and M9T also show improved design parameters like achieving high read stability, high write ability, fast read & write operation but higher leakage power consumption as compared to C6T.

(iv) Comparison of Results of Referenced Designs at 180nm Technology Among Themselves

In comparison with other published low power references with same transistor count, the 8T SRAM cell [13] and 12T SRAM cell [15] are top two cells with higher read stability, & higher write ability, 5T SRAM cell [12] has lowest read delay, 9T SRAM cell [10] has lowest write delay and 6T SRAM cell [12] has least leakage power consumption in hold mode.

(v) Effect of Technology Scaling

At 45 nm technology nodes, all proposed designs show 42.7% average increment in RSNM and 65.8% average increment in WSNM, 85.6% and 24.7% average reduction in read and write delay respectively and 24.9% increment in leakage power consumption in hold mode as compared to corresponding SRAM cells implemented at 180 nm. For few cells like 7T, 8T, and 12T, leakage power consumption reduces due to different cell design.

(vi) Modeling Analysis

At 0.4 V supply voltage, analytical equations, obtained under steady state condition for read, write and hold operation, give WSNM, RSNM, and Hold SNM within (5.4% to 11.7%), (6.9% to 24.5%), (3.84% to 3.9%) respectively as compared to simulated values.

(vii) Regression Analysis

At 0.4 V supply voltage, simplified equations which are obtained through multiple regression analysis (to obtain the impact of varying CR, PR, and V_{DD} on read, write and hold operation), give WSNM, RSNM, and Hold SNM within (14.7% to 41.7%), (10.4% to 34.8%), and (5% to 12.8%) respectively as compared to simulated values. These equations can be used to get first order estimate of the impact of varying CR, PR, and V_{DD} on read, write and hold stability.

For quick comparison, Figure 5.54 and Figure 5.55 show the comparative Design Space Exploration (DSE) chart of SRAM cells at 45 nm and 180 nm technology respectively.

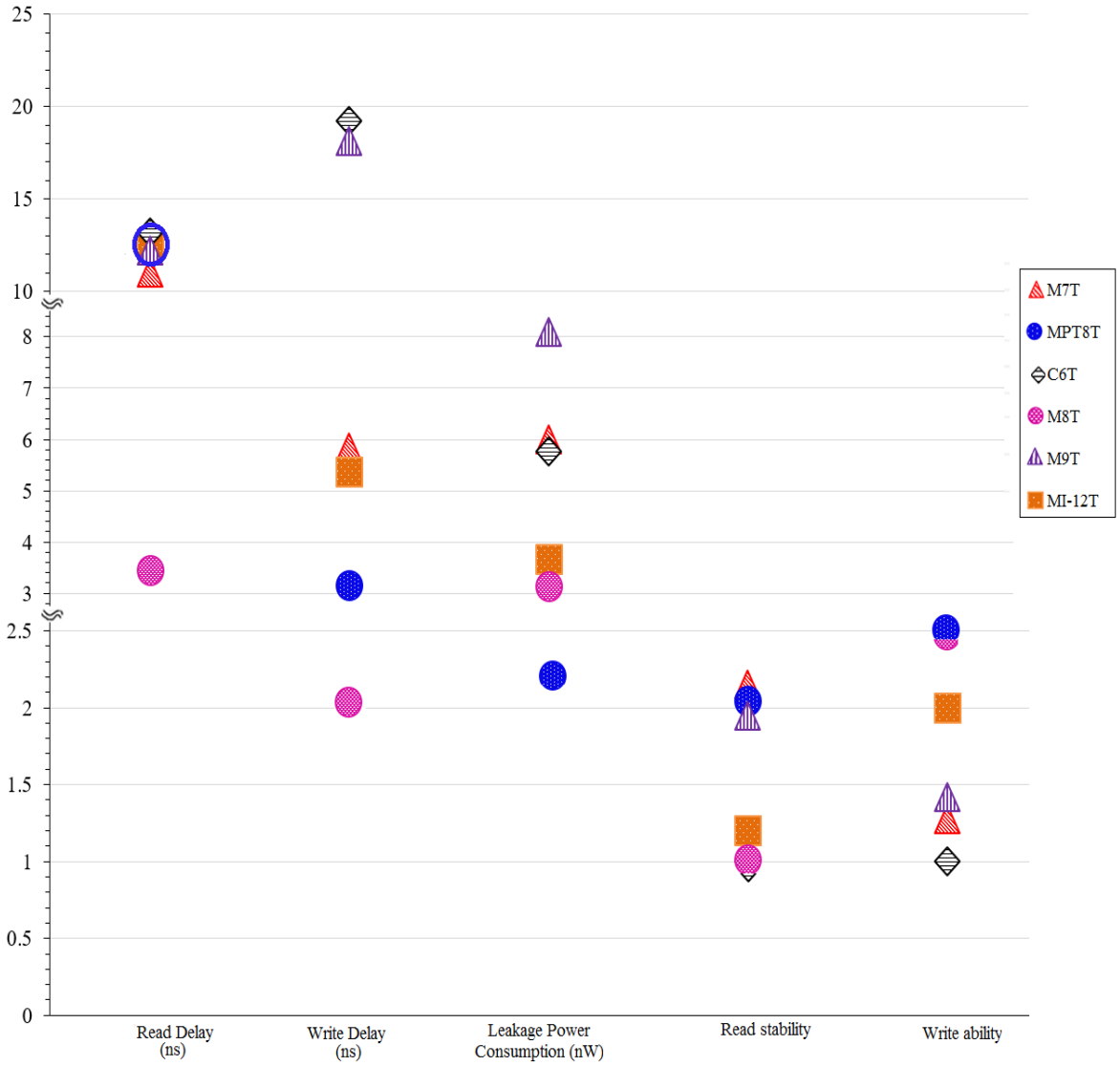


Figure 5.54: DSE chart of all five proposed SRAM cells as compared to C6T at 45 nm technology

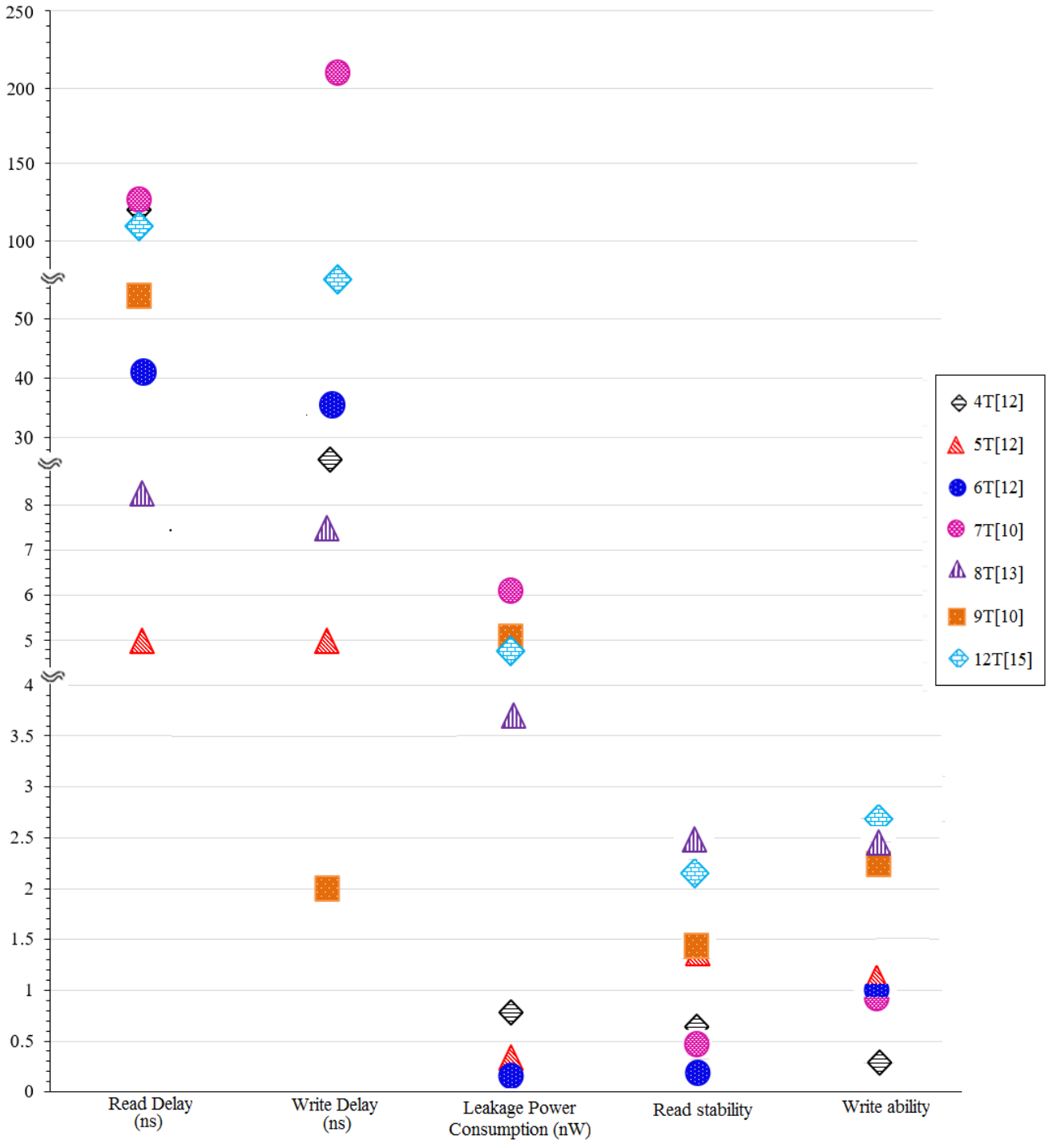


Figure 5.55: DSE chart of referenced SRAM cells at 180 nm technology

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CHAPTER 6

CONCLUSIONS & FUTURE SCOPE

The objective of this thesis is architectural exploration and implementation of low power arithmetic circuits and SRAM cells in sub-threshold region of operation. The main focus is to explore the optimum architectures and suitable logic families for low power consumption and propagation delay for logarithmic prefix adders, column compression multipliers and SRAM cells in sub-threshold regime at two different nanometer technology nodes.

In this thesis, we have chosen to explore the design space of parallel prefix adder architectures (CLA, KSA, and HCA), two column compressions multipliers (Wallace tree and Dadda multipliers) and SRAM cells in terms of power consumption, delay, and power-delay product in sub-threshold region. These are frequently used in arithmetic and on-chip memory units in an SOC. Their performance is also obtained at 45 nm and 180 nm technology nodes to find the impact of scaling on their performance. Outcomes of this exploration of adders, multipliers and SRAM cells are concluded in section 6.1, 6.2, and 6.3 respectively. Future scope of this work is included in section 6.4.

6.1. CONCLUSIONS ON ADDERS

The overall results of the CLA, KSA and HCA show following conclusions at 45 nm /180 nm technology nodes:

(i) Power Consumption

The amount of power consumption directly depends on operand sizes and the complexity of the adder architectures. The large operand size adders consume more power for all logic design style at the same voltage supply and both technology nodes.

- At 45 nm, HCA architecture has the least power consumption. HCA based designs consume lesser power consumption varying from 8.2% to 77.7 % as compared to KSA based designs. Whereas as compared to CLA designs, they consume lesser power consumption, ranging from 79.4% to 96.8 %, for all bit operands.
- Similarly, for 180 nm, HCA architecture (based designs) has the least power consumption. It consumes lesser power consumption varying from 21.2% to 56.1 % as compared to KSA.

Whereas as compared to CLA, it consumes lesser power consumption varying from 89.4% to 97.1 % for all bit operands.

Therefore, HCA is the most power efficient architecture as compared to KSA and CLA architecture in sub-threshold region.

(ii) Propagation Delay

As operand size increases, the complexity of the circuits and the number of gates count in the propagation path also increase leading to increase in propagation delay. The large operand size adders show higher propagation delay for all logic design style at the same voltage supply and both technology nodes.

- At 45 nm, CLA architecture (based designs) has the least propagation delay. It consumes lesser propagation delay varying from 44.8% to 76.4 % as compared to KSA. Whereas as compared to HCA (based designs), it gives lesser propagation delay varying from 66.6% to 79.8 % for all bit operands.
- Similarly, for 180 nm, CLA architecture has the least propagation delay. It consumes lesser propagation delay varying from 82.6% to 93.8 % as compared to KSA. Whereas for HCA, it gives lesser propagation delay varying from 81.2% to 88.6 % for all bit operands.

Therefore, CLA is the high-speed adder architecture as compared to KSA and HCA architecture for sub-threshold operation.

(iii) Power-Delay Product:

In comparison to other proposed design showing highest power-delay product (at both technology nodes):

- For low bit operands (i.e. 8b / 16b), KSA and HCA architecture using Static-CMOS logic gives lowest power-delay product.
    - (63.7% / 29.24%) lesser power-delay product for KSA.
    - (32.69% / 43.64%) lesser power-delay product for HCA.
- For higher bit operands (i.e. 32b / 64b), KSA and HCA architecture using HYB-TG logic gives lowest power-delay product
    - (40.59% / 58.99%) lesser power-delay product for KSA.
    - (3.23% / 15.32%) lesser power-delay product for HCA.

(iv) Effect of RBB

HYB-TG and HYB-PT logic families with RBB do not function properly at both technology nodes in sub-threshold region.

The use of RBB scheme improves sub-threshold conduction current to perform circuit operations in Static-CMOS logic. At 45 nm / 180 nm technology, the average decrement in propagation delay compared to circuit design without RBB is approximately 61.87% / 18.5%. The increments in average power consumption and power-delay product is by 77.03% / 22.5% and 38.3% / 7.3% respectively.

The use of RBB scheme in CMOS inverter shows that NM_L reduces by 62.2% / 71.7 % at 45nm /180nm technology respectively.

(v) Effect of Technology Scaling

At 45 nm, the power consumption is higher than 180 nm technology for all adder designs using different logic design styles. The power consumption is increasing due to increments in the leakage current at 45 nm technology as compared to 180 nm technology since supply voltage is kept same at 0.4V.

6.2. CONCLUSIONS ON MULTIPLIERS

The overall results of the Wallace tree and Dadda multipliers show following conclusions at 45 nm / 180 nm technology nodes.

(i) Power Consumption

- For LOC based architectures:

  For both technology nodes, **Dadda multiplier (based designs)** has the least power consumption in comparison to corresponding Wallace tree multiplier designs as given below.

  At 45 nm: For 4x4-bit, they have lesser power consumption varying from 28.6% to 30.9%. Whereas, for 8x8-bit, they consume lesser power consumption, varying from 23.2% to 24.1%.

  At 180 nm: For 4x4-bit, they consume lesser power consumption varying from 4.1% to 8.4%. Whereas, for 8x8-bit, they consume lesser power consumption, varying from 1.6% to 1.7%.

- For Mixed L/H based architectures:

  For both technology nodes, **Dadda multiplier (based designs)** has the least power consumption as compared to corresponding Wallace tree multiplier based designs as given below.

  At 45 nm: For 4x4-bit, they have lesser power consumption varying from 35.1% to 35.8%. Whereas, for 8x8-bit, they consume lesser power consumption, varying from 14.9% to 21.5% as compared to Wallace tree multipliers.

  At 180 nm: For 4x4-bit, they consume lesser power consumption varying from 12.6% to 12.9%. Whereas, for 8x8-bit, they consume lesser power consumption, varying from 1.7% to 4.1%.

- At 45 nm, for both sizes (4x4-bit and 8x8-bit), among all eight (LOC as well Mixed L/H based) proposed multipliers implemented, **Dadda-45-L-RCA** is the most power efficient architecture.

  It consumes 42.6% (for 4x4-bit), and 86.5 % (for 8x8-bit) less power in comparison to highest power consuming design which is Wallace tree-45-L/H-HCA.

- At 180 nm, for both sizes, **Dadda-180-L-RCA** is the most power efficient architecture among all eight proposed designs.

  It has 56.6% (for 4x4-bit) and 60.8% (for 8x8-bit) less power consumption less power in comparison to highest power consuming design which is Wallace tree-180-L/H-HCA.

(ii) Propagation Delay

- For LOC based architectures:

  Dadda multiplier (based designs) has the least propagation delay at both technology nodes in comparison to corresponding Wallace tree multiplier designs as given below.

  At 45 nm: For 4x4-bit, **Dadda multipliers** give lesser propagation delay varying from 19.9% to 28.9%. Whereas for 8x8-bit, they give lesser propagation delay varying from 7.3% to 10.5% as compared to Wallace tree multipliers.

  At 180 nm: For 4x4-bit, **Dadda multipliers** give lesser propagation delay varying from 0.9% to 2.2%. Whereas for 8x8-bit, they give lesser propagation delay varying from 0.8% to 1.1% as compared to Wallace tree multipliers.

- For Mixed L/H based architectures

  Dadda multiplier (based designs) have the least propagation delay at both technology nodes in comparison to corresponding Wallace tree multiplier designs as given below.
  At 45 nm: For 4x4-bit, Dadda multipliers give lesser propagation delay varying from 19.9 % to 21.3%. Whereas, for 8x8-bit, they give lesser propagation delay varying from 17.2% to 19.5% as compared to Wallace tree multipliers.
  At 180 nm: For 4x4-bit, the Dadda multipliers give lesser propagation delay varying from 2.1% to 9.1%. Whereas, for 8x8-bit, they give lesser propagation delay varying from 1.1% to 1.6% as compared to Wallace tree multipliers.

- Among all eight (LOC as well Mixed L/H based) proposed multipliers implemented at 45 nm, **Dadda-45-L/H-HCA** has the least propagation delay. It has 71.7% (for 4x4-bit), and 88.2% (for 8x8-bit) lesser propagation delay in comparison to most delay intensive design which is Wallace tree-45-L/H-HCA.

- Similarly, at 180 nm, **Dadda-180-L/H-HCA** has the least propagation delay. It has 71.3% (for 4x4-bit) and 69.1% (for 8x8-bit) less propagation delay in comparison to most delay intensive design which is Wallace tree-180-L/H-HCA.

(iii) Power-Delay Product

- For LOC based architectures:

  At 45 nm: For 4x4-bit, the **Dadda multipliers** give lesser power-delay product varying from 44.7% to 49.2%. Whereas, for 8x8-bit, they give lesser power-delay product varying from 28.9% to 32.1% as compared to corresponding Wallace tree multipliers.
  At 180 nm: For 4x4-bit, the **Dadda multipliers** give lesser power-delay product varying from 6.2% to 9.2%. Whereas, for 8x8-bit, they give lesser power-delay product varying from 2.5% to 2.6% as compared to corresponding Wallace tree multipliers.

- For Mixed L/H based architectures

  At 45 nm: For 4x4-bit, the Dadda multipliers give lesser power-delay product varying from 48.6 % to 49%. Whereas, for 8x8-bit, they give lesser power-delay product varying from a 31.5% to 35.1% as compared to corresponding Wallace tree multipliers.
  At 180 nm: For 4x4-bit, the Dadda multipliers give lesser power-delay product varying from 14.9% to 20.6%. Whereas, for 8x8-bit, they give lesser power-delay product varying from a 2.8% to 5.6% as compared to corresponding Wallace tree multipliers

- Among all eight (LOC as well Mixed L/H based) proposed multipliers implemented at 45 nm, **Dadda-45-L/H-HCA** has the least power-delay product. It has 49% (for 4x4-bit), and 31.5% (for 8x8-bit) lesser power-delay product in comparison to Wallace tree-45-L/H-HCA having highest power-delay product.
- Similarly, at 180 nm, **Dadda-180-L/H-HCA** has the least power-delay product. It has 20.6% (for 4x4-bit), and 2.5% (for 8x8-bit) lesser power-delay product in comparison to Wallace tree-180-L/H-HCA having highest power-delay product.
- Static-CMOS logic and HYB-TG design style are most power-delay product efficient design styles for LOC and Mixed L/H based Wallace tree and Dadda multipliers respectively.

(iv) Effect of Technology Scaling:

At same frequency of operation, at 45 nm, the propagation delay is smaller, power consumption is higher (due to increased leakage current since supply voltage is kept same at 0.4V) and power-delay product is smaller for all different implemented combinations of multipliers in comparison to 180 nm technology.

6.3. CONCLUSIONS ON SRAM CELLS

The overall results of the SRAM cells show following conclusions at 45 nm and 180 nm technology nodes.

(i) Comparison of Results of Proposed Designs among themselves at 45nm Technology

- **Impact of Design Configuration on RSNM of SRAM Cell:** Among all proposed SRAM cells, MPT8T has highest RSNM of 120mV. The increased RSNM values in MPT8T and M8T are due to addition of extra transistor in parallel to access transistor which helps in maintaining proper logic '0' at internal storage node. Also, this overcomes the voltage degradation at BLB/BL nodes i.e. increase the node voltage for logic '1' stored.
- **Impact of Design Configuration on WSNM of SRAM Cell:** Among all proposed SRAM cells, MI-12T has highest WSNM of 226mV. This is due to removal of positive feedback in bi-stable element in write operation due to stacking of pull down path.
- **Impact of Design Configuration on Average Read Delay of SRAM Cell:** Among all proposed SRAM cells, M8T has minimum read delay of 0.74 ns. This is due to extra current driven by extra added transistor in parallel to access transistor which consequently decreases

the charging/ discharging time of the internal node of SRAM cell, hence decreases the read delay. Variability of all proposed cell is observed to be ranging from 0.04 to 0.40 at supply voltage of 0.4V with M7T having the least value making it less sensitive to process variation. Read delay and its variability reduces with reduction in power supply voltage.

- **Impact of Design Configuration on Average Write Delay of SRAM Cell:** Among all proposed SRAM cells, M8T has minimum write delay of 0.71 ns. This is due to extra current driven by extra added transistor in parallel to access transistor which consequently decreases the charging/ discharging time of the of the internal node of SRAM cell, hence decreases the write delay. Variability of all proposed cell is observed to be ranging from 0.016 to 0.19 at supply voltage of 0.4V with MPT8T having the least value making it less sensitive to process variation. Write delay its and variability reduces with reduction in power supply voltage.

- **Impact of Design Configuration on Leakage Power Consumption in hold mode:** Among all proposed SRAM cells, MPT8T has least leakage power consumption (in hold mode) of 2.31 nW. This is due to proper logic '0' and logic '1' at internal storage nodes (Q, and QB). This causes full turn OFF of pull up and pull down transistors in bi-stable element of MPT8T thereby reducing the leakage current during hold mode.

(ii) Comparison of all proposed SRAM Cells with C6T at 45 nm

The comparative analysis exhibit that **M8T, MPT8T** and **MI-12T** designs have low leakage power consumption along with other improved design parameters like achieving high read stability, high write ability, fast read & write operation. Thus, these designs can be an attractive choice for low power based application in scaled technology. Whereas M7T and M9T also show improved design parameters like achieving high read stability, high write ability, fast read & write operation but higher leakage power consumption as compared to C6T.

(iii) Comparison of results of referenced designs at 180nm technology among themselves

In comparison with other published low power references (in Chapter 5) with same transistor count, the 8T SRAM cell [13] gives highest RSNM, & highest WSNM, 5T SRAM cell [12] gives lowest read delay, 9T SRAM cell [10] has lowest write delay and 6T SRAM cell [12] gives least leakage power consumption in hold mode.

(iv) Effect of Technology Scaling

At 45 nm technology nodes, all proposed designs show 42.7% average increment in RSNM and 65.8% average increment in WSNM, 85.6% / 24.7% average reduction in read / write delay respectively and 24.9% increment in leakage power consumption in hold mode as compared to corresponding SRAM cells implemented at 180 nm. For few cells like 7T, 8T, and 12T leakage power consumption reduces due to different cell design.

(v) Modeling Analysis

At 0.4 V supply voltage, analytical equations, obtained under steady state condition for read, write and hold operation, give WSNM, RSNM, and Hold SNM within (5.4% to 11.7%), (6.9% to 24.5%), (3.84% to 3.9%) respectively as compared to simulated values.

(vi) Regression Analysis

At 0.4 V supply voltage, simplified equations which are obtained through multiple regression analysis (to obtain the impact of varying CR, PR, and V_{DD} on read, write and hold operation), give WSNM, RSNM, and Hold SNM within (14.7% to 41.7%), (10.4% to 34.8%), and (5% to 12.8%) respectively as compared to simulated values. These equations can be used to get first order estimate of the impact of varying CR, PR, and V_{DD} on read, write and hold stability.

6.4. FUTURE SCOPE OF THE WORK

The present thesis work can be further augmented by doing following additional studies for adder, multiplier and SRAM cell architectures in sub-threshold region:

Adder: The study can be further improved by including the techniques of transistor sizing in the critical delay path and transistor-reordering to increase the speed of the adders in sub-threshold region. Also, we can use scaling of supply voltage and other scaled technology libraries to evaluate the matrices of all the architectures for different operand size in terms of figures of merit to validate their wide applicability area.

Multiplier: Exploration of multiplier designs can be further done for large operand sizes. The different architecture of multipliers in sub-threshold region can also be implemented with other parallel prefix adders (Brent Kung, Ladner-Fisher etc.) which supplement the logarithmic delay of the compression tree for future work and analysis. Also, the impact of scaling of supply voltage along with other scaled technology libraries can be studied to evaluate the performance matrices of all the architectures.

SRAM cells: The extensive exploration of SRAM cells can be built into a software tool that can be used to get the most suited SRAM architectural choice for given technology node. The simulation results can be tested for their accuracy by fabrication of proposed cells M7T, MPT8T, M8T, M9T and MI-12T SRAM cells and obtaining real time results.

Further, to find out the accurate value of the WSNM theoretically, the analytical expressions during write operation can be more accurately modeled. Also, analysis of read stability and write ability can be made more accurate by finding out the dynamic stability metrics which capture the inherent dynamic behavior of SRAM cell.

APPENDIX-A

SIMULATION RESULTS FOR POWER CONSUMPTION OF 8-BIT HCA USING STATIC-CMOS LOGIC AT 45 NM

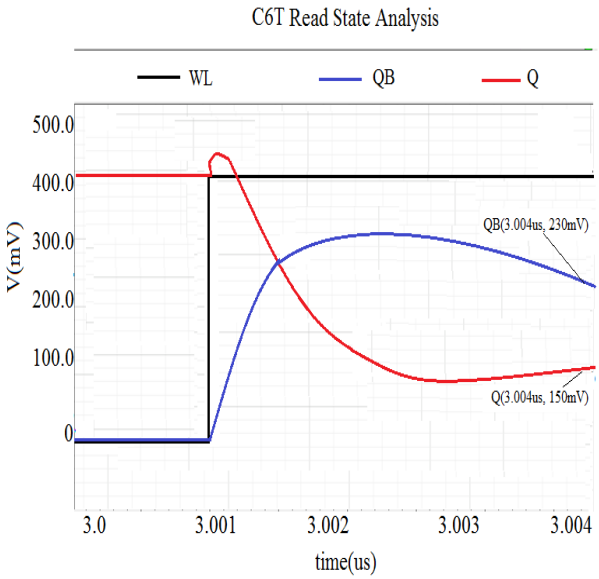
Transient Simulation Time	1 µs	10 µs	20 µs	25 µs	30µs
Power (µW)	0.012481	0.012483	0.012484	0.012487	0.012489

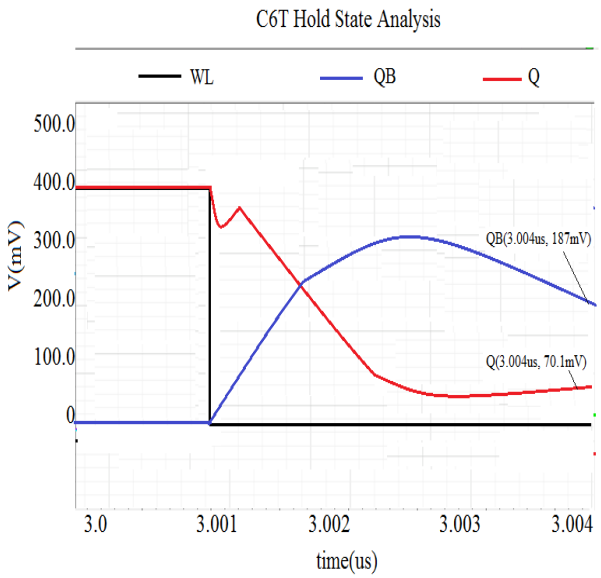
The change in power consumption value at 5^{th} place after decimal indicates that increasing the simulation time does not impact the power consumption value.

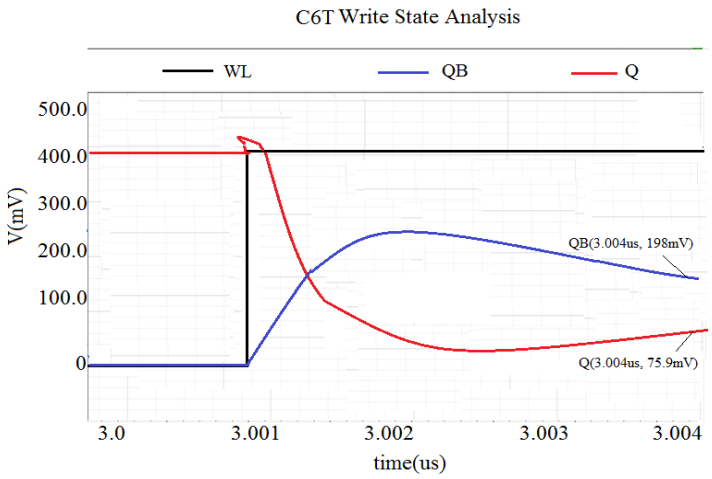
APPENDIX-B

TRANSIENT WAVEFORM OF Q, QB DURING READ, WRITE HOLD MODE FOR C6T AND PROPOSED SRAM CELLS (MPT8T, M8T, M9T, MI-12T)

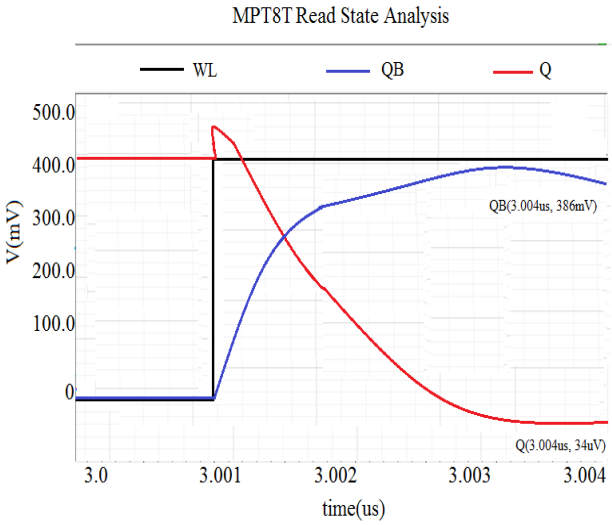
I. For C6T:

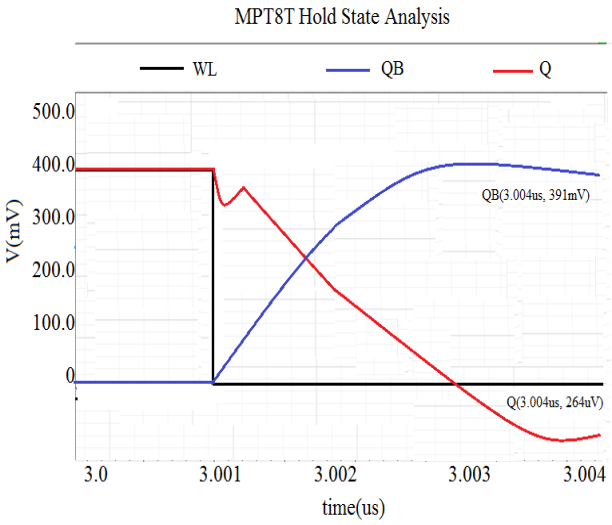


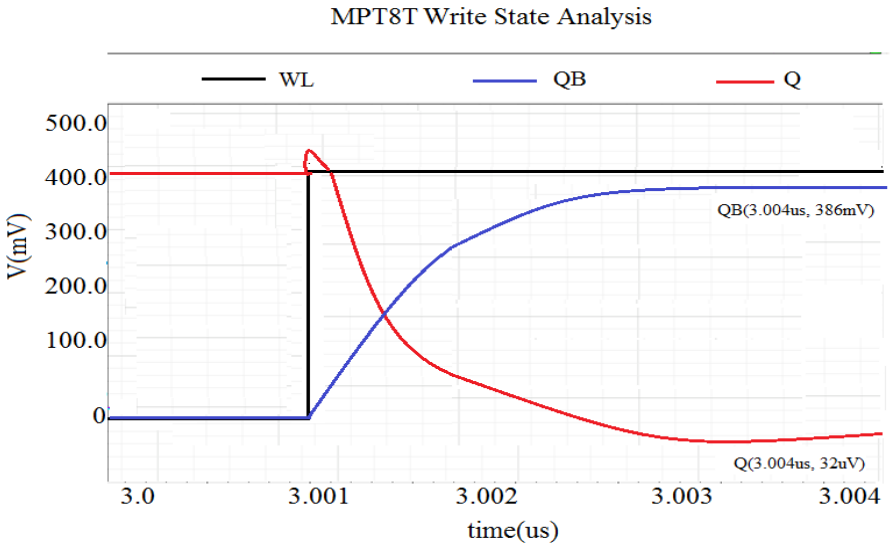




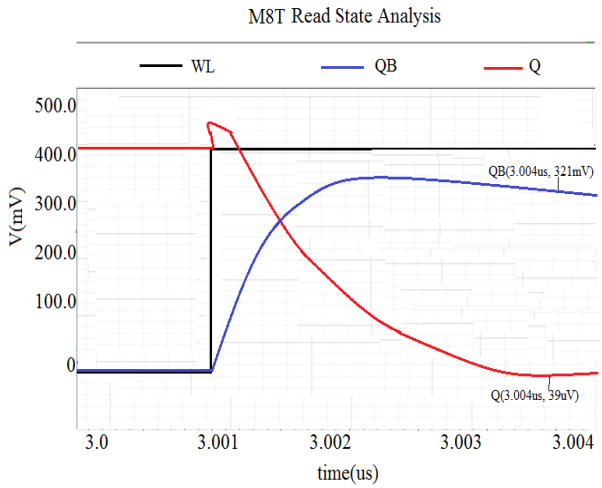
II. For MPT8T:

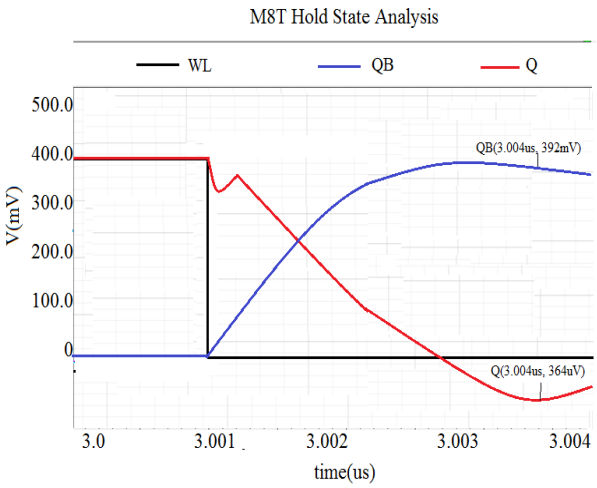

MPT8T Read State Analysis
WL
QB
Q
500.0
400.0
300.0
200.0
100.0
0
V(mV)
QB(3.004us, 386mV)
Q(3.004us, 34uV)
3.0
3.001
3.002
3.003
3.004
time(us)

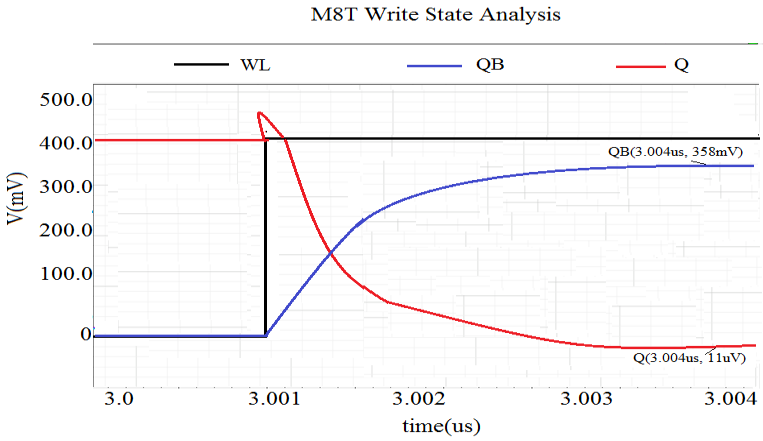

MPT8T Hold State Analysis
WL
QB
Q
500.0
400.0
300.0
200.0
100.0
0
V(mV)
QB(3.004us, 391mV)
Q(3.004us, 264uV)
3.0
3.001
3.002
3.003
3.004
time(us)


MPT8T Write State Analysis
WL
QB
Q
500.0
400.0
300.0
200.0
100.0
0
V(mV)
QB(3.004us, 386mV)
Q(3.004us, 32uV)
3.0
3.001
3.002
3.003
3.004
time(us)

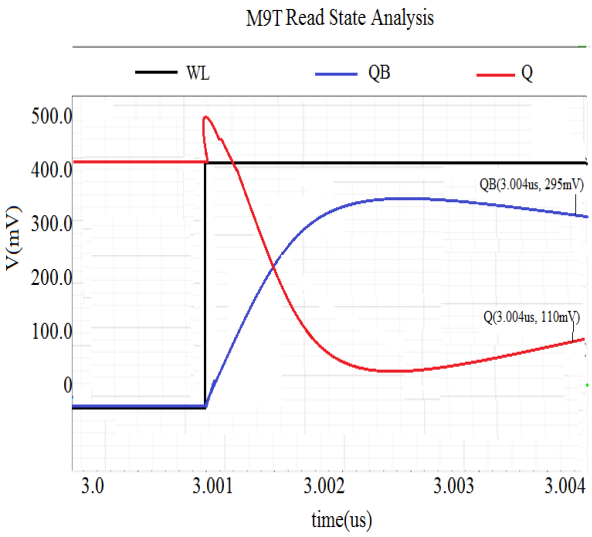
III. FOR M8T:

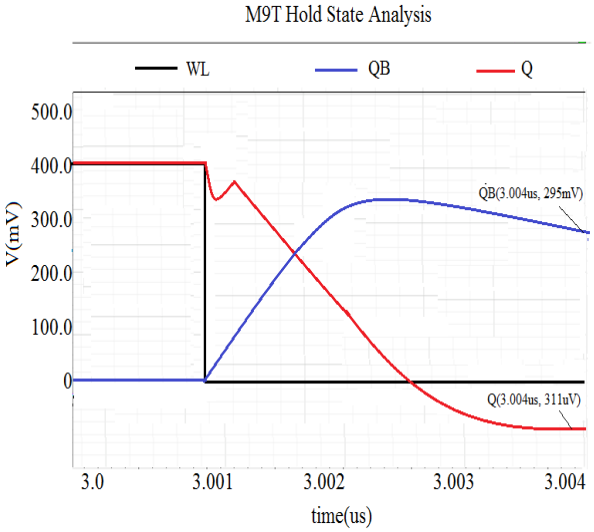


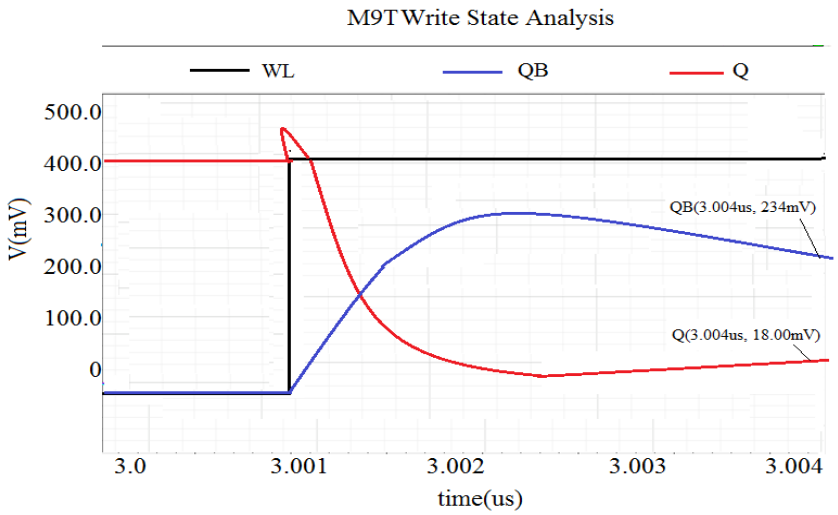




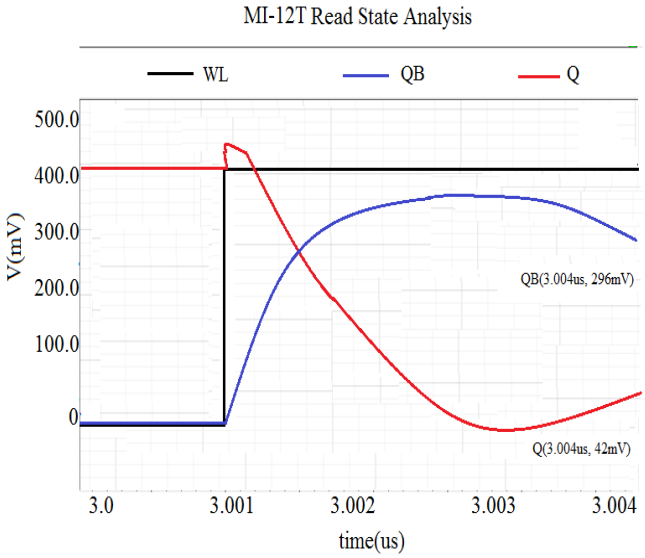
IV. FOR M9T:

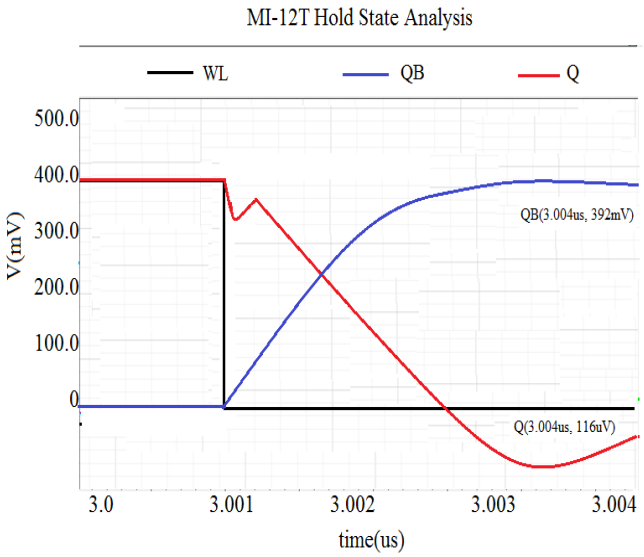


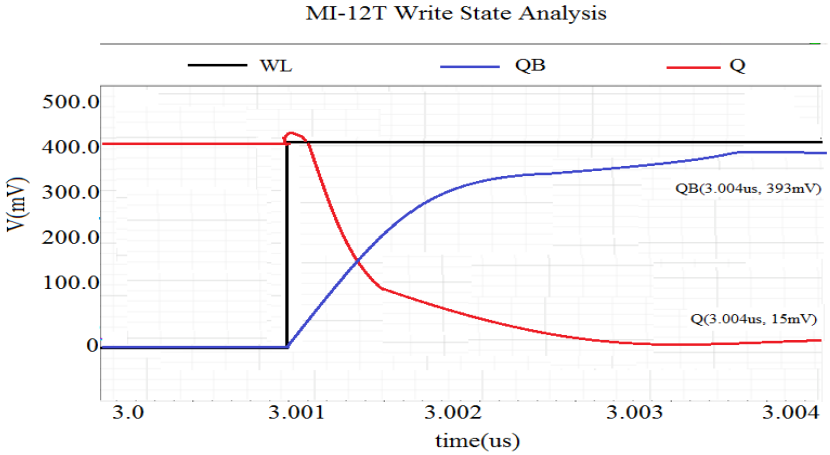



M9T Write State Analysis
WL
QB
Q
500.0
400.0
300.0
200.0
100.0
0
V(mV)
QB(3.004us, 234mV)
Q(3.004us, 18.00mV)
3.0
3.001
3.002
3.003
3.004
time(us)

V. FOR MI-12T:


MI-12T Read State Analysis
WL
QB
Q
500.0
400.0
300.0
200.0
100.0
0
V(mV)
QB(3.004us, 296mV)
Q(3.004us, 42mV)
3.0
3.001
3.002
3.003
3.004
time(us)


MI-12T Hold State Analysis
WL
QB
Q
500.0
400.0
300.0
200.0
100.0
0
V(mV)
QB(3.004us, 392mV)
Q(3.004us, 116uV)
3.0
3.001
3.002
3.003
3.004
time(us)


MI-12T Write State Analysis
WL
QB
Q
500.0
400.0
300.0
200.0
100.0
0
V(mV)
QB(3.004us, 393mV)
Q(3.004us, 15mV)
3.0
3.001
3.002
3.003
3.004
time(us)

APPENDIX-C

LEAKAGE POWER CONSUMPTION OF C6T AND PROPOSED SRAM CELLS

In deep-submicron technology, leakage current is of major concern in memory cell. Leakage current becomes a prominent factor of Power Consumption in an SRAM cell.

In an SRAM cell, the total leakage current (I_{LEAK}) is the combination of

- OFF state leakage (I_{SUB}),
- Gate leakage (I_G)
- Junction leakage (I_{JN}) through various devices (ignoring minor leakages such as I_{GIDL} and $I_{PUNCHTHROUGH}$).

All the equations are derived from the leakage current expressions mentioned in [33]. The major leakage components of C6T and proposed cells during hold mode are discussed below. Here, for each cell, arrow symbols show the leakage component in NMOS or PMOS only irrespective to the direction of current component.

I. Leakage Power Consumption of C6T

Figure 1 shows the major leakage components of C6T during hold mode.

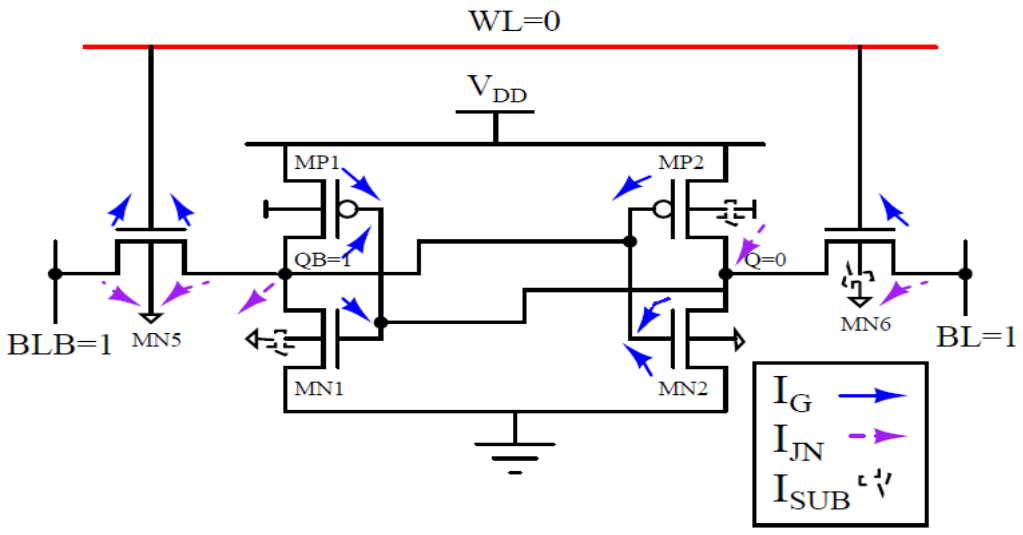


Figure 1: Major leakage components of C6T during hold mode

The major leakage components (I_{SUB}, I_G and I_{JN}) are given by the following equations (C5.1 - C5.4).

$$I_{SUB,C6T} = I_{SUB_{MN1}} + I_{SUB_{MP2}} + I_{SUB_{MN6}} \quad \text{(C5.1)}$$

$$I_{JN,C6T} = I_{JND_{MP2}} + I_{JND_{MN1}} + I_{JND_{MN6}} + I_{JNS_{MN5}} + I_{JND_{MN5}} \quad \text{(C5.2)}$$

$$I_{G,C6T} = I_{GD_{MP2}} + I_{GD_{MN2}} + I_{GS_{MN2}} + I_{GD_{MP1}} + I_{GS_{MP1}} + I_{GD_{MN1}} + I_{GD_{MN6}} + I_{GD_{MN5}} + I_{GS_{MN5}} \quad \text{(C5.3)}$$

$$I_{LEAK,C6T} = I_{SUB,C6T} + I_{JN,C6T} + I_{D,C6T} \quad \text{(C5.4)}$$

The overall leakage power of the cell depends on the total value of I_{LEAK} given in Table C5.1.

II. Leakage Power Consumption of MPT8T

Figure 2 shows the major leakage components of MPT8T during hold mode.

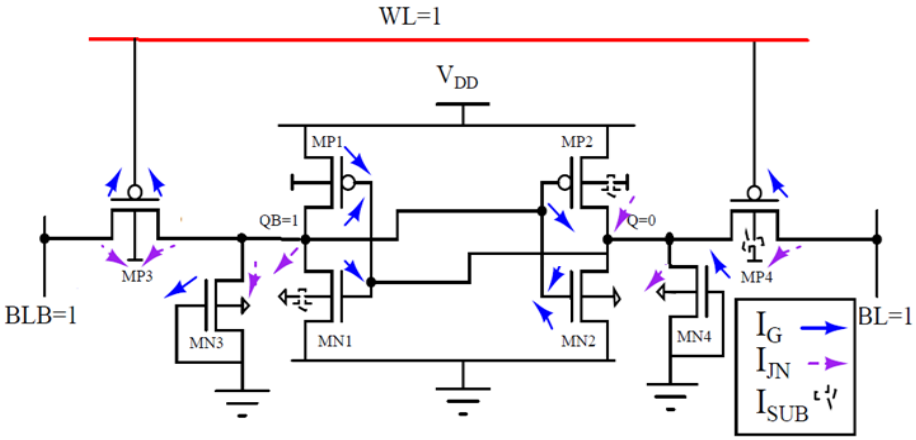


Figure 2: Major leakage components of MPT8T during hold mode

The major leakage components (I_{SUB}, I_G and I_{JN}) of MPT8T are given by the following equations (C5.5 - C5.8)

$$I_{SUB,MPT8T} = I_{SUB_{MN1}} + I_{SUB_{MP2}} + I_{SUB_{MN6}} \quad \text{(C5.5)}$$

$$I_{JN,MPT8T} = I_{JND_{MP2}} + I_{JND_{MN1}} + I_{JND_{MP3}} + I_{JNS_{MP3}} + I_{JND_{MP4}} + I_{JND_{MN3}} + I_{JND_{MN4}} \quad \text{(C5.6)}$$

$$I_{G,MPT8T} = I_{GD_{MP2}} + I_{GD_{MN2}} + I_{GS_{MN2}} + I_{GD_{MP1}} + I_{GS_{MP1}} + I_{GD_{MN1}} + I_{GD_{MP3}} + I_{GS_{MP3}} + I_{GD_{MP4}} + I_{GD_{MN3}} + I_{GD_{MN4}} \quad \text{(C5.7)}$$

$$I_{LEAK,MPT8T} = I_{SUB,MPT8T} + I_{JN,MPT8T} + I_{D,MPT8T} \quad \text{(C5.8)}$$

The total leakage current components for MPT8T are found to be more than the total leakage current components for C6T as shown in Table C5.1. But it consumes less leakage power due to the following reasons:

In hold mode, assume the node QB is at logic '1' and node Q is at logic '0' (See Figure 5.11). Under this condition modified pass transistor based access pairs (MP3-MN3) and (MP4-MN4) will be switched OFF as WL is connected to logic '1'. The gate terminals of these additional NMOS (MN3-MN4) transistors are connected to logic '0', hence in OFF state, due to which it

provides very high resistance path. Therefore, the current components ($I_{JND_{MN3}}, I_{JND_{MN4}}, I_{GD_{MN3}}, I_{GD_{MN4}}$) of MN3 and MN4 have negligible value, the off-state leakage current of these transistors prevents the leakage of the nodes, which precisely control the leakage current of the overall MPT8T.

5.4.2. Leakage Power Consumption of M8T

Figure 3 shows the major leakage components of M8T during hold mode.

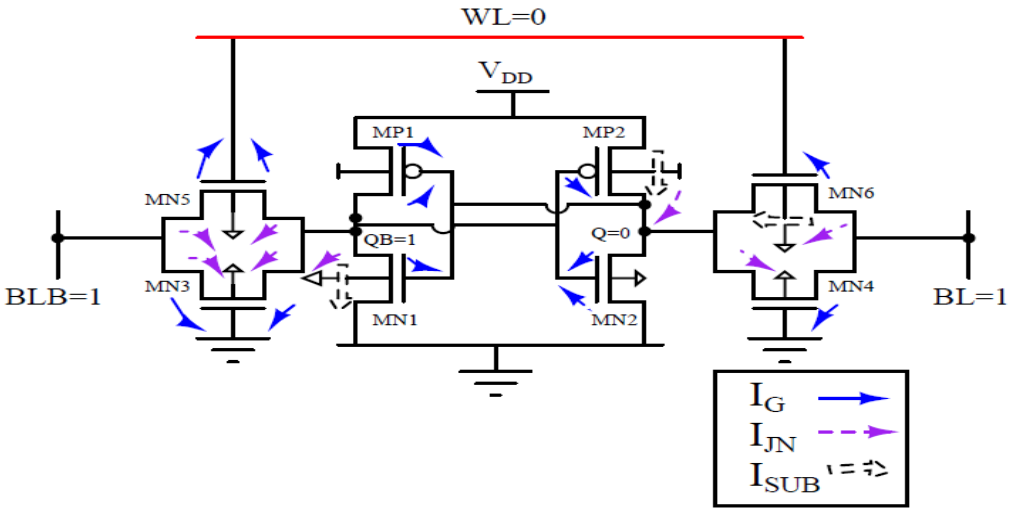


Figure 3: Major leakage components of M8T during hold mode

All the major leakage components (I_{SUB}, I_G and I_{JN}) of M8T during hold mode are expressed in equations (C5.9 - C5.12).

$$I_{SUB,M8T} = I_{SUB_{MN6}} + I_{SUB_{MP2}} + I_{SUB_{MN1}} \quad \text{(C5.9)}$$

$$I_{JN,M8T} = I_{JND_{MP2}} + I_{JND_{MN1}} + I_{JND_{MN6}} + I_{JND_{MN3}} + I_{JNS_{MN5}} + I_{JND_{MN5}} + I_{JNS_{MN4}} + I_{JND_{MN4}} \quad \text{(C5.10)}$$

$$I_{G,M8T} = I_{GD_{MP1}} + I_{GS_{MP1}} + I_{GD_{MN1}} + I_{GD_{MP2}} + I_{GS_{MN2}} + I_{GD_{MN2}} + I_{GD_{MN3}} + I_{GS_{MN4}} + I_{GD_{MN4}} + I_{GS_{MN5}} + I_{GD_{MP5}} + I_{GD_{MP6}} \quad \text{(C5.11)}$$

$$I_{LEAK,M8T} = I_{SUB,M8T} + I_{JN,M8T} + I_{D,M8T} \quad \text{(C5.12)}$$

The total leakage current components for M8T are found to be more than the total leakage current components for C6T as shown in Table C5.1. But it consumes less leakage power due to the following reasons:

In hold mode, assume the node QB is at logic '1' and node Q is at logic '0' (See Figure 5.15). Under this condition additional transistor pair (MN3-MN4) will be switched OFF as the gate terminals of these additional transistors are connected to logic '0', hence in OFF state, due to which it provides very high resistance path. Therefore, the current components ($I_{JND_{MN3}}, I_{JND_{MN4}}, I_{GD_{MN3}}, I_{GD_{MN4}}, I_{JNS_{MN4}}, I_{GS_{MN4}}$) of MN3 and MN4 have negligible value, the off-state leakage current of these transistors prevents the leakage of the nodes, which precisely control the leakage current of the overall M8T.

IV. Leakage Power Consumption of MI-12T

Figure 4 shows the major leakage components of MI-12T during hold mode.

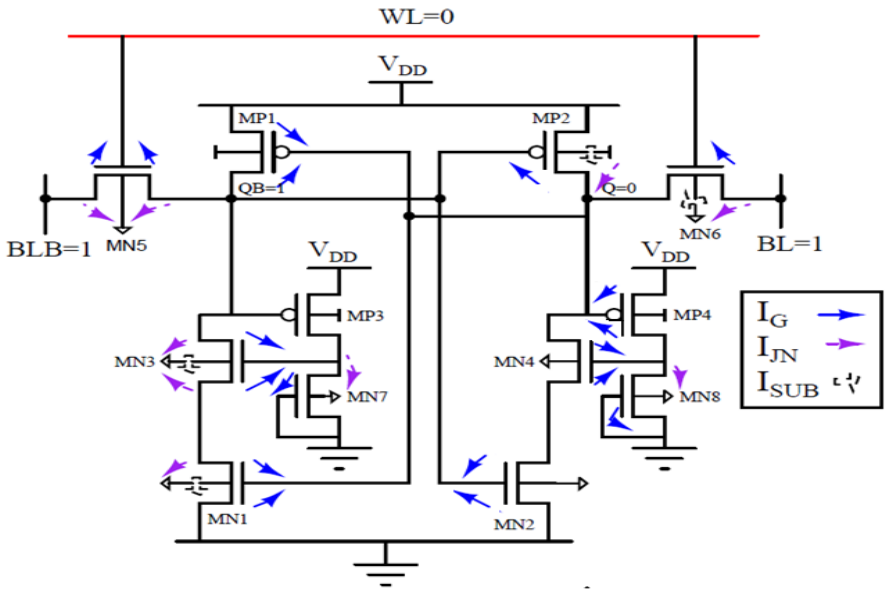


Figure 4: Major leakage components of MI-12T during hold mode

The major leakage components (I_{SUB}, I_G and I_{JN}) of MI-12T are given by the following equations (C5.13 - C5.16)

$$I_{SUB,MI-12T} = I_{SUB_{MN6}} + I_{SUB_{MP2}} + I_{SUB_{MN3}} + I_{SUB_{MN1}} \quad \text{(C5.13)}$$

$$I_{JN,MI-12T} = I_{JND_{MP2}} + I_{JND_{MN1}} + I_{JND_{MN6}} + I_{JNS_{MN3}} + I_{JND_{MN3}} + I_{JNS_{MN5}} + I_{JND_{MN5}} + I_{JND_{MN7}} + I_{JND_{MN8}} \quad \text{(C5.14)}$$

$$I_{G,MI-12T} = I_{GD_{MN5}} + I_{GS_{MN5}} + I_{GS_{MP1}} + I_{GD_{MP1}} + I_{GD_{MN1}} + I_{GS_{MN1}} + I_{GD_{MP2}} + I_{GD_{MP3}} + I_{GD_{MN3}} + I_{GD_{MN6}} + I_{GD_{MP4}} + I_{GS_{MP4}} + I_{GD_{MN4}} + I_{GS_{MN4}} + I_{GD_{MN2}} + I_{GS_{MN2}} + I_{GD_{MN7}} + I_{GD_{MN8}} \quad \text{(C5.15)}$$

$$I_{LEAK,MI-12T} = I_{SUB,MI-12T} + I_{JN,MI-12T} + I_{D,MI-12T} \quad \text{(C5.16)}$$

The total leakage current components for MI-12T are found to be more than the total leakage current components for C6T as given in equation (C5.1 - C5.4) and equation (C5.13 - C5.16). But it consumes less leakage power due to the following reasons:

- In hold mode, assume the node QB is at logic '1' and node Q is at logic '0' (See Figure 5.19). Under this condition additional transistor pair (MP3-MN3) will be switched OFF and other pair (MP4-MN4) will be switched ON.
- The additional transistor MN3/MN4 is stacked over MN1/MN2. Due to body bias effect, MN3/MN4 has an increased threshold voltage thereby reducing the OFF-state leakage current through it. The stacking is formed between the inverter (MN3-MN1) and (MN4-MN2), which reduces the leakage current of the overall MI-12T cell.
- Due to this stacking effect, all the current components $I_{SUB\ MN3}$, $I_{JNS\ MN3}$, $I_{JND,\ MN3}$, $I_{GD\ MP3}$, $I_{GD\ MN3}$, $I_{GD\ MP4}$, $I_{GS\ MP4}$, $I_{GD\ MN4}$, $I_{GS\ MN4}$, $I_{GD\ MN7}$, $I_{GD\ MN8}$, $I_{JND,\ MN7}$, $I_{JND,\ MN8}$ of MP3-MN3-MN7, MP4-MN4-MN8 have negligible value.

V. Leakage Power Consumption of M7T

Figure 5 shows the major leakage components of M7T during hold mode.

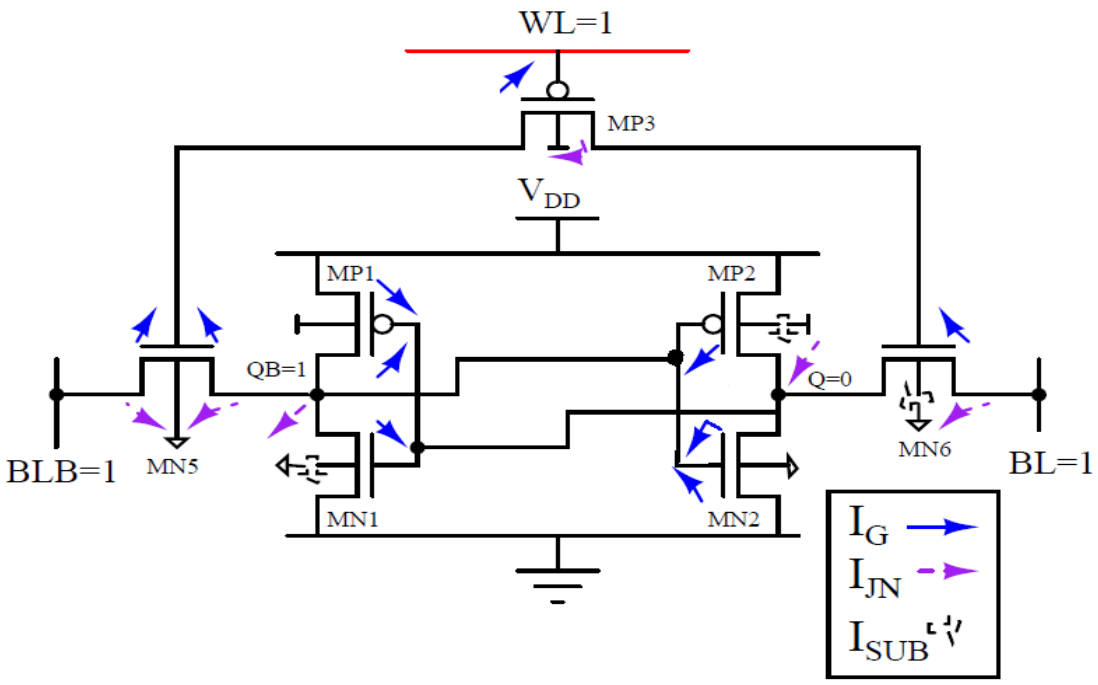


Figure 5: Major leakage components of M7T during hold mode

The major leakage components (I_{SUB}, I_G and I_{JN}) are given by the following equations (C5.17 - C5.20)

$$I_{SUB,M7T} = I_{SUB_{MN1}} + I_{SUB_{MP2}} + I_{SUB_{MN6}} \quad \text{(C5.17)}$$

$$I_{JN,M7T} = I_{JND_{MP2}} + I_{JND_{MN1}} + I_{JND_{MN6}} + I_{JNS_{MN5}} + I_{JND_{MN5}} + I_{JND_{MP3}} \quad \text{(C5.18)}$$

$$I_{G,M7T} = I_{GD_{MP2}} + I_{GD_{MN2}} + I_{GS_{MN2}} + I_{GD_{MP1}} + I_{GS_{MP1}} + I_{GD_{MN1}} + I_{GD_{MN6}} + I_{GD_{MN5}} + I_{GS_{MN5}} + I_{GD_{MP3}} \quad \text{(C5.19)}$$

$$I_{LEAK,M7T} = I_{SUB,M7T} + I_{JN,M7T} + I_{D,M7T} \quad \text{(C5.20)}$$

The total leakage current components for M7T are found to be more than the total leakage current components for C6T as shown in Table C5.1. Therefore, M7T consumes more leakage power than C6T.

VI. Leakage Power Consumption of M9T

Figure 6 shows the major leakage components of M9T during hold mode.

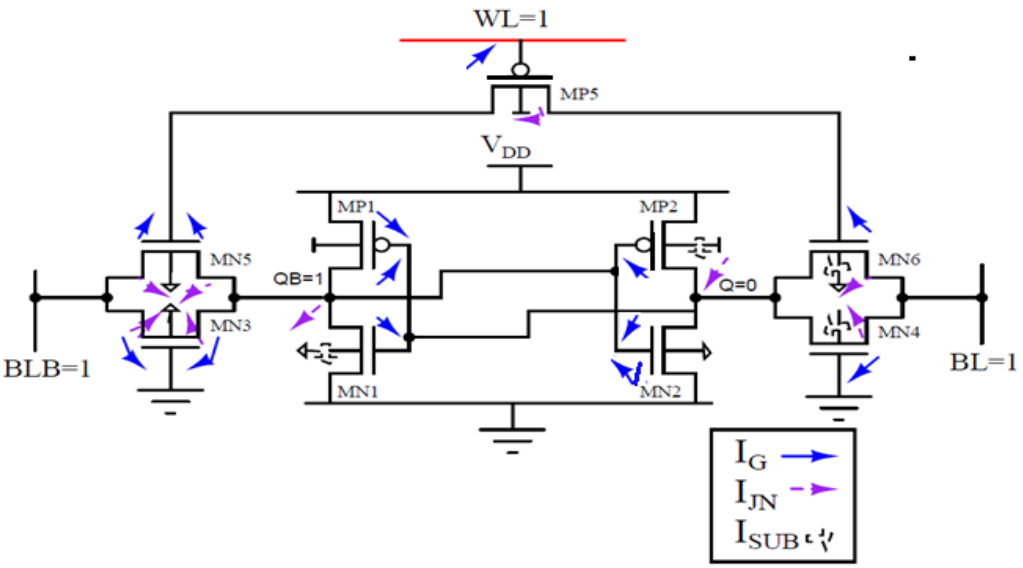


Figure 6: Major leakage components of M9T during hold mode

The major leakage components (I_{SUB}, I_G and I_{JN}) of M9T are given by the following equations (C5.21 - C5.24)

$$I_{SUB,M9T} = I_{SUB_{MN1}} + I_{SUB_{MP2}} + I_{SUB_{MN5}} + +I_{SUB_{MP5}} \quad \text{(C5.21)}$$

$$I_{JN,M9T} = I_{JND_{MN1}} + I_{JND_{MP2}} + I_{JND_{MN6}} + I_{JND_{MN5}} + I_{JNS_{MN5}} + I_{JND_{MN3}} + I_{JNS_{MN3}} + I_{JND_{MN4}} + I_{JND_{MP5}} \quad \text{(C5.22)}$$

$$I_{G,M9T} = I_{GD_{MP2}} + I_{GD_{MN2}} + I_{GS_{MN2}} + I_{GD_{MP1}} + I_{GS_{MP1}} + I_{GD_{MN1}} + I_{GD_{MN5}} + I_{GS_{MN5}} + I_{GD_{MN3}} + I_{GS_{MN3}} + I_{GD_{MN6}} + I_{GD_{MP5}} + I_{GD_{MN4}} \quad \text{(C5.23)}$$

$$I_{LEAK,M9T} = I_{SUB,M9T} + I_{JN,M9T} + I_{D,M9T} \quad \text{(C5.24)}$$

The total leakage current components for M9T are found to be more than the total leakage current components for C6T as shown in Table C5.1. Therefore, M9T consumes more leakage power than C6T.

The total number of effective leakage current components of C6T and proposed cells during hold mode along with simulated total current value is shown in Table C5.1.
It shows that leakage current is more for M9T which also has highest number of leakage current components.

Table C5.1: Leakage current components of conventional and proposed SRAM cells

Module Name	**I_{SUB}** **(i)**	**I_{JN}** **(ii)**	**I_G** **(iii)**	**$I_{LEAKAGE\ TOTAL}$** **No. of leakage current Components (i)+(ii)+(iii)**
C6T	3	5	9	17
M7T	3	6	10	19
MPT8T	3	5	9	17
M8T	3	5	9	17
M9T	4	8	13	25
MI-12T	3	5	9	17

APPENDIX D

PULL-UP, PULL-DOWN AND ACCESS TRANSISTOR CURRENT DURING READ, WRITE, AND HOLD MODE FOR C6T AND PROPOSED SRAM CELLS AT 45 NM

I. FOR C6T:

Mode of Operations / Transistor Name	Current in Hold '1'mode (A)	Current in Read '0' mode (A)	Current in Write '0' mode (A)
Pull-up transistor (MP2)	8.87E-9	41.7E-12	1.68E-6
Pull-down transistor (MN2)	8.87E-9	2.01E-6	3.79E-12
Access transistor (MN6)	4.77E-24	2.01E-6	1.68E-6

II. FOR M7T:

Mode of Operations / Transistor Name	Current in Hold '1'mode (A)	Current in Read '0' mode (A)	Current in Write '0' mode (A)
Pull-up transistor (MP2)	9.78E-9	69.74E-12	5.77E-6
Pull-down transistor (MN2)	9.78E-9	8.73E-6	8.99E-12
Access transistor (MN6)	107E-24	8.73E-6	5.77E-6

III. FOR MPT8T:

Mode of Operations / Transistor Name	Current in Hold '1'mode (A)	Current in Read '0' mode (A)	Current in Write '0' mode (A)
Pull-up transistor (MP2)	4.11E-9	72.1E-12	6.79E-6
Pull-down transistor (MN2)	4.11E-9	12.77E-6	10.7E-12
Access transistor (MP4)	187E-24	12.77E-6	6.79E-6

IV. FOR M8T:

Mode of Operations / Transistor Name	Current in Hold '1'mode (A)	Current in Read '0' mode (A)	Current in Write '0' mode (A)
Pull-up transistor (MP2)	6.59E-9	81E-12	7.81E-6
Pull-down transistor (MN2)	6.59E-9	14.39E-6	11.5E-12
Access transistor (MN6/MN4)	254E-23	14.39E-6	7.81E-6

V. FOR M9T:

Mode of Operations / Transistor Name	Current in Hold '1'mode (A)	Current in Read '0' mode (A)	Current in Write '0' mode (A)
Pull-up transistor (MP2)	10.11E-9	55.77E-12	3.44E-6
Pull-down transistor (MN2)	10.11E-9	6.47E-6	5.78E-12
Access transistor (MN6/MN4)	99E-24	6.47E-6	3.44E-6

VI. MI-12T:

Mode of Operations / Transistor Name	Current in Hold '1'mode (A)	Current in Read '0' mode (A)	Current in Write '0' mode (A)
Pull-up transistor (MP2)	7.09E-9	71.1E-12	6.11E-6
Pull-down transistor (MN2)	7.09E-9	10.74E-6	9.98E-12
Access transistor (MN6)	154E-24	10.74E-6	6.11E-6

APPENDIX E

TABLE OF PERCENTAGE CHANGE IN PERFORMANCE METRICS OF SRAM CELLS (WITH SAME TRANSISTOR COUNT) AT 45 NM IN COMPARISON TO 180NM TECHNOLOGY

No. of transistor	% Increment in RSNM at 45nm	% Increment in WSNM at 45nm	% Decrement in Read delay at 45nm	% Decrement in Write delay at 45nm	% Increment in Power consumption at 45nm
6T	45.6%	47.0%	53.2%	45.8%	97.3%
7T	55.5%	69.8%	95.4%	97.2%	1.64% (less)
8T	32.2%	62.2%	74.7%	72.1%	19.2% (less)
9T	45.5%	72.0%	72.1%	89.1% (more)	37.2%
12T	41.1%	69.6%	95.1%	93.4%	22.9% (less)

APPENDIX F

ESTIMATION OF WRITE ABILITY AND READ STABILITY THROUGH OBSERVATION

- **At 45 nm Technology:**

WRITE ABILITY

For robust write operation, performance order of proposed cells from best to worst is given below:

WSNM in decreasing order: H: MI-12T > MPT8T > M: M8T > M9T > L: M7T > C6T

WTI in increasing order: H: M8T < MI-12T < M: MPT8T < M7T < L: M9T < C6T

WTV in increasing order: H: MPT8T = M7T = M9T = C6T < M: M8T < L: MI-12T

As WSNM, WTI, and WTV are independent performance metrics for write operation, we have categorized their value as high (H), moderate (M), and low (L) based on their position from left to right. For MPT8T, WTI value is 3× more than MI-12T.

Table F1 shows the categorization of write ability metrics of proposed SRAM cells.

Table F1: Write ability metrics of proposed SRAM cells

SRAM cells	WSNM	WTI	WTV
MPT8T	H	M	H
M8T	M	H	M
M7T	L	M	H
MI-12T	H	H	L
M9T	M	L	H
C6T	L	L	H

Write ability of SRAM cell: Again, it is observed from above tables, that none of the proposed cell has best value for all three-metrics related to write ability (i.e. highest WSNM, least WTI, and least WTV). MI-12T has highest WSNM and lower WTI, and a highest WTV. Similarly, C6T has least WSNM and WTI, but a highest SVNM.

Thus, comparison is made on the basis of value of two metrics out of three. Based on this, in the order of their appearance, MI-12T, MPT8T, M8T, M7T = M9T, C6T show decreased write ability as per Table F1.

READ STABILITY

For stable read operation, performance order of proposed cells from best to worst is given below:

RSNM in decreasing order: H: MPT8T > M8T > M: M7T > MI-12T > L: M9T > C6T

SINM in decreasing order: H: MI-12T > M7T > M_H: M9T >> M_L: M8T > L: MPT8T > C6T

SVNM in decreasing order: H: C6T = M7T = MPT8T=M9T > M: M8T > L: MI-12T

As RSNM, SINM, and SVNM are independent performance metrics for read operation, we have categorized their value as high (H), moderate (M), and low (L) based on their position from left to right. For SINM, moderate category is split into moderate high (M_H) and moderate low (M_L) due to the fact that M9T has SINM 3× more than M8T.

Table F2 shows the categorization of read stability metrics of proposed SRAM cells.

Table F2: Read stability metrics of proposed SRAM cells

SRAM cells	RSNM	SINM	SVNM
MPT8T	H	L	H
M8T	H	M_L	M
M7T	M	H	H
MI-12T	M	H	L
M9T	L	M_H	H
C6T	L	L	H

Read stability of SRAM cell: It is observed that none of the proposed cell has best value for all three-metrics related to read stability (i.e. highest RSNM, highest SINM, and highest SVNM). MPT8T has highest RSNM and SVNM, but a lower SINM. Similarly, C6T has least RSNM and SINM, but a higher SVNM. Thus, comparison is made on the basis of value of two metrics out of three. Based on this, in the order of their appearance M7T, MPT8T, M8T, M9T, MI-12T, C6T show decreased read stability as per Table F2.

- **At 180 nm Technology:**

WRITE ABILITY

For robust write operation, performance order of proposed cells (as per Figure 5.53) from best to worst is given below:

WSNM in decreasing order: H: 8T[13]>12T[15] > MH: 6T[12] > M: 9T[10] > ML: 7T[10] > L: 5T[12] > 4T[12]

WTI in increasing order: H: 8T[13] < 9T[10] < MH: 12T[15] < M: 6T[12] < ML: 5T[12] < L: 7T[10] < 4T[12]

WTV in increasing order: H: 6T[12] < 7T[10] = 4T[12] < M: 5T[12] < 9T[10] < L: 12T[15] < 8T[13]

As WSNM, WTI, and WTV are independent performance metrics for write operation, we have categorized their value as high (H), moderate (MH, M, ML), and low (L) based on their position from left to right. Table F3 shows the categorization of write ability metrics of referenced SRAM cells at 180nm technology.

Table F3: Write ability metrics of SRAM cells at 180 nm

SRAM cells	WSNM	WTI	WTV
4T[12]	L	L	H
5T[12]	L	ML	M
6T[12]	MH	M	H
7T[10]	ML	L	H
8T[13]	H	H	L
9T[10]	M	H	M
12T[15]	H	MH	L

Write ability of SRAM cell: Here again, comparison is made on the basis of value of two parameters out of three as obtaining best value for all three-metrics related to write ability simultaneously is not always possible. Based on this, in the order of their appearance 8T[13], 6T[12], 9T[10], 12T[15], 7T[10], 5T[12], 4T[12] show decreased write ability as per Table F3.

READ STABILITY

For stable read operation, performance order of proposed cells (as per Figure 5.53) from best to worst is given below:

RSNM in decreasing order: H: 8T[13] > 12T[15] > M_H, M, M_L: 7T[10] > 9T[10] > 5T[12] > L: 6T[12] > 4T[12]

SINM in decreasing order: H: 8T[13] > 12T[15] > M_H, M, M_L: 5T[12] > 9T[10] > 4T[12] > L: 6T[12] >7T[10]

SVNM in decreasing order: H: 12T[15] < 9T[10] < M_H, M, M_L: 8T[13]=5T[12] < 7T[10] = L: 4T[12] <6T[12]

As RSNM, SINM, and SVNM are independent performance metrics for read operation, we have categorized their value as high (H), moderate (M_H, M, M_L), and low (L) based on their position from left to right. Table F4 shows the categorization of read stability metrics of referenced SRAM cells

Table F4: Read stability metrics of SRAM cells at 180 nm

SRAM cells	RSNM	SINM	SVNM
4T[12]	L	M_L	L
5T[12]	M_L	M_H	M
6T[12]	L	L	L
7T[10]	M_H	L	M_L
8T[13]	H	H	M_H
9T[10]	M	M	H
12T[15]	H	H	H

Read stability of SRAM cell: It is observed that obtaining best value for all three-metrics related to read stability simultaneously (i.e. highest RSNM, highest SINM, and highest SVNM) is not always possible. 12T [15] SRAM cell shows increased value of SVNM and SINM but moderate value for RSNM. Similarly, 4T has least RSNM, but a moderate SVNM and SINM. Thus, comparison is made on the basis of value of two parameters out of three. Based on this, in the order of their appearance 12T[15], 8T[13], 9T[10], 5T[12], 7T[10], 4T[12], 6T[12] show decreased read stability as per Table F4.

LIST OF PUBLICATIONS

Publication in Journals

1. **Priya Gupta**, Ishan Munje, Nikhil Kaswan, Anu Gupta and Abhijit Asati, "Effectiveness of body bias & hybrid logic: An energy efficient approach to design adders in sub-threshold regime", *International Journal of Circuits and Architecture Design*, vol. 2(2), 2016, pp. 155-168.

2. **Priya Gupta**, Anu Gupta and Abhijit Asati, "Ultra Low Power MUX Based Compressors for Wallace tree and Dadda Multipliers in Sub-Threshold Regime" *American Journal of Engineering and Applied Sciences*, vol. 8(4), 2015, pp. 702-715. (Scopus Indexed)

3. **Priya Gupta**, Anu Gupta and Abhijit Asati, "Leakage Immune Modified Pass Transistor based 8T-SRAM Cell in Sub-threshold Region" *International Journal of Reconfigurable Computing*, vol. 2015, 2015, pp. 1-10. (Scopus Indexed)

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