ABSTRACT

The rapid development of new and exciting applications ranging from AI-based driverless cars to remote health monitoring offers great challenges and opportunities for the semiconductor industry. The next-generation computing systems required for these applications need to be supported on increasingly small devices with shrinking dimensions and tighter energy budgets. However, power management is one of the key challenges in the sustainable deployment of these devices. Memories being one of the largest on-chip components plays an important role in these applications, and it is expected that the future chips will have more than 80% of the chip area occupied by the memories. The state-of-the-art 6T SRAM-based memories play a pivotal role in VLSI systems to support the increasing need for data storage in various applications. However, with technology scaling, memory cell size gets significantly minimized in order to boost the storage capacity where VDD_{min} of 6T SRAM does not scale well in advanced technologies. As a result, 6T SRAM dominates power consumption in advanced VLSI systems like data centers and Internet of Things (IoT) that have a growing need for low-power memories. The existing techniques such as ultra-dynamic voltage scaling allow the system to operate over a wide range of supply voltages. As a result, various low power operating modes can be achieved to lower the overall power consumption. However, it fails to address the increasing leakage power consumption in larger memories. This problem is further exacerbated for the IoT-based emerging applications that spend a significant portion of their time in the idle mode. As a result, these systems suffer from large standby leakage power dissipation, which often becomes a major performance bottleneck. The current techniques use direct gating of power supply, which poses another challenge where the system loses its current state and requires a boot process to wake up and re-initialize the state of the system. The boot process consumes thousands of processor cycles, hundreds of microseconds, and hundreds of nano-joules of energy, which makes it limiting for applications with stringent power requirements.

To address these challenges, we propose to implement normally-off computing with the proposed hybrid memory cells and hybrid flip-flops. In this technique, non-functional memory cells/blocks are completely turned-off, in order to achieve zero leakage power dissipation during standby mode without loss of data. The proposed hybrid structures are developed by integrating the conventional CMOS technology with the emerging non-volatile technology. The emerging non-volatile technologies are considered one of the most promising

candidates to realize hybrid embedded memories because of their non-volatility, low power consumption, small access time, and compatibility with the CMOS fabrication process.

Additionally, in recent times, the idea of energy autonomy is gaining popularity in the IoT sector due to its ecological and economic benefits. The energy demand needed to power billions of IoT nodes can be met with energy autonomy as a prospective solution. As it involves usage of ambient sources as the main power source, it offers an environment friendly method to obtain near-perpetual operation without maintenance. However, the energy-autonomous systems suffer from the unsteady and uncertain power supply, which causes frequent and unpredictable power failures. Therefore, in this work, we also explore hybrid memories as an efficient way to ensures reliable operation under frequent power failure in energy-autonomous systems.

Further, most autonomous sensor nodes in wireless sensor networks and IoT networks often have to switch context to integrate data from a large number of heterogeneous sensors, which requires entire cache data to be refreshed to fetch a new set of data/code relevant to a particular context. To address this challenge, in this thesis, we propose hybrid multi-storage memory cell design using emerging technologies to support fast, reliable context switching without refreshing/flushing the whole cache memory.

In this work, we also propose to incorporate asynchronous circuit design technique as an alternative approach to mitigate the large leakage power consumption. The hybrid asynchronous circuits employ the event-based behavior where power is consumed only if an event needs to be processed. As a result, the part of the circuit not active consumes almost zero static power. Therefore, we also explore hybrid asynchronous circuits as one of the possible low-power solutions for IoT applications.

Finally, we explore the feasibility of applying the emerging non-volatile technologies into the computing applications that support arithmetic & logic operations to define a new computing paradigm which addresses the fundamental problem of power management in the IoT based next-generation applications.

In summary, this works presents several alternative circuits and architectures to reduce power consumption in embedded memories varying from volatile Flip Flop to volatile SRAM and logic circuits for low-power energy-autonomous IoT applications.