LIST OF FIGURES

Figure 1.1: Number of connected devices in the IoT network 3

Figure 1.2: Sources of energy harvesting 8

Figure 1.3: Burst mode operation characteristic of IoT devices 9

Figure 2.1: Hierarchical memory organization 22

Figure 3.1: Different checkpointing techniques employed in energy harvesting based IoT applications (a) Conventional checkpointing scheme (b) Checkpointing scheme with NVM hierarchy 47

Figure 3.2: Percentage of the forward progress with conventional architecture and NVM checkpointing scheme under unstable power supply 47

Figure 3.3: Proposed hybrid 7T SRAM Cell 49

Figure 3.4: Writing logic '1' into the proposed hybrid 7T SRAM cell using single-phase write operation 50

Figure 3.5: Phase I: Writing logic '1' into the MTJ device of the hybrid 7T SRAM cell using two-phase write operation 50

Figure 3.6: Phase II: Writing logic '1' into the internal nodes of the hybrid 7T SRAM cell using two-phase write operation 51

Figure 3.7: Reading Logic '1' in hybrid 7T SRAM cell 52

Figure 3.8: Restore operation in hybrid 7T SRAM cell 52

Figure 3.9: Transient waveform of proposed non-volatile hybrid 7T SRAM Cell 53

Figure 3.10: Energy consumption during the various operation in proposed hybrid 7T SRAM cell at different technology nodes (a) Energy consumption during the write/backup operation in single phase and two phase write scheme (b) Energy consumption during the read and restore operation 55

Figure 3.11: Access latency while performing the write/backup, read and restore operation in the proposed hybrid 7T SRAM cell at different technology nodes 55

Figure 3.12: Proposed hybrid 8T SRAM cell 56

Figure 3.13: Direction of current flow and status of control signal during backup operation in

hybrid 8T SRAM cell 57

Figure 3.14: Restore operation in hybrid 8T SRAM cell 58

Figure 3.15: Simulation waveform of non-volatile hybrid 8T SRAM cell 59

Figure 3.16: Energy consumption and latency of various operation of hybrid 8T SRAM cell at different technology nodes 61

Figure 3.17: Proposed hybrid 11T SRAM Cell. 61

Figure 3.18: Simulation waveform of proposed hybrid 11T SRAM cell 64

Figure 3.19: Energy consumption and latency of various operation of hybrid 11T SRAM cell at different technology nodes 65

Figure 3.20: Layout design of (a) Hybrid 6T SRAM cell (b) Hybrid 8T SRAM cell (c) Proposed hybrid 8T SRAM cell 68

Figure 4.1: Proposed hybrid multi-storage SRAM cell 73

Figure 4.2: Store operation in proposed multi-storage SRAM cell 75

Figure 4.3: Load operation of proposed multi-storage SRAM cell 76

Figure 4.4: Simulation waveform of activating a context in proposed multi-storage SRAM cell 77

Figure 4.5: Simulation waveform performing context switch in proposed multi-storage SRAM cell 78

Figure 4.6: Proposed single-bit hybrid 8T SRAM cell with write termination circuit 79

Figure 4.7: Write operation of proposed hybrid 8T SRAM cell 80

Figure 4.8: Simulation waveform of the proposed single-bit 8T SRAM cell 81

Figure 4.9: (a) Block Diagram of proposed multi-storage SRAM cell (b) Proposed multi-storage SRAM cell with write/store assist circuit 83

Figure 4.10: Timing Waveform during store operation 84

Figure 4.11: Generation of WRE control signal by Store Enable circuit 85

Figure 4.12: (a) Generation of detection signal (b) Self-termination of store operation in multi-storage SRAM Cell 85

Figure 4.13: Simulation waveform for store operation in proposed multi-storage SRAM cell

.....86

Figure 4.14: Energy consumption and latencies are plotted for hybrid cell against number of contexts 87

Figure 5.1: Different approaches to state retention (a) Out-of-place Retention b) In-place Retention 92

Figure 5.2: Mutoh MTCMOS State Retentive FF 94

Figure 5.3: Balloon Flip-flop circuit 95

Figure 5.4: Operational mode and associated control signals for Balloon Flip-Flop 95

Figure 5.5: Memory Flip-Flop 96

Figure 5.6: Memory TG Flip-Flop 97

Figure 5.7: (a) Hybrid D Flip-Flop (b) NVM unit of FF-I connected to cross-coupled inverter of slave latch 98

Figure 5.8: Operational waveform of hybrid Flip-Flop (HFF-I) 98

Figure 5.9: Proposed Hybrid Flip-Flop (HFF-I) in its normal mode 99

Figure 5.10: Backup operation of HFF-I circuit (a) Phase I of backup operation of HFF-I circuit (b) Phase II of backup operation of HFF-I circuit 99

Figure 5.11: Restore operation of proposed hybrid flip-flop (HFF-I) 100

Figure 5.12: NVM unit of HFF-II connected to cross-coupled inverter of slave latch 101

Figure 5.13: Operational Waveform of hybrid Flip-flop FF-II 101

Figure 5.14: Normal mode of hybrid FF-II 102

Figure 5.15: Backup operation of hybrid FF-II 102

Figure 5.16: Restore operation of HFF-II 103

Figure 5.17: Test circuit for analyzing hybrid flip-flop 103

Figure 5.18: (a) Dynamic and (b) Static energy consumption for the proposed hybrid flip-flop HFF-I with respect to different activity factor 106

Figure 5.19: (a) Dynamic and (b) Static power consumption for the proposed hybrid flip-flop HFF-II with respect to different activity factor 107

Figure 5.20: Layout of (a) D Flip-Flop (b) Proposed hybrid HFF-I (c) Proposed hybrid HFF-II 112

Figure 6.1: Percentage of computation done by different processors against power failures 116

Figure 6.2: Martin's weak feedback c-element 117

Figure 6.3: Sutherland c-element 118

Figure 6.4: Van Berkel c-element 118

Figure 6.5: Proposed hybrid C-Element 119

Figure 6.6: Backup operation - storing logic '1' and logic '0' into the MTJ 120

Figure 6.7: Restore operation 121

Figure 6.8: Conventional Half-Buffer 121

Figure 6.9: Proposed non-volatile hybrid half buffer 122

Figure 6.10: Simulation waveform of proposed hybrid c-element 124

Figure 6.11: Simulation Waveform of proposed hybrid Half-Buffer 125

Figure 7.1: Conventional Von-Neumann Architecture 128

Figure 7.2: (a) NMC (b) IMC 129

Figure 7.3: (a) STT-MTJ based C-MRAM array (b) 2T-1MTJ bitcell (c) C-MRAM row 130

Figure 7.4: Logic function being performed by STT-MTJ based C-MRAM 131

Figure 7.5: The transient simulation waveform performing NAND logic function in STT-MTJ based C-MRAM 134

Figure 7.6: The transient simulation waveform for performing NOR logic function in STT-MTJ based C-MRAM 135

Figure 7.7: Proposed SHE-MTJ based Computational Magnetic Random-Access Memory 136

Figure 7.8: Status of control lines and direction of current flow through the 2T-1MTJ bitcell during (a) Write logic '1' operation (b) Write logic '0' Operation (c) Read Operation 137

Figure 7.9: (a) Status of control lines to perform logic operation in proposed C-MRAM array (b) Direction of current flow while performing logic function for cases: Case 1: A=0; B=0

and Case 4: A=1; B=1 (c) Direction of current flow while performing logic function for cases: Case 2: A=0; B=1 and Case 3: A=1; B=0 138

Figure 7.10: Simulation waveform for the NAND & AND logic operation in proposed SHE-MTJ based C-MRAM 141

Figure 7.11: Simulation waveform for the NOR & OR logic operation in proposed SHE-MTJ based C-MRAM 142

Figure 7.12: Computation steps to generate SUM_{approx} output of the proposed approximate full adder 145

Figure 7.13: Computation steps to generate $Carry_out_{approx}$ output of the proposed approximate full adder 145

Figure 7.14: Simulation waveform to validate the SUM_{approx} and $Carry_out_{approx}$ outputs of proposed adder 146

Figure 7.15: Simulation waveform to demonstrate all the operational modes of proposed SHE-MTJ based C-MRAM array 148

LIST OF TABLES

Table 3.1: Status of control signal during various operational modes of proposed hybrid 7T SRAM Cell..... 51

Table 3.2: Energy consumption and access latency of proposed non-volatile hybrid 7T SRAM Cell..... 54

Table 3.3: Status of control signals during various operation in hybrid 8T SRAM cell 58

Table 3.4: Energy consumption and access latency of the proposed hybrid 8T SRAM cell during various operation 60

Table 3.5: Status of control signal during various operational modes of proposed hybrid 11T SRAM cell 62

Table 3.6: Energy consumption and delay of proposed hybrid 11T SRAM cell..... 64

Table 3.7: Comparison results of different MTJ device based hybrid SRAM cell..... 67

Table 4.1: Status of control signal during normal operational mode..... 75

Table 4.2: Status of control signal during load operation..... 76

Table 4.3: Status of control signal during store operation..... 84

Table 4.4: Energy Consumption during different operational modes in Yanjun Ma and proposed multi-storage SRAM cell. 88

Table 5.1: Data restoration times of different state retentive flip-flop design..... 104

Table 5.2: Total power consumption during active mode by different state retentive flip-flops 105

Table 5.3: Energy Consumption during active mode for hybrid flip-flop HFF-I 106

Table 5.4: Energy Consumption during active mode for hybrid flip-flop HFF-II..... 107

Table 5.5: Leakage power consumption during sleep mode by different state retentive flip-flops..... 108

Table 5.6: Propagation delay calculated for different state retentive flip-flops..... 108

Table 5.7: Comparison of proposed state retentive hybrid FF with state-of-art state retentive FF 109

Table 5.8: Comparison of proposed hybrid flip-flops with existing MTJ based hybrid flip-

flop 111

Table 6.1: Truth table of c-element 117

Table 6.2: Simulation results of different volatile c-element 123

Table 6.3: Performance comparison of volatile and non-volatile hybrid c-element 123

Table 6.4: Energy consumption by volatile and non-volatile hybrid half-buffer 124

Table 7.1: Truth table of NAND logic operation 132

Table 7.2: Truth table of NOR logic gate 133

Table 7.3: Biasing voltage and switching time for NAND & NOR logic gates 134

Table 7.4: Truth Table for Two Input Logic Operations 139

Table 7.5: Truth Table of NAND & AND Logic Gates 139

Table 7.6: Status of Control Lines to Perform NAND & AND Logic Operations in Proposed C-MRAM 140

Table 7.7: Truth Table of NOR & OR gates 140

Table 7.8: Status of Control Lines to Perform NOR & OR Logic Operations in proposed C-MRAM 141

Table 7.9: Truth Table of proposed Approximate Adder (AX-ADD) 143

Table 7.10: Average Energy Consumption and Latency for Various Operations Performed in C-MRAM 148