Chapter-6. SPICE Modeling of Organic TFTs: Circuit Design and Simulation

6.1 INTRODUCTION

This chapter, details the modeling of an OTFT suitable for integration into the existing simulation tools and its use cases in design and simulation of OTFT based circuits. In the previous chapters, we tried to address the material related issues and the physics based modeling of OTFTs, which constitute a major part of the first phase of a new technology. The discussion in this chapter, is essentially about the **S**imulation **P**rogram for **I**ntegrated **C**ircuit **E**nvironment (SPICE) models which are extensively used for design and simulation of electronic circuits. Such models, are necessary to commercialize the OTFT technology and improve the yield when mass fabricated. Dedicated efforts from several researchers has led to a significant improvement in the performance of OTFTs. The state of the art OTFTs are now ready to compete with other existing technologies like oxide-TFTs and poly-Si TFTs. For the OTFT technology to make ways into the main stream electronics industry, it is necessary to make OTFT *designer friendly*. A retrospection into the CMOS technology, leads to a conclusion that: for an electronics technology to be successful, it is necessary to have reliable Electronic Design Automation (EDA) tools. EDA tools are a spectrum of tools which has the capability to convert a high level design description into a layout which when supplied to the foundry can be processed into a physical circuit. In the area of circuit simulation, **S**imulation **P**rogram for **I**ntegrated **C**ircuit **E**nvironment (SPICE) is a very useful simulation tool. SPICE is a basic tool among the various tools available in a commercial EDA design suite. It is one of the first tool to be used by a designer to design and analyse the performance of a circuit.

For an electronic technology to be successful, it is important that its analysis is supported by computer aided design (CAD) tools. These tools, facilitate the simulation and verification of the circuits prior to fabrication which not only saves the resources but also effectively cuts down the design cycle time. Success of these tools largely

depends on the efficiency of the device models used. An efficient model is the one which could replicate the characteristics of a physical device. Such models capture the charge transport mechanism and structure related effects of the actual devices. These effects are translated into suitable behavioral models which can be used for both DC, AC (frequency response) and transient analysis. Another important aspect for these models is their simplicity, which is necessary to implement the models in circuit simulators. Hence, it is essential and worthy to analyse the performance of an OTFT through an appropriate SPICE model. However, in developing SPICE models for an OTFT, the primary challenge is to accurately model and fit its complex charge transport mechanism. Converting the physical models into a SPICE model is not only a cumbersome process but also non-feasible due to the complex mathematical expressions and iterative numerical approaches used while arriving at the I-V characteristics in the physics based model. Therefore, a compact SPICE model is developed in a way, to mimic the OTFT characteristics in various regions. This is very much necessary to handle the simulation of complex circuits when put to simulation. There is little emphasis on the SPICE models for TFTs. This could be due to the wide variations in the existing technology, like: materials, architectures and carrier transport mechanism. Developing a unique, universal SPICE model which can fit a given TFT remains an open challenge.

In this chapter, we report a simple yet accurate SPICE Level-3 model adaptation for the OTFT. The model is chosen because of its empirical nature, its immediate relevance for the circuit designers and relatively less number of parameters, which simplifies the parameter extraction process. The model has been validated thoroughly against the IV characteristics obtained from a n-channel OTFT whose active layer is manufactured using a small molecule pentacene. Then the model has been put to use to simulate an inverter, which essentially tests the DC simulation ability. The inverter is further used to build a seven stage ring oscillator circuit where the transient response simulation has demonstrated the stability of the model. Later, a single stage common source amplifier (CSA) is demonstrated using the proposed SPICE model. The results obtained are promising and suggests that the approach used could be a suitable

technique for developing process design kits (PDKs) suitable to be used in complex circuit design and simulation.

6.2 COMPACT MODEL FORMULATION

Compact models are those models which are used in the semiconductor industry for circuit simulation. The primary objective of this model is to reproduce the terminal characteristics of a device under consideration. Compact model is a medium of exchange of information between the design engineer and the foundry. The essential features of a good compact model include: accuracy, computational efficiency, scalability for future technologies, ease of parameter extraction and relevance to circuit designers.

A compact model for any transistor should be able to model the physical processes occurring in it across all the regions of operation. Apart from the incorporation of the physical processes, it has to be reliable, that is, accurate with its results and should have less computation time. In addition to these factors, the model should also be free of any convergence problems. All these essential qualities can be found in a robust SPICE model. The MOS3 model or the SPICE Level 3 model is semi-empirical, as it considers the physical processes in the form of complex equations and includes empirical factors to reduce the complexity of the said equations. This reduction in complexity is actually compensated by the fact that with this approach, there are fewer chance of a non-convergent solution. Moreover, it increases the simulation speed considerably, which is an essential characteristic for a compact model to be used on complex circuits.

The SPICE Level 3 model was originally developed for silicon-based MOSFETs which has four terminals (Both physically and in the model definition too) namely: *source* (*S)*, *drain (D)*, *gate (G)*, and the *bulk* (or body) (*B*). While, an OTFT is essentially a three terminal device owing to its device architecture and charge transport mechanism. These three terminals, are: *S*, *D*, and *G*. Therefore, to adapt this model to use for an OTFT, the *S* and *B* terminals are internally connected. Any degradation in

electrical characteristics can be incorporated using contact resistances at the *S* and *D* contacts [171] Fig. 6-1 shows the equivalent small-signal model of an OTFT, where C_{GS} and C_{GD} are gate-source and gate-drain capacitances, respectively, g_m is channel trans-conductance, r_0 is the output resistance of the channel, V_{GS} is the potential difference between the gate and source terminals and R_S, R_D are the source and drain contact resistance, respectively.

The conduction mechanism of an OTFT differs from that of a MOSFET in terms of the conduction layer involved vis-à-vis, the type of mobile charge carriers conducting the current. In a MOSFET, the current is conducted by the minority charge carriers originating from the inversion layer, whereas in a TFT as well as in an OTFT, the current carriers are the majority charge carriers that arise in the accumulation layer [172]. It has been observed that the mobility of these mobile charge carriers is dependent on a variety of intrinsic factors like the molecular structure of the material, the ordering of the molecules to promote the inter-molecular π-π coupling, and region-chemical ordering in the bulk to offer short-range micro-crystallinity providing higher mobility conduction paths parallel to the plane of current conduction [173]. The intrinsic factors include the sample temperature, the lateral electric field, the free carrier density, and the carrier injection efficiency of the source and drain contact materials [173]. Another critical factor affecting the mobility of transport carriers is the trap state density in the semiconductor layer. Unlike a MOSFET, where the mobile charge carriers from the inversion layer wholly participate in the current conduction, in a TFT (and OTFT), the majority of the accumulation layer charge carriers get trapped in the tail states and the deep states in the bandgap.

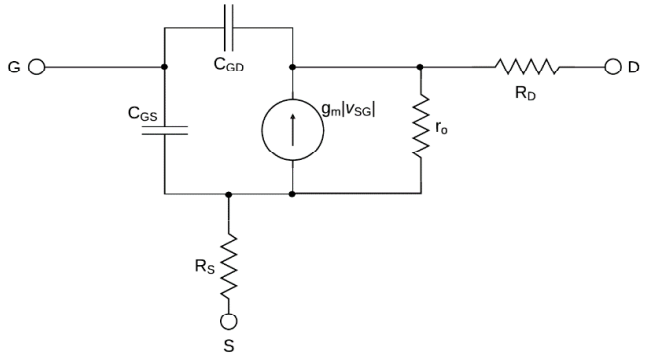


Figure 6-1 Small signal equivalent model of an OTFT

This implies that only a fraction of the entire accumulation layer population takes part in charge transport [174], resulting in the lower values of carrier mobilities observed in these devices. However, a parallel thermally-activated conduction pathway has been detected in such devices. On the increase of the device temperature, the traps contribute to the charge transport by releasing the trapped carriers in either of two processes, the multiple trapping and release (MTR), MTR in a relatively more ordered material, or the inter-trap hopping process in a highly disordered material [173], [175]. Thus, the mobility of an OTFT increases slightly with temperature. In adapting the SPICE Level 3 model to an OTFT, these differences must be encapsulated to obtain verifiable results. To accommodate this anomalous behavior of an OTFT as compared to a MOSFET, the aforementioned figure of merits, namely the threshold voltage (V_T), the effective field-effect mobility (μ_{Eeff}), the subthreshold swing (*SS*) and process trans-conductance parameter (*KP*) are extracted from experimental characteristics and are then employed to modulate the corresponding SPICE parameters. Fig.6-2 depicts a flowchart describing the model development strategy employed. Table 6.1 lists the SPICE Level 3 parameters and a brief description of their extraction procedure from the experimental data.

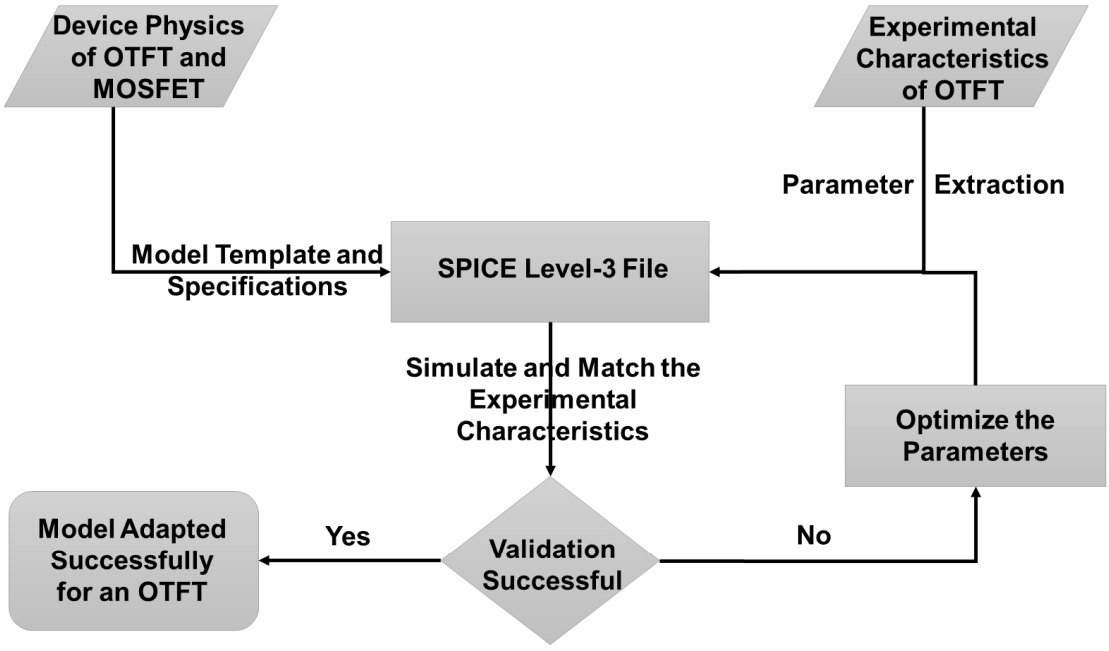


Figure 6-2 A flow-chart demonstrating the parameter extraction and model fitting

Table 6-1 SPICE Level 3 parameters and a short note on their extraction procedure

SPICE Parameter	Description	Remarks
VTO (V)	Threshold voltage (V_T)	Extrapolation from saturation region [176]
ETA (V^2/A-s-cm)	Static feedback factor	Calculate from the slope of threshold voltage vs. drain voltage [177]
SS (V/decade)	Subthreshold swing	Inverse slope of logarithm of drain current vs. gate voltage [178]
NFS (/cm^2V^1)	Fast surface state density	Calculated from subthreshold swing [172]
UO (cm^2/Vs)	Low field bulk mobility (μ_o)	Extrapolation from saturation region [173]
THETA (/V)	Mobility modulation parameter	Calculated from the slope of drain current vs. gate voltage [177]
Tox	Oxide thickness	Calculated from equivalent oxide thickness (EOT)
KP (A/ V^2 s)	Process trans-conductance parameter	Modified by the mobility and the oxide capacitance
RD, RS (Ω)	Drain/Source resistance	Models contact resistance effects on drain current

6.3 MODEL VALIDATION AND CIRCUIT APPLICATIONS

Any compact model developed with the aim of device or circuit simulation, has to be versatile. If the model is developed for a certain device, it should be applicable to every possible architecture of that device. Apart from its versatility, it is critical for the model to be benchmarked against existing literature to analyse its aptness. To this extent, section 6.3.1 presents a comparison of the SPICE model with that of an experimental device found in the literature.

6.3.1 Benchmarking of the Developed Model

The adapted SPICE Level 3 model could be fitted to replicate the performance of any OTFT regardless of the organic semiconductor or the gate dielectric. To verify the accuracy of the model, it has been compared with the experimental work on pentacene

OTFT by Su et al. [153]. From the experimental characteristics of the OTFT, SPICE Level 3 model performance parameters like the threshold voltage, low field bulk mobility, and subthreshold swing were extracted. Further, these parameters are used to extract secondary parameters like the fast surface state density, and the mobility modulation factor. The values of these extracted parameters are mentioned in Table 6-2. This transistor had an aspect ratio of 1500 μm/56 μm. Fig. 6-3 shows the circuit schematic while Fig.6-4 (a) and (b) show the simulated output and transfer characteristics of the transistor in comparison with the experimental data reported by Su et al. [153]

The software LTSpice® (from Analog Devices) is used to simulate the adapted SPICE Level 3 model. The Direct Current (DC) analysis in the software took a total of 60 ms. The spice directive governing the analysis performs a DC sweep from -2 V to 0.5 V in simulation steps of 10 mV. This gives a total of 251 steps with the time taken for each step being approximately 240 μs. The simulated results show a considerably good match with the experimental results with the transfer characteristics showing an excellent fit of the data. However, a small deviation from the data can be observed in all the simulated curves. This small deviation is due to the difference between the carrier transport mechanism of an OTFT and MOSFET. One has to note that any model which is originally developed for Si MOSFET can only capture the characteristics of an OTFT behaviourally rather physically. In the subsequent sections, the use of the model proposed is demonstrated by performing circuit simulations of some most commonly used circuits in digital and analog applications.

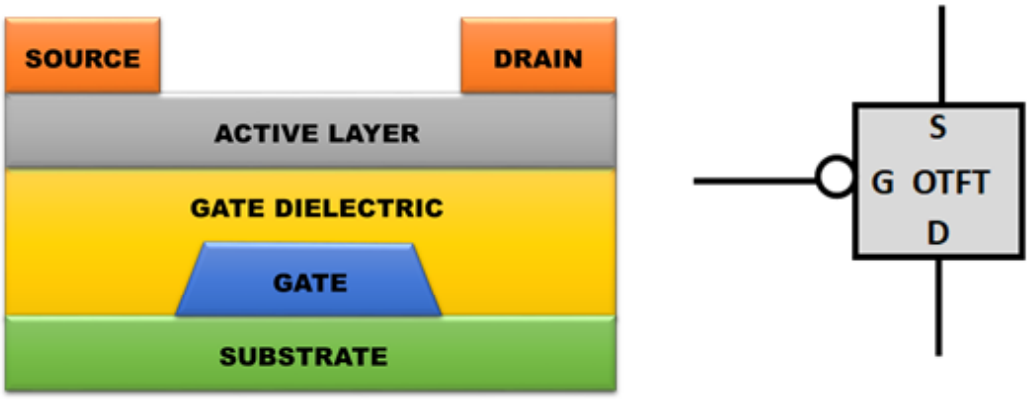
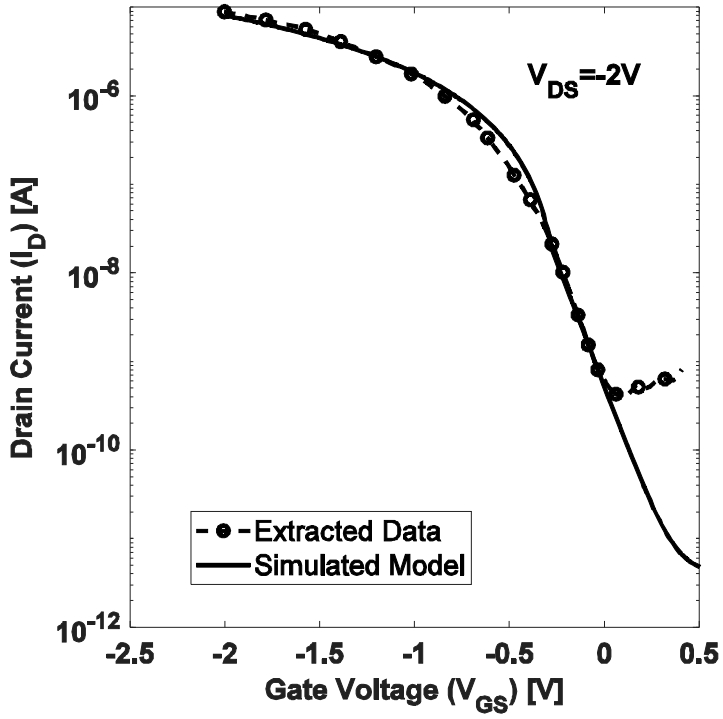


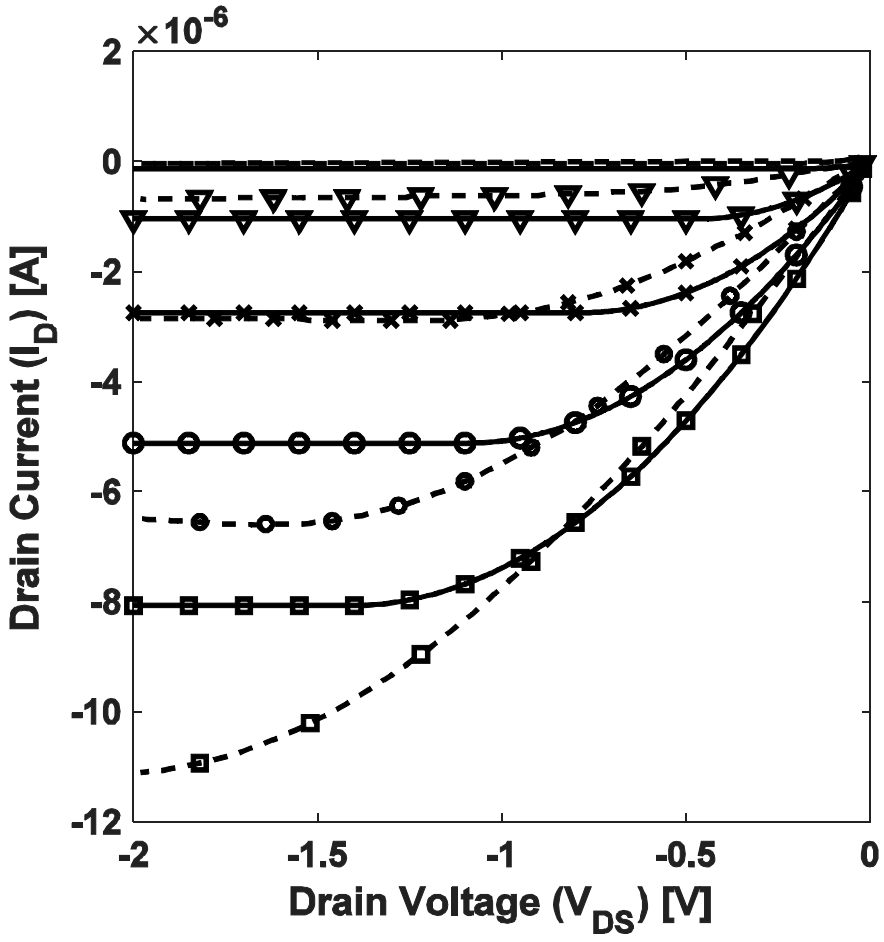
Figure 6-3 Structure of a bottom-gate to-contact (BGTC) OTFT and a symbol used for p-channel OTFT

Table 6-2 Values of the extracted SPICE Level-3 Parameters

SPICE Parameter	Description	Extracted value
VTO (V)	Threshold voltage (V_T)	-0.2 V
SS (V/dec)	Subthreshold swing	187.5 mV/decade
NFS (/cm^{2}V^1)	Fast surface state density	2.4E+12 /cm^{2}V
UO (cm^2/Vs)	Low field bulk mobility (μ_o)	1.38 cm^2/Vs
THETA (/V)	Mobility modulation parameter	0.2 /V
EOT (m)	Effective oxide thickness	14.7E-9 m



(a) Transfer Characteristics of the OTFT



(b) Output Characteristics of the OTFT

Figure 6-4 Comparison between simulated and experimental data (a) Transfer Characteristics (b) Output Characteristics: dotted lines indicate experimental data and solid line indicate Simulation output. Legend: Squares V_{GS}=-2V, Circles V_{GS}=-1.6V, Cross V_{GS}=-1.2V and Triangles V_{GS}=-0.8V

6.3.2 OTFT as an Inverter

An inverter, a single input, single output circuit in digital electronics, is a fundamental and most commonly used logic gate in realistic applications. It acts as the building block for much more intricate circuits like NAND gates, adders, multipliers, etc. It is also true that the behaviour of such derivative circuits can be extrapolated and interpreted using the behaviour of inverters. Thus, it is imperative for any model to be able to design and simulate an inverter with an acceptable voltage transfer characteristic (VTC). Accordingly, the model developed was used to create a resistive load inverter

with the resistance accomplishing the role of the pull-down network (PDN). The designed inverter employed a load resistance of 0.2MΩ and a load capacitance of 1pF and had a single rail supply of 5 V. The resistance was chosen as 0.2 MΩ to ensure decent noise margins and an approximately mid-rail value of switching threshold. The schematic for the same is given in Fig.6-5 shows the inverter circuit and Fig.6-6 shows the VTC of the designed inverter. Table 6-3 gives the values of the important performance parameters of the inverter.

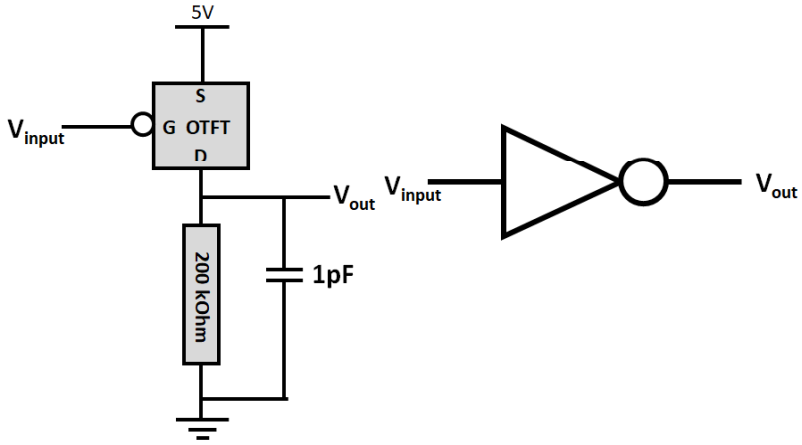


Figure 6-5 Circuit schematic and symbol of a resistive load inverter implemented using a p-type OTFT as a driver

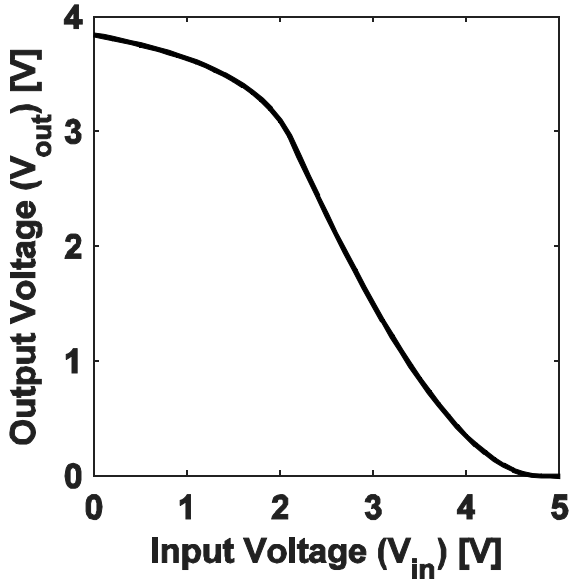


Figure 6-6 Voltage transfer characteristics (VTC) of the designed resistive load inverter

Table 6-3 Important performance parameters of the resistive load inverter shown in Fig.6-5

Design Parameter	Description	Value
V_m	Switching threshold voltage	2.41 V
V_{OL}	Min. output voltage when the output level is logic "0"	105.00 μV
V_{OH}	Max. output voltage when the output level is logic "1"	3.84 V
V_{IL}	Max. input voltage which can be interpreted as logic "0"	1.92 V
V_{IH}	Min. input voltage which can be interpreted as logic "1"	3.74 V
NM_L	Noise margin for low signal levels	1.92 V
NM_H	Noise margin for high signal levels	0.10 V
$P_{DC(avg.)}$	Average DC power consumed by the circuit	62.50 μW

6.3.3 Application as a Ring Oscillator

After demonstrating the success of a DC sweep analysis with the proposed SPICE model, a transient analysis test is performed for checking the stability of the model in handling the voltage and current variables over a range of values in a cyclic way. This analysis not only asserts the stability of the model but also shows the reproducibility. For this test we have opted for a ring oscillator.

A ring oscillator has multiple applications in digital electronics. One of the most fundamental applications of a ring oscillator is an astable pulse generator. This can also be used in a phase-locked loop (PLL) as the voltage-controlled oscillator (VCO), to test wafers for the effect of voltage and temperature, etc. Another application of a ring oscillator is to find the propagation delay of its constituent inverters to standardize them. For this purpose, a 7-stage ring oscillator is designed using the inverter developed. After the specification of an initial condition, transient analysis is performed to gauge the stability of the system. The circuit schematic for the ring oscillator is shown in Fig. 6-7. Table 6-4 summarizes the important parameters derived from the

analysis. Fig. 6-8 and Fig. 6-9 show the transient response of the circuit under free oscillations (generates a sine wave) and driven by an external square wave respectively.

Results obtained from the simulation of an inverter and a ring oscillator shows that the adapted SPICE Level 3 compact model for an OTFT was able to demonstrate an inverter with modifiable and desirable parameters and thus, has potential for circuit applications in digital electronics.

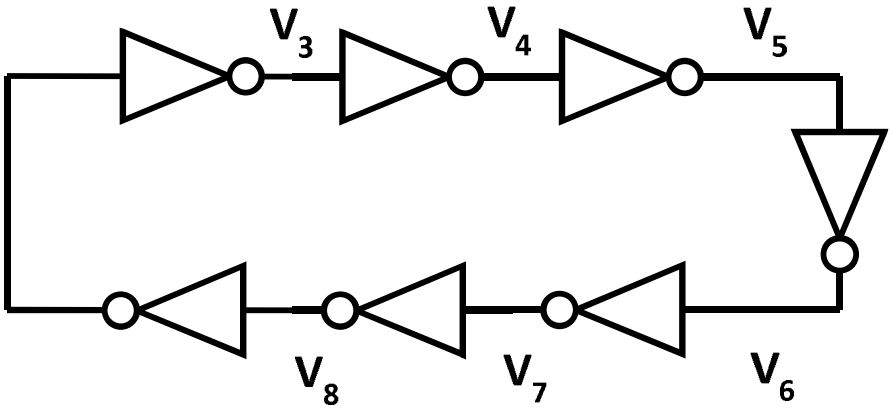


Figure 6-7 Circuit schematic for a 7-stage ring oscillator, each inverter is a resistive load inverter shown in Fig.6-5

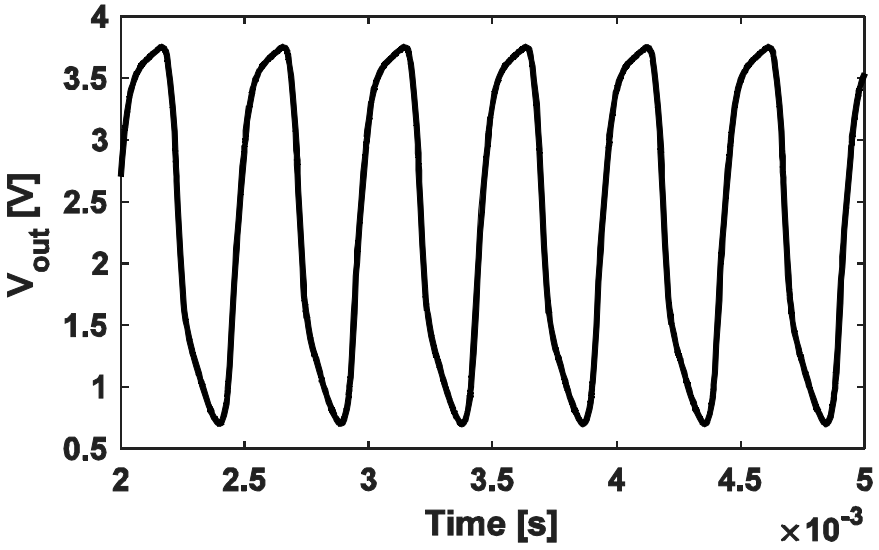


Figure 6-8 Free oscillations of 7-stage oscillator

Table 6-4 Performance parameters of the 7-stage ring oscillator

Design Parameter	Description	Value
f	Frequency	2.10 kHz
t_p	Propagation delay of the inverter	34.86 μs

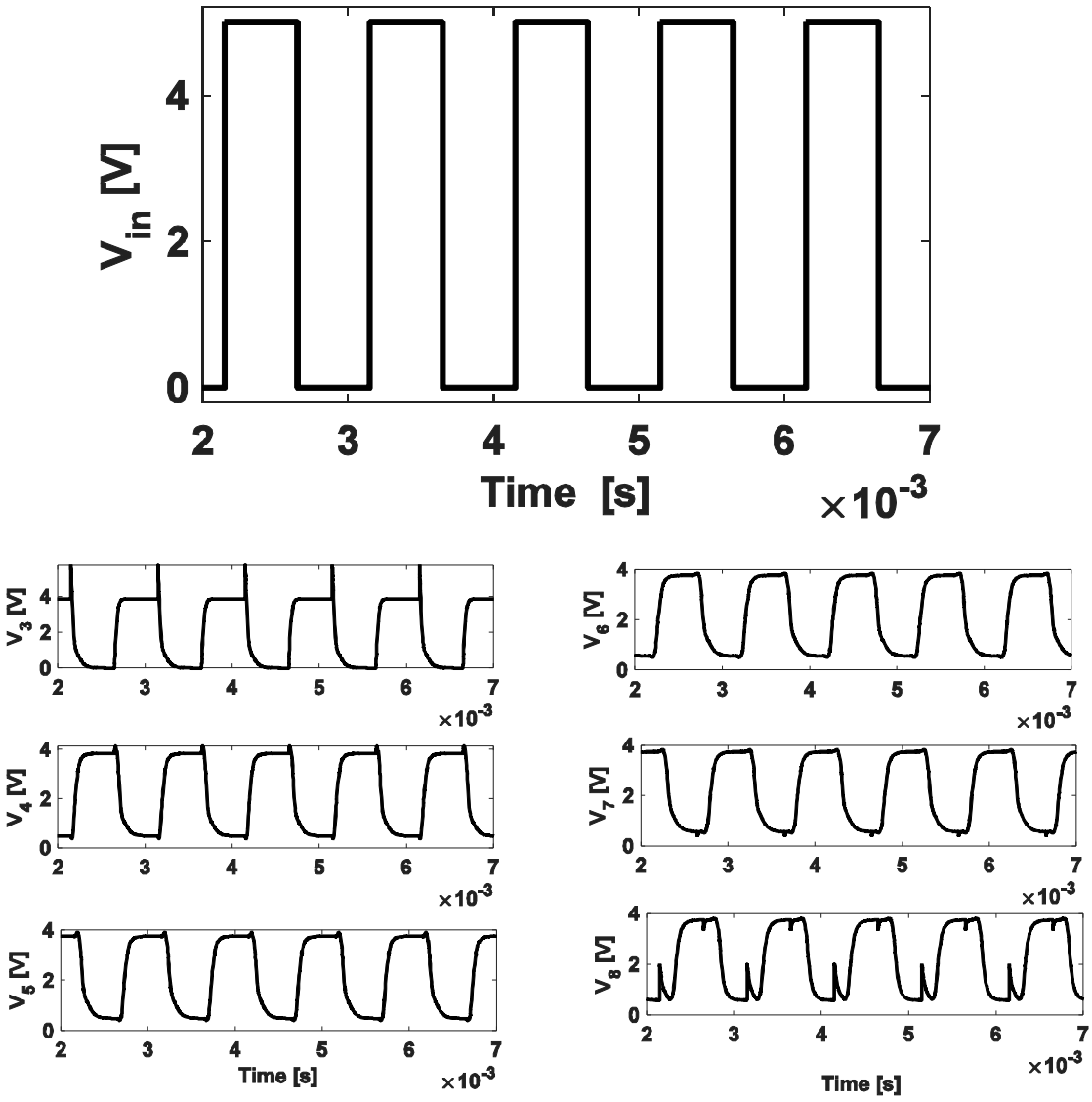


Figure 6-9 Transient analysis on the 7-stage ring oscillator using a square wave input (V_{in})) and the output at each stage (V_3 to V_8). These Voltages are marked in Fig.6-7

6.3.4 Application as a Common Source Amplifier

A common source amplifier (CSA) is one of the three basic configurations of a single stage amplifier in analog electronics domain. It is an ideal circuit for voltage amplification applications because of its: high input impedance, high voltage gain and low output impedance. A good behavioral device model should be able to capture the frequency response of an analog circuit apart from the transient and DC response. The CSA amplifier is a resistive-load, single stage amplifier with a 2 MΩ load resistance, and 1 pF load capacitance. Suitable DC bias voltage is applied at the gate terminal of the CSA to bias it in its saturation region. The 1pF capacitance is chosen here to replicate the realistic scenario of an OTFT driving the OLED in a pixel driver circuit. The schematic for the same is given in Fig. 6-10. Fig. 6-11 shows the voltage transfer characteristics and the transient response of the amplifier for a 1kHz sinusoidal signal is shown in Fig.6-12. The frequency response of the amplifier is shown in Fig.6-13. Table 6-5 gives the values of the performance parameters of the CSA amplifier. The biasing of the circuit was aimed at achieving a high gain from the circuit. Since the phase crossover frequency falls well after the gain crossover frequency (roughly a factor of 3350 times) for the designed common source amplifier, the circuit can be considered stable (doesn't break into oscillations) during negative feedback operation. Taking into consideration the observation that the phase margin is approximately 90º, it can be said that the circuit is found to be exceptionally stable. This also supports the potential use of the designed SPICE Level 3 compact model for an OTFT in analog circuit applications.

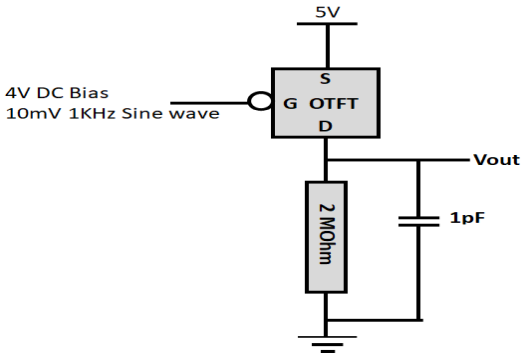


Figure 6-10 Circuit schematic of common source amplifier with a voltage gain of 18dB and 3-dB bandwidth of 74kHz

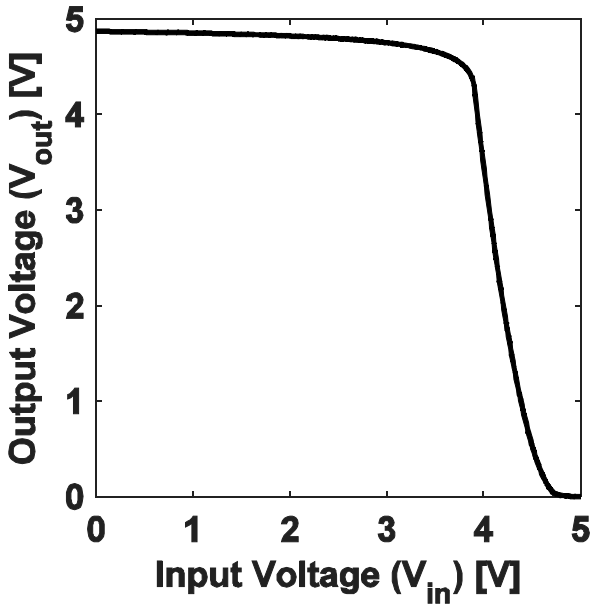


Figure 6-12 Voltage transfer characteristics for the common source amplifier

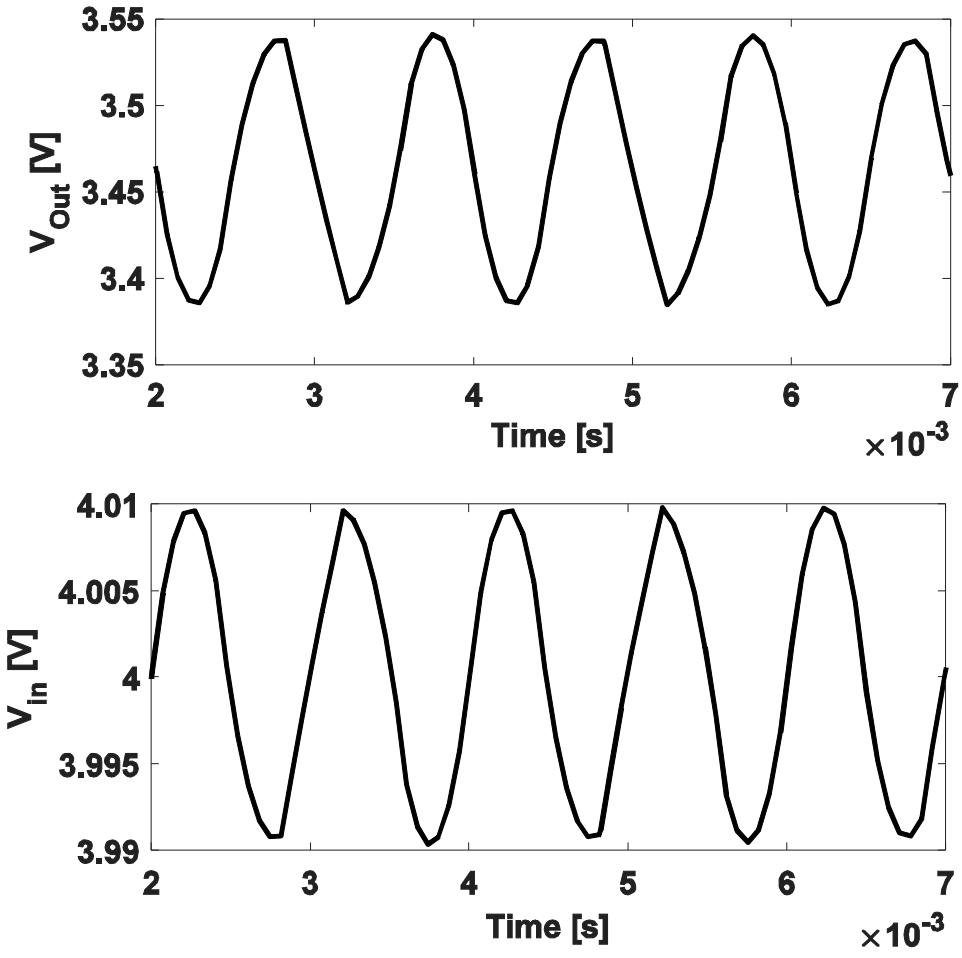


Figure 6-11 Transient analysis of the common source amplifier

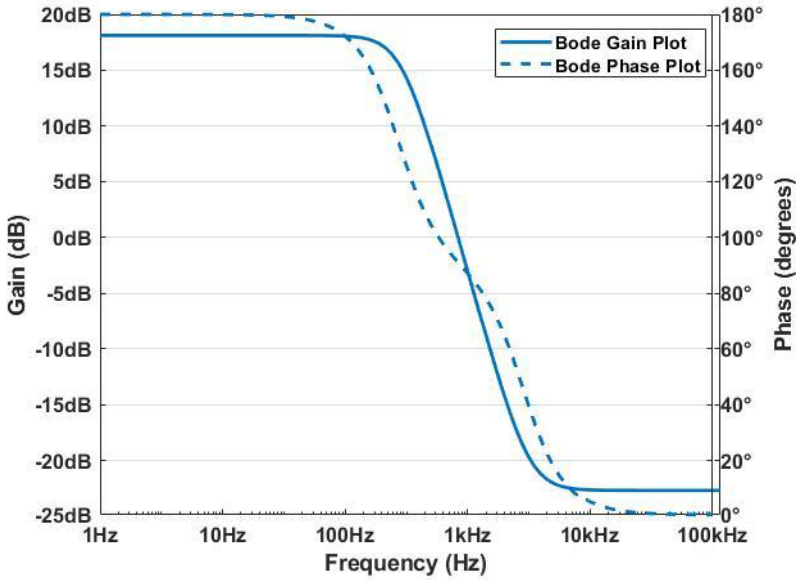


Figure 6-13 Frequency response of the common source amplifier

Table 6-5 Performance parameters of the common source amplifier

Design Parameter	Description	Value
Q-point	Quiescent point (DC bias point) (V_{GS},I_D)	(4V,1.73μA)
Input DC offset	DC voltage on which input ac signal rides	4 V
Output DC offset	DC voltage on which output ac signal rides	3.46 V
A_v	Voltage gain (magnitude)	18.12 dB
A_{max}	Maximum amplitude of input ac signal for amplification without clipping	175.16 mV
f_{3dB}	-3dB pole frequency	74 kHz

6.4 RESULTS AND DISCUSSION

The developed model for an OTFT is observed to follow the experimental data successfully. A smooth transition from linear to saturation region in the output characteristics (I_D Vs V_{DS}) could be observed. Also the transfer characteristics (I_D Vs V_{GS}) have a good matching in the near threshold and above threshold region. Through a very limited set of parameters, the model is able to replicate the behaviour of the OTFT. The significance of this result is that, using a single test device and standard I-

V characteristics captured through standard test equipment, it is possible to build a reasonably accurate, computationally efficient, stable and reliable compact model for circuit simulation. This simplifies the process of developing the library files which are a part of the process development kit (PDKs) necessary for the circuit engineers. Moreover, the adaptation of SPICE Level-3 model and its demonstration on a free tool like LTSpice® empowers the device engineers to develop the library files without resorting to commercial vendors.

The inverter VTC, is continuous, stable and has no anonymities. This clearly indicates the success of the model in DC sweep performance. This also emphasizes the continuity and practical values over a range of voltages. Since the SPICE models are behavioural models rather the physics based models this is necessary to check if there are un-realistic undesired values generated when subjected to different realistic input conditions. In the VTC simulation, the entire input voltage range (possible values are between 0V and the supply voltage) has been swept in fine steps (10mV). It is observed that the drain current for each of these steps is in close resemblance with practically possible values and no undesired value is obtained. Furthermore, the ring oscillator circuit simulation demonstrated the suitability of this model in a transient analysis. Moreover, in this analysis, the circuit has around 7 OTFTs and 14 other passive elements (resistors & capacitors). Continuous, smooth oscillations at the output waveform clearly indicates the ability of the model developed in a multi device environment and compatibility while simulation environment has other components. The rising, falling transitions are smooth with no sharp discontinuities. This demonstrates the validity of the model for large circuits.

The AC response of the CSA amplifier (Bode plot) and transient response shows the first order continuity of the I-V characteristics of the SPICE model developed. The satisfactory outcome of this model shows that it can be used in an analog environment. The analyses performed for the validation and demonstration of the circuit applications were all under 100 ms. The output characteristic simulation took 60ms while the transfer characteristic curve plot took a total of 75 ms. The DC analysis to plot the VTC of the inverter took 52 ms in all. The transient analysis for the ring oscillator consumed

95 ms. In the analog domain, the transient analysis of the common source amplifier took 78 ms and the ac analysis took 14 ms. These analysis show that the model is computationally efficient and fast.

6.5 CONCLUSION

A SPICE Level 3 model is successfully extended to capture the behavioral characteristics of an OTFT. The model is independent of the materials used for the OTFT and its architecture, thereby making it a generic model for any OTFT. The model is validated using the experimental characteristics extracted for a bottom gate top contact p-type OTFT. Subsequently, the model is used for demonstrating circuit design applications in both digital and analog environments. The computation time for all the circuits were found to be under 100 ms. This shows that the adapted model is computationally efficient and fast. Therefore, it can be used as a means of information exchange between the device and circuit engineers' community. With short development times and ready implications for the circuit level operation, the model serves both the device and circuit engineers.