Abstract

Multiplication is one of the basic arithmetic operations used in almost all computations. The performance of many computational units is dominated by the speed at which a multiplication operation can be executed. Taking this into consideration various researchers have developed novel algorithms and circuit techniques for multiplication to provide higher speeds and optimized use of silicon area.

This thesis explores different algorithms, architectures and circuit techniques used for parallel multiplier implementations. In this process ten architectures are defined. Each architecture is used to design multipliers of operand sizes 8, 16, 32, 54 and 64 bits. For each multiplier delay is calculated in terms of the delay of two-input XOR gate. All multipliers are synthesized using Magma EDA tool. Post synthesis delay, power, area and cell counts are found. Based on these results, best architecture for a multiplier of required operand size and preferred figure of merit is determined.

In the process of exploration of circuit techniques, a new Booth encoder and a new Booth selector circuit are proposed for partial product generation. These two circuits for partial product generation are smaller in transistor count and are comparable to the best-reported circuits in terms of delay and power consumption. A new 4:2 compressor circuit is also proposed, which outperforms other recently reported 4:2 compressors in terms of energy delay product and transistor count.

A novel final adder architecture named as CLEBC is proposed based on redundant binary arithmetic, equivalent bit conversion algorithm and carry-lookahead technique. This adder is faster than the carry-lookahead adder for any bit length. For addition of two 32-bit numbers, a CLEBC adder is 30% faster than a carry-lookahead adder.