Chapter 5

Parallel Multiplier Architectural Choices

The previous chapters discussed the three steps in parallel multiplication and various possible architectures for each step. This chapter presents ten different parallel multiplier architectures obtained by choosing different combinations of partial product generation methods, accumulation methods and final adders or RB to NB conversion methods. The worst-case delay in terms of T_{xor} is obtained for all multiplier architectures using the delay summary obtained from the previous chapters.

For proper understanding, each architecture is explained through the design process of a 16x16 multiplier. All 16x16 bit multiplier architectures, except the two using radix-64 encoding are designed with reference to the multiplication of two 16 bit signed binary numbers explained in Fig. 3.2 of chapter 3.The theoretical worst-case delay calculation in terms of T_{XOR} for each 16x16 multiplier architecture is explained clearly. The same methodology is adopted for designing multipliers for different operand sizes using each architectural choice and the corresponding theoretical worst-case delay calculation is carried out.

5.1 Array multiplier with CLA (AMCLA)

The array multiplier with CLA in the final adder stage is referred as AMCLA. In this architecture in the first step of multiplication, partial products are generated using BE-new and BS-new reported in chapter 2. In a 16x16 multiplier architecture shown in Fig. 5.1 “be0” generates three control signals Xj, Mj, PLj. These control signals are used by “BS row 0” to

generate the first partial product row containing 17 partial products, s-bit and $\bar{s}$-bit. Other partial product rows are also obtained using the bex and BS row x combinations, where x is the partial product row obtained. The critical delay in this step (as obtained in chapter 2, section 2.3.3) is $2.3T_{xor}$.

The obtained partial product rows are added using carry save adder rows. The "Adder row 1" adds first three partial product rows. A single adder in "Adder row 1" adds three partial products, each belonging to one of the first three partial product rows. In case no partial product is available for giving as one of the inputs to an adder, zero is given as input. So the first adder row consists of 23 adders. Each adder has outputs of one sum bit and one carry bit. The four lowest order adders' outputs (i.e. sum and carry) of "Adder row 1" are directly given as inputs to the final adder stage. The remaining 19 adders' sum and carry form the first row of adders along with the third partial product row are added by the second adder row. The first two adder outputs of the second adder row "Adder row 2" are directly applied to final adder. The other sums and carries are applied as inputs to the next adder row. In this way 8 adder rows accumulate the partial products to give the final sum and carry rows. The accumulation delay in this step as discussed in chapter 3 is equal to $11T_{xor}$.

The final sum and carry rows obtained after accumulation are added using a 32-bit CLA. The delay involved in this addition is$13.02T_{xor}$ (from chapter 4). So the worst-case delay of a 16-bit AMCLA is the summation of these three delays and is equal to $26.13T_{xor}$.

This same methodology is used for designing multipliers of different operand sizes and computing their worst case delays in terms of T_{xor} and the results obtained are summarized in Table 5.1.

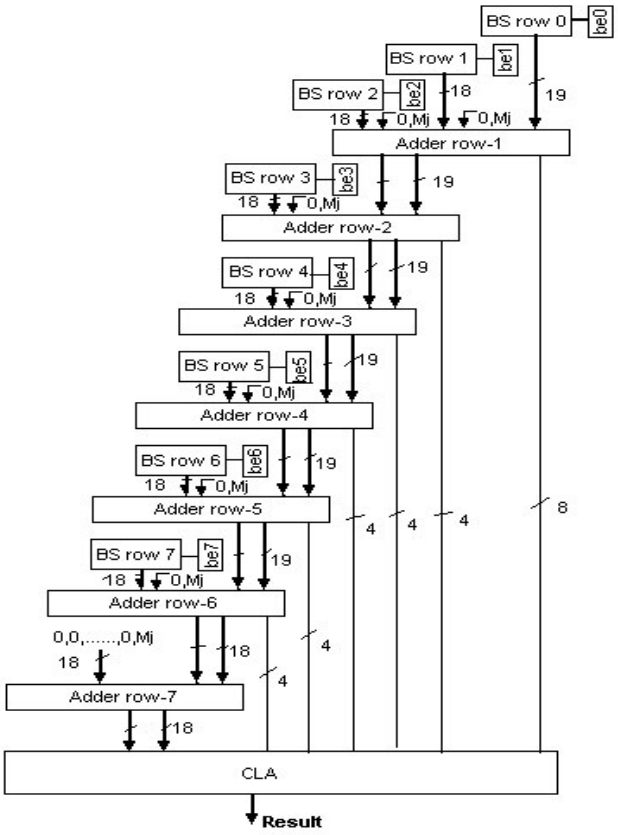

Fig. 5.1 A 16x16 multiplier based on AMCLA architecture.

Table 5.1 Summary of worst-case delays of AMCLA multipliers of different operand sizes in terms of T_{XOR}

Multiplier size	Delay in partial product generation	Delay in accumulation of partial product rows	Delay in final addition	Delay in multiplication
8x8	2.11	5	10.575	17.685
16x16	2.11	11	13.025	26.135
32x32	2.11	23	15.475	40.585
54x54	2.11	39	17.925	59.035
64x64	2.11	47	17.925	67.035

5.2 Array multiplier with CLEBC (AMCLEBC)

The array multiplier with CLEBC in the final adder stage is referred to as AMCLEBC. In this architecture the partial product generation and accumulation of partial product rows are done in the same way as in the AMCLA. A CLEBC is used as shown in Fig 5.2 to perform the final addition of the sum and carry rows after accumulation. The delay of a 32-bit CLEBC adder is $7.42T_{xor}$ (as obtained in chapter 4). So the worst-case delay for a 16x16 multiplier is $20.54T_{xor}$. To calculate the delay of multipliers of different operand sizes based on the AMCLEBC architecture, the final adder delays of Table 5.1 are replaced with the CLEBC adder delays for the corresponding operand sizes. The worst-case multiplier delays are the sum of delays in the three steps and are summarized in Table 5.2.

Table 5.2 Summary of worst-case delays of AMCLEBC multipliers of different operand sizes in terms of T_{XOR}

Multiplier size	Delay in partial product generation	Delay in accumulation of partial product rows	Delay in final addition	Delay in multiplication
8x8	2.11	5	4.87	11.98
16x16	2.11	11	7.42	20.53
32x32	2.11	23	9.97	35.08
54x54	2.11	39	12.52	53.63
64x64	2.11	47	12.52	61.63

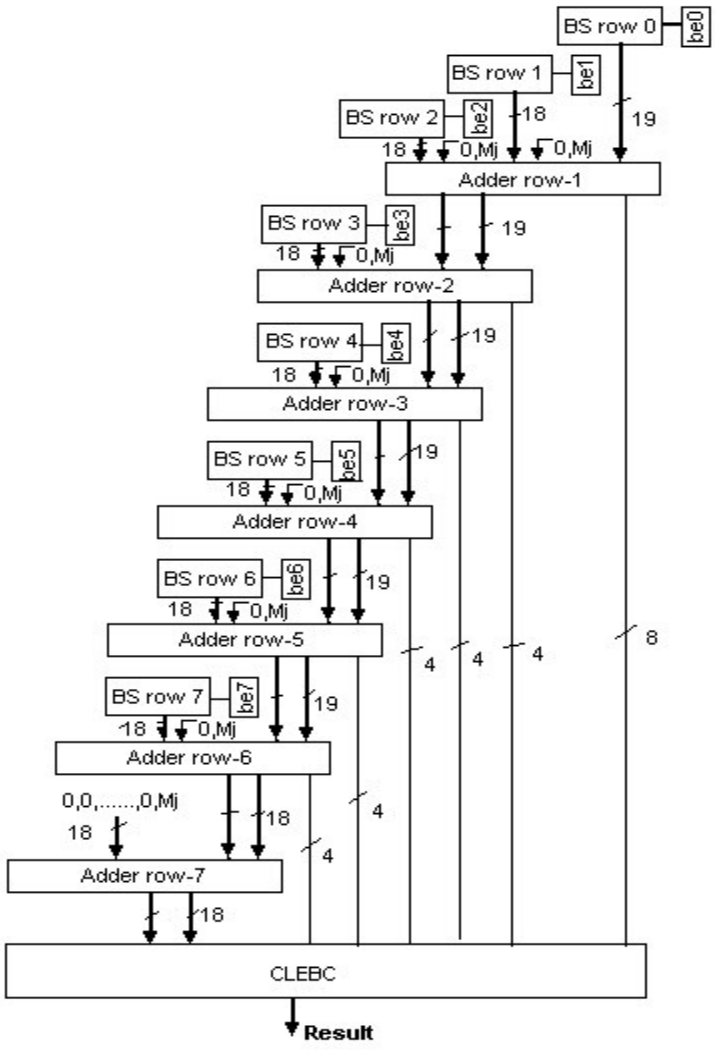

Fig. 5.2 A 16x16 multiplier based on AMCLEBC architecture.

5.3 Wallace tree multiplier using 3:2 compressors with CLA (WM32CLA)

In this section the multiplier architecture discussed uses 3:2 compressors in the accumulation stage and a CLA in the final adder stage. This architecture is referred to as the WM32CLA.

In WM32CLA architecture partial products are generated in the same way as in AMCLA using BE-new and BS-new circuits. The use of Booth encoders and Booth selectors to obtain partial products rows of a 16x16 multiplier is shown in Fig. 5.3. So the delay in partial product generation is $2.3T_{xor}$.

In this 16x16 multiplier, as shown in Fig. 5.3 the first three rows of partial products are obtained using Booth encoder (be) and Booth selector row (BS row) combinations. They are applied to a 3:2 compressor row (3:2 comp_00) consisting of 23 numbers of 3:2 compressors. A single 3:2 compressor in "3:2 comp_00" adds three partial products, each belonging to one of the first three partial product rows. In case no partial product is available to give as an input to an adder, zero is given as input. In the same way the next three partial product rows are applied as inputs to "3:2 comp_01". The sixth and seventh partial product rows along with the 0,0,…M8 are applied to "3:2 comp_02". All these three 3:2 compressor rows can add simultaneously. The sum and carry outputs of first four adders of "3:2 comp_00" are directly given to final adder stage. The remaining 19 sums and 19 carries along with the outputs (sum) of "3:2 comp_01" are applied to the next level of 3:2 compressor row (3:2 comp_10). Similarly "3:2 comp_11" is also used to add remaining carries and sums as shown in Fig. 5.3. Two more levels of 3:2 compressor rows are also used to finally give a sum row and a carry row. It is to be noted that, the three inputs to any single 3:2 compressor must have identical binary weights. This 16x16 multiplier architecture uses four levels of 3:2 compressors. The maximum delay in this accumulation stage is $8T_{xor}$.

The accumulated sum and carry rows are added using a 32-bit CLA. The delay involved in this addition is$13.02T_{xor}$. So the worst-case delay of a 16-bit WM32CLA is the summation of these three delays and is equal to $23.135T_{xor}$.

This same methodology is adopted for designing multipliers of different operand sizes and computing their worst case delays in terms T_{xor} and results obtained are summarized in Table 5.3.

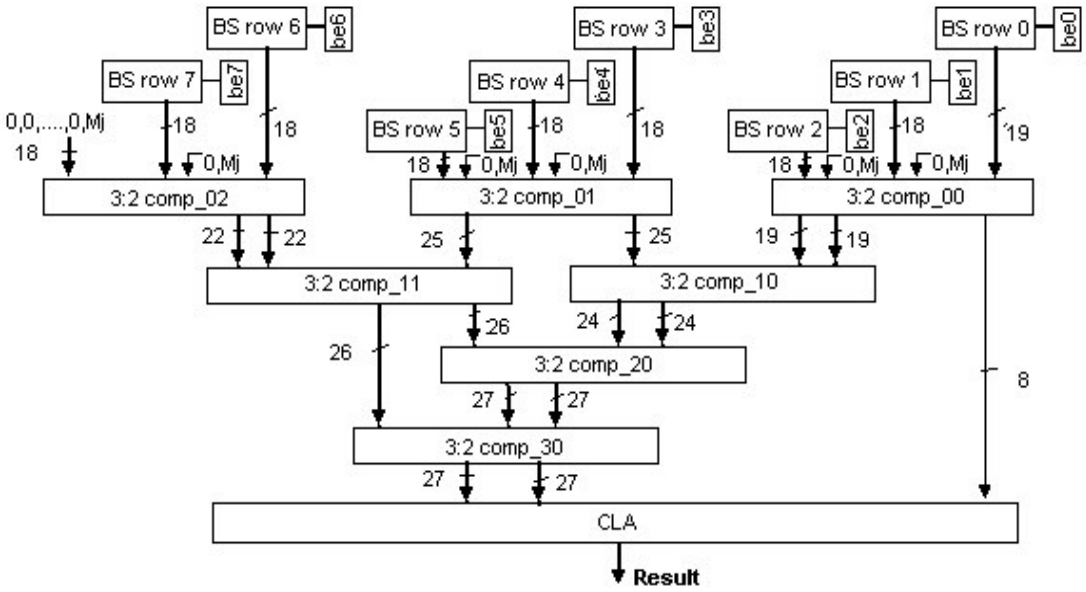

Fig. 5.3 A 16x16 multiplier based on WM32CLA architecture.

Table 5.3 Summary of worst-case delays of WM32CLA multipliers of different operand sizes in terms of T_{XOR}

Multiplier size	Delay in partial product generation	Delay in accumulation of partial product rows	Delay in final addition	Delay in multiplication
8x8	2.11	6	10.575	18.685
16x16	2.11	8	13.025	23.135
32x32	2.11	12	15.475	29.585
54x54	2.11	14	17.925	34.035
64x64	2.11	16	17.925	36.035

5.4 Wallace tree multiplier using 3:2 compressors with CLEBC (WM32CLEBC)

In this architecture the final adder stage of the WM32CLA is replaced by CLEBC adder stage and the architecture is named as WM32CLEBC. In this architecture the partial product generation and the accumulation of partial product rows are done in the same way as in a WM32CLA. Only the final addition of accumulated sum and carry rows is done by using

CLEBC as shown in Fig 5.4. So the delay in this final adder stage is $7.42T_{XOR}$ and the worst-case delay for a 16x16 multiplier is 17.53 T_{XOR}. The worst-case delays for multipliers of different operand sizes using WM32CLEBC architecture are obtained by replacing the final adder delays of Table 5.3 with the delays of that of CLEBC adders of corresponding operand sizes and are summarized in Table 5.4.

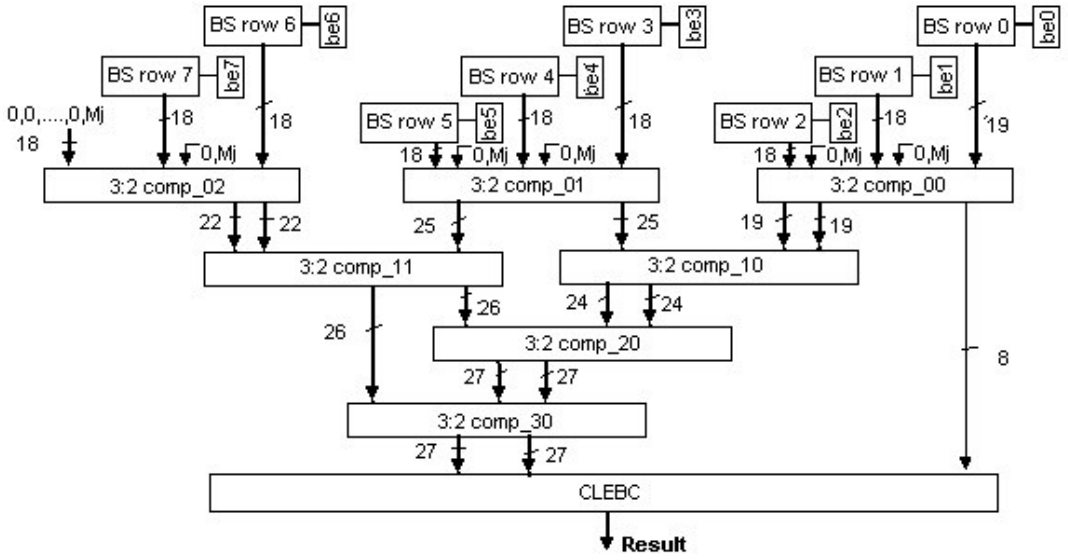

Fig. 5.4 A 16x16 multiplier based on WM32CLEBC architecture

Table 5.4 Summary of worst-case delays of WM32CLEBC multipliers of different operand sizes in terms of T_{XOR}

Multiplier size	Delay in partial product generation	Delay in accumulation of partial product rows	Delay in final addition	Delay in multiplication
8x8	2.11	6	4.87	12.98
16x16	2.11	8	7.42	17.53
32x32	2.11	12	9.97	24.08
54x54	2.11	14	12.52	28.63
64x64	2.11	16	12.52	30.63

5.5 Wallace tree multiplier using 4:2 compressors with CLA (WM42CLA)

This architecture uses 4:2 compressors in the Wallace tree structure for partial product accumulation and a CLA in the final adder stage. This architecture is referred to as the WM42CLA. Here the partial products are generated using the same radix-4 Booth encoding method. So the BE-new (for Booth encoder) and BS-new (for Booth selector) circuits are used for partial product generation as in the case of the AMCLA architecture.

The generation of partial product rows for a 16x16 multiplier using Booth encoder (be) and Booth selector row (BS row) combinations is shown in Fig. 5.5. The first four partial product rows are applied as input to the 4:2 compressor row "4:2 comp 00". The remaining four partial product rows are given as input to "4:2 comp 01". As the "4:2 comp 00" adds partial products with bit weight 2^0 (the LSB bit in first partial product row) to 2^{24} (the MSB bit in the fourth partial product row), it contains 25 numbers of 4:2 compressors. The number of 4:2 compressors used in a single compressor row is obtained by knowing the maximum and minimum weights of the bits to be added. The outputs of two 4:2 compressor rows are accumulated using a second level of 4:2 compressor rows. Finally to add the M_{14} bit, one more level of 4:2 compressors is used. This gives the final sum row and the carry row. It is to be noted that a single 4:2 compressor always compresses 4-bits of different partial product rows, but must have same binary weight. In case of non-availability of a partial product input, 0 is given as an input.

The sum and carry rows obtained after the accumulation are added using a 32-bit CLA. The delay involved in this addition is 13.02 T_{xor}. So the worst-case delay of a 16-bit WM42CLA is the summation of these three delays and is equal to 24.135 T_{xor}.

This same methodology is used in designing multipliers of different operand sizes and computing their worst-case delays in terms of T_{xor} and the results obtained are summarized in Table 5.5.

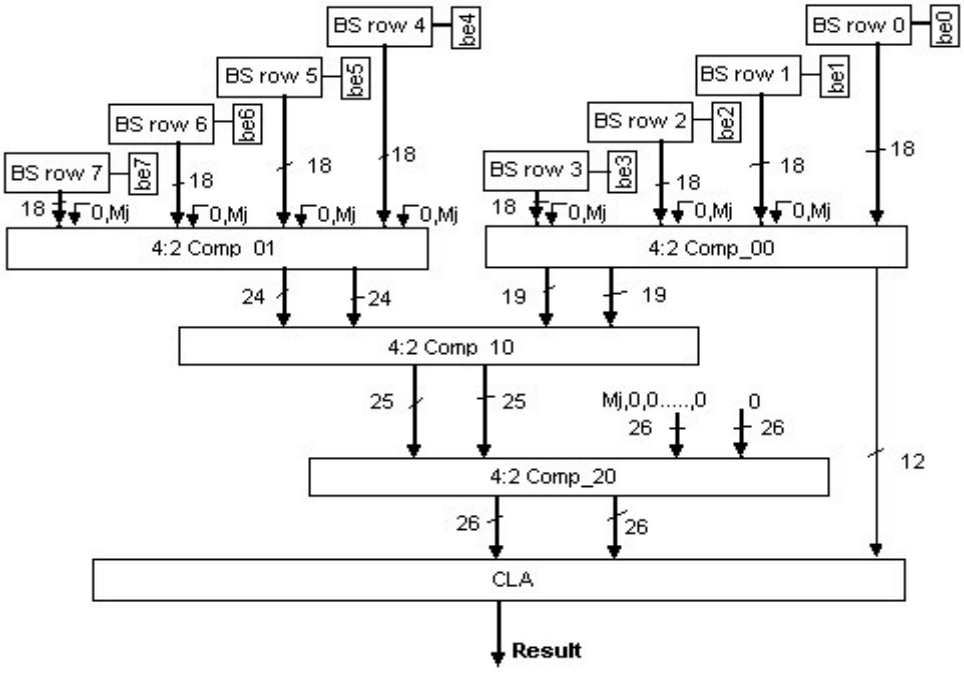

Fig. 5.5 A 16x16 multiplier based on WM42CLA architecture.

Table 5.5 Summary of worst-case delays of WM42CLA multipliers of different operand sizes in terms of T_{XOR}

Multiplier size	Delay in partial product generation	Delay in accumulation of partial product rows	Delay in final addition	Delay in multiplication
8x8	2.11	6	10.575	18.685
16x16	2.11	9	13.025	24.135
32x32	2.11	12	15.475	29.585
54x54	2.11	12	17.925	32.035
64x64	2.11	15	17.925	35.035

5.6 Wallace tree multiplier using 4:2 compressors with CLEBC (WM42CLEBC)

In this architecture the final adder stage of the WM42CLA architecture is replaced by a CLEBC adder and this architecture is referred to as the WM42CLEBC. In this architecture partial product generation and accumulation of partial product rows are done in the same way as in the WM42CLA. A CLEBC is used as shown in Fig 5.6 for performing the addition of the accumulated sum and carry rows. Since the delay in this final adder stage is $7.42T_{xor}$, therefore the worst-case delay for a 16x16 WM42CLEBC multiplier is $18.53T_{xor}$. The worst-case delays for multipliers of different operand sizes using WM42CLEBC architecture are obtained by replacing the final adder delays of Table 5.5 with delays of the CLEBC adders of corresponding operand sizes and are summarized in Table 5.6.

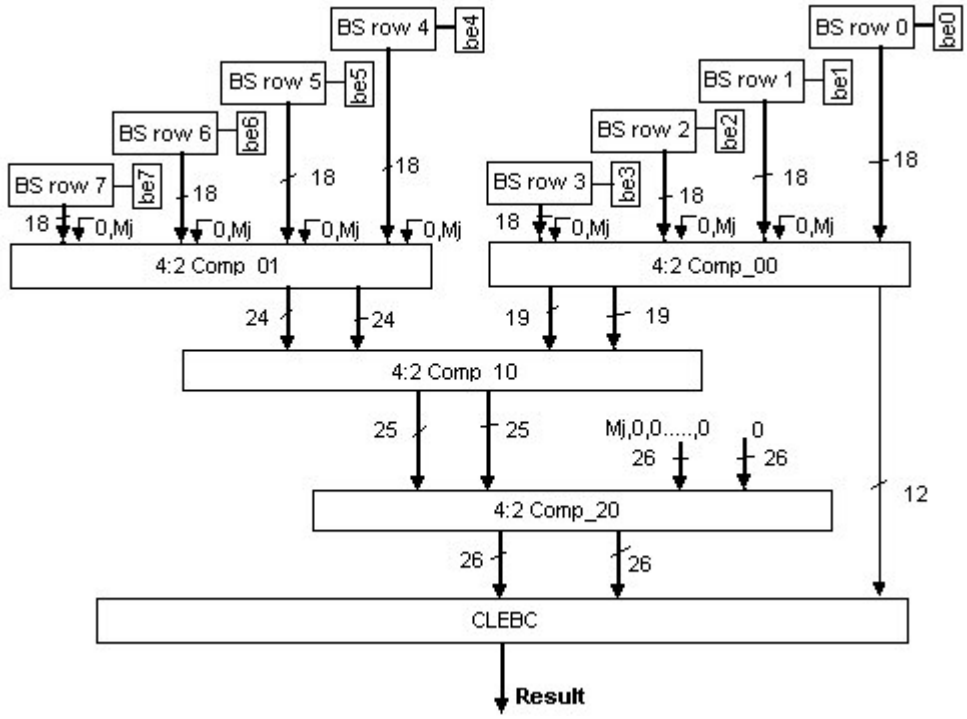

Fig. 5.6 A 16x16 multiplier based on WM42CLEBC architecture.

Table 5.6 Summary of worst-case delays of WM42CLEBC multipliers of different operand sizes in terms of T_{XOR}

Multiplier size	Delay in partial product generation	Delay in accumulation of partial product rows	Delay in final addition	Delay in multiplication
8x8	2.11	6	4.87	12.98
16x16	2.11	9	7.42	18.53
32x32	2.11	12	9.97	24.08
54x54	2.11	12	12.52	26.63
64x64	2.11	15	12.52	29.63

5.7 Wallace tree multiplier using RB adder with CLA (WMRBCLA)

This architecture uses RB adder in the accumulation tree and a CLA in the final adder stage. This architecture is referred to as the WMRBCLA. A 16x16 multiplier based on WMRBCLA architecture is shown in Fig. 5.7. In this architecture partial products are obtained in the same way as in the previous architectures using "be" and "BS row" combinations. These partial product rows are in the NB form. The first two partial product rows are combined to give a RB partial product row PPRB0 using the equation 1.1(i.e. A + B= (A, $\overline{B}$) - 1). So all the bits in the second partial product row are inverted. Adding a control digit row at the end takes care of the subtraction of 1. Similarly the combination of the third and the inverted of fourth partial product rows gives the PPRB1. In the same way PPRB2 and PPRB3 are obtained. The worst-case delay in RB partial product generation is the summation of NB partial product generation delay and inverter delay and is equal to $2.3T_{xor} + 0.88T_{xor} = 3.18T_{xor}$.

The first two RB partial product rows PPRB0 and PPRB1 are added using "RBAA row 00". Similarly the PPRB2 and PPRB3 are added using "RBAA row01" in the same level. The outputs of "RBAA row 00" and "RBAA row 01" are added by "RBAL row 10" consisting of RBAL adders at the next level. Finally a combination of Mj and control bits in

RB form are added to give the result in RB form. The worst case delay in this accumulation stage as obtained in chapter 3 is 7.09 T_{XOR}. The LSB input to the "RBAA row 00" is $P_{0,0}$ (LSB bit of first partial product row) and the MSB input is 1, which is the MSB bit of fourth partial product row. So the "RBAA row 00" consists of 25 RBAA adders. Similarly the number of adders required to be present in each adder row are determined.

The obtained multiplication result is in the RB form. This needs to be converted to NB form using a CLA with input carry as 1. The delay in this stage of RB to NB conversion is 13.02T_{xor}. So the worst-case delay in this 16x16 multiplier is 26.695T_{xor}.

This same methodology is used for designing multipliers of different operand sizes and computing their worst-case delays in terms T_{xor} and results obtained are summarized in Table 5.7.

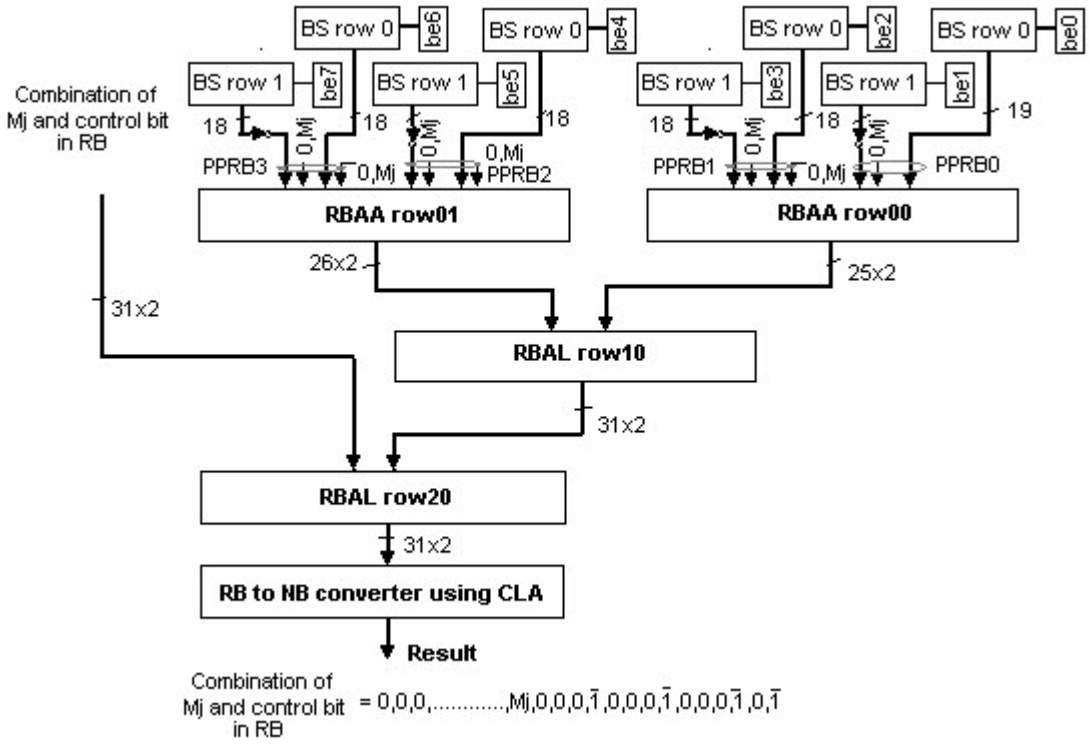

Fig. 5.7 A 16x16 multiplier based on WMRBCLA architecture.

Table 5.7 Summary of worst-case delays of WMRBCLA multipliers of different operand sizes in terms of T_{XOR}

Multiplier size	Delay in partial product generation	Delay in accumulation of partial product rows	Delay in final addition	Delay in multiplication
8x8	3.18	7.09	10.575	20.845
16x16	3.18	10.49	13.025	26.695
32x32	3.18	13.87	15.475	32.525
54x54	3.18	13.87	17.925	34.975
64x64	3.18	17.26	17.925	38.365

5.8 Wallace tree multiplier using RB adder with CLEBC (WMRBCLEBC)

In this architecture the RB to NB conversion stage of the WMRBCLA architecture is replaced by a CLEBC adder and the architecture is referred to as WMRBCLEBC. In this architecture the partial product generation and accumulation of partial product rows are done in the same way as in the WMRBCLA. A CLEBC as shown in Fig 5.8 does the RB to NB conversion. Since the delay in this RB to NB conversion stage is $7.42T_{xor}$ therefore the worst-case delay for a 16x16 WMRBCLEBC becomes $21.09T_{xor}$. The worst-case delay for multipliers of different operand sizes using WMRBCLEBC architecture are obtained by replacing the RB to NB conversion delays of Table 5.7 by the delays of CLEBC of corresponding operand sizes and are summarized in Table 5.8.

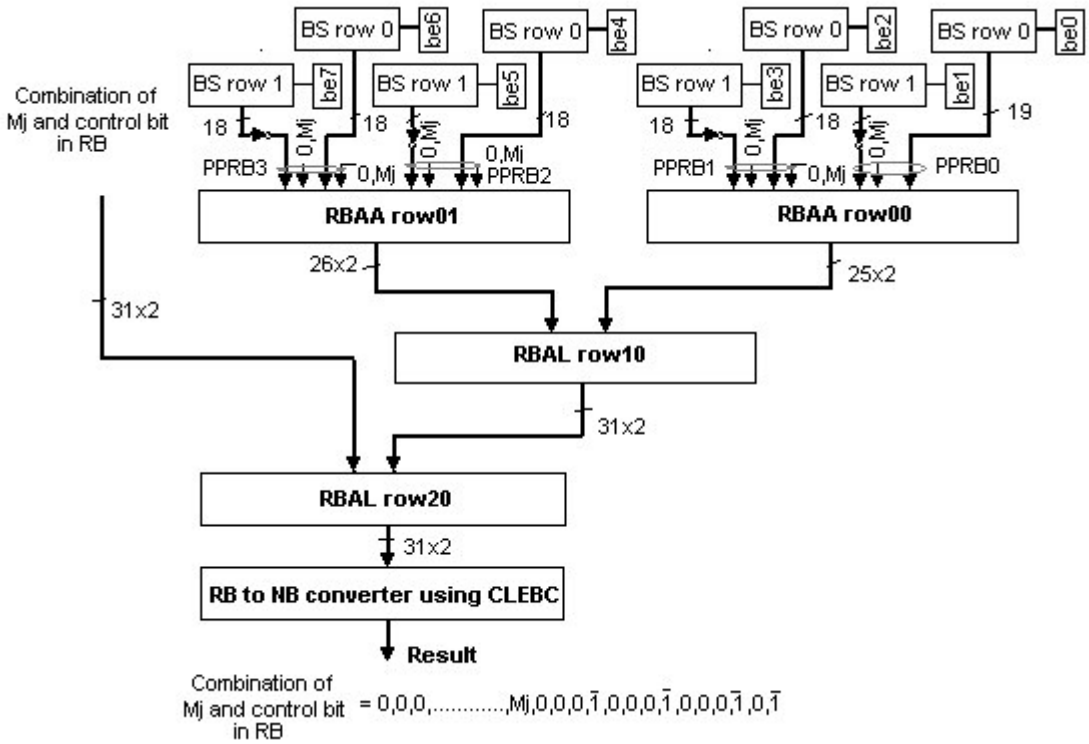

Fig. 5.8 A 16x16 multiplier based on WMRBCLEBC architecture.

Table 5.8 Summary of worst-case delays of WMRBCLEBC multipliers of different operand sizes in terms of T_{XOR}

Multiplier size	Delay in partial product generation	Delay in accumulation of partial product rows	Delay in final addition	Delay in multiplication
8x8	3.18	7.09	4.87	15.14
16x16	3.18	10.49	7.42	21.09
32x32	3.18	13.87	9.97	27.02
54x54	3.18	13.87	12.52	29.57
64x64	3.18	17.26	12.52	32.96

5.9 Radix 64 multiplier with CLA (Radix64CLA)

In previous architectures the numbers of partial product rows are reduced to half by using radix-4 Booth encoding. The present architecture named as Radix64CLA uses radix-64 Booth encoding, which reduces the number of partial products by a factor of 6. The generation of partial products using radix-64 encoding as discussed in detail in chapter 2 uses radix-64 encoder and selector circuits to give the partial products in the form of two RB numbers. A 16x16 multiplier using Radix64CLA architecture is shown in Fig. 5.9. First 6 bits of the multiplier padded with a 0 after the LSB are applied as inputs to "Radix-64 encoder 0". Its outputs are given to the partial product generator block. The partial product generator block consists of a row of selector circuits and a RBAA adder row. Input X (X, 0) and 3X (4X, X) are given as input in RB form to the selector, where X is the multiplicand. The selector selects two RB digits using the control signals obtained from "Radxi-64 encoder 0". These two RB digits are added using RBAA to give the partial product row. In the same way other two partial product rows are generated. So the worst-case delay for partial product generation using this scheme is the summation of delays for partial product generation in terms of two fundamental coefficients and their addition by RBAA adder and is equal to $6.6T_{xor}$.

The accumulation of the three generated partial product rows is shown in Fig. 5.9. The first and second partial product rows are added using RBAL row. The output of this RBAL row is added with the third partial product row to give the final multiplication result in RB form. Thus the accumulation delay is only due to two levels of RBAL adder and is equal to $6.78T_{xor}$.

The multiplication result obtained is in RB form. This is converted to NB form using a CLA with input carry equal to 1. The delay in this stage of RB to NB conversion is $13.02T_{xor}$. Thus the worst-case delay in the 16x16 Radix64CLA multiplier is $26.425T_{xor}$.

This same methodology is used for designing multipliers of different operand sizes and computing their worst-case delays in terms of T_{xor} and the results obtained are summarized in Table 5.9.

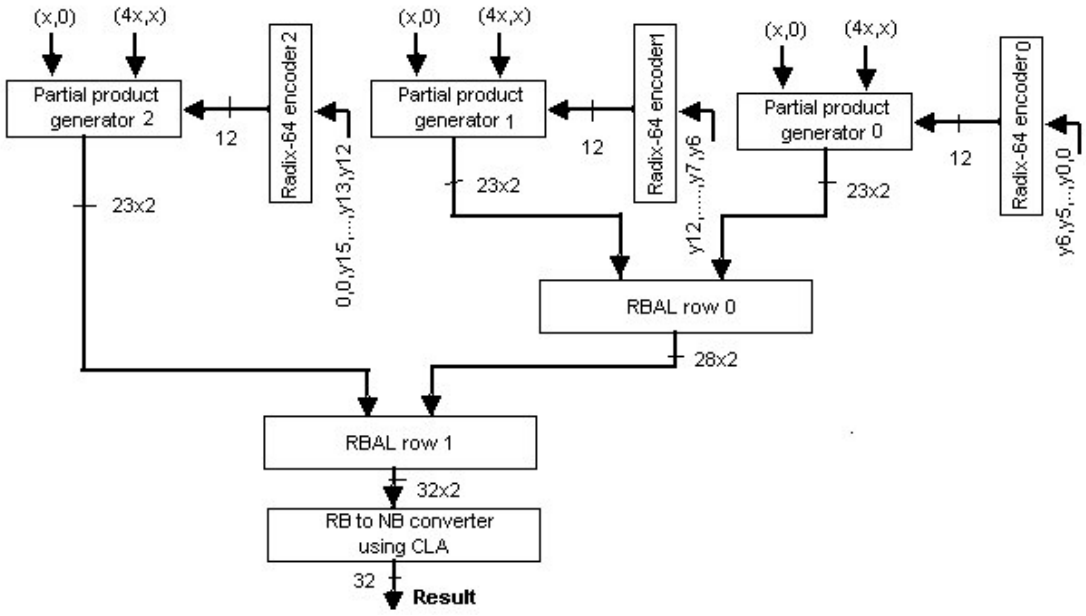

Fig. 5.9 A 16x16 multiplier based on Radix64CLA architecture.

Table 5.9 Summary of worst-case delays of Radix64CLA multipliers of different operand sizes in terms of T_{XOR}

Multiplier size	Delay in partial product generation	Delay in accumulation of partial product rows	Delay in final addition	Delay in multiplication
8x8	6.62	3.39	10.575	20.585
16x16	6.62	6.78	13.025	26.425
32x32	6.62	10.17	15.475	32.265
54x54	6.62	13.56	17.925	38.105
64x64	6.62	13.56	17.925	38.105

5.10 Radix 64 multiplier with CLEBC (Radix64CLEBC)

In this architecture the RB to NB conversion stage of the Radix64CLA architecture is replaced by a CLEBC and the architecture is referred to as the Radix64CLEBC. In this architecture the partial product generation and accumulation of partial product rows are done in the same way as in the Radix64CLA. A CLEBC as shown in Fig 5.10 is used to perform RB to NB conversion. Since the delay in this RB to NB conversion stage is $7.42T_{xor}$ the worst-case delay for a 16x16 Radix64CLEBC multiplier is $20.82T_{xor}$. The worst-case delay for multipliers of different operand sizes using Radix64CLEBC architecture are obtained by replacing the RB to NB conversion delays of Table 5.9 by delays of CLEBC of corresponding operand sizes and are summarized in Table 5.10.

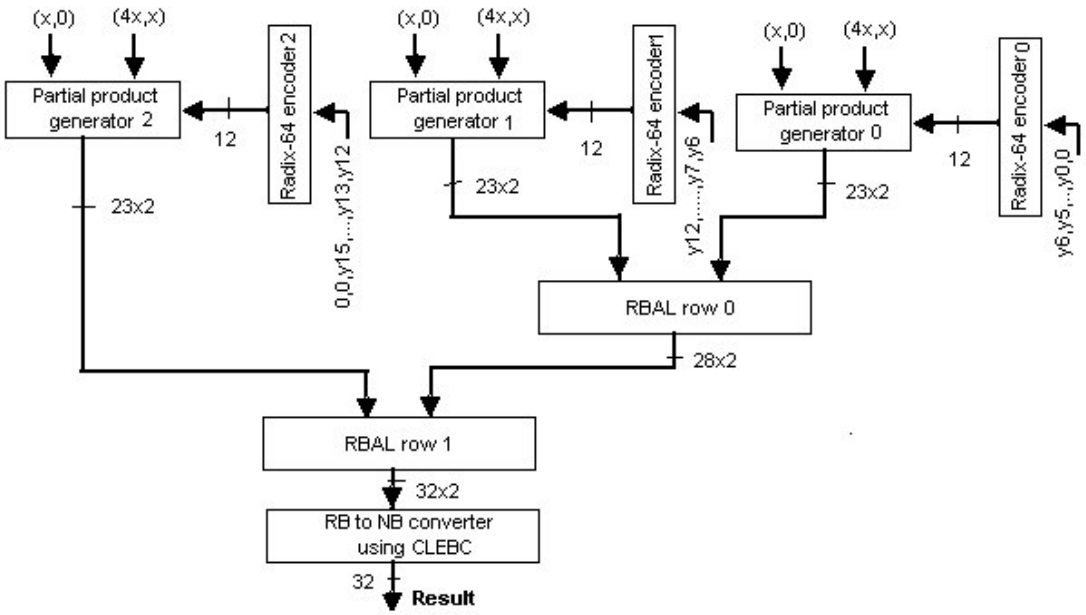

Fig. 5.10 A 16x16 multiplier based on Radix64CLEBC architecture

Table 5.10 Summary of worst-case delays of Radix64CLEBC multipliers of different operand sizes in terms of T_{XOR}

Multiplier size	Delay in partial product generation	Delay in accumulation of partial product rows	Delay in final addition	Delay in multiplication
8x8	6.62	3.39	4.87	14.88
16x16	6.62	6.78	7.42	20.82
32x32	6.62	10.17	9.97	26.76
54x54	6.62	13.56	12.52	32.7
64x64	6.62	13.56	12.52	32.7