Appendix A

Table A.1 Worst case delay, area, cell count and leakage power values for different operand sized multipliers implemented using AMCLA

Multiplier size	Multiplication delay in pico sec.	Area in mm^2	Cell count	Power in Micro watt
8x8	2659	0.015	770	149.4
16x16	4495	0.029	1453	302.2
32x32	8197	0.109	4353	977.5
54x54	13205	0.301	9947	2600
64x64	15198	0.423	12440	3700

Table A.2 Worst case delay, area, cell count and leakage power values for different operand sized multipliers implemented using AMCLEBC

Multiplier size	Multiplication delay in pico sec.	Area in mm^2	Cell count	Power in Micro watt
8x8	2570	0.018	833	209.9
16x16	4408	0.031	1461	327.4
32x32	6648	0.113	3749	775.1
54x54	12893	0.311	9978	2700
64x64	15249	0.430	14212	3800

Table A.3 Worst case delay, area, cell count and leakage power values for different operand sized multipliers implemented using WM32CLA

Multiplier size	Multiplication delay in pico sec.	Area in mm^2	Cell count	Power in Micro watt
8x8	2835	0.009	558	105.0
16x16	4974	0.034	2168	548.7
32x32	5392	0.134	4478	1100
54x54	6278	0.381	10583	3200
64x64	7095	0.534	14641	4500

Table A.4 Worst case delay, area, cell count and leakage power values for different operand sized multipliers implemented using WM32CLEBC

Multiplier size	Multiplication delay in pico sec.	Area in mm^2	Cell count	Power in Micro watt
8x8	2656	0.009	538	123.5
16x16	3788	0.036	1572	365.2
32x32	5214	0.136	4284	1100
54x54	6581	0.385	10122	3200
64x64	6992	0.539	13911	4500

Table A.5 Worst case delay, area, cell count and leakage power values for different operand sized multipliers implemented using WM42CLA

Multiplier size	Multiplication delay in pico sec.	Area in mm^2	Cell count	Power in Micro watt
8x8	2593	0.008	580	112.4
16x16	3758	0.033	1805	365.4
32x32	5144	0.131	4692	1100
54x54	6594	0.388	11040	3000
64x64	6817	0.534	15567	4400

Table A.6 Worst case delay, area, cell count and leakage power values for different operand sized multipliers implemented using WM42CLEBC

Multiplier size	Multiplication delay in pico sec.	Area in mm^2	Cell count	Power in Micro watt
8x8	2312	0.012	686	150.1
16x16	3693	0.035	1368	299
32x32	5114	0.134	4360	1100
54x54	6579	0.392	10555	3000
64x64	6842	0.538	14644	4300

TableA.7 Worst case delay, area, cell count and leakage power values for different operand sized multipliers implemented using WMRBCLA

Multiplier size	Multiplication delay in pico sec.	Area in mm^2	Cell count	Power in Micro watt
8x8	3376	0.014	771	174.2
16x16	5230	0.056	3004	798.7
32x32	6659	0.245	8953	2400
54x54	7916	0.714	20768	6500
64x64	8636	1.072	30318	9500

Table A. 8 Worst case delay, area, cell count and leakage power values for different operand sized multipliers implemented using WMRBCLEBC

Multiplier size	Multiplication delay in pico sec.	Area in mm^2	Cell count	Power in Micro watt
8x8	3367	0.064	931	221.2
16x16	4786	0.059	2877	720.2
32x32	6731	0.251	8482	2400
54x54	7823	0.724	20993	6500
64x64	8690	1.072	30496	9400

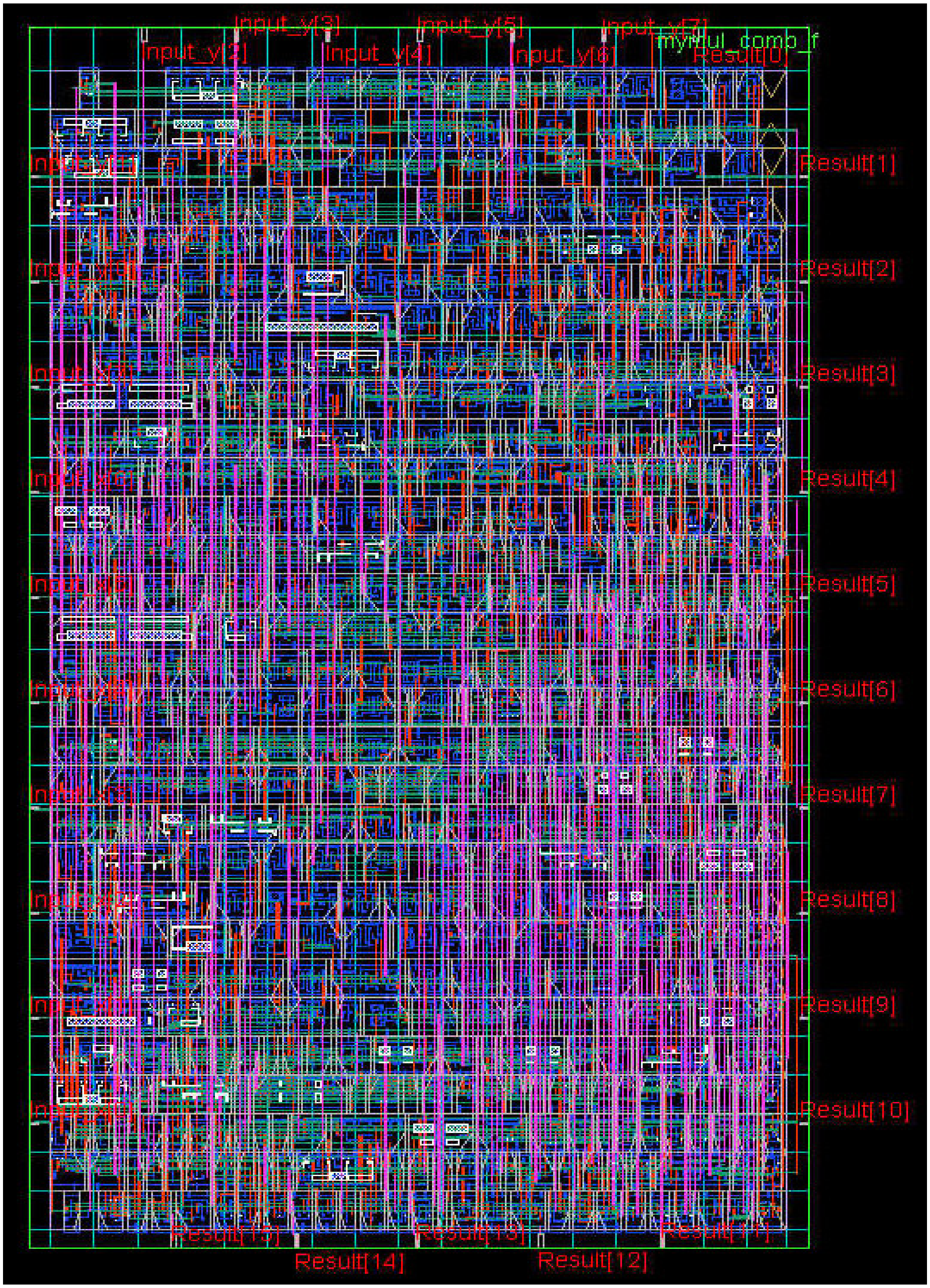
Table A. 9 Worst case delay, area, cell count and leakage power values for different operand sized multipliers implemented using Radix64CLA

Multiplier size	Multiplication delay in pico sec.	Area in mm^2	Cell count	Power in Micro watt
8x8	3446	0.040	1541	340.3
16x16	4973	0.083	3634	844.2
32x32	6601	0.348	11099	2800
54x54	8156	0.942	28568	7900
64x64	8509	1.356	39339	11100

Table A.10 Worst case delay, area, cell count and leakage power values for different operand sized multipliers implemented using Radix64CLEBC

Multiplier size	Multiplication delay in pico sec.	Area in mm^2	Cell count	Power in Micro watt
8x8	3558	0.036	1204	263.1
16x16	4817	0.083	3677	873.7
32x32	6585	0.351	10918	2900
54x54	8023	0.948	27820	7600
64x64	8443	1.363	38325	10700

Appendix B



Snapshot view of an 8x8 multiplier core layout based on WM42CLA architecture.

Method of Power Estimation

To estimate the power consumption, a default toggle rate of 10MHz is specified by using the command "config activity default $10e^6$ ". This assigns all the pins a default toggle rate of 10MHz. This toggle rate is applied to all architectures and for all operand sizes of multipliers. This switching activity is used for average current calculation. After defining the switching activity, the leakage power, switched-capacitance power dissipation and the dynamic power dissipation are estimated by using the command "report power analysis". *Leakage* power is the power dissipation through leakage current, when the signal is stable. S*wcap* is the power dissipated to charge and discharge any capacitance of input load and wire. The *internal* power dissipation is because of the short circuit current that flows through the PMOS and NMOS parts, when both are conducting. So as the switching activity changes the internal and swcap power dissipation also changes.

A typical power analysis report for different toggle rate for a 32x32 WM42CLA is given in Fig. A.1 below. Here initially a toggle rate of 5MHz is defined and the power analysis report is obtained. Then the switching activity is doubled and the power analysis report is obtained. It indicates that the internal and swcap power increases approximately by two fold as the toggle rate doubles.

Fig. A.1 Power analysis report of a 32x32 multiplier for toggle rate of 5MHz and 10MHz.

```
mantle[6]:>config activity default 5e6
mantle[7]:>report power analysis $m
######################################################################

cell   model            leakage    internal   swcap      total
----   --------------   ---------  ---------  ---------  ---------
      (H) mymul_comp    80.6 uW   291.0 uW   221.3 uW   592.9 uW
######################################################################
mantle[8]:>config activity default 10e6
mantle[9]:>report power analysis $m

######################################################################

cell   model            leakage    internal   swcap      total
----   --------------   ---------  ---------  ---------  ---------
      (H) mymul_comp    80.6 uW   582.0 uW   442.6 uW     1.1 mW
######################################################################
```

Brief- Biography of Dr. Chandra Shekhar

Dr. Chandra Shekhar is presently the Director of CEERI, Pilani. He completed his Ph. D. from BITS, Pilani in 1975 and joined as Research Fellow and then Scientist `B' in Solid State Devices Division, CEERI, Pilani in 1977. He was responsible for IC Design related activities at CEERI, Pilani since 1982 till he took charge as Director, CEERI in Novemeber, 2003.

He was awarded UNDP fellowship for study and training in the area of Computer Aided Design at EFCIS, Grenoble, France in 1980. Dr. Chandra Shekhar received the UNESCO/ROSTSCA Young Scientist Award in 1986 for his contributions in the area of Informatics and Applications of Computers in Scientific Research. He was the project leader of the DoE sponsored project "VLSI Design Center for Industrial ASICs" at CEERI, Pilani from 1987 to 1993. He lead the DoE sponsored project "Design of a 68010-compatible Microprocessor for Telecommunication Applications" at CEERI, Pilani from 1993 to 1997. Under this project, a synthesizable resistor transfer level VHDL description cycle-compatible with MC 68010 microprocessor was developed for M/s C-DOT. This was the first mainstream microprocessor design project within the country. This project also was the first instance of usage of VHDL based design methodology within the country.

He was the project coordinator of the DIT/MIT/DOE sponsored multi-institutional project "Special Manpower Development for VLSI Design and Related Software" at CEERI, Pilani from 1998 till 2003. This project aimed at developing learning material, laboratory material, design case studies and faculty training of 12 participating institutes (RECs/Universities).

He was also the project leader of the DIT/MCIT sponsored project "Application Specific Processor Based Speech Synthesis Technology Development for Hindi Language" at CEERI, Pilani and Delhi from 2001 to 2003. This project successfully designed and developed an Application Specific Instruction Set Processor (ASIP) chip to provide a platform for developing portable/handheld devices for converting Hindi text to speech using the *formant based parametric speech synthesis* approach.

He acted as the coordinator for formulating, planning and initiating the ME (Microelectronics) degree programme jointly with BITS, Pilani in 1989. This was the first program of its kind within the country, and was then emulated by several other institutes.

His areas of research interest include VLSI Design and Design Methodologies, Analog IC Design and Mixed Signal Design, Processors and Application Specific Processors (Architecture and Design), CAD for VLSI, Physics and Modeling of MOS Devices and VLSI Systems' Applications.

Dr. Chandra Shekhar has over 60 research papers (contributed and invited) in various reputed international/national journals and conferences. He also has conducted two tutorials in the VLSI design conferences. He has supervised 4 Ph. D. theses and over 110 M.E./M.Tech theses in the area of Microelectronics/VLSI Design.

Brief-Biography of S. K. Sahoo

S. K. Sahoo completed his B.E. in Electronics and telecommunication engineering from Orissa Engineering College, under Utakal University in the year 1994 with honors securing fifth position in the university. He obtained his M.E. degree in Electronic Systems and Communication from R.E.C. Rourkela in 1998. He joined the Birla Institute of Technology and Science, Pilani, in June 1999. For the last 7 years, he has been working as a faculty member of the Electrical and Electronics group. He has published six research papers in National and International Conferences. His areas of research are high performance arithmetic circuits and VLSI circuits for communication applications.

List of Publications

[1] Subhendu Kumar Sahoo, Chandra Shekhar, "Application Specific Parallel Multiplier Design: An Exploration," *IETE Golden Jubilee Seminar on Electronics Design Automation : Issues & Challenges* , Jaipur, India, 2003.

[2] Subhendu Kumar Sahoo, Anu Gupta, Chandra Shekhar, "A Compact Fast Parallel Multiplier Using Modified Equivalent Binary Conversion Algorithm," *VLSI Design and Test 2004*, Mysore, India, pp 53-64.

[3] Prasanthi. R , Anuradha. V, S.K.Sahoo, Chandra Shekhar, "Multiplier Less FFT Processor Architecture For Signal And Image Processing, " *Proceeding of Second International Conference on Intelligent Sensing and Information Processing- ICISP 05*, Chennai, India, pp. 326 –330.

[4] Subhendu Kumar Sahoo, Chandra Shekhar , "Novel High-Speed Serial Parallel Multiplier For Moderate Speed Digital Signal Processing," *Asia and South Pacific International Conference on Embedded SoCs (ASPICES) , 2005,* IISC, Bangalore, India, pp. 26.

[5] Subhendu Kumar Sahoo, Chandra Shekhar, "Design And Analysis Of A Compact Fast Parallel Multiplier For High speed DSP Applications Using Novel Partial Product Generator And 4:2 Compressor," *13th International Conference on Advanced Computing and Communication,2005,* Coimbatore, India.