Effect of Silicon Surface States on MOS Devices and Studies on Schottky Barrier Solar Cells

Thesis

Submitted in partial fulfilment of the requirements for the degree of

Doctor of Philosophy

in

Physics

by

(Mrs.) SWARAJ SRIVASTAVA

Birla Institute of Technology and Science

Dilani (Rajasthan)

DECEMBER, 1978

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE

PILANI, RAJASTHAN

C E R T I F I C A T E

This is to certify that the thesis entitled 'EFFECT OF SILICON SURFACE STATES ON MOS DEVICES AND STUDIES ON SCHOTTKY BARRIER SOLAR CELLS' and submitted by Mrs. Swaraj Srivastava, ID No. 71/Ph D/ Phy/3 for award of Ph.D. degree of the Institute, embodies original work done by her under my supervision.

Signature in full of the Supervisor	G. P. Srivastava ....
Name in capital block letters	GAURAVA PRADEEP SRIVASTAVA
Designation	Lecturer in Physics Educational Development Division.

Date: 7th Dec., 1978.

PREFACE

The semiconductor devices have generated a tremendous amount of interest among physicists and technologists, mainly because of their miniaturized size and low power. The progress towards understanding the basic properties of solid materials has stimulated a parallel progress in the development and use of these solid state electronic devices. These devices, however, were found to be very sensitive to surface effects. This led to the investigations of the semiconductor surfaces.

An important class of semiconductor devices consists of metal-oxide-semiconductor (MOS) devices. The main causes of instability in MOS devices have been found to be mobile alkali ions in the oxide layer and the interface states present at the silicon-silicon dioxide ($Si-SiO_2$) interface. Moreover, the characteristics of these devices are found to change on irradiation. This makes them useless for space applications. It has, therefore, been considered worthwhile to investigate these phenomena; and such an experimental study forms a part of the present work. The other part of the work is a theoretical study on MOS solar cells. Solar cells are the devices which convert solar energy directly to electrical energy. The need to harness solar energy has accelerated the researches on solar cells.

The conventional p-n junction solar cells have not become very common due to their high fabrication costs. The MOS solar cells, commonly known as Schottky barrier solar cells (SBSC), are found to give good efficiencies and are easier and cheaper to fabricate. In the present work on SBSC, influences of various factors on the conversion efficiency of these cells have been studied theoretically in an attempt to find conditions for the maximum efficiency.

The first chapter of the thesis deals with the surface states, which are the most important factor in the study of surface properties of semiconductors. The origin and theory of surface states and the theory behind some important experimental methods used for their determination, have been explained briefly. The second chapter presents a detailed analysis of the $Si-SiO_2$ system, considering the effect of surface states. The capacitance of MOS devices under applied bias conditions and the charges in the space charge region for low and high ac signal frequencies, have been explained in detail. In addition, a survey of the earlier work done on interface state density, oxide charge and radiation effects, has also been made.

It is known that the oxidation of silicon in the presence of chlorine improves the properties of $Si-SiO_2$ interface.

In the present study, trichloroethylene (TCE) was used as a chlorine source and the effects of its concentration, during oxidation, on the oxide charge density, interface states, and sodium ion neutralization, have been studied. These results are given in the third chapter. It is observed that the interface state density reduced for 0.3 to 0.4 per cent TCE concentration. Also, the sodium ions are found to be completely neutralized for 0.9 per cent TCE concentration.

The results of the radiation (x-rays) effect on the MOS devices are presented in the fourth chapter. The formation of radiation induced charge is found to be strongly dependant on the growth condition of SiO_2 layer, the gate metal and the exposure time for and the gate bias applied during the irradiation.

The last two chapters of the thesis are devoted to a theoretical study of MOS solar cells or Schottky barrier solar cells (SBSC). In the fifth chapter p-n junction solar cells have been compared with these cells and the theory of SBSC has been given, alongwith a brief review of the earlier work done on them. The results of the present calculations done to study the effects of various factors, namely, oxide layer thickness, interface state density, metal work function and donor density, on the conversion efficiency of this

device, have been presented in the sixth chapter. The transmission coefficient for the tunneling of electrons across the interfacial layer, which has a strong dependence on the thickness of the interfacial layer, has properly been taken into account. This transmission coefficient had been taken to be unity in the earlier works of other authors, which was not realistic. The present results show that the oxide layer thickness and the donor density need be optimized for the maximum efficiency of the Schottky barrier solar cells.

S Srivastava

(Mrs. Swaraj Srivastava)

Physics Group,
Birla Institute of Technology and Science,
PILANI-333031.

December, 1978.

ACKNOWLEDGEMENTS

I am extremely grateful to Dr. G. P. Srivastava, Lecturer in Physics, Birla Institute of Technology and Science , Pilani under whose able guidance the present work has been done. He has given me constant guidance and encouragement, for which I will always be indebted to him.

I owe my sincere and heartfelt thanks to Dr.H.M.Ghule and Dr. B. R. Singh for their keen interest and all possible help during the course of this work.

My special thanks are due to Sri R.C. Dubey, Sri U.C. Sharma, Sri N.K. Swami, Sri S.C. Bawa, Dr. A.K. Jain and Dr. S.K. Jain for their unforgetable help. Cordial thanks are also due to Dr. Chandra Shekhar, Dr. N.K. Joshi and Dr. A. K. Pandey.

I take this opportunity to thank Prof. S.Y. Tiwari, Dr. R.S. Srivastava, Dr. W.S. Khokle, Dr. B. R. Marathe, Dr. S.K. Sharma, Prof. T.N.R.K. Kurup, Dr. P.R. Marwari and Dr. P.K. Raman for various kinds of help and discussions.

I wish to express my deep appreciation to Dr. and Smt. Ved Parkash, Sri and Smt. S.C. Srivastava and their families for their affectionate encouragement and personal help.

My thanks are due to Sri Banwari Lal, Sri S.L.Sharma, Sri Ashok Tewathia and Sri B.P. Singh for helping during my computational work. I also thank Sri S.K. Sinha for efficient typing of the manuscript and Sri B.D. Sukheja for the drawing work.

I am thankful to the Director, B.I.T.S., Dean, Research and Consultancy Division, Chief, I.P.C. and Dean, Faculty Division III, for providing necessary facilities during the course of this work. The author is also thankful to University Grants Commission for financial assistance.

S. Srivastava

(Mrs. Swaraj Srivastava)

C O N T E N T S

		Page
Certificate		i
Preface		ii
Acknowledgements		vi
Chapter		
I	Surface States	1
II	MOS Devices	24
III	Surface Properties of Silicon-TCE Oxide System	58
IV	Effect of Radiation on MOS Divices	73
V	Schottky Barrier Solar Cell	87
VI	Efficiency Calculations on Schottky Barrier Solar Cell	117
Appendix		
A	Determination of Charges in the Surface States	143
B	Determination of Recombination Currents	147

Chapter-I

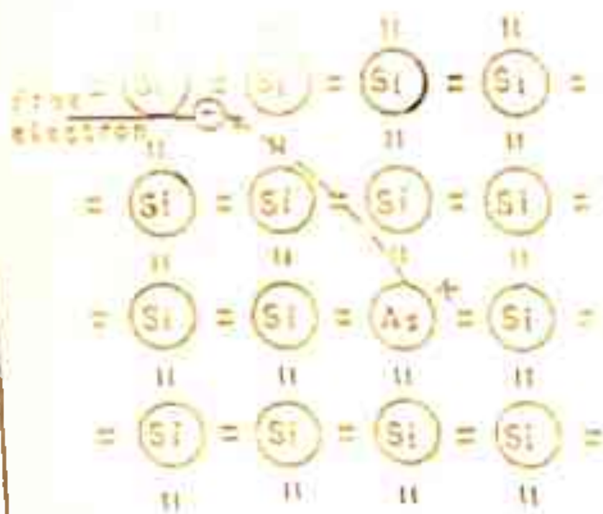
SURFACE STATES

The semiconductor surface has been studied very thoroughly since the observation had been made that various surface phenomena have detrimental effects on the properties and the stability of p-n junction devices. It was first reported by Atalla and his coworkers[1] in 1959 that thermally grown silicon dioxide films can have a stabilizing action on the surface properties of silicon. These silicon dioxide films also separated the metal electrode from the semiconductor and this gave rise to the metal-oxide-semiconductor (MOS) devices. The properties of these MOS devices were found to be dependent on the surface properties of semiconductors, which include the orientation of the crystal and density of surface states. Also, these surface properties showed changes, when the devices were subjected to ionizing radiations. The ionizing radiations were found to cause an increase in the surface state density, which in turn decreases the transconductance of the device, causes a change in the threshold voltage and shift in the capacitance-voltage characteristics of the device along the voltage axis. In the case of Schottky barrier solar cells, the surface states are found to act as charge transfer centres and the efficiency of the device is found to depend strongly on the density of

surface states. The barrier height at the surface of the semiconductor is also found to depend on the density of surface states.

1.1 Semiconductors

It is well known that the electrical conduction in solids can take place only when the allowed energy bands are partially filled. A crystal behaves as an insulator if the bands are either filled or empty and are separated by a wide energy gap. The conductors are characterized by one or more partly filled bands. Semiconductors have electrical resistivities in the range 10^{-2} to 10^{9} ohm cm at room temperature, which is intermediate between good conductors' ($\sim 10^{-6}$ ohm cm) and insulators' (10^{14} to 10^{22} ohm cm) resistivities. In semiconductors, the conduction and valence bands are separated by a forbidden energy gap, which is not as wide as in the case of insulators. At absolute zero temperature, the conduction band in semiconductors is empty and the valence band is full, but at room temperature some of the electrons gain sufficient thermal energy to go to the conduction band leaving behind holes in the valence band. These electrons and holes are then in a position to conduct electricity. Such semiconductors, in which equal number of electrons and holes take part in



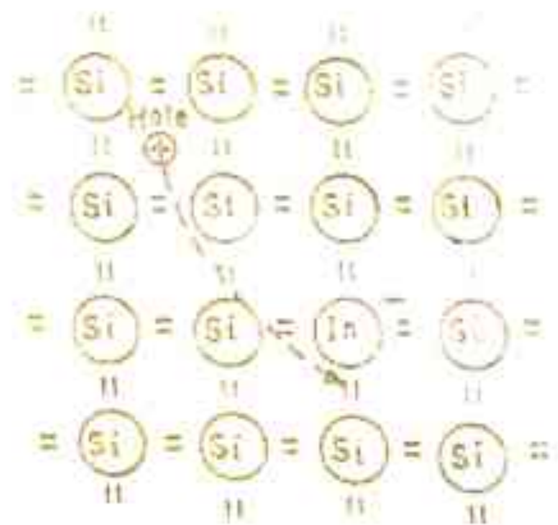


FIG. 1.1 (a) FREE ELECTRON ARISING FROM IONIZATION OF A SUBSTITUTIONAL ARSENIC IMPURITY ATOM.

(b) FREE HOLE ARISING FROM IONIZATION OF A SUBSTITUTIONAL INDIUM IMPURITY ATOM.

conduction, are known as the 'intrinsic semiconductors'. The most common examples of the intrinsic semiconductors are silicon and germanium.

If an impurity atom of a fifth group element (say, arsenic) is added to silicon, it would normally occupy a lattice site. Four of the five valence electrons of this impurity atom are used in the formation of four covalent bonds with the neighbouring semiconductor atoms and the fifth electron remains bound to this atom by the electrostatic forces, as shown in Fig. 1.1a. This atom can, therefore, be easily ionized at room temperature and provides an extra electron for conduction. The crystals containing this type of impurities are known as 'n-type semiconductors', because there are more negative charge carriers (electrons) than holes. These impurity atoms are called 'donor atoms'.

If, instead of fifth group atoms, third group atoms (say, indium) are introduced as impurity into a silicon crystal, a different situation is created. Such an atom, having only three valence electrons, needs an additional electron to form the four covalent bonds with the neighbouring host atoms. Such an electron associated with the impurity atom, creates a hole in the neighbourhood, as shown in Fig. 1.1b. The energy required for the migration of the hole is of the

same order as the energy required to remove the extra electron from the donor atom in n-type semiconductor. Therefore, at room temperature the holes would be migratory. In crystals containing this type of impurity, the number of positive charge carriers (holes) is more than the number of negative ones and they are termed as 'p-type semiconductors'. The impurity atoms, in this case, are known as 'acceptor atoms'.

The semiconductors containing introduced impurity atoms are called 'extrinsic semiconductors'. The conductivity of materials being directly proportional to the concentration of charge carriers, the conductivity of extrinsic semiconductors is more than that of intrinsic semiconductors. Moreover, the Fermi level for n-type semiconductors is close to the conduction band edge and that for p-type semiconductor is close to the valence band edge, whereas in intrinsic semiconductor it lies in the middle of the band gap.

1.2 Bulk band structure

In an ideal crystal, the electrons may be thought of moving under the influence of an infinite array of ion cores. The potential energy of such an electron is a function of its position and the wave functions may be obtained, in the

one electron approximation, by solving the Schrodinger equation

$$\nabla^2 \psi(\vec{r}) + \frac{2m}{\hbar^2}(E - V(\vec{r}))\psi(\vec{r}) = 0 \qquad (1.1)$$

where $V(\vec{r})$ is the potential energy of the electron and has the periodicity of the lattice. The solutions of the above equation are the familiar Bloch functions

$$\psi_k(\vec{r}) = e^{i\vec{k}.\vec{r}} U_k(\vec{r}),$$

where the function $U_k(\vec{r})$ also has the periodicity of the lattice. One important consequence of the crystal being infinite is that the wave vector $\vec{k}$ of the Bloch states has to be real in order to have finite non zero wave function every where inside the crystal. This restricts the set of solutions to have very few physically meaningful ones and these give the allowed energy levels clustered in the valence and conduction bands separated by a forbidden energy gap.

1.3 Surface states

A crystal surface is created, when an infinite crystal is cut. In this case, instead of an infinitely periodic potential, one has a periodic potential terminated at the

surface. To solve the Schrodinger equation at a surface of discontinuity, one can determine the general solutions on both the sides and match them to have the wave function and its derivative continuous across the boundary. In this case, therefore, the solution would consist of two types of functions, one corresponding closely to the Bloch functions having the periodicity of the lattice throughout the crystal and the other being confined largely to the surface regions of the crystal. The second type of functions decay exponentially in the direction normal to the boundary plane. These are the solutions which are known as the 'surface states' and give rise to energy levels in the forbidden energy gap.

Various methods are used in solving the Schrodinger equation at a surface. Classification of these methods is usually made on the basis of the type of expansion function chosen for the wave function. Three methods are common : (i) 'Plane wave method' - This is the most simple one, wherein linear combinations of plane waves are taken and the coefficients are determined by imposing on them the required symmetry conditions. (ii) 'Cellular method' - In this method, the functions used are products of a radial and an angular factors. Here, the Bloch conditions enter as boundary conditions on the wave function within a unit cell. Such methods

FIG. 1.2 TAMM'S POTENTIAL MODEL FOR A ONE DIMENSIONAL LATTICE TERMINATED AT ONE END.

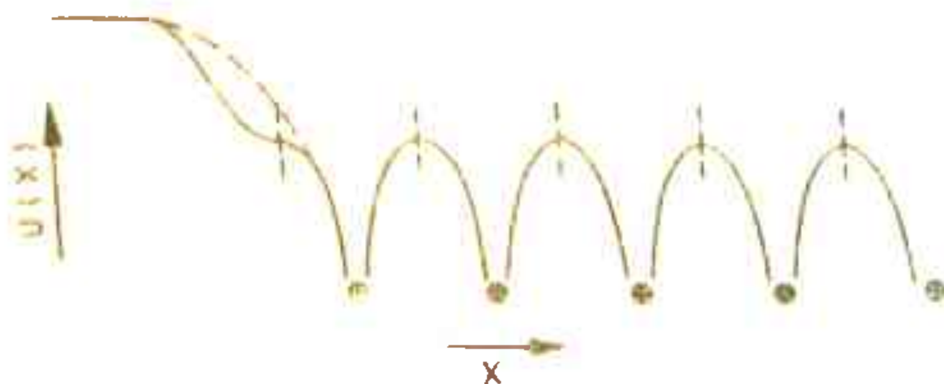


FIG. 1.3 SHOCKLEY'S POTENTIAL MODEL FOR A ONE DIMENSIONAL LATTICE SYMMETRICALLY TERMINATED. DASHED CURVE SHOWS ASYMMETRICAL TERMINATION (TAMM'S MODEL)

were first used by Weigner and Seitz[2] and Slater[3] in realistic band structure calculations. This plays an important role in the surface states calculations also and was used by Shockley[4].
(iii) 'Tight binding method' - In this method, the atomic wave functions are used as a zero order approximation. This has been used by Goodwin[5] for surface states calculations.

1.4 Historical review of the theory of surface states:

One of the earliest applications of quantum theory to periodic crystals was the Kronig-Penney model[6], introduced in 1931. According to this the periodic potential inside a crystal may be represented by square well potential. Tamm[7] was the first to introduce the concept of surface states in such an application. He considered the potential to be terminated at a free surface. The termination was taken as a step discontinuity and the wave functions and their derivatives were matched across the boundary. He inferred from his calculations that localized states appear at the surface. The model used by Tamm is shown in Fig. 1.2. This model gives discrete allowed energy levels in the forbidden energy gap. These are in addition to the allowed energy bands of the Kronig-Penney model. Tamm's work was later extended to more general cases in one and three dimensions. Maue[8] considered

the nearly free electron model of a crystal and expanded the crystal potential in a Fourier series. He also took a step discontinuity at the surface at maximum or minimum of the potential and obtained the conditions for surface states. In 1939, Goodwin[9] published a series of three papers. The first was a generalization of Maue's work and the other two developed approaches which were new at that time and were based on the linear combination of atomic orbitals (LCAO) method. During the same year, Shockley[4] also examined this problem by considering a more general one dimensional potential terminated at its maximum symmetrically by a step, as shown in Fig. 1.3. This is in contrast to the asymmetrical termination used by Tamm[7] (Fig. 1.2). Shockley found that no surface states are possible for large interatomic distances, in which case the energy bands correspond to discrete energy levels of isolated atoms. As the interatomic distance is decreased, the allowed energy levels broaden into energy bands and their edges approach each other. Beyond a particular value of the lattice constant , the boundary curves of the bands intersect. Shockley found that when bulk bands cross, the surface states appear as a result of the perturbation at the surface, which was considered to be small by him. It may be noted that the Tamm's perturbation was large. The energy states thus obtained by Shockley correspond to localized wave functions. According

to him, the negligible perturbation corresponds to the situation found in silicon and germanium crystals.

It has been of general interest in the field, to distinguish Tamm and Shockley type states. The states obtained when the periodic potential is symmetrically terminated at the surface and the atoms are close together, are indentified as Shockley states. The Tamm states arise due to asymmetrical termination of the periodic potential, the atomic separation being large.

The 'free electron model' has proved to be a successful tool for determining the surface band structure. Rijanow[10] and Maue[8] made use of this method and confirmed the possibility of existence of surface states in three dimensional crystals. Goodwin[9] obtained the explicit wave functions and energies for these states in terms of certain Fourier components of the lattice potential. He[9] also used the 'tight binding approximation' method and investigated the wave functions and the energies for both, one and three dimensions. It became apparent from these studies that surface state energies are found to lie in the band gap. Also, it was found that the number of surface states is one per atom.

Tomasek[11] also investigated these states using tight binding approach and retaining overlap integrals upto first

neighbours only, whereas Koutecky[12,13] considered the distortion in the two outermost layers. Pugh[14] calculated along the same lines and reported that the surface state band lies somewhat below mid gap. Grimley[15] showed that adsorption of the foreign atoms on the surface also gives rise to surface states. Levine and Mark[16] studied surface states on ionic crystals. Heine[17] used the complex wave vectors to solve the problem. Davison and Levine[18] reviewed the subject, taking both theoretical and experimental aspects into consideration.

Recently, the surface states have gained more importance and are being studied due to their technological applications in rectifiers, transistors, integrated circuits etc. Bardeen[19] explained the Meyerhof's anomolous results[20] on metal-semiconductor contacts, in terms of the surface states. Shockley and Pearson[21] tested the Bardeen's hypothesis. Using a field plate, they modulated the potential of a semiconductor free surface- the so called 'field effect' experiment. They showed that part of the surface states charge was mobile, but most of it was immobile when a secondary field was applied parallel to the surface. The immobile charge was ascribed to the charges trapped in surface states. Later, the surface states were classified into 'slow' and 'fast' states. The 'fast states ' are those which interact with the interior space

charge region very quickly, whereas the 'slow states' interact very slowly with the interior of the crystal. The fast states are usually regarded as residing at the surface of the semiconductor crystal, while the slow states are thought of being associated with the outside surface of a few Angstroms thick oxide layer ordinarily present on germanium or silicon surfaces. The slowness of these states is attributed to the difficulty that the electrons experience in penetrating the intervening insulating layer[23]. The surface states are also classified into 'donor' and 'acceptor' surface states. A 'donor state' is one which is neutral when occupied and becomes positive by donating an electron, whereas an 'acceptor state' is neutral when unoccupied and becomes negative by accepting an electron.

1.5 Surface recombination

When the density of electrons or holes is more than its value at thermal equilibrium conditions, the recombination of the excess charge carriers takes place, whether in bulk or at the surface. Experimental observations have shown that such recombination occurs through localized levels in the band gap. Shockley and Read[22] gave a theory for recombination in bulk and Braittain and Bardeen[23] extended it to the surface.

The single level recombination is one, in which only one trapping centre is present in the band gap. This takes place in different ways, discussed in Appendix A. An expression for the total number of carriers recombining at the surface per unit area per unit time is given by Sah et al[24].

1.6 Experimental methods

Determination of the surface properties is not easy as such, because most of the electronic phenomena can only be detected for the sample as a whole. The surface properties can be derived only if the bulk properties can be accounted for. Such a separation of bulk and surface properties can be effectively achieved by varying the barrier height at the surface and following the resulting change in electrical properties. This method also helps in the determination of surface state density and energy distribution. The equilibrium barrier height is a function of the surface state distribution, which depends on the method used for surface preparation and the surrounding ambients. Braittain and Bardeen[23] used this idea to vary the barrier height.

Potential barrier can also be varied by the capacitive application of field normal to the surface. The charge induced by the field gets distributed between the space charge region and the surface states. The change in the space charge brings about a change in the barrier height. The so called

'field effect experiments' describe the change in sample conductance as a result of the application of field normal to the surface. In fact, the experimental proof for the existence of surface states was provided by these experiments.

In such an experiment, a high voltage is applied to a parallel plate condenser of which one plate is made of a semiconductor and the other of a metal. A large amount of negative surface charge is induced on the surface of the semiconductor from a high voltage supply. If the area of the plates is A and the separation between them is d, the charge q induced on the semiconductor, when the applied voltage is V_o, is given by

$$q = C\ V_o = V_o A \frac{\kappa_s\ \varepsilon_o}{d}\ , \tag{1.2}$$

where κ_s is the dielectric constant of the medium between the two plates and ε_o is the free space permittivity.

In the absence of surface states, this charge would consist of free electrons in the conduction band. Thus, the number of induced electrons ΔN would be

$$\Delta N = \frac{q}{e} = V_o \frac{A\varepsilon_o\ \kappa_s}{ed}\ , \tag{1.3}$$

e being the electronic charge. The induced electrons should cause a change in the conductivity of the sample, given by

$$\Delta\sigma = e\,\mu_n\,\Delta n = e\,\mu_n\,\frac{\Delta N}{V}\,, \qquad (1.4)$$

where μ_n is the mobility of electrons, Δn the number of electrons induced per unit volume and V the volume of the semiconductor sample ($V = A\,h$, h being the thickness of the sample). Thus, the change in conductivity expected from the above experiment was

$$\Delta\sigma = \frac{e\mu_n}{Ah}\cdot\frac{V_o\,A\,K_s\,\epsilon_o}{ed} = \frac{V_o\mu_n\,K_s\,\epsilon_o}{hd}\;. \qquad (1.5)$$

But the observed change in conductivity was only about one tenth of the value predicted by the above expression. This difference was explained by Bardeen[19], who accounted for the surface states. According to him, most of the induced charges go into the surface states and these electrons in the surface states are immobile and hence the change in the conductivity is small.

Another effect observed was the slow relaxation of the field effect. When a voltage is applied, the surface potential gets built up immediately, but on removing the voltage, it is found to decay gradually to the zero field value in time, which varies from a few seconds to hours or days. This effect was attributed to the presence of fast and slow surface states. The relaxation time for the field effect was found to be very

large, when thick oxides were present at the semiconductor surface. The surface potential decays to a value close to the zero field value in a short time (this is due to the fast states), but it takes very long to come to exact zero field value due to the presence of the slow states at the surface.

Some important experimental methods are briefly described below.

1.6(a) Surface conductance

The potential barrier introduces a space charge region in the surface layer. The conductance of this barrier dependant space charge region is different from that of a layer of the same thickness in the bulk region. The changes in the surface conductance, due to variation in the barrier height, can be measured directly. The surface conductance $\Delta\sigma$ at any barrier height V_s is defined as the change in the sample conductance per unit area of its surface, resulting from a change in the barrier height 0 to V_s. Thus,

$$\Delta\sigma = \frac{l^2}{A}\left(\frac{1}{R} - \frac{1}{R_o}\right), \qquad (1.6)$$

where l and A are the length and the surface area, respectively and R is the resistance of the sample, whose value at $V_s = 0$, is R_o.

To determine the surface conductance, resistance of the sample, in the form of a thin rectangular filament, is measured, while the potential barrier is varied by external means. It is obvious from eq. (1.6) that $\Delta \sigma_{min}$ is obtained when R is maximum. The V_{sm}, at which R becomes maximum, is given by

$$v_{sm} = \frac{eV_{sm}}{kT} \simeq 2\,u_b - \ln\left(\frac{\mu_n}{\mu_p}\right), \qquad (1.7)$$

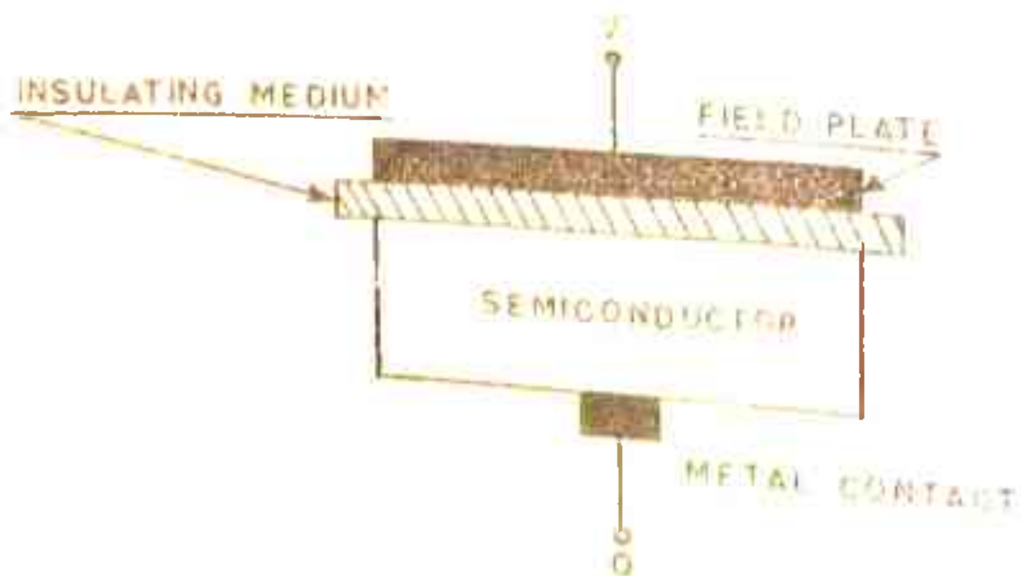
which is a function of temperature and impurity concentration. Here, $u_b = (e\varphi_b)/kT$, where φ_b is the separation between Fermi level and conduction band in the bulk. Knowing the conductance, the barrier height can be obtained, which in turn depends on the surface state density[25, 26, 27].

1.7(b) Surface capacitance

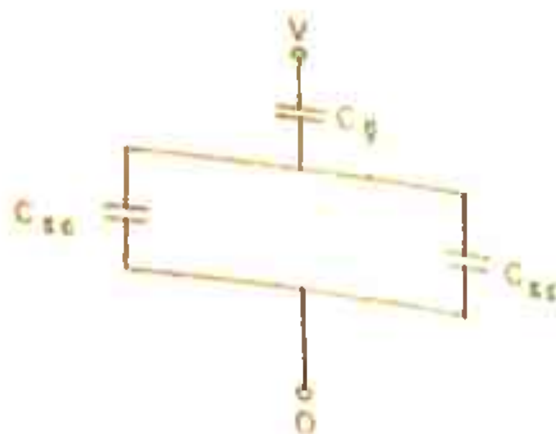
With the knowledge of surface capacitance, change in the surface charge can be correlated with the corresponding change in the barrier height. The surface capacitance is defined as

$$C_s = \left|\frac{\Delta Q_s}{V_s}\right| = \left|\frac{(Q_{sc} + \Delta Q_{ss})}{V_s}\right| = C_{sc} + C_{ss}, \qquad (1.8)$$

where ΔQ_s and ΔQ_{ss} are, respectively, the total change in the surface charge density and the change in surface state



(a) A METAL INSULATOR SEMICONDUCTOR (MIS) STRUCTURE



b) EQUIVALENT CAPACITANCE CIRCUIT OF MIS STRUCTURE

FIG. 1.4 FIELD PLATE - SEMICONDUCTOR CAPACITANCE

charge density, both due to the change in barrier height from 0 to V_s. Q_{sc} is the space charge density and C_{sc} is the space charge capacitance. The surface state capacitance C_{ss} is defined as

$$C_{ss} = \left| \frac{-Q_{ss}}{V_s} \right| . \tag{1.9}$$

The space charge capacitance C_{sc} is a unique function of V_s for a given impurity concentration and temperature and can be easily calculated. The surface state capacitance C_{ss} depends on the distribution of the surface states.

To measure surface capacitance C_s, a plane parallel capacitor is formed between the semiconductor sample and a metal plate, separated from each other by a thin insulating film, (MIS structure), as shown in Fig. 1.4a. Fig. 1.4b shows the equivalent capacitance circuit , where C_g is the geometric capacitance (per unit area) between the metal electrode and the surface, i.e., the cpacitance that would be measured, when the semiconductor is replaced by a metal. The effective capacitance C_o, measured by an external circuit, is given by

$$\frac{1}{C_o} = \frac{1}{C_g} + \frac{1}{C_s} = \frac{1}{C_g} + \frac{1}{C_{sc} + C_{ss}} . \tag{1.10}$$

In practice, the differential capacitance C_o is measured by superimposing a small a.c. signal on the d.c. bias voltage and measuring the capacitance as a function of the bias voltage.

$$C_o = \left| \frac{dQ_s}{dV_o} \right| , \qquad (1.11)$$

where dV_o is the change in the applied voltage across the capacitor, required to change the barrier height from 0 to V_s.

A substantial amount of information about the surface state distribution is obtained by determining the differential surface capacitance as a function of the barrier height v_s ($\equiv (qV_s)/kT$). The density and energy distribution of the surface states are obtained by comparing the theoretical and experimental curves.

1.6(c) Dc field effect

This consists of the steady state changes in surface conductance, induced by electrostatic fields. For each applied voltage, the system is allowed to reach equilibrium and the resistance of the filament (sample) is measured, when no further change in its value is detectable. The measuring voltage across the filament is kept small, compared to that applied at the field plate, so as to maintain the entire surface

at effectively the same potential. This method gives the density and energy distribution of the surface states, by comparing the results of the experiment (ΔQ_{ss} as a function of V_s) with the theoretical expression for the occupation statistics. This straight forwardness of the method holds, only when the distribution of surface states is discrete and the dominant sets of states are widely separated in energy. Additional information is required to get the distribution, if this condition does not hold.

In dc field effect experiments, both slow and fast surface states participate. The density of slow states being large, most of the charges are trapped in these states and the variation of barrier height becomes very small even for very high fields applied, due to the long time constants of the slow states. This is generally the case for germanium and silicon surfaces.

1.6(d) Low frequency field effect

In order to study the fast surface state effects, dc field can be used only when the surface conductance is measured soon after the application of the field, before any appreciable charge can be trapped in or released from the slow states[28,29]. This is quite useful at low temperatures, where

the time constant of slow states is quite long (hours).
At room temperature alternating fields can be used[30, 31,32].
A considerable frequency range is available in which slow states are inoperative, while the fast states are in complete equilibrium with the space charge region. The filament resistance is measured as a function of the ac voltage applied to the field plate and density and energy distribution of the surface states is obtained as in the last case (section 1.6c).

REFERENCES

(Chapter - I)

1. M.M. Atalla, E. Tannenbaum and E.J. Schreibner, Bell Syst. Tech. J., 38 , 749 (1959)
2. E.P. Weigner and F. Seitz, Phys. Rev., 43 , 804 (1933)
3. J.C. Slater, Phys. Rev., 45 , 794 (1934)
4. W. Shockley, Phys. Rev., 56 , 317 (1939)
5. E.T. Goodwin, Proc. Camb. Phil. Soc., 35 , 221 (1939)
6. R. de L. Kronig and W. G. Penney, Proc. Roy. Soc., A130 , 499 (1931)
7. I. Tamm, Phys. Z. Sowjet, 1 , 733 (1932)
8. A. W. Maue, Z. Physik, 94 , 717 (1935)
9. E.T. Goodwin, Proc. Camb. Phil. Soc., 35 , 205, 221, 232 (1939)
10. S. Rijanow, Z. Physik, 89 , 806 (1934)
11. M. Tomasek, Surface Sc., 2, 8 (1964)
12. J. Koutecky, Semiconductor Surfaces, Proc. second Conf., Pergaman Press, Edited by J.N. Zemel, 233 (1960)
13. J. Koutecky and M. Tomasek, Semiconductor Surfaces, Proc. second Conf., Pergaman Press, Edited by J.N.Zemel, 241, (1960)

14. D. Pugh, Phys. Rev. Lett., 12 , 390 (1964)

15. T.B. Grimley, Proc. Phys. Soc. London, 72 , 103 (1958)
J. Phys. Chem. Solids, 14 , 227 (1960)

16. J.D. Levine and P. Mark, Phys. Rev., 144 , 75 (1966)

17. V. Heine, Proc. Phys. Soc. London, 81 , 300 (1963)

18. S.G. Davison and J.D. Levine, Solid State Physics, 25 , 1 (1970)

19. J. Bardeen, Phys. Rev., 71 , 717 (1947)

20. W.E. Meyerhof, Phys. Rev., 71 , 727 (1947)

21. W. Shockley and G. Pearson, Phys. Rev., 74 , 232 (1948)

22. W. Shockley and W. T. Read, Phys. Rev., 87 , 835 (1952)

23. W. H. Braittain and J. Bardeen, Bell System Tech. J., 32 , 1 (1953)

24. C. T. Sah, R.N. Noyce and W. Shockley, Proc. IRE, 45 , 1228 (1957)

25. J. R. Schrieffer, Phys. Rev., 97 , 641 (1955)

26. R. H. Kingston and S.F. Neustadter, J. Appl. Phys., 26 , 718 (1955)

27. C. G. B. Garrett and W. H. Braittain, Phys. Rev., 99 , 376 (1955)

28. A.Many Y. Margoninski, E. Harnik and E. Alexander, Phys. Rev. 101 , 1433, 1434 (1955)

29. A.Many, E. Harnik and Y. Margoninski, 'Semiconductor Surface Physics', Edited by R. H. Kingston, University of Pennsylvania Press, Philadelphia, p. 85 (1957)

30. H. C. Montgomery and W. L. Brown, Phys. Rev., 103 , 865 (1956)

31. W. L. Brown, Phys. Rev., 100 , 590 (1955)

32. J. Bardeen and S.R. Morrison, Physica, 20 , 873 (1954)

****

Chapter-II

MOS DEVICES

In order to overcome various adverse surface phenomena associated with semiconductor devices, like MOS field effect transistors and p-n junction devices, the semiconductor surfaces have been intensively investigated for many years since it was first reported[1] that thermally grown SiO_2 film can have a stabilizing action on the surface properties of silicon. In fact, one of the principal reasons for the success of planar technology is that planar junctions are covered by a thermally grown SiO_2 layer. This reduces many surface effects and therefore, results in better control over device characteristics. This is the reason why SiO_2 layers have found a wide spread use in the semiconductor device technology. Moreover, it was demonstrated that the basis for all silicon device passivation is thermally grown SiO_2. Though other dielectrics, such as vapour deposited silicon oxide or nitride, phosphosilicate glass or aluminium oxide, are useful, they are generally employed as secondary layers, either over the thermal SiO_2 or over the metal.

2.1 Thermal oxidation of silicon

The thermal oxidation of silicon is commanly carried out in a water vapour or oxygen atmosphere over the temprature

range of 800-1250°C. The kinetics of thermal oxidation of silicon surfaces with H_2O or O_2 ambient, beyond the oxide thickness of 20 nm, is generally described by the combined linear-parabolic relation of the form[2]

$$x_o^2 + Ax_o = B\,(\,t + \tau\,), \qquad (2.1)$$

where A, B and τ are constants and x_o is the oxide thickness after a time t.

Whereas the linear growth is controlled by reaction of the oxidising species at the Si-SiO_2 interface, the parabolic growth is dependant on diffusion and/or solubility of oxidising species through the growing oxide. The oxidation rate is observed to be affected by the presence of phospho-silicate glass ($P_2O_5 . SiO_2$) or borosilicate glass ($B_2O_3 . SiO_2$) on the silicon surface, which changes the diffusion of oxidising species. In addition, oxidation rate is also dependant on the crystal orientation and doping density.

2.2 Charges in the Si-SiO_2 system

In an ideal case, SiO_2 can be considered to be an insulator,which does not contain any charges. But in practice the thermally grown SiO_2 film is found to contain positive charges and is associated with at least four types of centers,

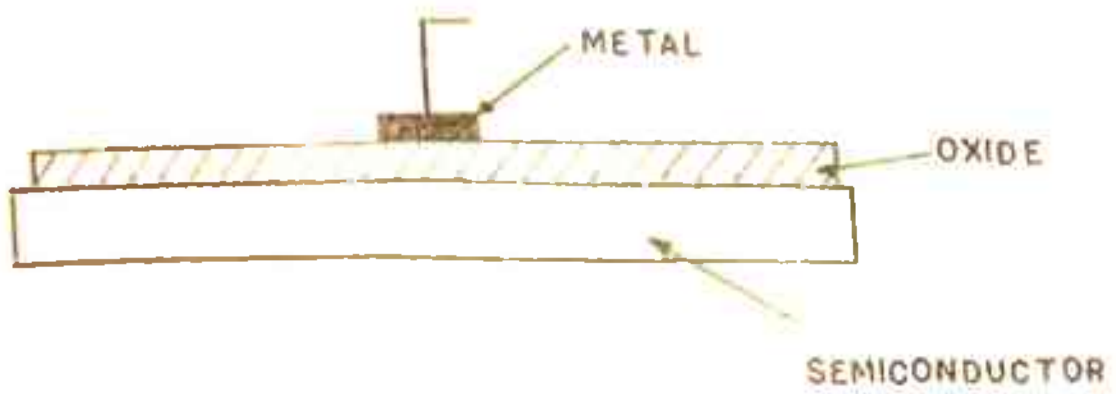


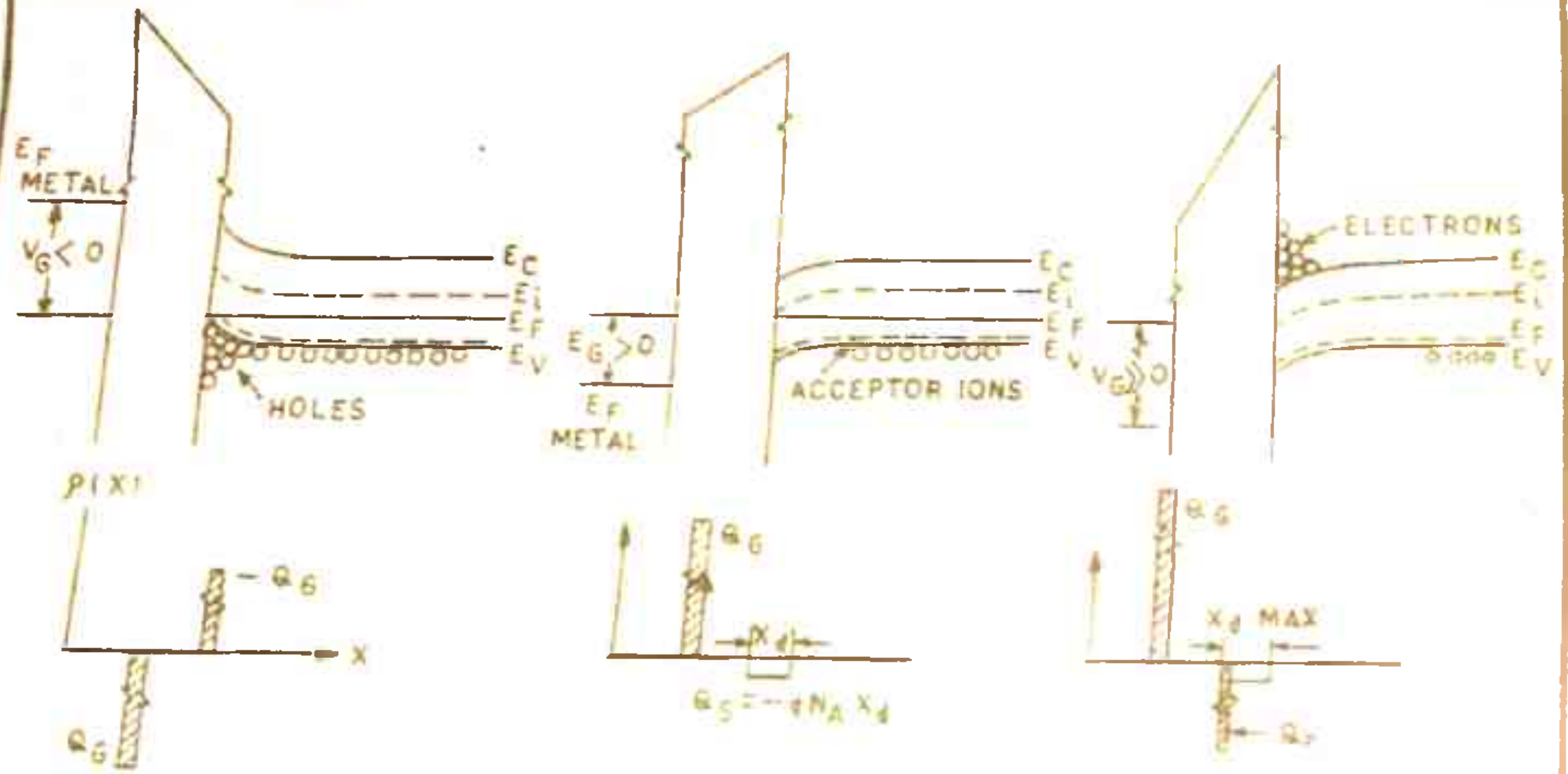
FIG. 2.1 M – O – S – STRUCTURE

namely, fixed oxide charge or surface state charge, mobile charge in oxide, fast surface states or interface states and traps within oxide which may be ionized by an incident radiation. The fixed oxide charge, usually referred to as Q_{ss}, may vary from 10^{10}- 10^{12} charges/cm^2, depending upon the growth conditions. The mobile charge arises from contamination of the oxide during processing and is thought to be due to either alkali ions (Na^+) or protons. It's magnitude also ranges from less than 10^{10} charges/cm^2 to more than 10^{12} charges/cm^2. The fast surface states do not represent a fixed charge, because they can exchange charges easily with silicon. Lastly, positively charged centres with a concentration of the order of $10^{18}/cm^3$, have been observed in oxide, after its exposure to ionizing radiations, such as x-rays, electrons or gamma rays.

In view to study the nature of above mentioned charges, the C-V characteristics of metal-oxide-semiconductor (MOS) devices have been used in the present investigation. Because of the ease in fabrication and greater sensitivity, this technique has been very commanly used and its details are discussed below.

2.3 Surface space charge and capacitance

The MOS structure is a thermally grown oxide film sandwitched between metal and semiconductor, as shown in Fig. 2.1. It is basically a metal-insulator-semiconductor

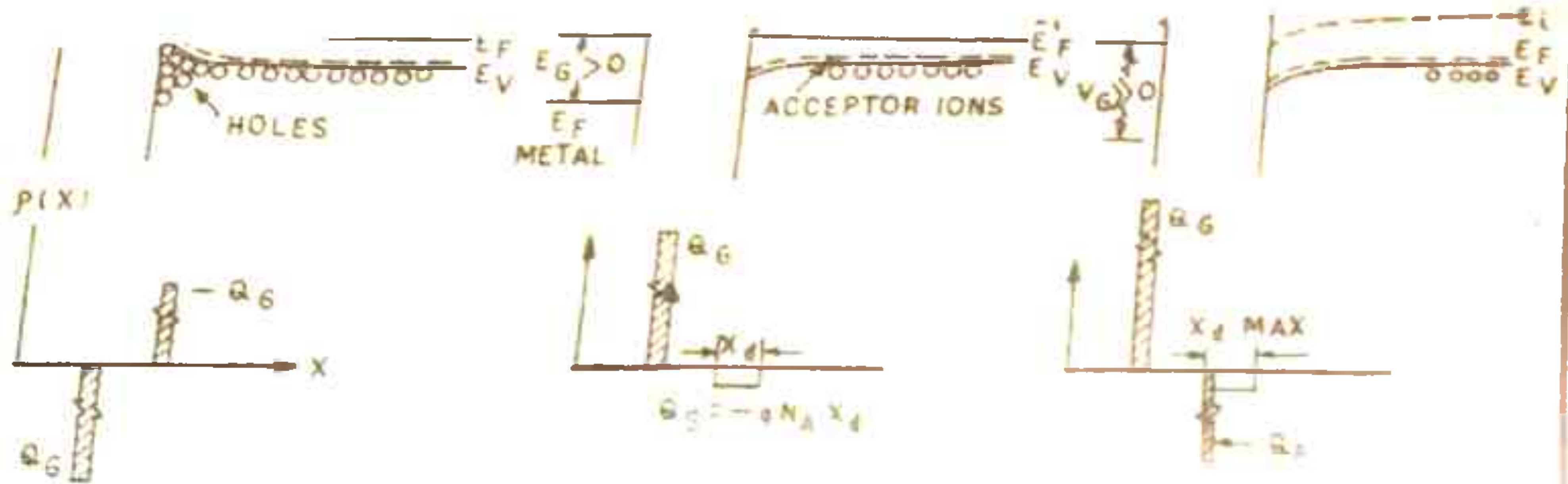


(a) ACCUMULATION OF MAJORITY CARRIERS NEAR SURFACE

(b) DEPLETION OF MAJORITY CARRIERS FROM SURFACE

(c) INVERSION: ACCUMULATION OF MINORITY CARRIERS NEAR SURFACE

FIG. 2.2 ENERGY BANDS AND CHARGE DISTRIBUTION IN AN M-O-S STRUCTURE, IN ABSENCE OF SURFACE STATES AND WORK FUNCTION DIFFERENCE



(a) ACCUMULATION OF MAJORITY CARRIERS NEAR SURFACE

(b) DEPLETION OF MAJORITY CARRIERS FROM SURFACE

FIG. 2.2 ENERGY BANDS AND CHARGE DISTRIBUTION IN AN M-O-S STRUCTURE, IN ABSENCE OF SURFACE STATES AND WORK FUNCTION DIFFERENCE

(MIS) structure, in which the insulator is an oxide. The metal electrode over the SiO_2 film is used to apply electric field normal to the surface. When a potential is applied on the metal, bending of the conduction and the valence bands takes place, which depends on the voltage applied and the type of semiconductor (n-type or p-type). (Here we are considering the case when the surface states are absent, otherwise they also cause a band bending even in the absence of applied voltage). Under this condition, the charge density in a small region near the surface is different from that in the semiconductor bulk and this region is known as the 'surface space charge region'. When this region is in thermal equilibrium, there is no flow of dc current and the Fermi level is same throughout the semiconductor; consequently, $np = n_i^2$ holds. The space charge phenomena in silicon, including various aspects of MOS capacitances, are well discussed in books[3-8] and research papers[9-14].

Energy bands and charge distribution in p-type MOS structure, under different bias conditions, are illustrated in Fig. 2.2. When a negative bias ($V_G < 0$, where V_G is the potential on the metal plate) is applied to the gate (metal), the majority carriers (holes) in the p-type semiconductor get attracted towards the metal and accumulate in the surface space charge layer. In this case, the density of majority carriers is more in the surface layer than in the bulk and therefore,

the surface region is known as the 'accumulation region'. When the bias on the metal plate is positive ($V_G > 0$), the majority carriers (holes) are repelled and the surface space charge layer gets depleted of them and is, therefore, known as the 'depletion region'.

The charge per unit area in the semiconductor space charge region, Q_{sp}, is given by

$$Q_{sp} = - e N_A x_d , \qquad (2.2)$$

where e is the electronic charge, N_A is the density of acceptor atoms and x_d is the width of the depletion region. The integration of the Poisson's equation gives the potential in the depletion region as

$$\varphi = \varphi_s \left(1 - \frac{x}{x_d} \right)^2 , \qquad (2.3)$$

φ being the potential at any point x in the depletion region and φ_s , the potential at the surface (which is equal to the total bending of the bands from the bulk of the semiconductor to its surface). φ_s is given by

$$\varphi_s = \frac{e N_A x_d^2}{2\epsilon_s} , \qquad (2.4)$$

where ϵ_s is the semiconductor permittivity.

When the gate potential ($V_G > 0$) is further increased, the minority carrier density in the space charge region increases and the width of the space charge region also increases. If V_G goes on increasing, a situation comes when the bands are bent so much that the conduction band comes closer to the Fermi level at the surface than the valence band. When this happens, the concentration of electrons near the interface increases sharply, so much so that the electron density at the surface is more than the hole density in the bulk and the surface layer is then known as 'inversion region' . The accumulation, depletion and inversion regions are shown in Figs. 2.2a, b and c, respectively.

2.4 Capacitance-voltage characteristics of MOS structure

The nature of C-V characteristics of MOS structure is discussed below for negative and positive bias conditions.

In case of a p-type silicon, when the gate voltage V_G is negative, there is an accumulation of positive charges (holes) near the Si-SiO_2 interface. The measured value of the capacitance (C) under this bias condition is that of the oxide (C_o) only, i.e., $C = C_o$. (All the capacitances are per unit area , for simplicity.) As V_G is made less negative , the charge variation does not take place very close to the interface,

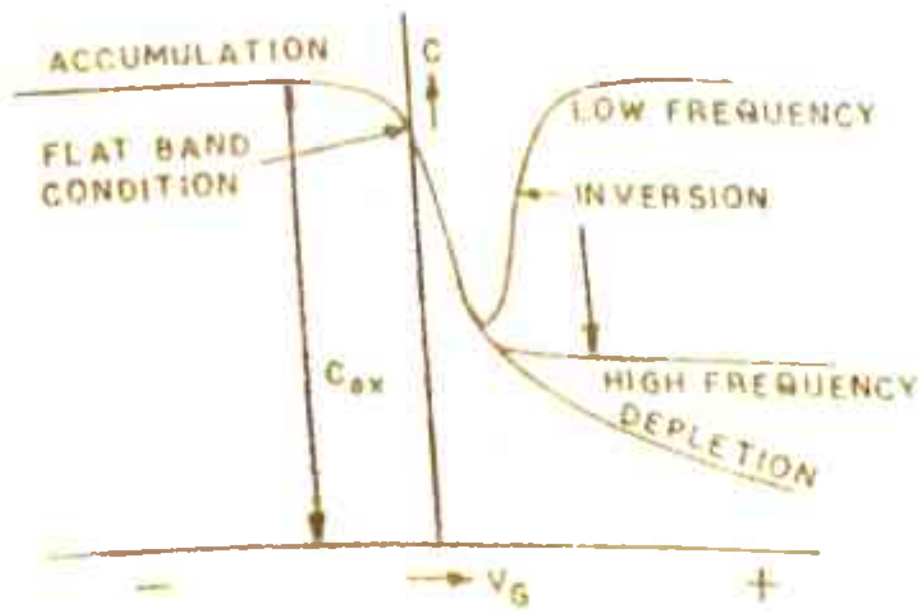


FIG. 2.3 C-V CURVE OF A M-O-S STRUCTURE ON p-TYPE SILICON FOR HIGH AND LOW MEASURING FREQUENCIES

thereby the space charge capacitance (C_{sp}) decreases, which now becomes comparable to C_o. Thus, for zero and small negative values of V_G, the MOS capacitance is smaller than the oxide capacitance. Now, when the gate potential is made positive, the depletion region is formed and the charge variation takes place at the edge of the space charge region. So, the increase in positive voltage at the gate, increases the depletion region width and hence, the capacitance C_{sp} decreases, thereby decreasing C. But for sufficiently high V_G , the band bending becomes so much that an inversion layer is formed at the Si-SiO_2 interface. At still larger positive bias and high measurement frequency, additional charge induced in silicon appears in the form of electrons in the narrow inversion layer at the interface and the depletion region width approaches a maximum value. The corresponding capacitance reaches its minimum value. At low measurement frequency, both the majority carriers (holes) and minority carriers (electrons) can follow the applied signal and the capacitance starts increasing and reaches the maximum value equal to the oxide capacitance (C_o). The nature of the C-V characteristics for both the cases is shown in Fig. 2.3.

2.5 MOS capacitance in absence of surface states

The voltage V_G applied on the MOS structure appears partly across the oxide layer (V_o) and partly across silicon (φ_s), i.e.,

$$V_G = V_o + \varphi_s \, . \tag{2.5}$$

Assuming that there are no charges in the oxide layer and at the interface, the electric displacement should be continuous, as required by Gauss's law. These assumptions lead to the voltage across the oxide V_o to be given by

$$V_o = -\frac{Q_{sp}\, x_o}{\varepsilon_{ox}} = -\frac{Q_{sp}}{C_o}, \tag{2.6}$$

where ε_{ox} is the permittivity of the oxide layer.

If Q_G is the charge per unit area on the gate, the capacitance of the MOS structure would be

$$C = \frac{dQ_G}{dV_G} = -\frac{d\,Q_{sp}}{d\,V_G} = -\frac{d\,Q_{sp}}{-\frac{d\,Q_{sp}}{C_o} + d\psi_s} \tag{2.7}$$

$$\text{or} \quad C = \frac{1}{\frac{1}{C_o} + \frac{1}{C_{sp}}}, \tag{2.3}$$

$$\text{where } C_{sp} = -\frac{d\,Q_{sp}}{d\,\psi_s} = \frac{\varepsilon_s}{x_d} = \frac{k_s\,\varepsilon_o}{x_d}. \tag{2.9}$$

These equations give

$$\frac{C}{C_o} = \frac{1}{\sqrt{\{1+(2\varepsilon_{ox}^2\, V_G)/(e\, N_A \varepsilon_s x_d^2)\}}}. \tag{2.10}$$

This equation shows that the capacitance would fall as the depletion region width increases. However, eq. (2.10) does not

hold when V_G is zero or negative, since no depletion region is then present and the measured MOS capacitance would be only that of the oxide layer, i.e., $C = C_o$, because in this case the semiconductor acts just as a resistor in series.

The space charge capacitance C_{sp} and hence the MOS capacitance C, are frequency dependant, while oxide capacitance C_o does not depend on frequency.

The charge Q_{sp} in the semiconductor space charge region under dc bias is given by

$$Q_{sp} = \int_0^{\infty} \rho(x)\, dx, \qquad (2.11)$$

where $\rho = e\,(p - n + N_D - N_A)$,

p and n being the hole and electron concentrations, respectively and N_D and N_A are the donor and acceptor concentrations, respectively. Integration of the Poisson's equation gives the space charge as

$$Q_{sp} = -2\frac{U_s}{|U_s|}\, e\, n_i\, L_D\, [2\{\cosh(U_s - U_F) - \cosh U_F + U_s \sinh U_F\}] \qquad (2.12)$$

where $L_D = \frac{kT}{e}\left(\frac{\varepsilon_s}{2en_i}\right)^{1/2}$

is the intrinsic Debye length and

$$U_s = \frac{e}{kT}\varphi_s \text{ and } U_F = \frac{e}{kT}\varphi_F,$$

φ_F being the Fermi potential (separation between the Fermi level and intrinsic Fermi level in the bulk).

2.6 Theoretical C-V characteristics

The information about the surface properties of oxidized silicon, without considering surface states and oxide charge, is obtained from the measurements of the differential capacitance (dQ/dV) of MOS structures as a function of dc voltage applied across it. A large contact is made on the semiconductor side of the device, so that the contribution of the capacitance of this side to the total capacitance can be neglected. At high frequencies the capacitance of the MOS structure is given by the series combination of capacitance of oxide layer (C_o) and that of the space charge layer (C_{sp}), i.e.,

$$C = \frac{C_o C_{sp}}{C_o + C_{sp}} . \qquad (2.13)$$

Here, C_o is constant and is given by

$$C_o = \frac{k_o \varepsilon_o}{x_o} . \qquad (2.14)$$

The space charge capacitance depends on the width of space charge region and is given by eq. (2.9), where depletion region width $x_d = [(2\varepsilon_s \varphi_s)/(eN_A)]^{1/2}$. (2.15)

The capcitance of the space charge region is different at low and high frequencies. At high frequency the space charge

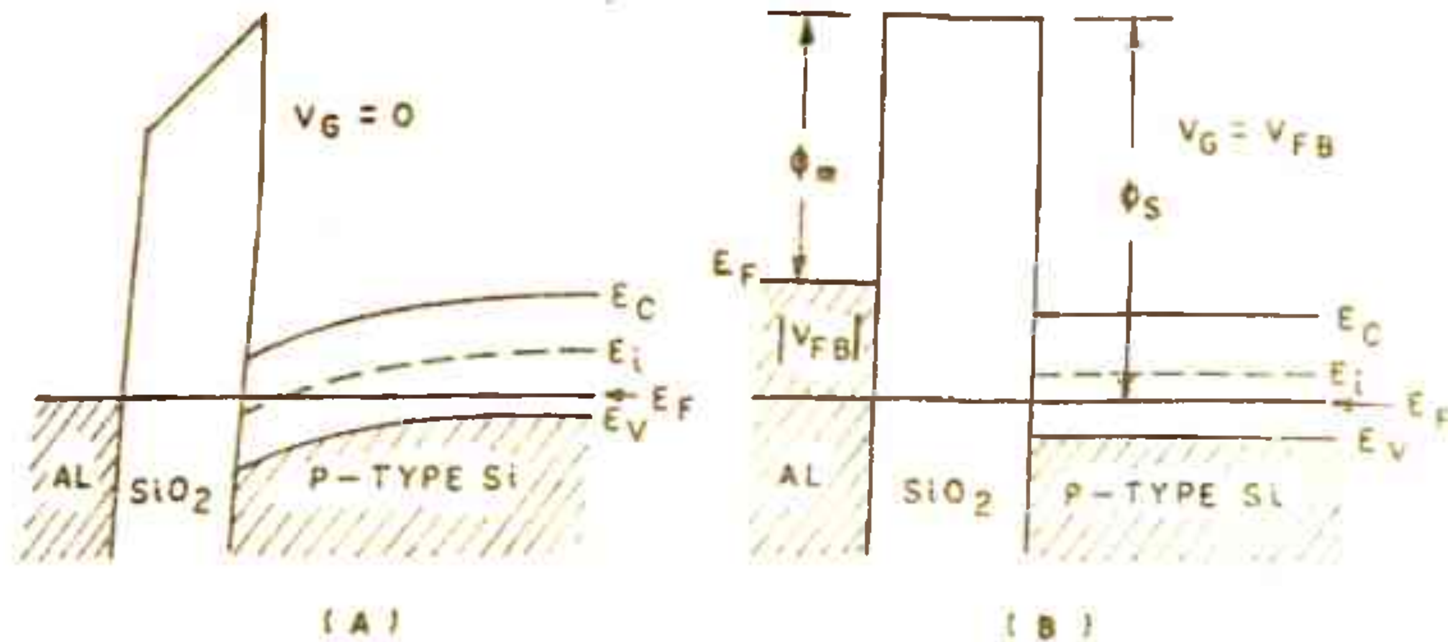


FIG. 2.4 THE EFFECT OF METAL SEMICONDUCTOR WORK FUNCTION DIFFERENCE ON THE POTENTIAL DISTRIBUTION IN AN M-O-S STRUCTURE.

(A) CONDITIONS FOR $V_G = 0$

(B) FLAT BAND CONDITION

capacitance is as given by eq. (2.9). At low frequency the charge carriers can follow the signal frequency and therefore, under this condition the space charge capacitance can be obtained by differentiating the charge Q_{sp} (as given by eq. 2.12) with respect to surface potential φ_s. This gives

$$C_{sp} = \frac{k_s \varepsilon_o e(p - n + N_D - N_A)}{Q_{sp}} . \qquad (2.16)$$

2.7 Effect of metal work function

It has been found that the difference in work functions of semiconductor (φ_s) and metal (φ_m) causes a shift of the C-V characteristic. This shift is caused by the band bending due to the work function difference. Because of the band bending some additional charges are present in the space charge region, which induce charges on the metal-oxide interface. These charges cause the shift of C-V characteristic.

The flat band condition is achieved, when we apply just sufficient voltage to metal, so that the already bent bands become flat. This voltage is known as 'flat band voltage' V_{FB}. From Fig. 2.4 , it is clear that

$$V_{FB} = \varphi_m - \varphi_s . \qquad (2.17)$$

2.8 Effect of surface states

If the surface states are also present, the charges in these states would also induce charges of opposite polarity

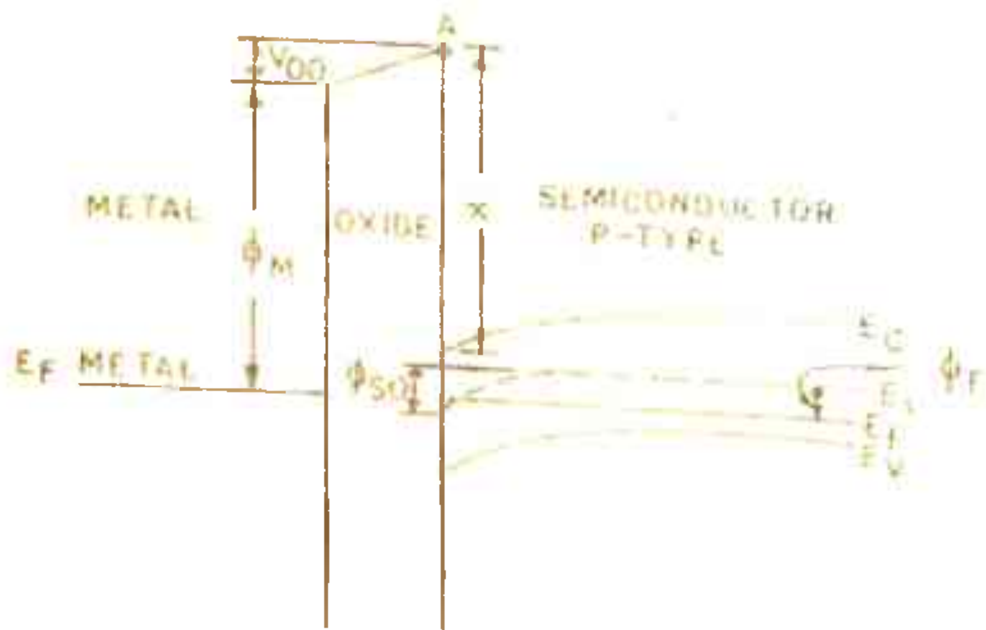


FIG. 2.5 EFFECT OF SURFACE STATE AND WORK FUNCTION DIFFERENCE ON ENERGY BANDS IN M-O-S STRUCTURE FOR $V_G = 0$

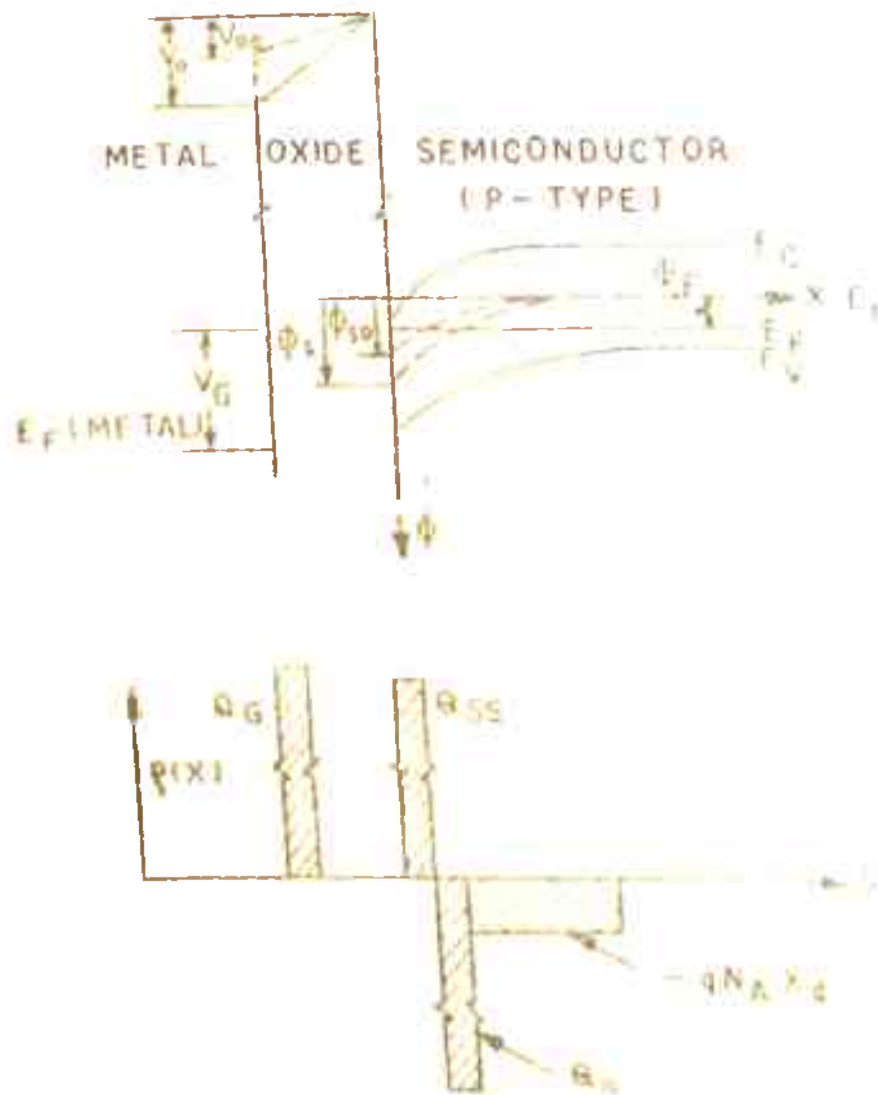


FIG. 2.6 THE ENERGY BANDS AND CHARGE DISTRIBUTION IN M-O-S STRUCTURE UNDER APPLIED GATE BIAS

on the metal-oxide interface and in the space charge layer. The charges in the surface states vary with the band bending (or the surface potential φ_s). The effect of the work function difference and the surface state charges, is shown in Fig. 2.5, for zero gate bias.

From Fig. 2.5, we see that

$$\varphi_m + V_{oo} = \chi_s + \frac{E_G}{2} - (\varphi_{so} - \varphi_F) \qquad (2.18)$$

$$\text{or} \quad \varphi'_{ms} = \varphi_m - (\chi_s + \frac{E_G}{2} + \varphi_F) = - (\varphi_{so} + V_{oo}), \qquad (2.19)$$

where φ'_{ms} is effective metal to semiconductor work function difference, V_{oo} is voltage drop across the oxide layer at zero gate bias ($V_G = 0$), φ_{so} is the surface potential at $V_G = 0$, χ_s is the electron affinity and E_G is band gap of the semiconductor.

Fig. 2.6 shows the energy bands and charge distribution in MOS structure, under applied gate bias. In the figure, φ_s and V_o are the quantities (φ_{so} and V_{oo}) as defined above , when gate bias is not zero. The charge on the metal electrode Q_G, when a voltage V_G is applied to it, is equal to the charges on the semiconductor surface and in the oxide layer. Under the assumption that the charge in oxide layer is small and may be neglected (see Fig. 2.6), we may write

$$Q_G = Q_{sp} - Q_{ss} , \qquad (2.20)$$

where $Q_G = V_o C_o$ with $C_o = (k_o \varepsilon_o)/x_o$. k_o is dielectric constant of oxide , ε_o is the permittivity of free space, x_o is oxide thickness and Q_{ss} is the charge in the surface states. From Fig. 2.6 we find that

$$V_G = V_o - V_{oo} + \varphi_s - \varphi_{so} . \qquad (2.21)$$

Using eq. (2.19), $V_G = V_o + \varphi_s + \varphi'_{ms}$. (2.22)

Substituting V_o from (2.22) in eq. (2.20), one gets

$$V_G - \varphi'_{ms} + \frac{Q_{ss}}{C_o} = \varphi_s - \frac{Q_{sp}}{C_o} . \qquad (2.23)$$

The cpacitance of the MOS structure in the presence of surface states is given by

$$C = \frac{1}{\frac{1}{C_o} + \frac{1}{C_{sp} + C_{ss}}} . \qquad (2.24)$$

C_{ss} being surface state capacitance . Assuming the charges in surface states to be constant ($dQ_{ss}=0$) , the capacitance may be written as

$$C = \frac{C_o C_{sp}}{C_o + C_{sp}} . \qquad (2.25)$$

The charge in surface states is , however, not constant, but it depends on the frequency of the applied signal.

2.9 Theoretical calculation of C-V curve considering surface states

Knowing the Fermi potential U (in units of kT/e) and taking the arbitrary value of surface potential U_s, the charge Q_{sp} may be calculated from eq. (2.12). The space charge capacitance is given by eq. (2.9) and (2.16) for high and low frequencies, respectively. The effective voltage V_{eff}, as given by eq. (2.23), is

$$V_{eff} = V_G - \varphi'_{ms} + \frac{Q_{ss}}{C_o} = \varphi_s - \frac{Q_{sp}}{C_o} . \qquad (2.26)$$

Theoretical curve is plotted between V_{eff} and capacitance. The experimental C vs V_G curve is also obtained. The shift between the two curves represents $\frac{Q_{ss}}{C_o} - \varphi'_{ms}$. Thus, knowing φ'_{ms} from eq. (2.19), the charge in the surface states and thereby the density of surface states can be calculated.

2.10 Surface state measurement techniques

Various techniques have been developed to determine surface state parameters from MIS capacitors. The surface states are found to affect the capacitance of MOS devices by giving an additional capacitance C_{ss} in parallel with the space charge capacitance. Following are some of the techniques used for surface states measurements.

2.10(a) Differentiation method

This method, given by Terman[9], consists of measuring C-V curve of MOS device at very high frequency, when it is free from the capacitive influence of surface states. The comparison of this curve with an ideal MIS curve gives the integrated charge in the surface states. The total charge in the surface states is given by

$$Q_{ss} = C_o \Delta V , \qquad (2.27)$$

where ΔV is the voltage differential between the high frequency curve and the ideal curve for a particular surface potential. Thus, the surface states density per electron volt is obtained as

$$D_{ss} = \frac{1}{e} \left(d\, Q_{ss}/d\varphi_s \right) . \qquad (2.28)$$

However, it was pointed out by Zaininger and Warfield[11] that only the integral of surface states density is measured and there is uncertainty about the magnitude of the space charge capacitance.

2.10(b) Integration method

In the integration method, proposed by Berglund[15], the semiconductor surface potential is determined as a function of applied voltage, from differential capacitance measurement at

low frequency. The expression used for this is

$$\varphi_s(V_1) - \varphi_s(V_2) = \int_{V_2}^{V_1} \left(1 - \frac{C}{C_o}\right) dV, \qquad (2.29)$$

where $\varphi_s(V_1)$ and $\varphi_s(V_2)$ are the surface potentials at applied voltages V_1 and V_2. This is evaluated by integrating $(1 - \frac{C}{C_o})$ vs V curve. The charge neutrality condition is given by

$$Q = \frac{\varepsilon_{ox} V_o}{x_d} = e D_{ss} + Q_{sp} , \qquad (2.30)$$

where Q is the charge in the oxide, D_{ss} the surface state density and Q_{sp} the charge in the semiconductor space charge region. Differentiation of eq. (2.30) with respect to φ_s gives

$$\frac{\partial \varphi_s}{\partial V_o} = \frac{\varepsilon_{ox}/x_d}{\frac{dQ_{sp}}{d\varphi_s} + eD_{ss}} . \qquad (2.31)$$

Comparing the $\frac{\partial \varphi_s}{\partial V_o}$ vs φ_s curve with the one given by eq. (2.29), the density of surface states can be obtained.

2.10(c) Conductance method

In this method, first used by Nicollian and Goetzberger[16], surface state density is determined by measuring conductance of the device. This method gives better results as compared to other methods in the case of low surface state density, which is the case with the thermally grown $Si-SiO_2$ interface.

The frequency dependant conductance G_p is a function of surface state capacitance C_{ss} and resistance R_s only, as given by

$$\frac{G_p}{\omega} = \frac{C_{ss}\,\omega\tau}{1+\omega^2\tau^2}\,,$$ where $\tau(=R_s C_{ss})$ is the surface state life time and ω is the angular frequency of ac signal. The G_p/ω vs ω curve passes through a maximum at $\omega\tau = 1$, where its value is $C_{ss}/2$. Knowing C_{ss}, the density of surface states can be calculated from

$$D_{ss} = \frac{C_{ss}}{e\,A}\,, \qquad (2.32)$$

where A is the metal plate area.

2.10(d) <u>Temperature method</u>

This method was suggested by Gray and Brown[17], using which the surface state distribution near the conduction and valence band edges, may be obtained. It was found that the C-V curves shift along the voltage axis with the decrease in temperature. For a p-type sample the shift is towards the negative direction, whereas for n-type sample it is in the positive direction.

In this method, the change in voltage (and hence, the change in surface charge) is measured. This is required to

maintain the flat band condition, as the Fermi level within the silicon is varied by changing the sample's temperature in the range 80 to 300°K. The measurements are done at very high frequency to ensure that any charge in the surface states does not contribute appreciably to the ac capacitance, which means that the measured capacitance is due to free carriers only.

In the case of p-type semiconductor, at temperature T_1 the Fermi level is assumed to be above the surface states which are filled with electrons and are therefore neutral. When the temperature is decreased to T_2, the Fermi level moves closer to the valence band and some electrons are lost by surface states, which become positively charged. Now more negative voltage is required to reach the flat band and this is entirely due to the charge in the surface states, since the potential drop in the semiconductor is zero at both the temperatures. The change in the flat band voltage, as the temperature is changed, gives the change in the surface state charge directly. The surface potential φ_s, however, being equal to the bulk Fermi level, can be calculated.

The experimental procedure consists of varying temperature and maintaining the flat band condition. This is done by observing the changes in the capacitance and adjusting

the bias. Knowing the change in flat band voltage with temperature , the surface charge vs surface potential curve can be obtained , which gives the surface state density as

$$D_{ss} = \frac{1}{e} \quad \frac{\partial Q_{ss}}{\partial \varphi_s} . \tag{2.33}$$

2.11 A survey of the work done on Si-SiO_2 interface

In early sixties Atalla and his coworkers[1] from Bell Laboratories suggested that the silicon devices could be passivated by their native oxide, SiO_2, resulting in various improvements in device performance and reliability. As a result of its importance in the planar process, concentrated efforts were made to study the Si-SiO_2 interface and it is probably the most well characterized interface. Initial studies on this topic showed very high density of interface states and oxide charges[9,10]; and instability due to alkali ion contamination during operation further delayed the development of MOS devices. Continuous scrutiny of different process steps and studies of related parameters resulted in vast understanding of the subject and as a result sophisticated MOS and bipolar devices can be routinely fabricated. On the other hand, many questions still remain unanswered. A brief review of this subject along with some important results are discussed here.

It is now well established that a positive,fixed oxide charge Q_{ox} exists very near the $Si-SiO_2$ interface[11-13,16,18,19]. It is somehow related to the oxide structure in the interface region between the SiO_2 and silicon and is thus, dependant on the growth and annealing conditions. The dependence of the oxide charge density on the annealing ambient, such as O_2, H_2O, nitrogen or argon, and on the annealing temperature, is also relatively well known[7,18,20]. Not so well understood is the proposed mechanism, which explains the Q_{ox} dependence upon oxidation and annealing conditions.

The dependence of Q_{ss} on silicon orientation is also well documented and is more for (111) oriented silicon than for (100). This dependence is apparently related to the oxidation reaction.

Whereas Deal et al[18] observed an increase in Q_{ox} with temperature nitrogen annealing, the results of Lamb and Badcock[21] are contradictory. There is also disagreement on the influence of the oxide thickness on the surface charge Q_{ox}. Deal et al[18] found no influence of oxide thickness on the charge, whereas Badcock and Lamb[22] and Revesz and Zaininger[23] found lower values for higher oxice thicknesses.

The nature and origin of Q_{ox} have been the subject of considerable discussion. Most investigators now agree in

principle that Q_{ox} results from a non-stoichiometric silicon-oxygen structure in the Si-SiO_2 interface region. Both excess silicon and deficient oxygen would result in positive charge and density of the charge is dependant on the final high temperature annealing or oxidation condition and silicon orientation.

In mid-sixtees, intensive investigations were started and considerable empirical data concerning interface states have become available[7,20,24,25]. Because of its ease and sensitivity, the C-V method of analysis of MOS, has most commonly been used. This method has also been used to obtain a more accurate measure of interface state density, by carrying out the measurement at liquid nitrogen temperature[17] and has also been used in the present investigation.

Tamm and Shockley[4] predicted theoretically that because of disruption of the periodicity of lattice at a surface, a semiconductor would have a high density of localized energy levels introduced into its forbidden energy gap. With regards to interface states, it is widely believed that there are two high density blocks of states in the silicon forbidden gap, one close to valence band and the other close to conduction band, with a lower density continuum across the gap between them[7,17,20,24,25]. It is agreed that the interface state densities are generally proportional to Q_{ox} (initially ,in

particular) and they also depend on silicon orientation. It is also known that high temperature anneals in inert ambients, such as nitrogen, increase interface state densities. Similarly, treatment in hydrogen or active hydrogen species produced by the reaction of an active metal with water on the oxide surface, reduces surface state density[26].

The confusion over the type of states, i.e., donor or acceptor, still exists. From the frequency dependence of MOS C-V curves, Whelan[27] obtained a relatively large capture cross-section for electrons for the states near the conduction band edge and thus , deduced that these states were positively charged before electron trapping and hence, were donor states. In contrast to this, Gray and Brown[17] observed that for a p-type MOS capacitor, as the Fermi level moves towards the valence band a larger positive charge density is seen in the interface states, which they attribute to a set of donor states.

With regard to the physical origin of interface states, it is assumed at present that these states result from either defects in the structure of the interface region between silicon and the oxide, or from impurities in this region, or from both.

The presence of mobile impurity ions in thermal oxides causes building up and decay of space charge and other allied

polarization effects, resulting in change in the built-in-field and therefore, in the flat band voltage of MOS capacitor. First of all Kerr et al[28] observed this phenomenon in SiO_2 films, but later on Snow et al[29,30] were first to correlate it with the presence of alkali ions,mainly Na^+. These ions can be incorporated into oxide during any or all device processing steps and any processing material, solvent or ambient, can serve as a source. Other species, such as protons[31,32], immobile negative ions[33,34] and oxygen vacancies[33], produced due to the reaction of aluminium with SiO_2, have also been shown to contribute to ionic charge. Initial work of Hofstein[31] indicated that more than one hydrogen species might migrate in oxides alongwith the multiple types of sodium. Conflicting data have been presented regarding alkali content, particularly sodium, in the thermal oxides. The majority of results to date indicates that more sodium is present than is indicated electrically. Thus, the question arises regarding the nature of inactive sodium and conditions in which it could be electrically active or vice-versa.

Recently, Kriegler[35] gave a powerful method to prepare sodium free oxide films. His suggestion was to grow SiO_2 layers in oxygen with a few percent of HCl added to the gas stream. The HCl reacts with oxygen and gives out chlorine, which gets incorporated into oxide near the Si-SiO_2 interface. The built

in atoms passivate the surface by trapping Na^+ ions. Not only sodium ions get neutralized by the addition of chlorine or HCl, but also the oxidation rate was found to be more in case of chlorine oxides. The interface state density was found to be reduced by one order of magnitude in case of HCl oxides, as compared to the oxides grown in HCl free atmosphere[32,36-38].

The reduction in the oxide charge was not observed for the chlorine oxide, as compared to ordinary oxides[36,37,39-41]. The oxidation in the presence of chlorine or its compounds results in high concentration of chlorine near the Si-SiO_2 interface. The neutralization of sodium ions at the interface by chlorine helps in the passivation of the device. The higher concentration of sodium ions has been observed at the interface as compared to the oxide bulk[42]. There is a contradiction about the dependence of the passivation efficiency (fraction of the neutralized sodium ions) on the contamination level of the device. Kriegler et al[43] observed that the passivation efficiency is independant of contamination level, upto a value of 4×10^{12} ions/cm^2, whereas the observation of Van der Meulen et al[44] is that only one third of the sodium ions are neutralized.

Most of the above mentioned beneficial effects have been observed, using HCl or Cl_2 as a chlorine source, which are hazardous and difficult to handle and require extra installation.

A more manageable chlorine source-trichloroethylene (TCE)-was proposed by Declerck et al[45], which gives sufficient amount of chlorine in the gas phase and is equally or perhaps more effective as compared to HCl or Cl_2. However, at present very little information regarding its effect on $Si-SiO_2$ interface properties and chlorine incorporation is available. Our work, which used TCE as chlorine source, presented in this thesis , would throw some more light on the subject.

Radiation effect: The MOS devices subjected to ionizing radiations, such as x-rays, gamma rays, and high and low energy electrons, have been the object of considerable study. The radiation produces electron-hole pairs in the oxide layer . The electrons being quite mobile (electron mobility[46]- μ_n - 29 $cm^2/V/sec$) are swept away towards the positive electrode and holes, which are relatively immobile, are trapped or they recombine with electrons[47,48]. The result is that a negative charge is built up at the metal and a positive charge in the oxide near the interface, when positive bias is applied to the metal. In the later studies these holes were found to have non zero mobilities[49-52]. Another effect observed is the increase in density of surface states[53,54]. The radiation induced charges cause shift in C-V characteristics of MOS capacitors. The main disadvantage of this effect is that the MOS devices could not be used for applications, such as space

flights, where radiations would be an important factor.

The study made by Zaininger[55] and Grove and Snow[48] showed that a greater effect is observed with positive bias, in comparison to negative bias, during irradiation. They also found that the saturation is attained sooner, if the dose level is increased, however, this saturation is higher in value for higher gate biases. Aitken et al[56] irradiated devices with positive and negative biases applied to the metal. Their observation was that under positive bias the space charge was within 50 Å of the Si-SiO_2 interface, while it was within 50 Å of the Al-SiO_2 interface for negative bias.

Hughes et al[50] worked on MOS devices irradiated by x-rays and oxides grown by wet, dry and ion implantation methods. They observed that the mobility of holes depends very strongly on the oxide preparation method. In case of dry oxides, the hole mobility was found to be much higher as compared to the wet oxides case. It was also found to be strongly dependant on temperature (at liquid nitrogen temperature no hole motion was detected). They explained the low temperature charging of the device due to bulk trapped holes, whereas the room temperature charging was dominated by trapping close to the Si-SiO_2 interface.

Srour et al[51] studied the radiation tolerance of devices at room temperature and at 77°K. They observed that

the oxides exhibiting the radiation tolerance at room temperature, show large amount of radiation induced charges at low temperature. They also showed that this problem can be reduced to a great extent, by using ion implanted oxide or by applying high field to the oxide during irradiation.

A number of authors (e.g. , Grunthaner and Maserjian[57], Winokur et al[58], etc.) found that changes in the interface state density and oxide charge, as a result of irradiation, depend strongly on the method of fabrication of the device. Winokur et al[58] found that the increase of surface state density was much more for wet oxides, as compared to that for dry oxides. Revesz[59] observed that hydrogen, which was the most common impurity in $Si-SiO_2$ structure, had a strong effect on the defect production, which in turn affects the density of surface states. Revesz[60] and Sah[61] studied the chemical reaction taking place at the $Si-SiO_2$ surface after irradiation and found that the presence of OH^- and H has a strong effect on the interface state density. According to Sah[61] a large number of trivalent silicon atoms are present at the interface due to the deficiency of oxygen. These trivalent silicon bonds get neutralized by forming Si-OH bonds when the oxide is exposed to a wet ambient. When the ionizing radiation falls on the device, the Si-OH bonds are broken and the OH^- ions are drifted away to the positive electrode and the space charge builds up.

The flat band voltage shift, after irradiating the device, was found to depend not only on the fabrication ~~to~~ process of the device[52,62], but also on the thickness of oxide layer. EerNisse and Derbenwick[63] observed that the charge build up was proportional to oxide thickness squared (d_{ox}^2) or the flat band shift (ΔV_{FB}) was proportional to d_{ox}^3. Vishwanathan and Maserjian[64] proposed a model for the thickness dependence of radiation charging in MOS. This model shows that ΔV_{FB} depends on the thickness of oxide in a manner, in which the square and cube dependences are the limiting cases. According to them, when $d_{ox} \gg \lambda$, (λ being the average distance from a trap, within which holes should be generated to fill up the trap), $\Delta V_{FB} \propto d_{ox}^2$ and when $d_{ox} \ll \lambda$, $\Delta V_{FB} \propto d_{ox}^3$.

The radiation sensitivity of the devices was also found to depend strongly on the metal as well as the semiconductor substrate. Lindmayer[65] is of the opinion that interaction of certain dopants with host atoms appear to affect the radiation sensitivity. Peel et al[66] reported that the radiation sensitivity of the contamination in the silicon film affects the stability of the device. Lindmayer[65] studied the effect of different metals, viz., Al, Mo and Cr, on the stability and found that Cr is the best of the three. Phillips[67] also compared Cr and Al as gate metals for MOS

structure and observed that radiation hardness shown by Cr was more than that shown by Al, by a factor of 25. Another advantage found with Cr was that the induced surface state density was found to be less[67,68].

The results of the present experimental study made on MOS devices are contained in the following two chapters. In chapter III, the effect of trichloroethylene concentration, during oxidation, on the oxide charge, interface state density and sodium ion neutralization is studied and in chapter IV, the results of the variation of radiation induced charge with different gate metals, energy of radiation and gate bias applied during irradiation are presented.

REFERENCES

(Chapter- II)

1. M.M. Atalla, E. Tannenbaum and E.J. Schreibner, Bell Syst. Tech. J., 38, 749 (1959)
2. B.E. Deal and A.S. Grove, J. Appl. Phys., 36, 3770(1965)
3. J.T.Wallmark and H.Johnson (Editors) 'Field Effect Transistors', Prentice Hall, Inc. Englewood Cliffs, N.J.(1966)
4. A. Many, Y. Goldstein and N.B. Grover, 'Semiconductor Surfaces', North Holland Publishing Company, Amsterdam (1955)
5. A.R. Plummer, 'The Semiconductor-gas and Semiconductor-metal Systems', The Electrochemistry of Semiconductors, Ed. P.J. Holmes, Academic Press, London, New York (1962
6. A.S. Grove, 'Physics and Technology of Semiconductor Devices', John Wiley and Sons Inc., New York (1967)
7. E. Kooi, 'The Surface Properties of Oxidised Silicon', Philips Technical Library, Springer-Verlag, New York Inc. Netherlands (1967)
8. S.M. Sze, 'Physics of Semiconductor Devices', John Wiley and Sons, New York (1969)
9. L.M. Terman, Solid State Electronics, 5 , 285 (1962)
10. K. Lehovec, A Slobodskoy and J.L. Sprague, Phys. Stat. Solidi, 3 , 443 (1963)
11. K. H. Zaininger and G. Warfield, IEEE Trans. Electron Devices, ED-12 , 179 (1965)
12. A.S. Grove, B.E. Deal, E.H. Snow and C.T. Sah, Solid State Electronics, 8 , 145 (1965)

13. D.R. Lamb, Thin Solid Films, 5, 247 (1970)

14. A. G. Revesz and K.H. Zaininger, RCA Review, 29, 22 (1968)

15. C. N. Berglund, IEEE Trans Electron Devices, ED-13, 701 (1966)

16. E. H. Nicollian and A. Goetzberger, Bell Syst. Tech. J., 46, 1055 (1967)

17. P. V. Gray and D.M. Brown, Appl. Phys. Lett., 8, 31(1966)

18. B.E. Deal, M. Sklar, A.S. Grove, and E.H. Snow, J. Electro-chem. Soc., 114, 266 (1966)

19. P. V. Gray, Proc. IEEE, 57, 1543 (1969)

20. F. Montile and P. Balk, , J. Electrochem. Soc., 118, 1463 (1971)

21. D. R. Lamb and F.R. Badcock, Int. J. Electronics, 24, 11 (1968)

22. F.R. Badcock and D.R. Lamb, Int. J. Electronics, 24, 1(1968)

23. A.G. Revesz and K. H. Zaininger, IEEE Trans. Electron Devices, ED-13, 246 (1966)

24. A. Goetzberger and S.M. Sze, 'Applied Solid State Science', Vol. 1, p. 154-238, Academic Press, New York (1969)

25. H. Deuling, E. Klausmann and A. Goetzberger, Solid State Electronics, 15, 599 (1972)

26. P. Balk, Paper 109 Presented at the Electrochemical Soc. meeting, Sanfrancisco, California, May, 9-13 (1965)

27. M. V. Whelan, Philips Res. Reports Suppl. No. 6 (1970)

28. D.R. Kerr, J.S. Logan, P.J. Burkhardt and W.A. Pliskin, IBM Res. J., 8, 376 (1964)

29. E. H. Snow, A.S. Grove, B.E. Deal and C.T. Sah, J. Appl. Phys., 36 , 1664 (1965)

30. E.H. Snow, and B.E. Deal, Trans. Met. Soc. of AIME, 242 , 512 (1968)

31. S. R. Hofstein, IEEE Trans. Electron Devices, ED-13 , 222 (1966)

32. B.R. Singh, B.D. Tyagi, A. N. Chandorker and B.R. Marathe, Paper 42 presented at the Electrochemical Soc. meeting, San Fransisco, California, May 12-17 (1974)

33. J.E. Thomas and D.R. Young, IBM J. Res. Dev. 8 ,368 (1964)

34. E.S. Schleigel and G.L. Schnable, J. Electrochemical Soc., 119 , 165 (1972)

35. R. J. Kriegler, 'Semiconductor Silicon', page 363, Ed. by H.R. Huff and R.R. Burgess, (Princeton: Electrochemical Society) 1973

36. M. Severi and G. Soncini, Electronics Lett., 8, 402(1972)

37. E. A. Fogels and C.A. T. Salama, J. Electrochemical Soc., 118 , 2002 (1971)

38. G. Baccarni, M. Severi and G. Soncini, ibid, 170 , 1436 (1973)

39. S. Brojdo, J. V. Dalton, W. J. Polito and M. A. Waggner, paper 244 presented at the Electrochemical Soc. meeting, Miami Beach, Fla., Oct. 8-13 (1972)

40. R. J. Kriegler, Y. C. Cheng and D.R. Colton, J. Electrochem. Soc., 119 , 388 (1972)

41. E. J. Janssens and G. J. Deoklerck, ESSDERC Grenbole, Sept. 8-12 (1975)

42. R. J. Kriegler, Appl. Phys. Lett. 20 , 449 (1972)

43. R. J. Kriegler, A. Aitken and J. D. Morris, Suppl. J. Jpn. Soc. Appl. Phys., 43 , 341 (1974)

44. Y.J. Van der Meulen, C. M. Osburn and J. F. Ziegler, J. Electrochem. Soc., 120 , 308 (1973)

45. G. J. Declerck, T. Hattori, G.A. May, J. Beaudouin and J. D. Meindl, J. Electrochem. Soc., 122 , 436 (1975)

46. A. M. Goodman, Phys. Rev., 164 , 1145 (1967)

47. K. H. Zaininger, Appl. Phys. Lett., 8 , 140 (1966)

48. A. S. Grove and E. H. Snow, Proc. IEEE, 54 , 894 (1966)

49. R. J. Powel and G. F. Derbenwick, IEEE Trans. Nuclear Devices, NS-18, 99 (1971)

50. R. C. Hughes, E. P. EerNisse and H. J. Stein, ibid, NS-22 , 2227 (1975)

51. J. R. Srour, O.L. Curtis, Jr., and K.Y. Chiu, ibid, NS-21 , 73 (1974)

52. G. F. Derbenwick and B.L. Gregory, ibid, NS-22 , 2151 (1975)

53. J. R. Szedon and J. E. Sander , Appl. Phys. Lett., 6 , 181 (1965)

54. D. R. Collins and C.T. Sah, ibid, 8, 124 (1966)

55. K. H. Zaininger, IEEE Trans. Nuclear Devices, NS-13, 237 (1966)

56. J. M. Aitken, D. J. DiMaria and D. R. Young, ibid, NS-23 , 1526 (1976)

57. F. J. Grunthaner and J. Maserjian, ibid, NS-24 , 2108 (1977)

58. P.S. Winokur, H. E. Boesch, Jr., J.M. McGarrity and F.B. McLean, ibid, NS-24, 2113 (1977)

59. A. G. Revesz, ibid, NS-24, 2102 (1977)

60. A. G. Revesz, ibid, NS-18, 113 (1971)

61. C.T. Sah, ibid, NS-23 , 1563 (1976)

62. P. K. Aubuchon, ibid, NS-18 , 117 (1971)

63. E. P. EerNisse and G.F. Derbenwick, ibid, NS-23, 1534 (1976)

64. C.R. Vishwanathan and J. Masserjian, ibid, NS-23 , 1540 (1976)

65. J. Lindmayer, ibid, NS-18 , 91 (1971)

66. J. L. Peel, M. D. Barry and L. G. Green, ibid, NS-23 , 1594 (1976)

67. D. H. Phillips, ibid, NS-22 , 2190 (1975)

68. R.A. K jal and and D.K.Nicolas, ibid, NS-22, 2193 (1975)

****

Chapter - III

SURFACE PROPERTIES OF SILICON-TCE OXIDE SYSTEM

The successful fabrication of MOS devices requires adequate control of silicon-silicon dioxide interface properties as an essential condition. In early sixties, two major problems, one of high density of interface states and fixed oxide charges and the other of instability due to alkali ions (Na^+) associated with silicon-silicon dioxide interface, were realized. Continued efforts to overcome these problems led to the realization of two processes, namely, the phosphosilicate glass (PSG) stabilization and sealing of SiO_2 with Si_3N_4 layer. Each of these layers, acts as a barrier to sodium ion migration, resulting in improved stability. In both the cases, breakdown behaviour of the insulator is also improved, however, at a price of obtaining a polarizable PSG or an electrically somewhat unstable SiO_2- Si_3N_4 system.

Given such a situation, reports about the positive effects of oxidation of silicon in the presence of chlorine containing species (HCl, Cl_2), on various Si-SiO_2 interface properties and silicon substrate quality, seemed quite interesting. In most of the previous studies[1-5], HCl or Cl_2 was used as a chlorine source. The lack of safety and special installation requirements involved in the use of HCl, forced

people to look for safer chlorine sources, such as ,trichloroethylene (TCE), carbon tetrachloride (CCl_4) and 1.1.1 trichloroethane.

The present chapter deals with the results of investigations on the dependence of TCE concentration on the fixed oxide charge density and interface state density. This also includes the results on sodium ion neutralization and its correlation with the chlorine concentration in the gas phase during TCE oxide growth.

3.1 Device fabrication

The n-type silicon wafers of 4-6 ohm cm resistivity and of < 100 > orientation were used in the present investigation. These wafers were first cleaned in organic solution etched in HF , followed by thorough cleaning in deionized water. Further cleaning was done in 1: 1: 5 mixture of H_2O_2 : NH_4OH : H_2O and H_2O_2 : HCl : H_2O.

The wafers were oxidized at 1100 °C with varying TCE concentration in the gas phase, from 0.1 - 1.0 % TCE/O_2 The TCE was added to the oxygen ambient by flowing a controlled amount of N_2 through a quartz bubbler maintained at 35 ± 0.5 °C. Devices for oxide charge and interface state density studies, were annealed in situ in N_2 ambient for 30 min. Aluminium dots were evaporated on the oxidised surface through a metal mask, in a vacuum system maintained

at 10^{-6} Torr. Before aluminium evaporation, backside oxide is stripped in buffered HF. The backside metallization is followed by a low temperature annealing for 30 min. at $500^{\circ}C$ in forming gas.

In view to establish a close correlation between chlorine concentration in the gas phase and sodium ion neutralization, the devices for this study were not annealed in N_2 ambient. This is because chlorine may come out during annealing and the correlation between the two may not be justified. Oxidised samples were intentionally contaminated in a 1×10^{-5} N solution of NaOH in an ultrasonic vibrator, for about 5 min. at room temperature. No sintering of aluminium contacts was done on the devices used for sodium ion neutralization, which resulted in a bit higher oxide charge density. The C-V measurement was done with the help of LCR Bridge Type 921 made by Systronics, which was operated at frequency 10 KHz and measurements were done with variable dc bias applied internally to the device. In order to determine the contamination level, Bias Temperature Stress (B.T. Stress) test ($200^{\circ}C$, 10^{6}V/cms, 25 min.) was conducted on uncontaminated dry grown oxide. This showed a slight shift of 0.2 volt in C-V characteristic , indicating no mobile charge. It is unlikely that this shift is due to mobile sodium ions and could be due to high temperature effects.

Dry grown oxides contaminated simultaneously showed contamination level of 3×10^{12} sodium ions/cm^2.

3.2 Evaluation techniques

3.2(a) Determination of fixed oxide charge density

The capacitance voltage technique has proved very useful in studying the properties of oxidised silicon surfaces. It provides a fast, sensitive and easily interpretable technique.

As discussed in the last chapter, the silicon-silicon dioxide interface is always charecterised by a positive charge and it results in a parallel translation of the C-V characteristics of MOS devices along the voltage axis, towards negative voltages. The determination of fixed oxide charge density (Q_{ox}) would require the knowledge of theoretical ideal C-V characteristics, which has been calculated taking all the device parameters, like oxide thickness, substrate doping concentration, into consideration. The details of the calculation are discussed in the previous chapter. The oxide charge density has been calculated using the following relation

$$\Delta V = \frac{Q_{ox}}{C_{ox}} - \varphi'_{ms} \quad (3.1)$$

where ΔV is the shift along the voltage axis, C_{ox} is the oxide capacitance and ϕ'_{ms} is the metal to semiconductor work function difference.

3.2(b) Determination of interface state density

The determination of interface state density has been done by 'temperature method', proposed by Gray and Brown[6] in 1966. This method is based on the principle that as the temperature is reduced, the Fermi level comes closer to the valence band edge. The surface states which were full with electrons and neutral at a temperature T_1, lose electrons when the temperature is lowered to T_2 and become positively charged. Hence, to achieve flat band condition, more negative voltage is applied. This change in the voltage is due to the charge in surface states, since the potential drop in the semiconductor is zero at both temperatures. Hence, the temperature is varied and the flat band condition is maintained by observing changes in the capacitance and adjusting the bias. The flat band voltage is then plotted as a function of temperature. This graph gives the surface states charge Q_{ss} as a function of surface potential.

As our interest was limited to compare the magnitude of interface state densities present in differently grown TCE oxides, rather than its distribution in the band gap, all the C-V measurement were taken at room temperature and

liquid nitrogen temperature. The flat band voltage monitored at both these temperatures gave us surface state density in a particular region (0.18 eV away from the conduction band) of the forbidden gap. However, the distribution of surface states in the forbidden gap could be calculated using the following relation.

$$N_{ss} = \frac{1}{e} \frac{d\, Q_{ss}}{d\, \varphi_{s}} \qquad (3.2)$$

3.2(c) Technique for Na^{+} neutralization study

In order to study the migration kinetics of sodium ions and its effect on $Si-SiO_2$ interface properties, B.T. stress technique was employed. The devices were polarized by applying a positive field of the order of 10^6 V/cm at 200°C , for about 25 min. (sufficient to attain saturation). After having kept the devices under this stress condition, they were cooled rapidly to room temperature with the bias still applied. The C-V characteristic was measured at room temperature without appreciably disturbing the system. The negative shift of the C-V characteristic along the voltage axis , as compared to the initial one, would be indicative of the amount of charge induced in silicon due to migration of alkali ions and its density could be calculated using the following relation.

$$\Delta V = \frac{Q_{ox}}{C_{ox}} - \varphi'_{ms} \qquad (3.3)$$

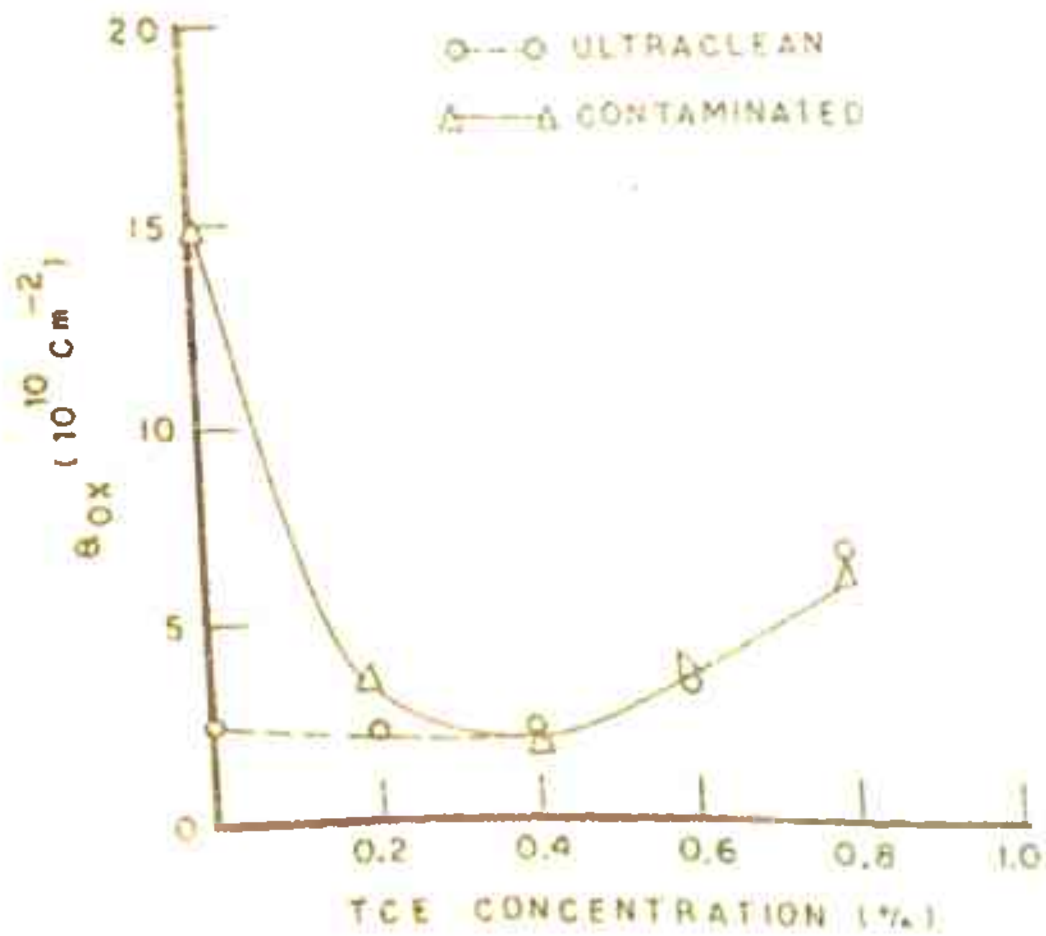


FIG. 3.1 DEPENDENCE OF TCE OXIDE CHARGE ON TCE CONCENTRATION.

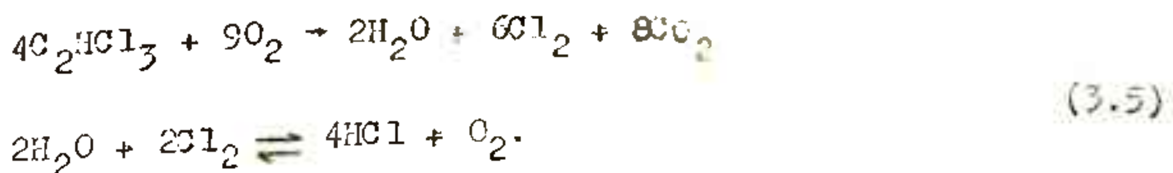
In view to study the sodium ion neutralization in TCE oxides, a term passivation (P) is defined as follows:-.

$$P = \frac{(N_{mob} - N)}{N_{mob}} \qquad (3.4)$$

where N_{mob} is the mobile sodium ion concentration per square centimeter, i.e., N_{mob}; and N is the number of unneutralized sodium ions.

3.3 Chemistry of the chlorine process

To interpret the effect of chlorine and its compounds on the oxidation kinetics or $Si-SiO_2$ interface properties, it is essential to know the gas phase composition of the reaction products. TCE in the gas phase would atleast partially react with O_2 to form Cl_2 and H_2O and follow the reaction



$$4C_2HCl_3 + 9O_2 \rightarrow 2H_2O + 6Cl_2 + 8CO_2$$

$$2H_2O + 2Cl_2 \rightleftharpoons 4HCl + O_2. \qquad (3.5)$$

Thermodynamic calculations show that at 1100°C the above reaction would yield for 1 % TCE/O_2 ambient approximately the same amount of Cl_2, 0.95 % HCl and 0.05 % H_2O. At lower temperatures somewhat more H_2O is formed.

3.4 Results and discussions

It is clear from Fig. 3.1 that TCE oxides do not show any significant reduction in the oxide charge density,

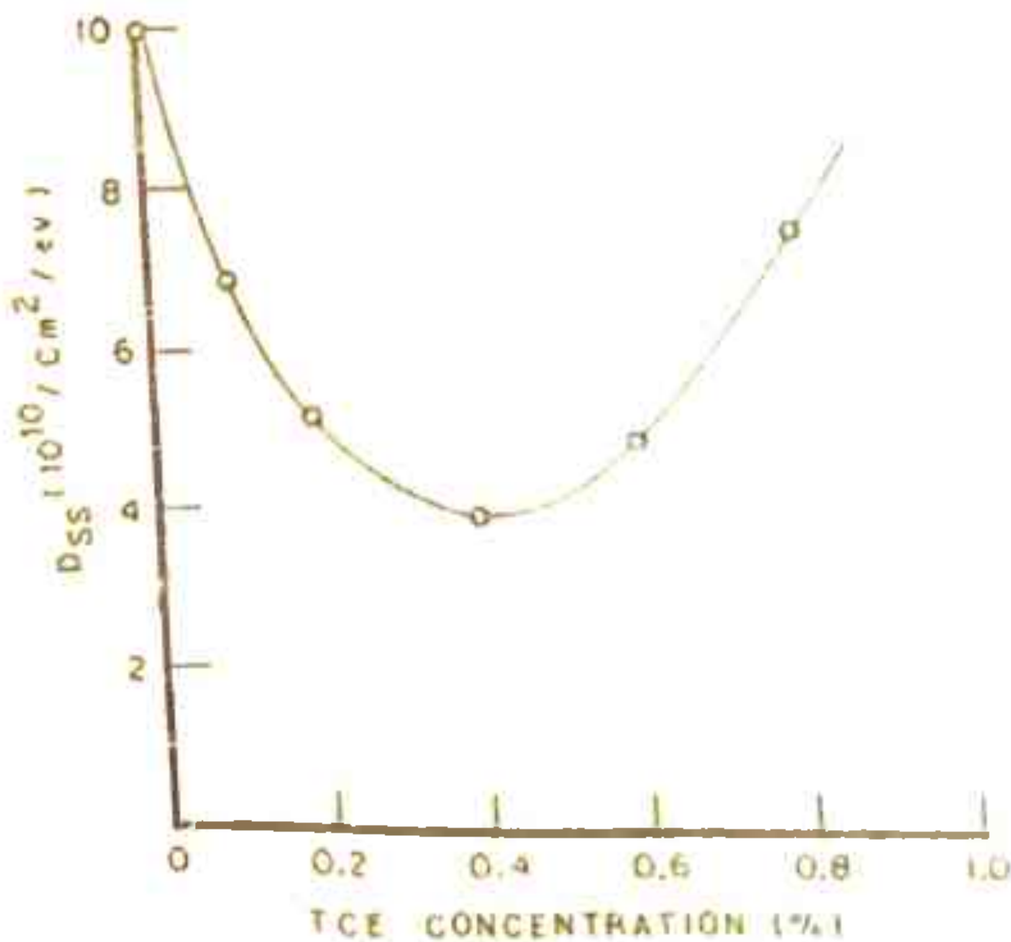


FIG. 3.2 EFFECT OF TCE CONCENTRATION ON THE DENSITY OF SURFACE STATES.

compared to the dry oxides grown in ultra-clean growth and proper annealing condition. However, it is true that TCE oxidation has positive effect if the growth condition is not ideal (contaminated) . As indicated in Fig. 3.1, devices fabricated in non ideal growth conditions, using TCE as a chlorine source, showed appreciable decrease in fixed oxide charge density, upto 0.4 - 0.5 % TCE concentration, compared to dry oxides grown in the same furnace. For the devices grown in clean growth and annealing conditions, almost the same small value of charge density was observed upto 0.5 % TCE. Further increase in TCE concentration resulted in increase of charge density.

Fig. 3.2 shows the dependence of interface state density with varying TCE concentration in the gas phase during the growth. A significant reduction from 1×10^{11} states per cm^2 per eV to 4.2×10^{10} states per cm^2 per eV in state density could be seen for 0.4 % TCE, compared to dry oxides grown in ideal conditions. Similar to the oxide charge behaviour, interface state density also increases for higher TCE concentration (> 0.4 % TCE) in the gas phase. Similar observation was made by Declarck et al[7,8].

It is clear from the above mentioned results that TCE oxidation carried out in ultraclean growth and annealing conditions, reduces the interface state density considerably

without affecting the fixed oxide charge density, atleast upto TCE concentration of 0.5 % in the gas phase. This shows the effectiveness of TCE oxidation process particularly in reducing the interface state density under ideal growth conditions. However, it has positive effect on both the parameters, if the growth conditions are not ideal. Similar dependences have also been observed in oxides grown in HCl and Cl_2 as chlorine sources[9-12].

The origins of interface states and oxide charge are different. Whereas the oxide charge is fixed, interaction of interface states with silicon depends on the position of the Fermi level at the surface, within the forbidden gap. It is well established that unsaturated bonds at the surface, i.e., disorder at the interface, is mainly responsible for the interface states. The states situated outside the silicon forbidden gap, like excess silicon ions and oxygen deficiency, are known to be the source of oxide charge density. It is , thus, obvious that the physical origin of all the charges may well be based upon the factors related to the silicon bond structure or defects there of . Whether a particular oxide growth process causes a silicon bond defect, depends on the structural configuration, bond energy and other considrations. Whether the defects in silicon bonds in turn will result in either fixed oxide charge density

(Q_{ox}) or interface state density (D_{ss}) would depend primarily upon its location in the oxidized silicon structures. Here, the possible effect of metallic and /or ionic impurities and defects on both the parameters could not be denied. The presence of these species could physically distort the silicon oxygen bond structure and lead to charge effects.

Our observation of the reduced interface state density with TCE upto 0.5 % during oxidation could be attributed to the pairing of unsaturated silicon bonds with active hydrogen or OH^- groups produced during high temperature TCE oxidation[9,11,13,14]. Most probably these active species of hydrogen are produced due to the availability of water produced during TCE oxidation as a product of the reaction[15] given by eq. (3.5). The observed reduction in interface state density could also be partly due to the gettering of the chemical impurities[16].

The observed increase in both, interface state density and oxide charge density, for the devices grown under high (> 0.5 %) TCE concentrations (Figs. 3.1 and 3.2) could be ascribed to the etching of silicon surface due to high chlorine concentration present during oxide growth[3,17,18]. This phenomenon causes the presence of excess ionic silicon in the oxide very near the $Si-SiO_2$ interface resulting in the

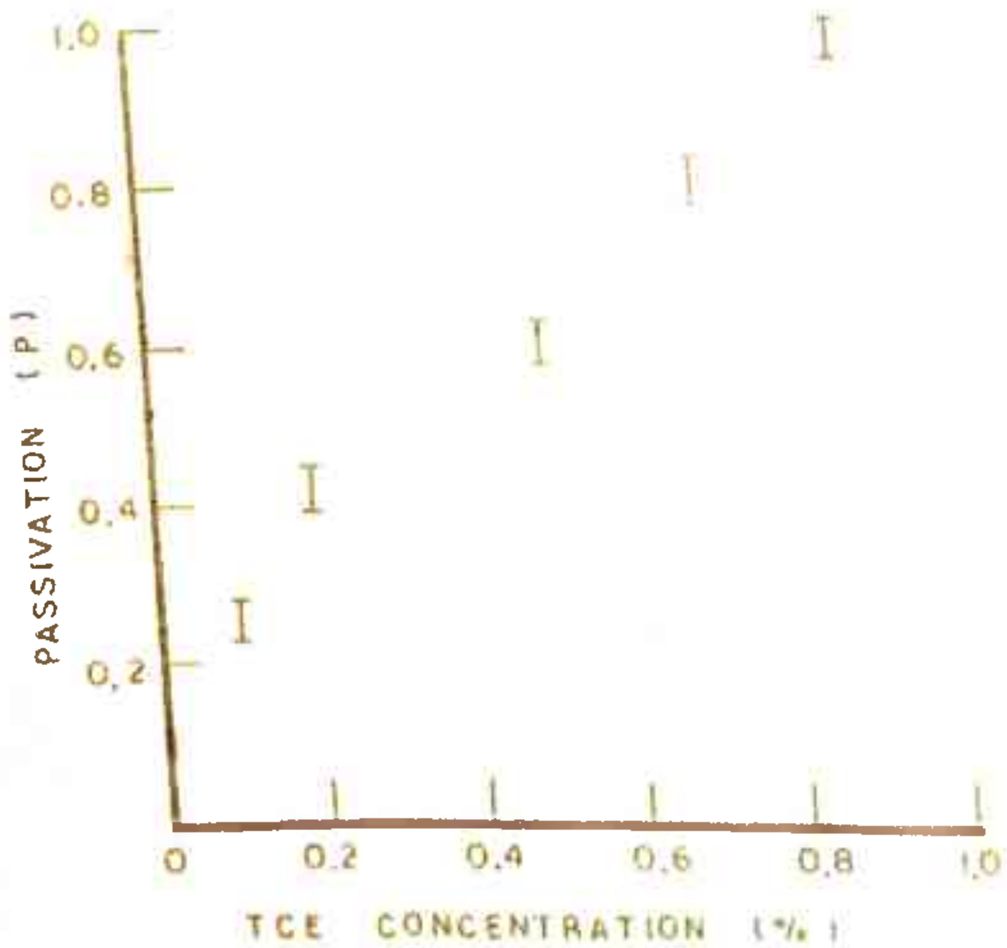


FIG. 3.3 EFFECT OF TCE CONCENTRATION ON THE FRACTION OF THE NEUTRALIZED SODIUM IONS.

increased values of oxide charge density. This view is also supported by the recent findings[1,20] that the chlorine produced as a product of reaction during TCE oxidation especially at this temperature and concentration play a dominant role on the oxidation kinetics. The increase in surface state density at high TCE concentration may be related to less water generation which may come out once the equilibrium has been disturbed by the reaction at the interface[19]. Here the surface roughness caused by relatively high chlorine concentration during growth may create defects at the Si-SiO_2 interface resulting in the interface state density.

<u>Na^+ neutralization</u> : It is now well established that apart from the cleaning effect (removal of impurities present in the furnace by purging the furnace in chlorine ambient), chlorine oxides show positive improvement even if the ionic contamination occurred after oxidation. This is believed to be mainly due to the neutralization of Na^+ ions after interacting with chlorine present in large amount at the Si-SiO_2 interface of chlorine oxidation.

Fig. 3.3 shows the results of BT stress on Na^+ neutralization (defined as the fraction of the Na^+ which got neutralized). Nearly complete neutralization of Na^+ ions in our case (3×10^{12} Na^+/cm^2) takes place for the

TCE concentration of 0.9 % at 1100°C. Data for HCl oxides[17,18,21,22,23] and some reported results on TCE oxides[7], lead to similar chlorine concentration[7,17,18,21,22,23].

In HCl oxides, it is observed that Na^+ neutralization takes place suddenly in a narrow range of HCL concentration, between 3 - 4 % , for the devices having Na^+ contamination level of the order of 10^{12} ions/cm^2. This is indicative of the fact that Na^+ neutralization is achieved once a certain minimum level of chlorine is incorporated in SiO_2 film. However, exact mechanism of this threshold behaviour is still a matter of discussion. Contradictory results are available on the dependence of Na^+ contamination level on the passivation efficiency. Whereas Kriegler et al[17] are of the opinion that it is independant of contamination level upto a value of 4×10^{12} ions/cm^2 , Van der Meulen et al[24] observed that only one third of the Na^+ ions are neutralized. Results on the TCE oxide indicate that this phenomenon is not very effective at high level of the contamination[16]. Our results of TCE oxides show that complete neutralization of Na^+ ions (3×10^{12} ions/cm^2) could be achieved by growing oxides at TCE concentration of 0.9 % at 1100°C. However, a threshold effect could not be distinguished in our data (Fig. 3.3).

3.5 Conclusion

The present study shows that one order reduction in interface state density could be easily achieved by 0.3-0.4 % TCE during TCE oxidation. The fixed oxide charge density is not very much affected by this process under clean growth conditions. However, this process has beneficial effects on this parameter (Q_{ox}), if growth condition is not ideal. The large chlorine conception near the $Si-SiO_2$ interface is effective in passivating against Na^+ ion drift.

REFERENCES

(Chapter - III)

1. R.J. Kriegler, Y. C. Cheng and D.R. Colton, J.Electrochemical Soc., 119 , 388 (1972)

2. Y.J. Van der Meulen and J. G. Cahill, J. Electron. Mat., 3 , 371 (1974)

3. K. Hirabayashi and J. Iwamura, J. Electrochemical Soc., 120 , 1595 (1973)

4. D.W. Hess and B.E. Deal, Paper 323 , Electrochemical Soc. meeting, Las Vegas, Oct. 17-22, (1976)

5. K. Hirabayashi and J. Iwamura, International Conference on Solid State Devices, Tokyo, August 29-31 (1973)

6. F.V. Gray and D. M. Brown, Appl. Phys. Lett. 8 , 31(1966)

7. G. J. Declerck, T. Hattori, G.A. May, J. Beaudouin and J. D. Meindl, J. Electrochemical Soc., 122, 436 (1975)

8. D. M. Heald, R. M. Das and R.P. Khosla, J. Electrochemical Soc., 122 , 302 (1975)

9. M. Severi and G. Soncini, Electron. Lett., 8,402(1972)

10. E.A. Fogels and C.A.T. Salama, J. Electrochemical Soc., 118 , 2002 (1971)

11. B.R. Singh, B.D. Tyagi, A.N. Chandorker and B.R. Marathe, Paper 42, Electrochemical Soc. meeting, San Fransisco, California, May 12-17 (1974)

12. G. Baccarni, M. Severi and G. Soncini, J. Electrochemical Soc., 120 , 1436 (1973)

13. E. Kooi, Philips Research Reports, 20 , 518 (1965)

14. F. Montillo and P. Balk, J. Electrochemical Soc., 118 , 1463 (1971)

15. B.R. Singh and P. Balk, J. Electrochemical Soc., 125, 453 (1978)

16. E.J. Janssens and G. J. Declerck, ESSDERC Grenbole, Sept. 8-12, (1975)

17. R. J. Kriegler, A. Aitken and J.D. Morris, Suppl. J. Jpn. Soc. Appl. Phys., 43 , 341 (1974)

18. R.J. Kriegler, 'Semiconductor Silicon 1973' Ed. H.R. Hoff and R.R. Burgers, Page 363, The Electrochemical Society Softbound Symposium Series, Princeton N.J.(1973)

19. B.R. Singh and P. Balk, Paper presented at 'Symposium on Electron Devices', CEERI, Pilani, Sept. 21-23 (1978)

20. W.M. Grubbs, M.B. Das, J. Stach and R.E. Tressler, Paper 325, Electrochemical Soc. meeting, Las Vegas, Nevada, Oct. 17-22 (1976)

21. R.J. Kriegler, Thin Solid Films, 13, 11 (1972)

22. R.J. Kriegler, Appl. Phys. Lett., 20, 449 (1972)

23. R.L. Meek, J. Electrochemical Soc., 120, 308 (1973)

24. Y.J. Van der Meulen, C.M.Osburn and J.F.Ziegler, J. Electrochemical Soc., 120, 308 (1973)

*****

Chapter-IV

EFFECT OF RADIATION ON MOS DEVICES

Early in the development of MOS transistors, it has been found by many workers that even low energy electrons, x-rays and gamma rays can have significant effects on $Si-SiO_2$ interface properties[1-9]. The two most important effects, which occur when MOS structures are exposed to ionising radiation environment, are : (i) the introduction of positive oxide charge and (ii) an increase in the fast interface state density at the $Si-SiO_2$ interface.

Fortunately, both these induced charges, which are permanent at room temperature, could be annealed out during low temperature annealing (300°C)[2,4,3,10]. The only disadvantage was that these devices could not be used for space applications, where ionising radiation would be a factor.

The ever increasing demand of semiconductor devices in space applications, because of their miniaturised size and low power, lead to extensive research activity in this area. Major efforts have been aimed towards understanding the mechanisms of the radiation induced space charge in oxides and getting this charge eliminated or minimized. Various modifications in device fabrication processes, uses of particular gate layers, compositions of oxide layer and effects of passivating layers have been suggested[11-13].

The present chapter deals with the effects of gate metals (Al, Cr, Au), oxide growth conditions and energy of x-ray radiations, on the charge formation in MOS structures . The C-V analysis technique has been used to study the charge formation.

4.1 Device fabrication

The n-type silicon crystals of 1 ohm cm resistivity and [100] orientation were used in the present investigation. The cleaning of the wafers was done in similar manner as described in the previous chapter. The cleaned wafers were oxidized at 1100°C, in dry oxygen and in dry/wet/dry oxygen ambients, separately. The thicknesses of these oxides were found to be 920 and 960 Angstroms, respectively, which were measured by Ellipsometer within an accuracy of ± 2 % . Before metal evaporation, backside oxide was etched in buffered HF. On the front side Al, Au and Cr dots of approximately 1 mm diameter, were evaporated through a metal mask, in vacuum system maintained at 10^{-6} Torr. Al was used for backside contact. The wafers were annealed in nitrogen atmosphere at 500°C for about 25 mins.

4.2 Measurement technique

The capacitance-voltage method of analysis has been used to study the radiation induced charge formation in MOS

devices. The C-V characteristics were measured using Systronics LCR bridge type 921, at an internal frequency of 10 KHz. The devices were exposed to x-rays with appropriate contacts on gate and substrate for biasing. For irradiation Rich Seifert x-ray unit was used, which can be run for accelerating voltages between 25 Kv to 60 Kv. After irradiation C-V characteristics were measured and by determining the shifts in the flat band voltage along the voltage axis, effects of different parameters, such as, gate bias during irradiation, x-ray energy and exposure time, on the radiation induced charge formation was studied. These studies were made with differently grown oxides and different gate metals. As the induced charge is observed to be quite permanent at room temperature, any time lapse during the measurements is not expected to change the density of radiation induced charge.

4.3 Determination of radiation induced charge

As discussed in chapter-II, the formation of positive space charge in the insulator, results in a displacement of MOS C-V curve to the left along the voltage axis. The nature of radiation induced space charge was determined with the help of shift along the voltage axis, as compared to the initial C-V characteristics (i.e., without irradiation). The induced charge has been calculated using the following relation.

$$\Delta V_{FB} = \frac{Q_s'}{C_o} - \varphi_{ms}' , \qquad (4.1)$$

where ΔV_{FB} is the flat band shift along the voltage axis, φ'_{ms} is the metal to semiconductor work function difference, Q'_{s} is the induced surface charge and C_o is the oxide capacitance.

4.4 Results

The C-V characteristics obtained after x-ray irradiation for different exposure times have been presented in this chapter. The initial C-V characteristics , without any exposure, are also shown. Considerable shifts along the voltage axis have been obtained, until after a few minutes of exposure, when more or less stable value is reached. It has been found that a relatively large shift is obtained during the initial exposure, at all gate biases. In addition, the magnitude of capacitance change (i.e., C/C_o) is also increased after irradiation, indicating the increased leakage in the devices due to irradiation.

The effect of exposure time and that of the bias applied to the gate during irradiation, are shown in Figs. 4.1 and 4.2. Fig. 4.3 shows the radiation induced charge, when the positive biases applied to the metal during irradiation were 2,4 and 6 volts. It is apparent from the figure that the induced charge first increases with exposure time and then saturates. The saturation time depends upon the gate voltage applied during irradiation. Rapid saturation of induced charges was obtained at higher positive bias applied during irradiation. As is clear

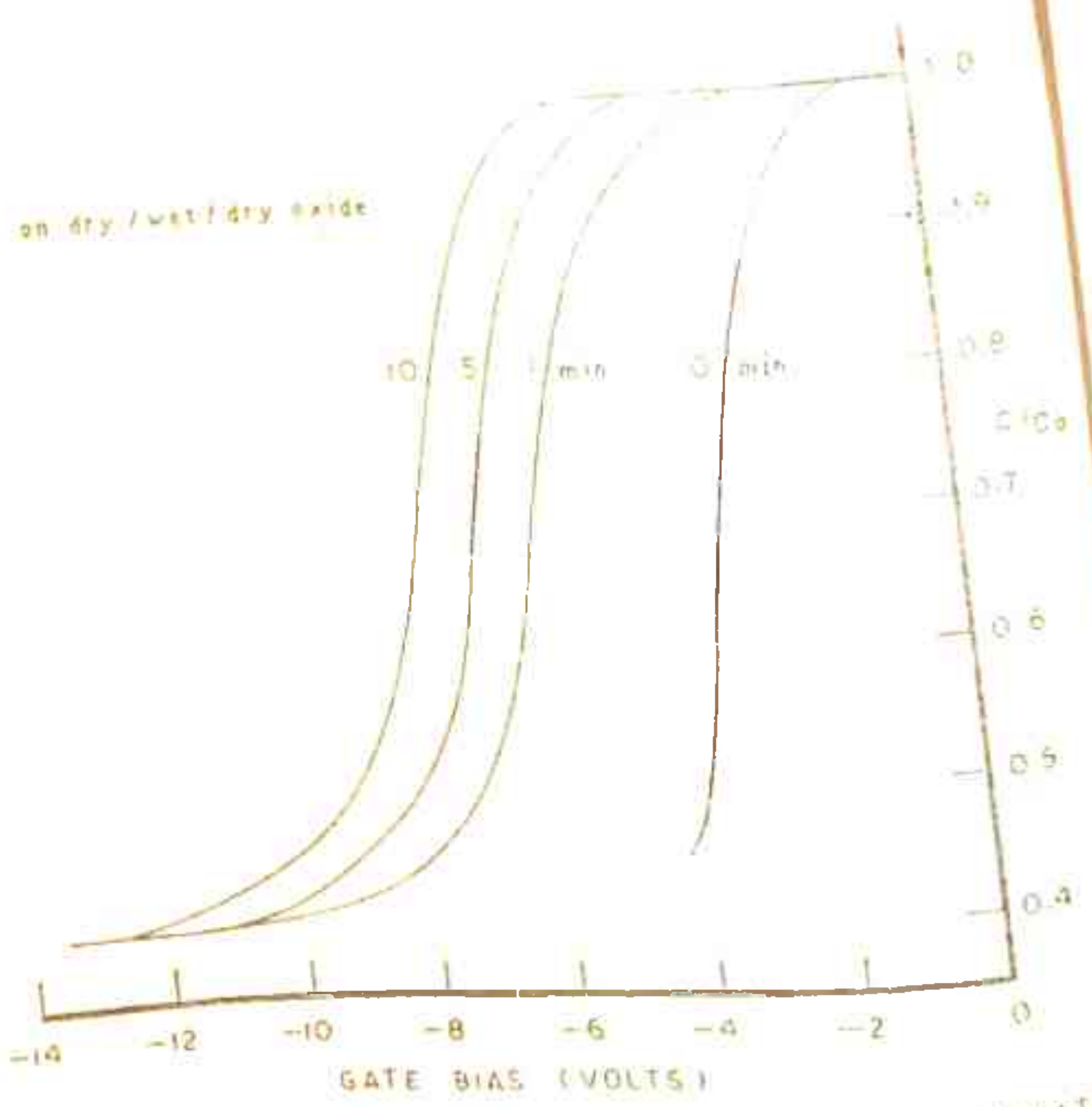


FIG. 4.1 C – V CHARACTERISTICS OF THE DEVICE IRRADIATED BY 32 KeV X – RAYS AT + 2 V GATE BIAS

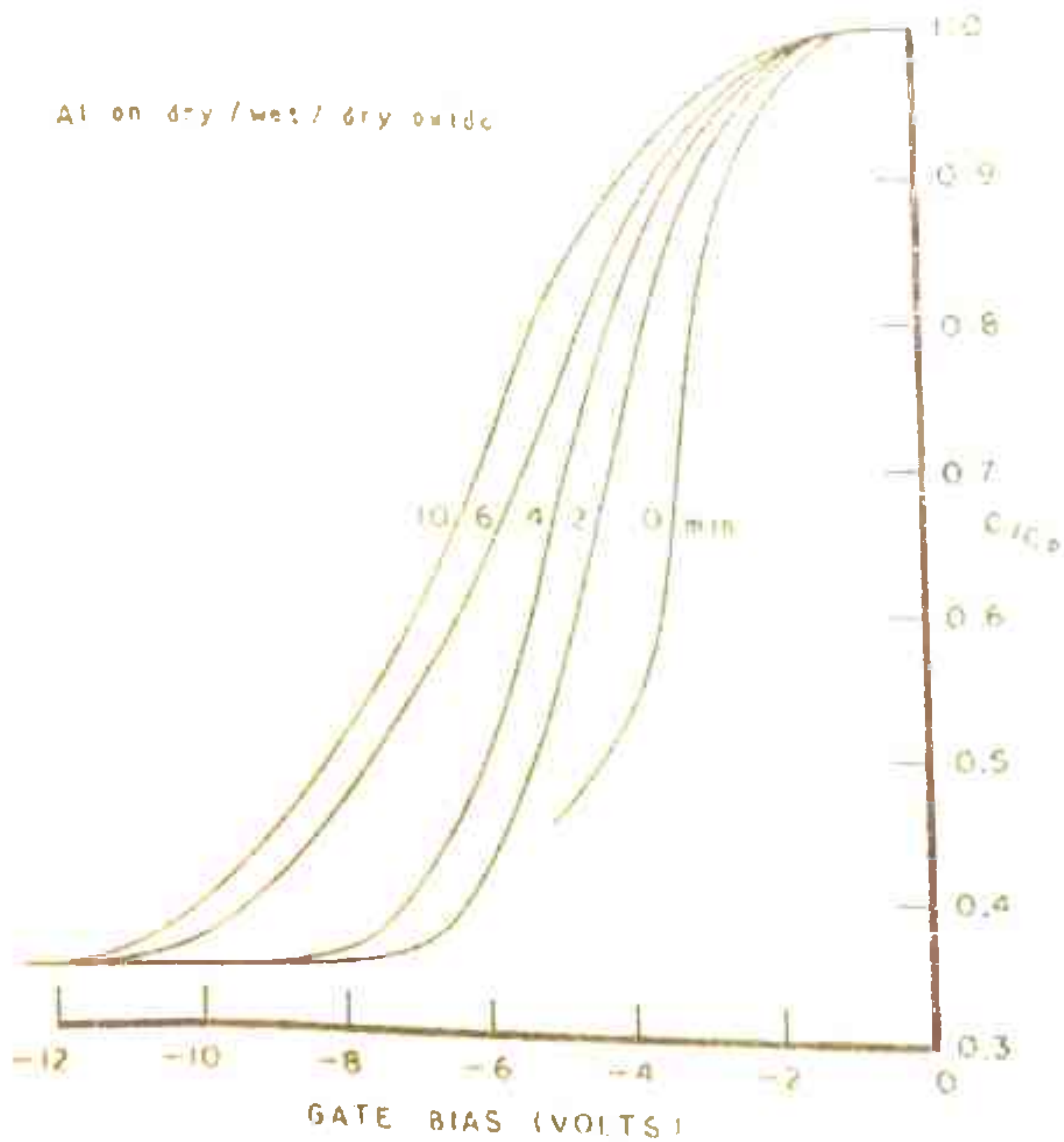


FIG. 4.2 C-V CHARACTERISTICS OF THE DEVICE IRRADIATED BY 32 K V X-RAYS AT +4 V GATE BIAS

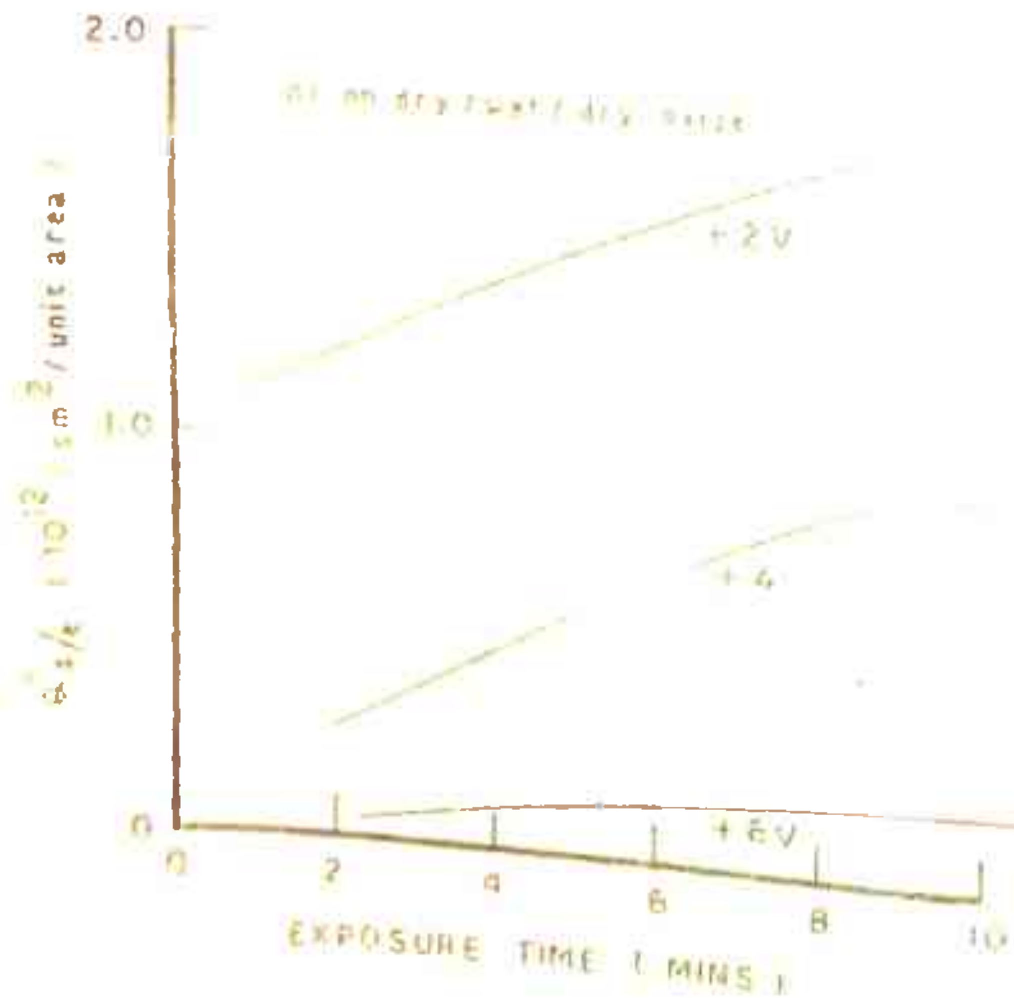


FIG. 4·3 INDUCED SURFACE CHARGE VS. TIME FOR DIFFERENT GATE BIASES DURING IRRADIATION

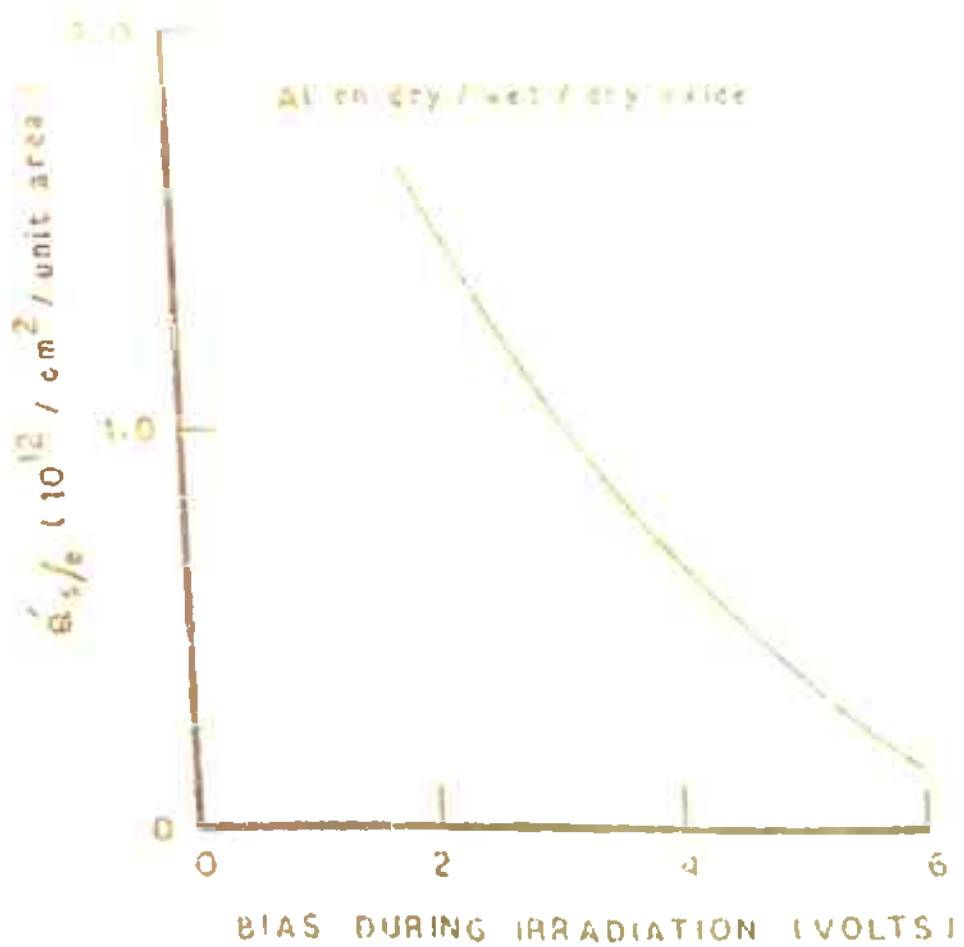


FIG. 4.4 INDUCED SURFACE CHARGE VS. GATE BIAS FOR 6 MINS. OF IRRADIATION

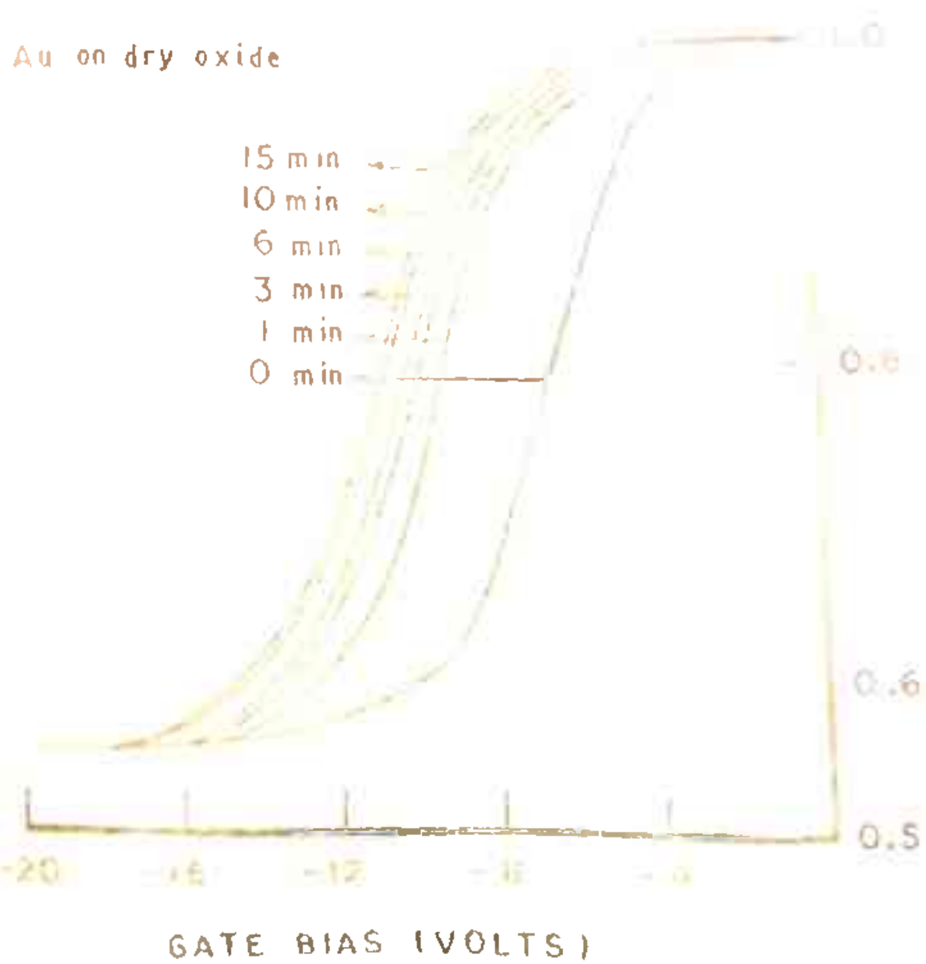


FIG. 4.5 C—V CHARACTERISTICS OF THE DEVICE IRRADIATED BY 32 KeV X-RAYS AT + 2 V GATE BIAS

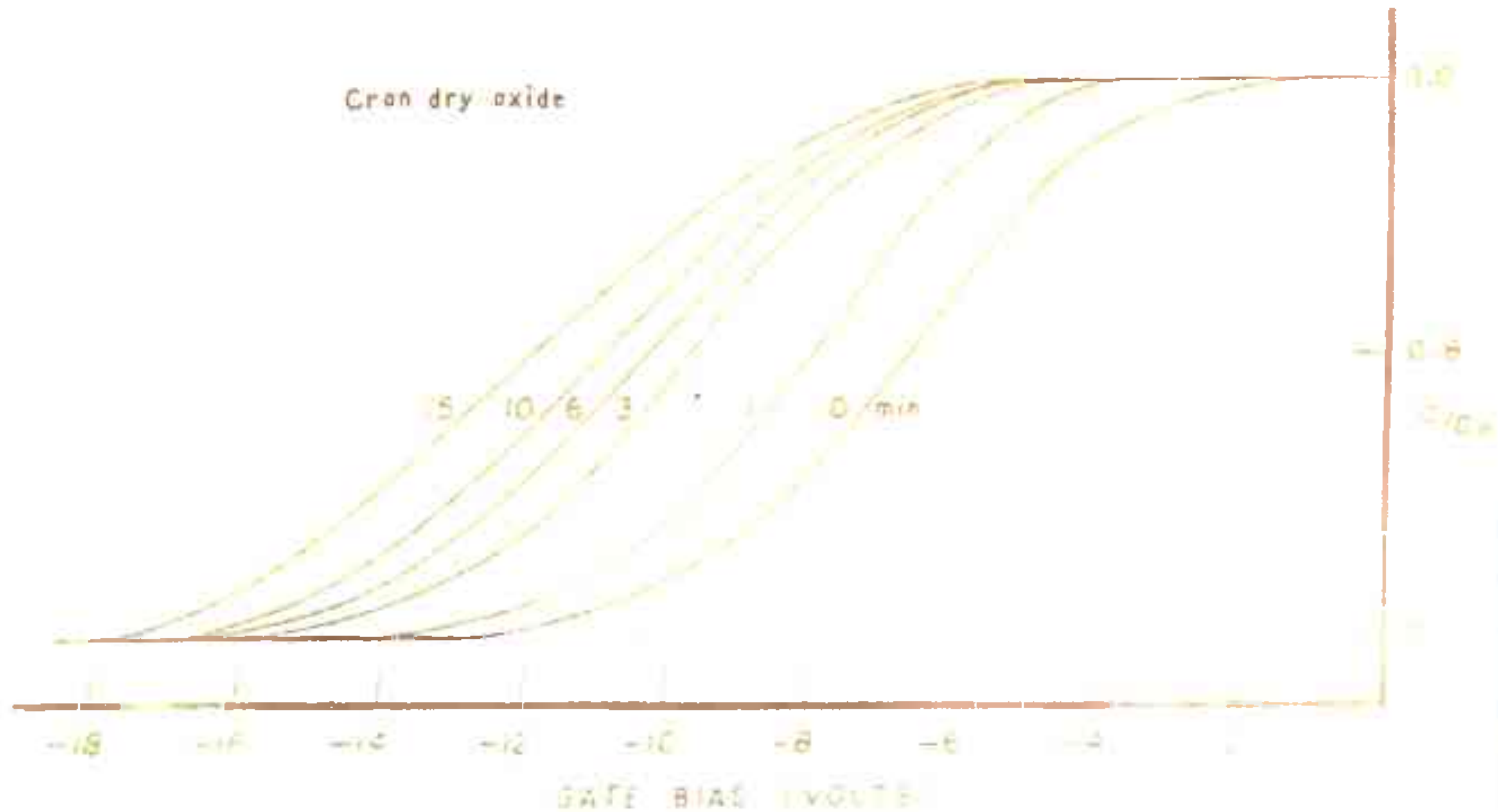


FIG. 4.6 C–V CHARACTERISTICS OF THE DEVICE IRRADIATED BY 32 KeV X–RAYS AT +2V GATE BIAS

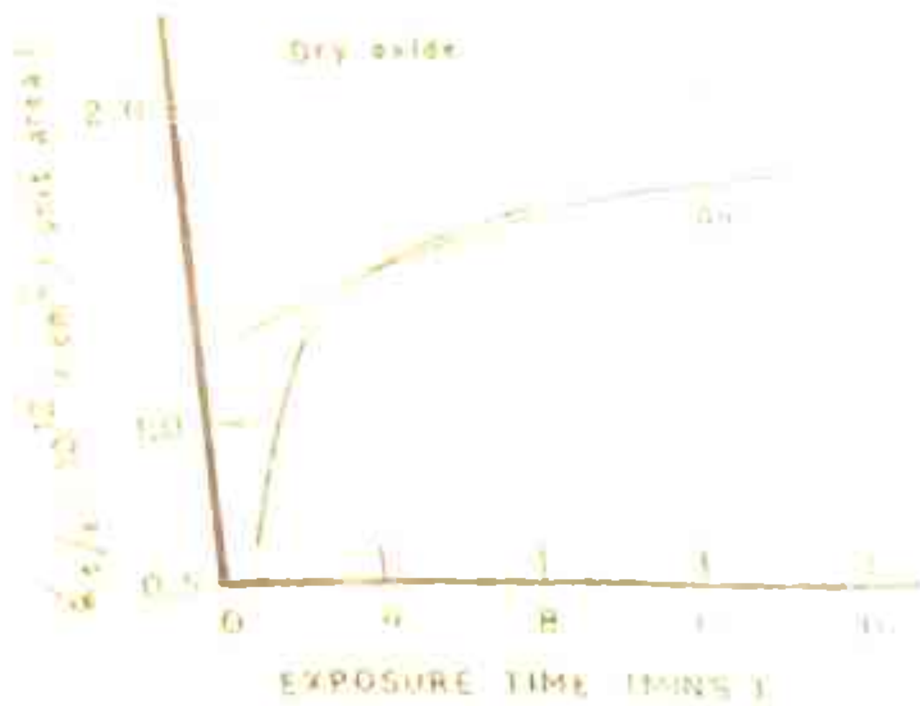


FIG. 4.7 INDUCED SURFACE CHARGE V.S. TIME FOR DIFFERENT GATE METALS

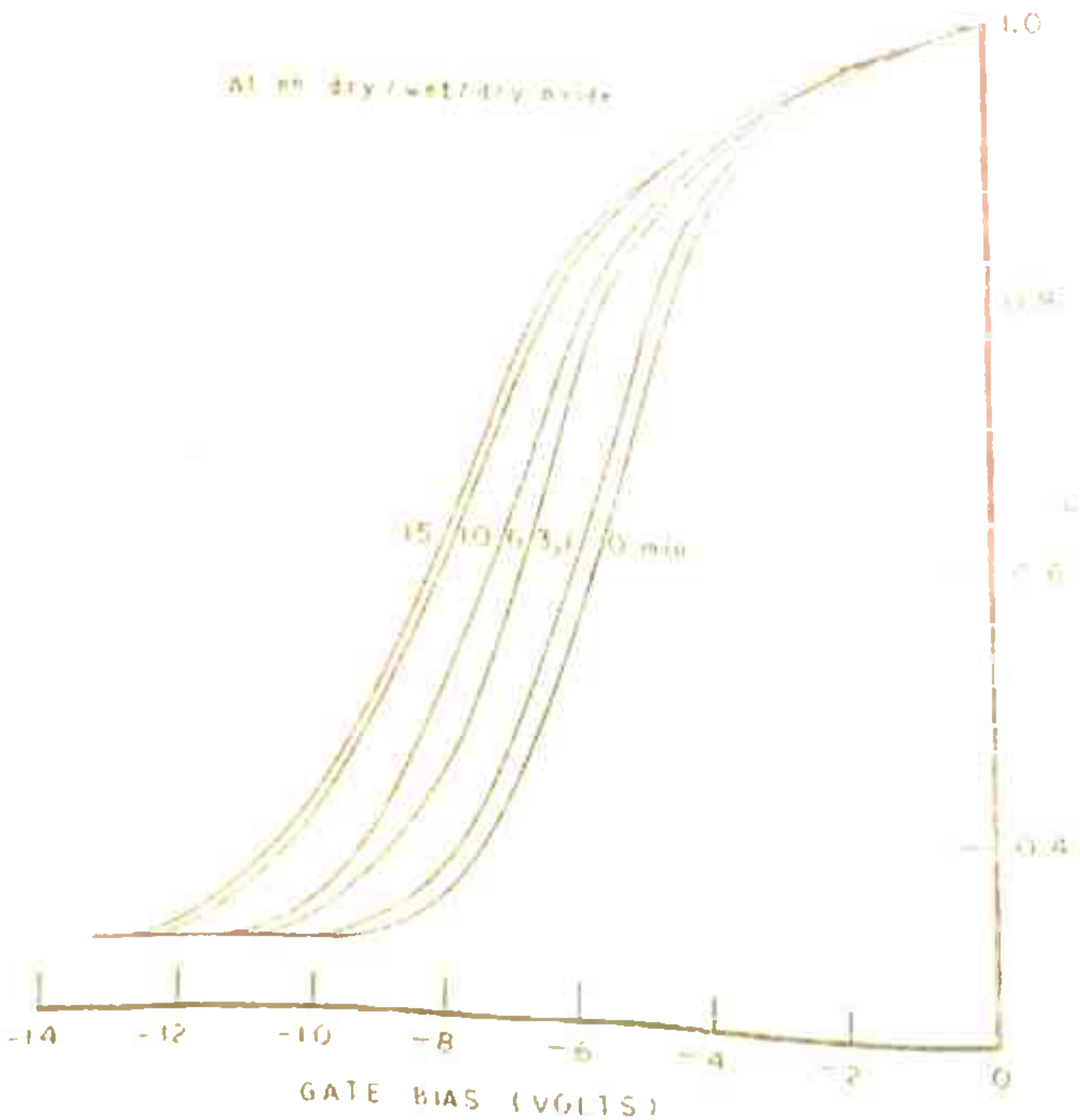


FIG. 4.8 C – V CHARACTERISTICS OF THE DEVICE IRRADIATED BY 39 KeV X – RAYS AT + 2 V GATE BIAS

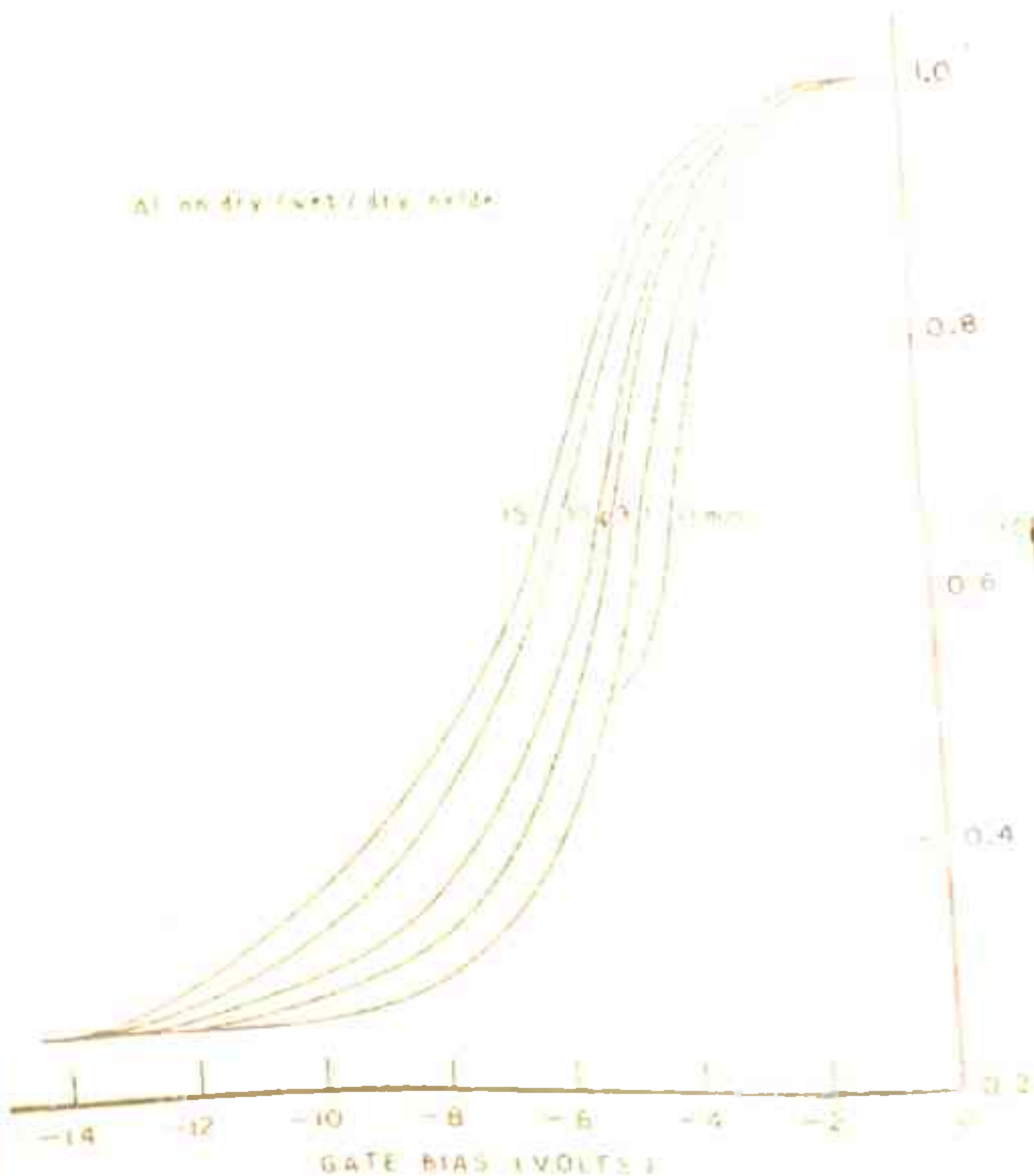


FIG. 4.9 C−V CHARACTERISTICS OF THE DEVICE IRRADIATED BY 46 KeV X−RAYS AT +2V GATE BIAS

FIG. 6.10 C-V

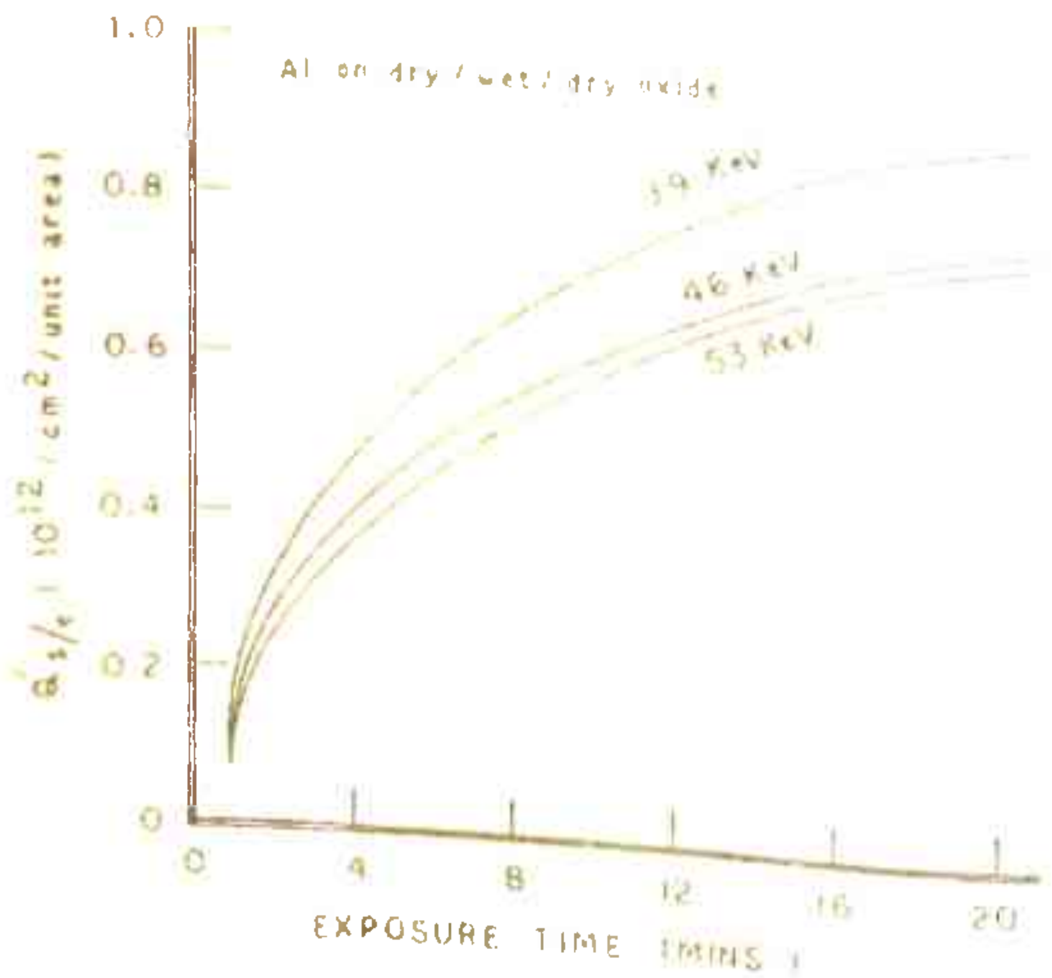


FIG. 4.11 INDUCED SURFACE CHARGE VS. TIME FOR DIFFERENT X-RAY ENERGIES

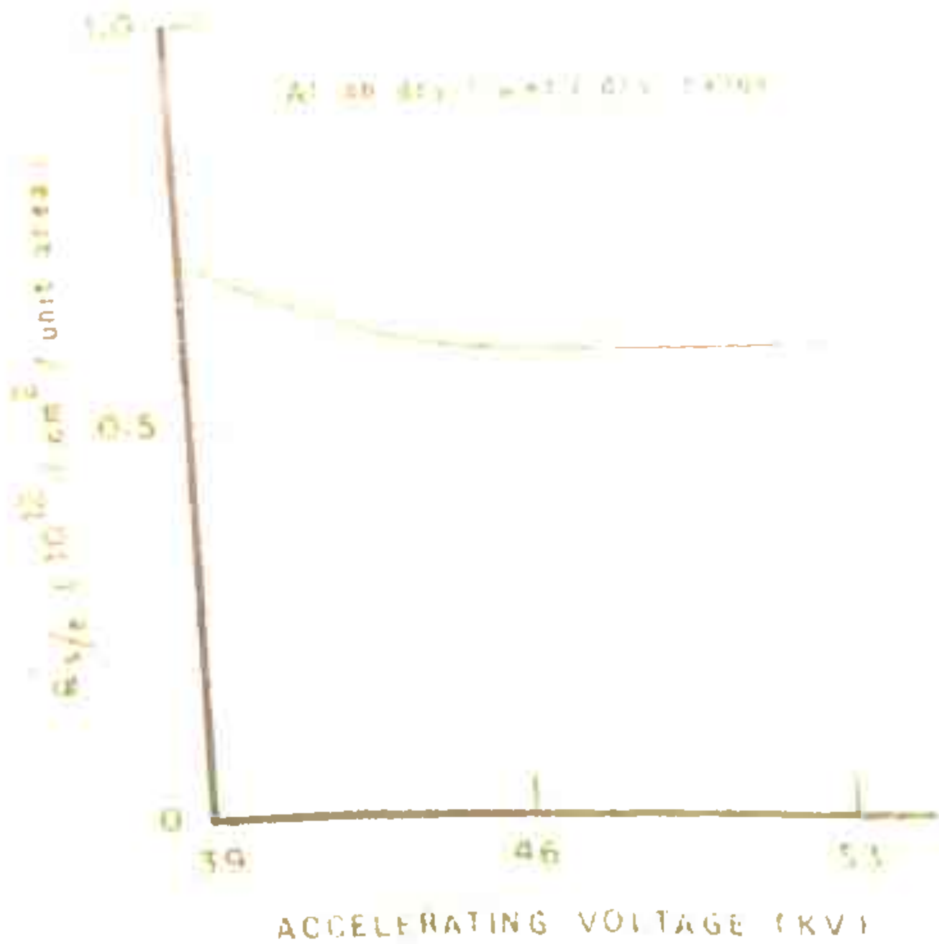


FIG. 4.12 INDUCED SURFACE CHARGE VS. ACCELERATING VOLTAGE FOR 10 MINS. OF IRRADIATION

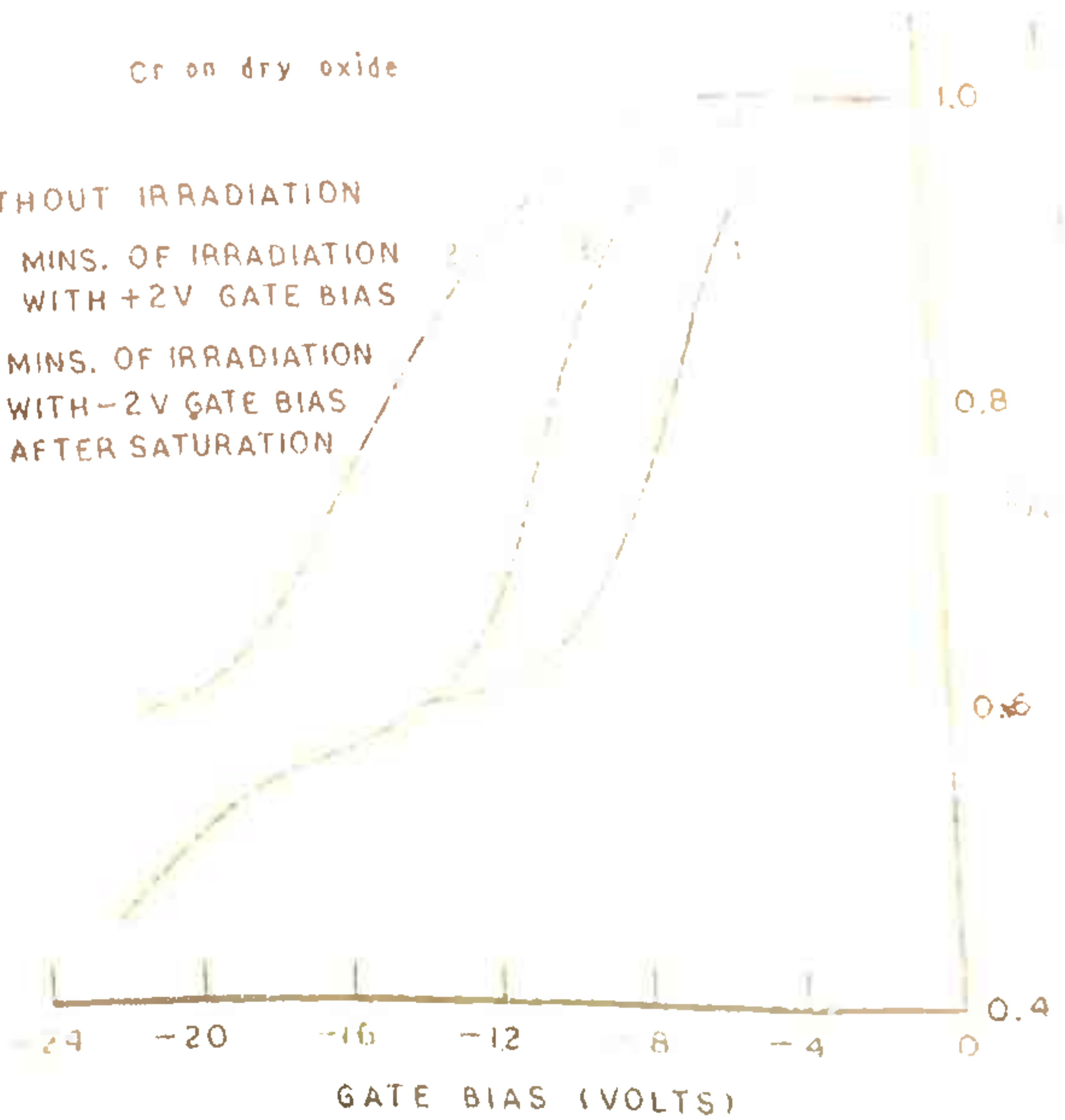


FIG. 4.13 C − V CHARACTERISTICS SHOWING PARTIAL RECOVERY

from Fig. 4.4, our devices showed decreasing value of induced charge with the increasing gate biases,for constant energy of radiation and exposure time.

In order to study the gate metal dependence on radiation induced charge, all other parameters, such as oxide layer, gate bias applied during irradiation and exposure time, were kept constant. The C-V characteristics obtained for Cr and Au layers on dry grown oxide, are illustrated in Figs. 4.5 and 4.6. The radiation induced charges, calculated for different metals, are plotted in Fig. 4.7. It is apparent from this figure that the chromium layer showed considerable radiation hardness during initial irradiation, as compared to gold layer. Whereas devices with gold layer showed systematic increase and saturation with increasing exposure time, chromium showed erratic behaviour and became even more radiation sensitive under prolonged exposure.

The MOS devices having dry/wet/dry oxide and Al as a gate metal , were irradiated by x-rays having different maximum energies, corresponding to the accelerating voltages of 39, 46 and 53 KV, for constant gate bias and exposure time. The radiation induced charges, calculated from the C-V curves (Figs. 4.8, 4.9 and 4.10), are plotted in Figs. 4.11 and 4.12. It is clear from these figures that the formation of radiation induced charge is independant of the radiation energy, at least

for dry/wet/dry oxide having Al as a metal layer.

The radiation induced charges could be annealed either by heating the devices or by irradiating them with ultraviolet light, x-rays or low energy electrons. In order to study the recovery phenomenon, the devices were first irradiated with 32 KeV x-rays for 25 minutes, which is sufficient for the devices to reach the saturation. The devices were then exposed to x-rays, with negative bias applied at the gate during irradiation. Most of our devices showed complete recovery and the C-V characteristics shifted back to the original one. Interestingly, some of the devices could not be completely recovered even after prolonged irradiation at negative biases (Fig. 4.13). In addition, the inversion region was also not observed in these devices.

4.5 Discussion

Before we discuss our experimental findings, it would be worthwhile to summarize the main features of these experimental observations.

(i) A positive space charge appears in the oxide layer, when MOS devices are exposed to ionizing radiation.

(ii) The radiation induced space charge gets saturated with prolonged irradiation. The saturation is rapid at higher positive biases applied during irradiation.

(iii) The magnitude of saturated radiation induced charge in the oxide depends strongly on the gate voltage applied during irradiation.

(iv) The building up of radiation induced charge is highly dependant on the gate metal. Chromium is observed to have more radiation hardness, as compared to gold for short exposures, but it showed greater sensitivity after prolonged exposures.

(v) The radiation induced charge is permanent at room temperature; however, it could be neutralized if the devices are heated or irradiated with UV or other ionizing radiations with negative bias applied at the gate.

Two schools of thoughts have developed for postulating a mechanism for the formation of radiation induced positive space charge. One model is based strictly on the consideration that ionising radiation beam interacts first with the gate and then with the insulator to form a cloud of electron-hole pairs within the insulator[1-9]. It is these pairs, which cause the observed effect by subsequently interacting with trapping sites within the insulating film. The electrons which have been generated due to radiation, either recombine with the holes or move out of the insulator because of the applied positive field, whereas the holes diffuse

in the insulator - some of them recombine with electrons, but many are captured into the stationary traps. This gives rise to the observed positive charge. The remaining holes, which are not trapped and have not recombined, are neutralized either at the metal electrode or with the electrons injected from the silicon. In the absence of electric field during irradiation, the electron-hole pairs recombine and relatively small number of holes will be trapped resulting in no significant accumulation of charge in the insulator. In the case of biased bombardment, the electrons readily move out of the insulator under the influence of the field and the trapping of holes is enhanced resulting in a significant positive space charge. The formation of space charge takes place at the $Si-SiO_2$ interface and moves into the insulator with continued bombardment, if the gate bias is held positive. Most of this charge is imaged in the semiconductor surface and therefore, the capacitance measurements show a shift along the voltage axis. During initial studies in the field, this model was widely supported and some modifications to this model, which included the electron injection through the metal layer, were also proposed.

The second model, which is based on recent studies, proposes that much of the radiation induced positive space charge is due to the ionic drift within the SiO_2 film[14-16].

It is postulated that ions, such as sodium and protons, are liberated during irradiation and they either diffuse or drift in the SiO_2 film. When these ions drift to the $Si-SiO_2$ interface, the flat band and threshold voltages are perturbed due to corresponding modifications in the electric field at the silicon surface. This results in the shift of C-V characteristics.

Our results on voltage dependence of radiation induced charge (Fig. 4.3), show that relatively less charge is being formed at higher voltages applied during irradiation. On the basis of the first model, one would expect that with the positive field applied on the gate during irradiation, more holes would be drifted towards the $Si-SiO_2$ interface and be trapped, resulting in high density of radiation induced charge. This is not reflected from our experimental data. Hughes et al[14] feel that the magnitude of radiation induced charge strongly depends on the growth conditions and hence, on the impurity contents of the oxide and the metallic layer. They also observed that Al layer after sintering diffused through the oxide and acted as a sodium getter. Devices sintered at higher temperature ($500^{o}C$) showed higher Na^+ concentration and hence, an enhanced radiation induced charge was observed. There seem to be atleast two reasons for our observed voltage dependence of the radiation induced charge. One is the non-uniformity of the sodium content in the oxide and the other,

the nonuniform diffusion of Al through the oxide. As discussed in chapter II, the sodium ions could be incorporated into the oxide during any or all device processing steps, resulting in nonuniformity of Na content and this could not be avoided due to our experimental limitations. Our devices were also sintered at 500°C and nonuniform diffusion of Al, which acts as a sodium getter, might also result in observed effect. B T stress was conducted to verify this nonuniformity, but no significant mobile Na^+ ion concentration was observed. It is believed that in our devices most of the sodium is bound by Coulomb forces to non bridging oxygen, thus behaves as immbobile neutral species when B T assesments are conducted. However, on irradiation the sodium ions are liberated and consequently, drift in the oxide due to applied field, resulting in radiation induced charge. Perhaps the migration of positively charged Na^+ ions is accelerated at higher positive bias and rapid saturation is observed in this case.

With regards to the dependence of radiation induced charge on the gate metal layers, it is clear from Fig. 4.7 that the chromium layer has more radiation hardness for short exposures than gold layer, on dry oxides. The low value of radiation induced charge for short exposures and higher values for longer exposures in case of Cr, as compared to Au layer, rules out the possibility of nonuniform Na distribution at the metal-oxide interface or in the bulk of the oxide layer,

at least for these samples. It seems that similar to Al, Cr layer also acts as a sodium getter and sodium ions are located in the deep traps at the metal-oxide interface. These sodium ions are believed to be liberated only after prolonged exposures, resulting in increased radiation sensitivity. The presence of nonuniform traps at the metal-oxide interface in sodium contaminated devices, has been reflected by the results of many authors[17,18].

As indicated earlier, the density of neutral Na at metal-oxide interface or SiO_2 layer decides the magnitude of radiation induced charge. Increase in x-ray energy did not have considerable effect on charge formation, as shown in Figs. 4.11 and 4.12. It seems that if the sodium content is constant, even low energy of x-ray is sufficient to release all the sodium ions and further increase in x-ray energy would not have any significant effect on the radiation induced charge.

The recovery of the devices may be explained to be due to the migration of Na^+ ions back to the metal-oxide interface. Partial recovery obtained in some of the devices may be attributed to fast and slow charge migration in contaminated devices under B T stress, as proposed by Hofstein[17] and Singh et al[18]. It seems that some residual charge is retained by the devices during recovery due to some structural changes in SiO_2 film in that area.

4.6 Conclusion

The formation of radiation induced charge is strongly dependent on the growth conditions of SiO_2 layer and the gate metal. In order to fabricate the radiation-hard MOS devices, which could be used for space applications, the growth of sodium free oxide and metal layers is an essential condition.

REFERENCES

(Chapter-IV)

1. E.H. Snow, A.S. Grove and J.Fitzgerald, Proc. IEEE, 55 , 1168 (1967)

2. A.S. Grove and E. H. Snow, Proc. IEE (Letters), 54 , 894 (1966)

3. K.H. Zaininger and A. G. Holmes-Siedle, RCA Review, 28 , 208 (1967)

4. K.H. Zaininger, IEEE Trans. Nucl. Sc., NS-13 , 237 (1966)

5. E. Kooi, Philips Res. Reports, 20 , 306 (1965)

6. E. Kooi, Philips Res. Reports, 20 , 595 (1965)

7. B. Andre, J. Buxo, D. Esteve and H. Mortinot, Solid State Electronics, 12 , 123 (1968)

8. J. P. Mitchell, IEEE Trans. Electron Devices, ED-14 , 762 (1967)

9. A.J. Speth and F.F. Fang, Appl. Phys. Lett., 7 , 145 (1965)

10. M. Simons and H.L. Hughes, IEEE Trans. Nucl. Sc., NS-18 , 106 (1971)

11. J. Lindmayer, ibid, NS-18 , 91 (1971)

12. H.L. Hughes, IEEE Trans. Catalog, 71-C-9-Phy 33 (1971)

13. K.G. Aubuchon, IEEE Trans. Nucl. Sc. , NS-18 , 117 (1971)

14. H.L. Hughes, R.D. Baxter and B. Phillips, ibid, NS-19 , 256 (1972)

15. D.V. McCaughan and V.T. Murphy, IEEE Trans. Nucl. Sc., NS-19 , 249 (1972)

16. H.L. Hughes, ibid, NS-16 , 195 (1969)

17. S.R. Hofstein, IEEE Trans. Electron Devices, ED-13 , 222 (1966)

18. B.R. Singh, B. D. Tyagi and B.R. Marathe, Int. J. Electronics, 41 , 273 (1976)

***

Chapter - V

SCHOTTKY BARRIER SOLAR CELL

Solar cells are devices which directly convert solar energy into electrical energy. The race between various nations of the world for rapid industrial growth and the fast dwindling conventional sources of energy have forced us to look for alternative sources of energy. The commonly used energy sources are the fossil fuels and the hydraulic power. These sources cannot meet the demands of the world for more than a few decades. The most promising sources of energy in the future appear to be the solar energy and the nuclear energy released as a result of the fusion of lighter nuclei.

5.1 Solar energy

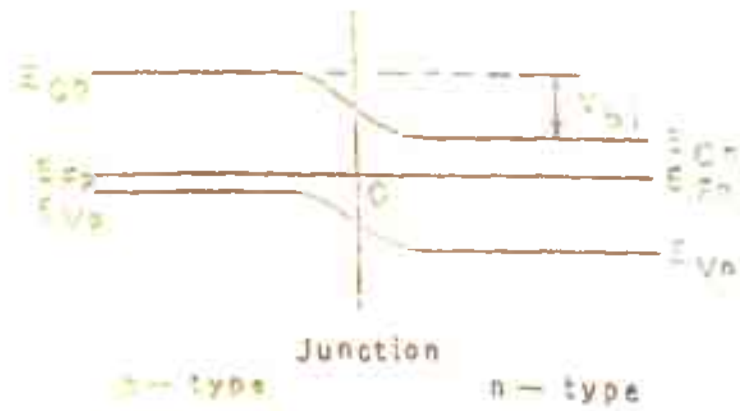
The sun has been radiating enormous amounts of energy, which is about a million Q every three seconds, for over 500 million years, (1Q represents 12.93 x 10^{14} KW hr energy). This radiation is expected to continue at this rate for at least next 50 million years. If even a small amount of the solar energy reaching the earth could be used, it would solve most of our energy supply problems. One singular feature of the solar energy is that it is free of the danger of pollution, which is associated with other sources of energy. Solar energy however, has its own problems. The energy falling per square

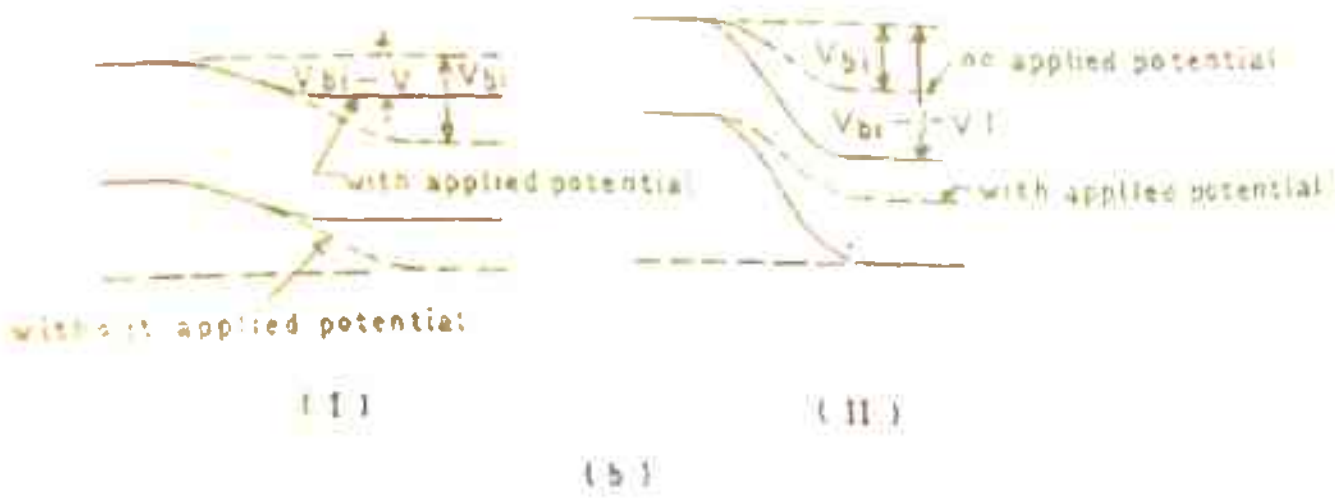
cm of earth's surface is hardly 0.1 Watt. For generating appreciable amounts of power, it is necessary to concentrate the solar energy to large values, with the help of concentrators or large area collectors.

Any process of energy conversion in which the efficiency is large is a desirable process. Efficiency is defined as the ratio of the output power to the input power. Compared to the efficiency of energy conversion processes in which one form of energy is converted to another involving intermediate steps, the efficiency is likely to be larger in processes wherein intermediate steps are absent. Thus, efficiency in direct conversion processes would be better and can be achieved at lower costs.

5.2 Photovoltaic conversion

Solar cells are the devices which are used for direct conversion of the solar energy to electrical energy. They have been used in space programmes for over a decade. The appearance of a voltage across the device, when light falls on it (in absence of any other current source), is known as the 'photovoltaic effect'. This effect was first discovered by Edmond Becquerrel in 1839. It was found that a voltage is developed, when light is directed onto one of the electrodes in an electrolyte solution. In the fifties of this century, scientists





(b)

FIG. 5.1 ENERGY BAND DIAGRAM OF A p – n JUNCTION
(a) IN THE ABSENCE OF APPLIED VOLTAGE
(b) (I) FORWARD BIAS APPLIED TO THE JUNCTION
(II) REVERSE BIAS APPLIED TO THE JUNCTION

started thinking of using this effect (known to occur in solids too) for energy conversion. Bell Telephone Laboratory first produced high efficiency solar cells. Since then a lot of work has been done in this field. The success of solar cell in space research has more than justified the large amount of effort put in for its development. It would be useful for the mankind in general, only when solar cells are put to use for terrestrial purposes also.

5.3 The p-n junction solar cell

The type of solar cells commonly used these days, is nothing but a simple p-n junction, with silicon as the host lattice. When the junction is formed, electrons from n-side near the junction diffuse to the p-side, leaving behind the positively charged donor impurity ions. This results in an increase in the potential on n-side. Similarly, holes from p-side diffuse to the n-side leaving behind the negatively charged acceptor ions. The potential on p-side, thereby, gets lowered. The process continues till a built-in -potential V_{bi}, (Fig. 5.1a), is set up under thermal equilibrium, at which the net flow of charge carriers on either side is zero. From the point of view of the energy band diagram, electrons trying to go from n-side to p-side have to climb the potential hill. The condition for zero net flow of charge carriers

across the junction, under thermal equilibrium, is met when the Fermi levels E_{fn} and E_{fp} of the electrons on both the sides of the junction coincide, as shown in Fig. 5.1a. In fact, there will always be some electrons on n-side, which will have sufficient energy to climb up the hill and go to the p-side and recombine with holes there, thereby constituting, what is called, a 'recombination current density' J^{o}_{nr}, (current density is current per unit area). Since electrons are negatively charged, J^{o}_{nr} is directed from p-to n-side. Similarly, the thermally generated electrons on p-side can climb down the hill towards n-side, constituting a 'generation current density' J^{o}_{ng}, directed from n-to p-side. In the same way, there is a hole recombination current density J^{o}_{pr} (from p-to n-side) and a hole generation current density J^{o}_{pg} (from n- to p-side). Under thermal equilibrium,

$$J^{o}_{nr} = J^{o}_{ng} \quad \text{and} \quad J^{o}_{pr} = J^{o}_{pg} . \qquad (5.1)$$

The total current density from p- to n-side, in thermal equilibrium, can be written as ($J^{o}_{nr} + J^{o}_{pr}$) and this is balanced by an equal current density ($J^{o}_{ng} + J^{o}_{pg}$) from n- to p-side.

Now, if we apply a bias to the p-n diode, with the p-side as positive and n-side negative, the external potential difference V lowers the built-in -potential from the value V_{bi} in thermal equilibrium to ($V_{bi} - V$) under this bias, known as

'forward bias' (Fig. 5.1bI). Now more electrons can diffuse from n- to p-side, increasing the current density J_{nr}; $J_{nr} > J^o_{nr}$. Likewise, the hole current density J_{pr} also increases; $J_{pr} > J^o_{pr}$. However, since the temperature of the diode is not changed, J_{ng} and J_{pg} continue to have the same values , J^o_{ng} and J^o_{pg} , as before. This results in a net current from p- to n-side, given by

$$J = (J_{nr} + J_{pr}) - (J^o_{ng} + J^o_{pg})$$

$$= (J^o_{ng} + J^o_{pg}) (e^{eV/kT} - 1) = J_o(e^{\beta V} - 1), \qquad (5.2)$$

where $\beta = \dfrac{e}{kT}$.

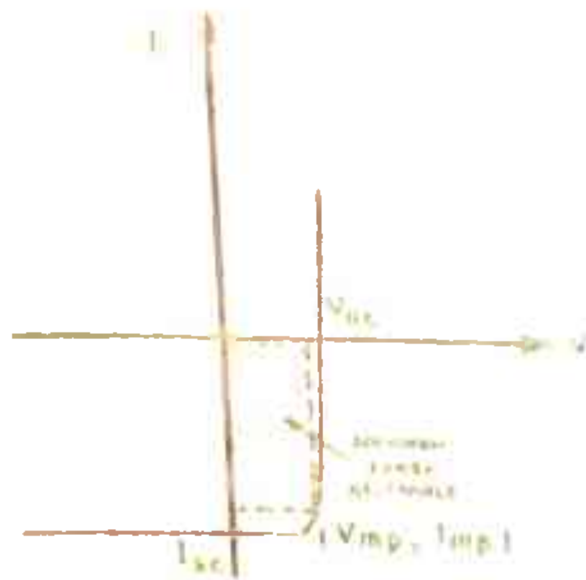
When the diode is 'reverse biased', (n-side positive and p-side negative), the applied voltage increases the potential barrier, from V_{bi} in thermal equilibrium to $(V_{bi}+V)$ under reverse bias, as shown in Fig. 5.1bII. Again, this affects only the recombination currents, which decrease to $J_{nr} < J^o_{nr}$ and $J_{pr} < J^o_{pr}$. The net current from p- to n-side is given by

$$J = J_o (e^{-\beta V} - 1). \qquad (5.3)$$

It is clear that J is negative in eq. (5.3). Both the eqs. (5.2) and (5.3) may be expressed as the single diode equation

$$J = J_o (e^{\beta V} - 1) . \qquad (5.4)$$

(a)



(b)

FIG. 5.2 CURRENT — VOLTAGE CHARACTERISTIC

(a) FOR A p — n JUNCTION

(b) FOR A p — n JUNCTION SOLAR CELL

The current-voltage characteristics (Fig. 5.2a) show that a positive V gives $J > 0$ (i.e., from p- to n-side), and a negative V gives $J < 0$. The product of current and voltage is always positive, which means dissipation of power.

Now, if the diode is illuminated, the generation of the carriers on p- and n-sides of the junction increases much above the thermal equilibrium values. If J_{pg}^{L} and J_{ng}^{L} be the hole and electron generation currents on illumination, $J_{pg}^{L} > J_{pg}^{o}$ and $J_{ng}^{L} > J_{ng}^{o}$. Electrons from p-side, where they are minority carriers, fall downhill constituting a greater generation current J_{ng}^{L} than what it was in thermal equilibrium. The flow of electrons lowers the potential on n-side. Similarly, the flow of holes from n- to p-side, raises the potential on p-side. This has the effect of reducing the thermal equilibrium potential drop from V_{bi} to ($V_{bi} - V$). In effect, the diode acts as if it is forward biased. This also increases the recombination current from ($J_{nr}^{o} + J_{pr}^{o}$) to ($J_{nr} + J_{pr}$). The net current density on illumination is given by

$$
\begin{aligned}
J &= (J_{nr} + J_{pr}) - (J_{ng}^{L} + J_{pg}^{L}) \\
&= (J_{nr}^{o} + J_{pr}^{o}) e^{\beta V} - (J_{ng}^{o} + J_{pg}^{o}) - (J_{ph}) \\
&= J_{o} (e^{\beta V} - 1) - J_{ph},
\end{aligned} \tag{5.5}
$$

where $J_{ph} = (J_{ng}^{L} + J_{pg}^{L}) - (J_{ng}^{o} + J_{pg}^{o})$. Since, J_{ph} is

much larger than the first term in eq. (5.5), a positive value of V yields a negative current J. Hence, the product of voltage and current is negative, meaning thereby that the device generates power. The current-voltage characteristic of a solar cell under illumination is shown in Fig. 5.2b. For greater efficiency, J should be large and negative. This means that the forward bias current component $J_o(e^{\beta V} - 1)$ should be as small as possible. This current component is called the 'dark current'. Thus

$$J = J_d - J_{ph}, \tag{5.6}$$

$$\text{where } J_d = J_o(e^{\beta V} - 1). \tag{5.7}$$

For a solar cell, we define 'open circuit voltage' V_{oc} as that value of V, for which the current is zero. Therefore,

$$0 = J_o(e^{\beta V_{oc}} - 1) - J_{ph}$$

$$\text{or} \quad V_{oc} = \frac{kT}{e} \ln\left(\frac{J_{ph}}{J_o} + 1\right). \tag{5.8}$$

The 'short circuit current' density J_{sc} is defined as that value of J for which V is zero, i.e.,

$$J_{sc} = -J_{ph}. \tag{5.9}$$

The 'efficiency' η of a solar cell is defined as the ratio

$$\eta = \frac{\text{Power output}}{\text{Power input}}. \tag{5.10}$$

We inscribe a maximum area rectangle in the voltage-current (V-I) characteristic of the solar cell (Fig. 5.2b) and define the power output as $V_{mp} \times I_{mp}$. The 'fill factor' f of a solar cell is defined as

$$f = \frac{V_{mp} \times I_{mp}}{V_{oc} \times I_{sc}} . \qquad (5.11)$$

5.4 Materials and efficiency considerations for solar cells

The material that is to be used for preparing photo-voltaic converters, or solar cells, should have some specific properties. The basic phenomenon which takes place in solar cells is that the photons are absorbed in the semiconductor material and generate electron-hole pairs. Loferski[1,2] found that the number of absorbed photons, having energy greater than the band gap, decreases as the band gap increases. He also studied the maximum solar energy conversion efficiency as a function of band gap. The curve η_{max} versus band gap, as obtained by him, predicts the values of η_{max} for semi-conductors having energy gaps between 1.1 eV and 2.3 eV (e.g., In P, Ga As, Al Sb, etc.), to be higher than that for silicon- the most commonly used material for solar cells - which has a band gap of 1.1 eV. However, the absorption of ultraviolet radiation in the solar spectrum by the atmosphere and the occurence of intensity peak[3] at about 5000 Å , favour

the semiconductors with smaller band gaps. The performance of large band gap materials is deteriorated, because the number of photons with energies necessary to create electron-hole pairs, reaching the photovoltaic convertor is insufficient. In addition to this, another important factor is the lifetime of the minority carriers. It is required that the carriers should not recombine and annihilate before being collected, which means that the minority carrier lifetime should not be very small.

The gallium arsenide solar cells have been found to give higher efficiencies and are favourable in high temperature operation too. But the development of Ga As solar cells has been hindered due to the high absorption coefficient arising from its direct band gap and the high price of the raw material. Taking all the factors into account, including the cost of raw material, silicon is found to be the most useful one and most of the research in this field is being done with silicon, though people are working with other materials also.

5.5 Limitations of p-n junction solar cell

Even after so much work has been done on the p-n junction solar cells, the cost of such cells is high compared to other energy sources. Active research is still going on to reduce

the cost. There are also some disadvantages in using these cells. They degrade on being subjected to high energy radiations. This effect has been minimized to a great extent by covering the cell with glass, so that most of the damage occurs in the glass rather than in the cell. Other method to do this is to add an impurity to the base material, which, on account of its high mobility, quickly migrates to the defects in the crystal and neutralizes the broken bonds. Another disadvantage is that a part of the solar energy gets reflected from the surface of the cell. The reflection losses have also been reduced to a considerable extent by the use of antireflection coatings.

The minimum energy which is required to produce electron-hole pairs, is equal to the band gap of the material. It is obvious, therefore, that the part of solar spectrum having energy less than the band gap, goes waste. A photon whose energy is greater than the band gap, creates an electron-hole pair and the extra energy contributes to lattice vibrations and is eventually dissipated as heat. Wolf[4] reported that only 46 % of the solar energy is utilized for electron-hole pair generation in a semiconductor with 0.9 eV band gap.

The electron-hole pairs, which are generated at a greater distance from the junction, recombine before reaching the junction, meaning thereby that the collection of all the

generated carriers does not take place. Also, the series resistance of the cell causes the degradation of the fill factor, which results in the reduction of its conversion efficiency.

5.6 Advantages of the Schottky barrier solar cell

The interest in the field of Schottky barrier solar cells (SBSC), which are simple metal-semiconductor contacts, is rising since the advantages of these structures over the p-n junction solar cells have been recognized. The SBSC can be fabricated, so as to give efficiencies approaching that of p-n junction solar cells[5]. The fabrication of these devices can be done at much lower temperatures, so that no degradation of diffusion length and life time occurs. Moreover, it is much more easy and simple to evaporate a metal on the semiconductor than to diffuse impurity into it to form a junction. This also makes the device cheaper. The top layer in SBSC is that of a metal, which has very small resistivity. In addition to all this, another advantage is that polycrystalline substrates can also be used for the fabrication of this device.

5.7 Metal-semiconductor contact

The transport theory of semiconductors, based on the

generated carriers does not take place. Also, the series resistance of the cell causes the degradation of the fill factor, which results in the reduction of its conversion efficiency.

5.6 Advantages of the Schottky barrier solar cell

The interest in the field of Schottky barrier solar cells (SBSC), which are simple metal-semiconductor contacts, is rising since the advantages of these structures over the p-n junction solar cells have been recognized. The SBSC can be fabricated, so as to give efficiencies approaching that of p-n junction solar cells[5]. The fabrication of these devices can be done at much lower temperatures, so that no degradation of diffusion length and life time occurs. Moreover, it is much more easy and simple to evaporate a metal on the semiconductor than to diffuse impurity into it to form a junction. This also makes the device cheaper. The top layer in SBSC is that of a metal, which has very small resistivity. In addition to all this, another advantage is that polycrystalline substrates can also be used for the fabrication of this device.

5.7 Metal-semiconductor contact

The transport theory of semiconductors, based on the

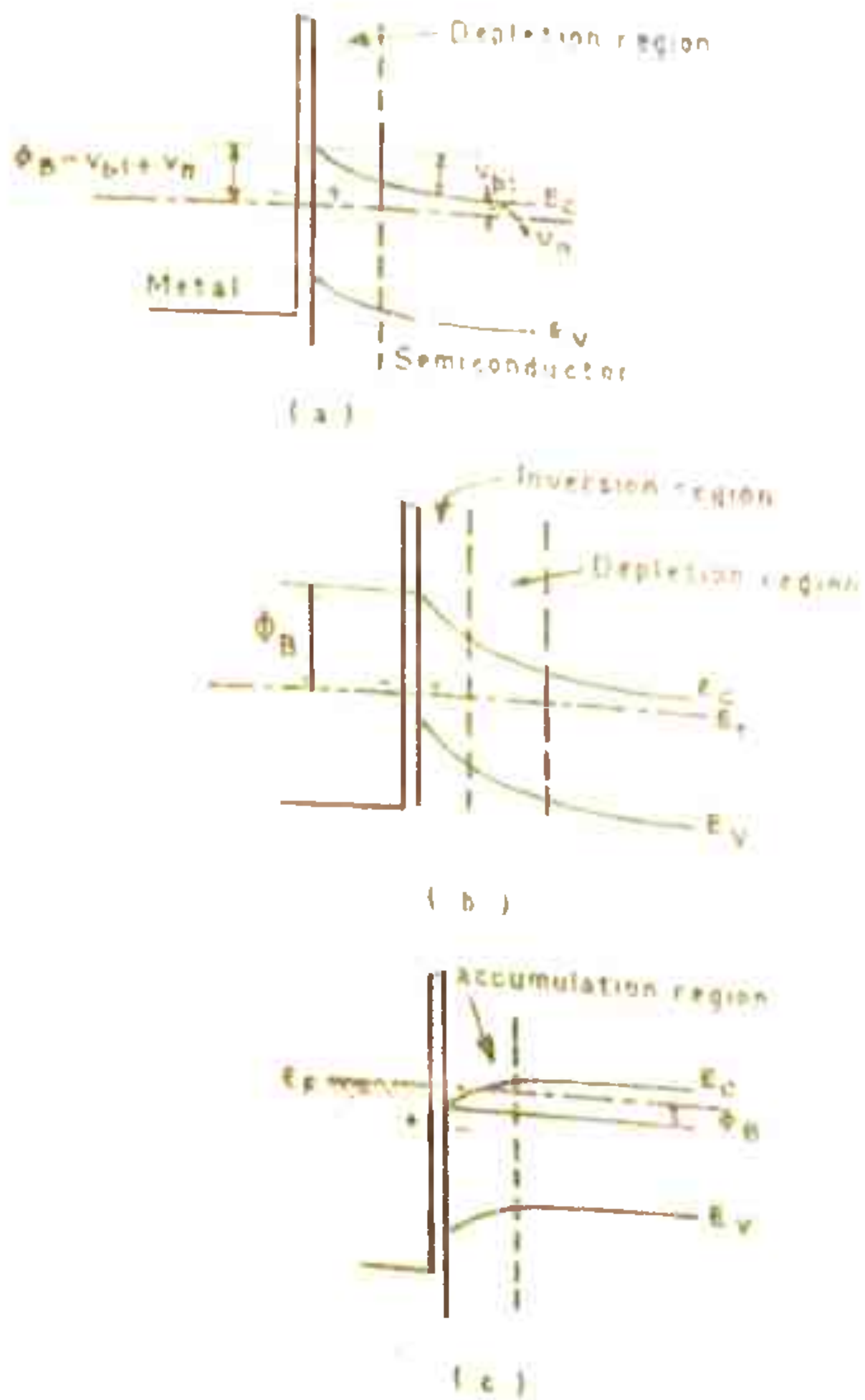


FIG. 5.3 ENERGY BAND DIAGRAMS OF A METAL-SEMICONDUCTOR CONTACT SHOWING THE FORMATION OF (a) DEPLETION REGION (b) INVERSION REGION (c) ACCUMULATION REGION

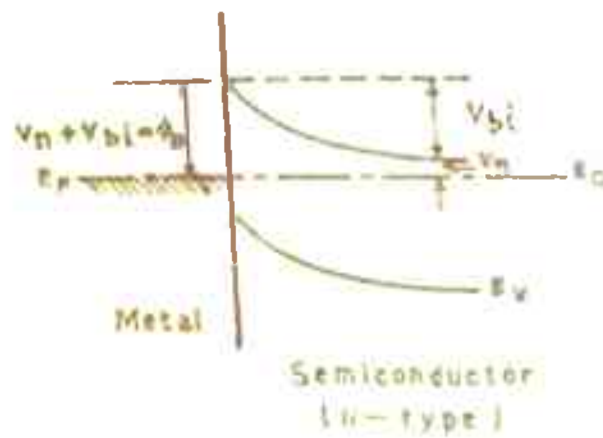
band theory of solids, was formulated by Wilson[6] and Schottky[7] applied this theory to metal-semiconductor contacts. Schottky found that a potential barrier arises from the stable space charges in semiconductors. The metal-semiconductor contacts were, therefore, named after him and are known as 'Schottky barriers'.

When a metal of higher work function is brought closer to an n-type semiconductor of lower work function and the distance between them is reduced to such an extent that the electrons can tunnel from one to the other, then the flow of electrons takes place from the semiconductor to the metal. This lowers the Fermi level of the semiconductor. The transfer of electrons continues till an equilibrium is reached. In equilibrium, the Fermi levels of both, the metal and the semiconductor, coincide. Due to transfer of electrons, the region of the semiconductor near the contact becomes depleted of the charge carriers and this layer, known as the 'depletion region', contains mostly the positively charged donor ions. This results in the bending of conduction and valence bands. The potential energy of the electrons in the depletion region is greater than that of the electrons in the semiconductor bulk. Thus, a built-in-potential V_{bi} is produced in the depletion region, as shown in Fig. 5.3a. The potential barrier φ_B (which is equal to the separation between the top of the conduction band and the metal Fermi level)

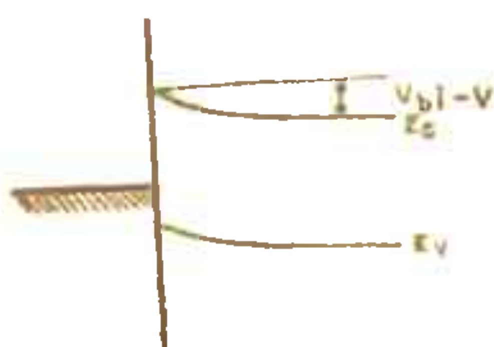
prevents the flow of electrons from one region to the other, in the same way as does the built-in-potential V_{bi} in the case of p-n junction (Fig. 5.1a).

If the work function of the metal is very high, the valence band of the n-type semiconductor comes closer to the Fermi level at the surface and the surface region effectively becomes p-type. This is known as the 'inversion region'. The depletion and inversion regions are shown in Figs. 5.3a and b, respectively. On the other hand, if an n-type semiconductor is put in contact with a metal of lower work function, the electrons flow from metal to semiconductor and the surface region accumulates more electrons. Thus, an 'accumulation region' is formed. In this case, the metal surface gets positively charged and the semiconductor surface becomes negatively charged. This causes the bands to bend downwards at the surface, as shown in Fig. 5.3c. Similarly, for a p-type semiconductor, the depletion and inversion regions are obtained with a metal of lower work function than that of the semiconductor, and the accumulation region is found with a metal of higher work function.

The potential barrier at the interface is responsible for the rectifying action of the metal-semiconductor contact. The concentration of carriers in the depletion region being small, the externally applied voltage appears across this layer.



(a)



(b)

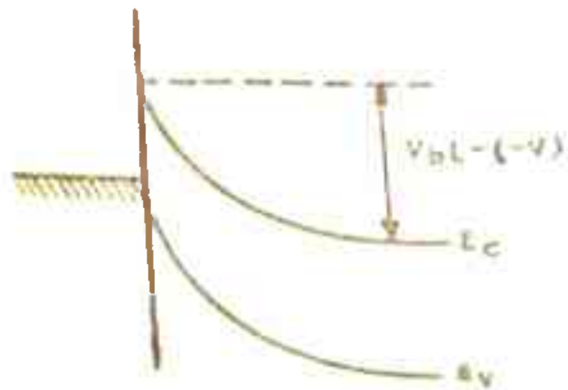

(c)

FIG. 5.4 ENERGY BAND DIAGRAMS OF A METAL–SEMICONDUCTOR CONTACT (a) IN EQUILIBRIUM (b) UNDER FORWARD BIAS (c) UNDER REVERSE BIAS.

This applied voltage increases or decreases the built-in-potential, as shown in Fig. 5.4. If the voltage applied is +V (forward bias), the effective built-in-potential becomes $V_{bi} - V$, whereas reverse bias increases it to $V_{bi} + V$. In fact, there are always a few electrons in semiconductor conduction band, which have enough energy to surmount the potential barrier. The electron current density from semiconductor to metal is denoted by J_n^- and corresponds to a conventional current in the opposite direction. Similarly, J_n^+ denotes the electron current density from metal to semiconductor, corresponding to a conventional current in its opposite direction. In equilibrium, J_n^+ and J_n^- should be equal, so that there is no net electron current flowing through the device.

In addition to J_n^+ and J_n^- , there are two hole current densities also, represented by J_p^+ and J_p^- . J_p^+ is due to the holes in the valence band at the semiconductor surface, having sufficient energy to enter the bulk region. And J_p^- consists of holes diffusing to the semiconductor surface and recombining with the electrons from the metal. The conventional currents corresponding to J_p^+ and J_p^- are from metal to semiconductor and semiconductor to metal, respectively. Again, J_p^+ and J_p^- must be equal in magnitude in the equilibrium condition. Thus, in equilibrium, when the net current is zero,

$$|J_n^-| + |J_p^+| = |J_n^+| + |J_p^-| . \tag{5.12}$$

When external voltage is applied to the contact (Figs. 5.4a and c), J_n^- and J_p^+ change, because they depend on the number of charge carriers having sufficient energy to surmount the barrier. These current densities, for applied voltage V, are given by

$$J_n^- = - J_{no} \exp [- \beta (\varphi_B - V)] \quad (5.13)$$

$$J_p^+ = J_{po} \exp [- \beta (\varphi_B - V)] \quad (5.14)$$

where J_{no} and J_{po} are, respectively, the magnitudes of the total electron and hole current densities, incident upon the surface barrier in equilibrium. The direction of motion of the charge carriers is considered to be positive from metal to semiconductor. The other two current densities, J_n^+, J_p^-, are the functions of temperature only and do not depend upon the externally applied voltage. Since, in equilibrium,

$$J_n^+ = - J_n^- \quad (5.15)$$

and $J_p^- = - J_p^+$, $\quad (5.16)$

therefore, $J_n^+ = J_{no} \exp (- \beta \varphi_B)$ $\quad (5.17)$

and $J_p^- = - J_{po} \exp (- \beta \varphi_B)$. $\quad (5.18)$

Thus, the total electron and hole current densities are

$$J_n = J_n^+ + J_n^- = - J_{no} \exp (-\beta\varphi_B) [\exp (\beta V) - 1] \quad (5.19)$$

and $J_p = J_p^+ + J_p^- = J_{po} \exp (-\beta\varphi_B) [\exp (\beta V) - 1]$. $\quad (5.20)$

These give the total current density as

$$J = (J_p - J_n) = J_o [\exp (\beta V) - 1] , \qquad (5.21)$$

where $J_o = (J_{po} + J_{no}) \exp (- \beta\varphi_B)$. (5.22)

This equation shows that both, the metal-semiconductor contact and the p-n junction, have similar current - voltage characteristics (see eq. 5.3); only the saturation current is different in the two cases. Thus, Fig. 5.2a may also be taken as the current-voltage characteristic for metal-semiconductor contact.

The results of the above theory, somehow, did not agree with experiments. According to this theory the results should be extremely sensitive to the metal work function, whereas they were found to be almost independent of the metal work function. This discrepancy was explained by Bardeen[8], who took into account the role of surface states.

5.8 Schottky barrier and surface states

Surface states, as explained by Bardeen[8], are the localized states existing in the forbidden energy gap between the conduction and valence bands at the surface of the semiconductor.

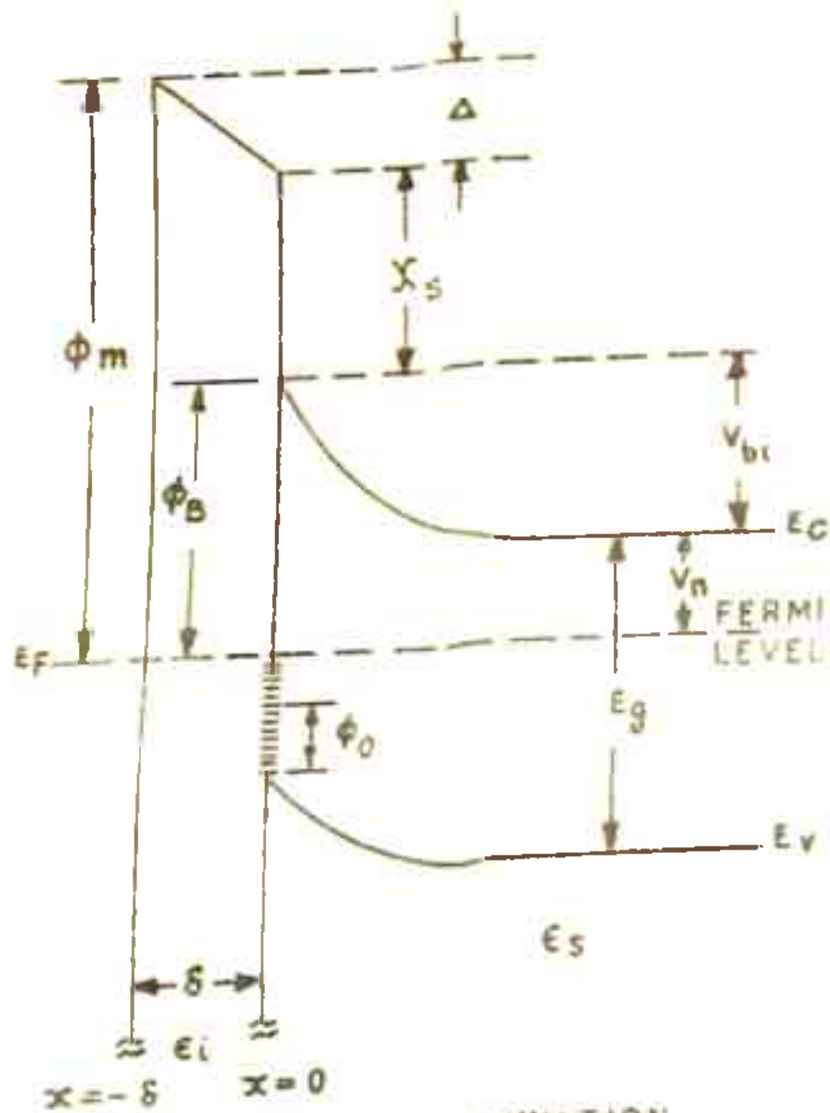
If we consider a metal of higher work function and an n-type semiconductor (of lower work function) brought close

to each other to such an extent that tunneling of electrons can take place between the two, then a negative charge would build up on the metal surface and a positive charge in the semiconductor space charge region, (the carrier concentration being low in semiconductor, the positive charge would not be confined to the surface only). The barrier height thus produced depends on the metal work function and the electron affinity of the semiconductor.

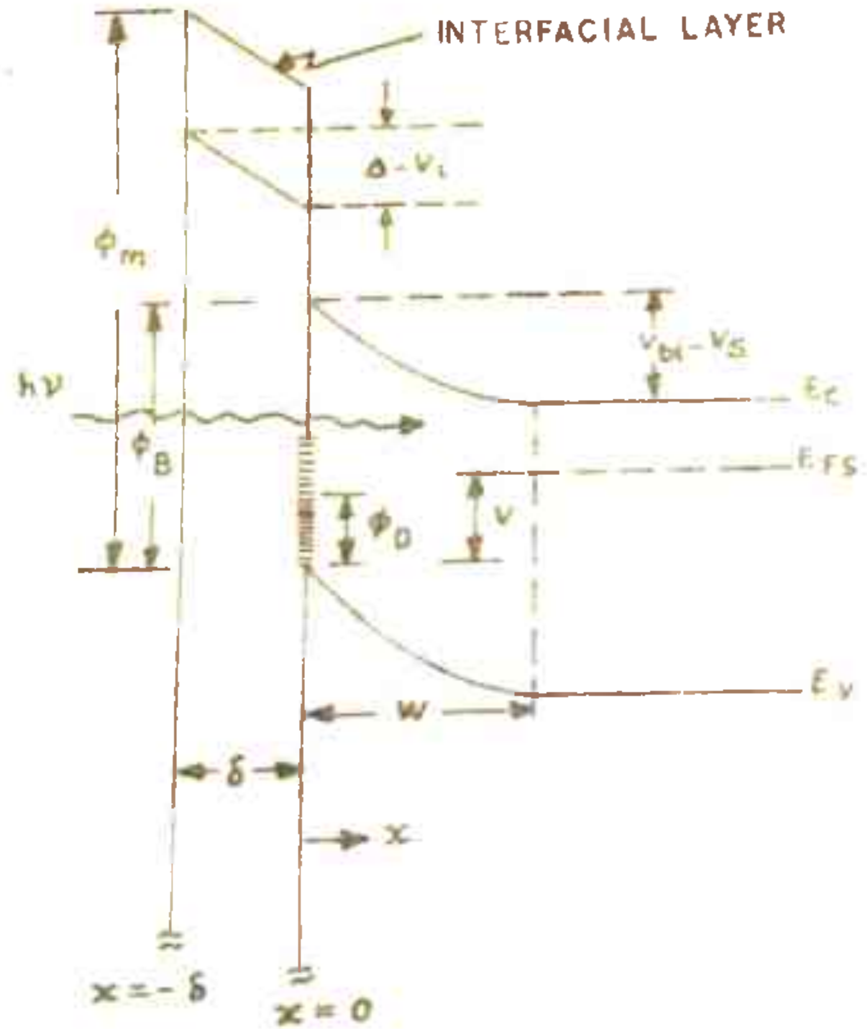
But, in case a large density of surface states is present, the charges produced by diminishing the separation between the metal and semiconductor, get accomodated in the surface states without affecting the space charge of the semiconductor. Thus, the potential barrier of the metal-semiconductor contact (Schottky barrier), in this case, becomes dependant on the property of the semiconductor surface rather than on the metal work function.

5.9 Schottky barrier solar cell

The Schottky barrier solar cell (SBSC) is a simple metal-semiconductor junction, as already mentioned. In these cells, light falls on the metal and reaches the semiconductor, because metal being thin, is almost transparent to light. The electron-hole pairs are generated in the semiconductor depletion



(a) WITHOUT ILLUMINATION



(b) WITH ILLUMINATION

FIG. 5.5 METAL — SEMICONDUCTOR SYSTEM

region, with the result that now more electrons have sufficient energy to overcome the potential barrier. This is equivalent to forward biasing the device. The Fermi level rises in the semiconductor by an amount, say V. Now, if metal and semiconductor ends are connected to a circuit, a flow of current would take place. These SBSC's were known to give lower open circuit voltages than those given by p-n junction solar cells (0.55 volt). Fonash[9] reported that the efficiency of SBSC increases with the density of surface states, when an insulating layer is sandwitched between metal and semiconductor. Ponpon and Stiffert[10] observed that SBSC with an insulating oxide layer between metal and semiconductor, gave open circuit voltage upto 0.55 volt. Since then, there has been considerable activity in this field and these MIS (metal-insulator-semiconductor) or MOS (when oxide is the insulating layer) devices are being extensively investigated. However, the exact role of the interfacial layer is still not well understood.

The system studied in the present work is a gold-silicon dioxide-n silicon structure. Such a system (SBSC), with metal having higher work function than semiconductor, is shown in Fig. 5.5a. Here, Δ is the potential drop across the interfacial layer and V_{bi} is the built-in-potential

in the semiconductor depletion region due to bending of the bands. In equilibrium condition, there is no net flow of current and Fermi levels in metal and semiconductor coincide.

When the device is illuminated (Fig. 5.5b), the voltage V developed in the cell appears partly (V_s) across the semiconductor depletion region of width ω and partly (V_i) across the interfacial layer of width δ. Therefore,

$$V = V_i + V_s \quad (5.23)$$

The electron current density from metal to semiconductor is given by

$$J^e_{ms} = A^* T^2 \exp (-\beta \varphi_B) \exp (-\beta V_i) \quad (5.24)$$

and that from semiconductor to metal is

$$J^e_{sm} = A^* T^2 \exp (-\beta \varphi_B) \exp (\beta V_s); \quad (5.25)$$

here A^* is the Richardson's constant. These two, J^e_{sm} and J^e_{ms}, together constitute the net electron current density J_n from semiconductor to metal.

$$J_n = A^* T^2 \exp [-\beta (\varphi_B + V_i)] [\exp(\beta V) - 1] \quad (5.26)$$

In addition to the electron current, hole current also exists, and consists of two components. One of these

is the hole current generated by light in the depletion region, given by

$$J_h^L = e\,\Phi\,[\,1 - \exp(-\alpha\,\omega)\,]\,, \tag{5.27}$$

where Φ is the light flux density defined as the number of photons falling on unit area per second and α is the absorption coefficient of the material. The other component $J_h(\omega)$ is the net hole current density towards the junction, expressed as

$$J_h(\omega) = D_p \left.\frac{dp}{dx}\right|_{x=\omega}, \tag{5.28}$$

where $p(x)$ is hole concentration in the semiconductor at a position x and D_p is the diffusion coefficient for holes. The current density $J_h(\omega)$ is obtained by solving the continuity equation for hole concentration,

$$\frac{d^2p}{dx^2} - \left(\frac{p - p_{no}}{D_p\,\tau_p}\right) + \frac{\alpha\,\Phi\,\exp\left(-\alpha\frac{x}{\omega}\right)}{D_p} = 0\,. \tag{5.29}$$

In this p_{no} is the unilluminated hole concentration far away from the junction and τ_p is the lifetime for holes. Integration of the above equation gives $J_h(\omega)$ as

$$J_h(\omega) = \frac{e\,\alpha\,L_p\,\Phi\,\exp(-\alpha\omega)}{1 + \alpha\,L_p} - \frac{e p_{no} D_p}{L_p}\,[\,\exp(\beta V) - 1\,]\,, \tag{5.30}$$

where L_p is the diffusion length for holes. In this equation (5.30) the first term corresponds to the holes generated by light, in the bulk region. Thus, the total light generated current density is

$$J_{ph} = e \bar{\Phi} [1 - \exp (-\alpha \omega)] + \frac{e \alpha L_p \bar{\Phi} \exp (-\alpha \omega)}{1 + \alpha L_p}$$

$$= e \bar{\Phi} [1 - \frac{\exp (- \alpha \omega)}{1 + \alpha L_p}] . \qquad (5.31)$$

Considering the electron current positive and therefore hole current negative from semiconductor to metal, the total current density is written as

$$J = J_n - J_h (\omega) - J_{ph}$$

$$= J_o [\exp (\beta V) - 1] - J_{ph} \qquad (5.32)$$

where

$$J_o = A^* T^2 \exp [-\beta (\varphi_B + V_i)] + \frac{e p_{no} D_p}{L_p} \qquad (5.33)$$

is the saturation current density.

Thus, the current - voltage expression for SBSC is similar to that for p-n junction solar cell (eq. 5.6). The light generated current density being greater than the forward dark current density $J_d = J_o (e^{\beta V} - 1)$, the total current density J becomes negative for positive values of

7, which means that the device generates power.

The short circuit current, the open circuit voltage, the efficiency and the fill factor for SBSC also are defined in the same way as in the case of p-n junction solar cell (see section 5.3).

5.10 Brief review of the work done on SBSC

The simplicity of fabrication and low cost of SBSC are the reasons which have made such solar cells an object of intensive investigations. It was predicted by Pulfrey and McOut[11], on the basis of their theoretical calculations, that efficiency of about 22% can be obtained with a metal-n silicon SBSC, about 24% with metal-p silicon one and about 25% with SBSC employing semiconductor of band gap between 1.4 and 1.6 eV. According to them, these high efficiencies could be obtained if the barrier height is of the order of the energy gap. They, however, considered unit quantum efficiency and negligible recombination and used a metal of very high work function. Later, the same authors[12] made allowance for recombination and incomplete absorption , which resulted in an efficiency lower than the value reported earlier. They also found that there is an optimum metal thickness which gives maximum conversion efficiency.

Landsberg and Klimpke[13] and Fonash[9] studied the effect of surface states at the interface between the semiconductor and the insulating layer and found that it improves the performance of SBSC. They, however, did not consider the effect of the thickness of the interfacial layer and took the transmission coefficient across the interfacial layer to be unity.

The present work, first reported[14] in 1976, takes into account the effect of interfacial layer thickness and the transmission coefficient, on the conversion efficiency of the gold-silicon dioxide-n silicon system (SBSC). It is found that there is an optimum thickness of the interfacial layer which gives the maximum efficiency.

Fonash, in his later work[15,16,17], accounted for the fixed charge in insulating layer and obtained the modified metal work function

$$\varphi_m^{eff} = \varphi_m - \frac{Q_{fix}\,\delta_{eff}}{\varepsilon_i}, \qquad (5.34)$$

where φ_m is the metal work function, Q_{fix} is the fixed charge in the oxide layer at an effective distance δ_{eff} and ε_i is the permittivity of the insulating layer. He also reported that the insulating layer has direct influence on the nucleation and growth of the metal electrode, which

affects the light transmitted to the semiconductor. Pulfrey[18], in such a study, found that the barrier height increases with both, the increase in insulating oxide layer charge and the surface charge density.

Lillington and Townsend[19] observed with the gold-n silicon system that the open circuit voltage increases by 38% and the efficiency by 35%, when an oxide layer is included between metal and semiconductor. The optimum thickness of oxide layer for maximum effieiency was observed to be 19 Å. Smith and Rhoderick[20] had earlier reported ageing in Schottky barrier diodes, fabricated by evaporation of gold on p silicon. Lillington and Townsend[19], however, observed that no such aging occurs if the substrate is heated to 120°C prior to and during the evaporation.

Stirn and Yeh[21] used various oxidation techniques and antireflection coating on the metal surface while studying gold-oxide-gallium arsenide system. The efficiency was found to increase from 8.5% to 15% with antireflection coating and the open circuit voltage observed was 750 milli volts.

Pompon and Stiffert[10] worked with thermally grown oxide and deposited silicon dioxide. The latter one was

this increase to the lower metal work function caused by slow deposition of chromium on the oxide surface.

Olsen[27,28] and Landsberg and Klimpke[13] have made extensive calculations on MIS solar cells. Olsen has worked on p-type silicon, whereas the latter authors have made studies on n-type silicon. Olsen considered the transmission coefficient for tunneling of electrons across the interfacial layer, as given by Card and Rhoderick[29]. But, Landsberg and Klimpke[13,30] have taken the transmission coefficient to be unity, although they took into account the participation of surface states as charge transfer centres.

In the next chapter, the theory and results of the present study on gold-silicon dioxide- n silicon, are presented. It is known that the current I in a solar cell is given by $I = I_d - I_{ph}$, from which it is clear that the current responsible for power generation can be increased by decreasing the dark current I_d. The inclusion of an interfacial layer between metal and semiconductor, decreases the dark current. However, the thickness of the interfacial layer cannot be increased indefinitely. Therefore, in the present study, the thickness of the interfacial layer has been optimised to give maximum efficiency, by taking into account

the transmission coefficient for tunneling of electrons. The transmission coefficient is found to help in reducing the dark current. Further, the band to band recombination of the carriers and recombination due to the interface states, have also been taken into account. These factors also reduce the dark current component. The effects of metal work function and donor density too on the conversion efficiency of the solar cell, have been studied and presented in the following chapter.

REFERENCES

(Chapter-V)

1. J.J. Loferski, J. Appl. Phys., 27, 777 (1956)
2. J.J. Loferski, Proc. IEEE, 51, 667 (1963)
3. M.P. Thekaekara and A.J. Drummond, Nature Phys. Sci., 229, 6 (1971)
4. M. Wolf, Proc. IRE, 48, 1246 (1960)
5. R.J. Stirn and Y.C.M. Yeh, 10th IEEE PV Sp. Conf., New York (1973)
6. A.H. Wilson, Proc. Roy. Soc., A133, 458 (1931)
7. W. Schottky, Natarwiss, 26, 843 (1938)
8. J. Bardeen, Phys. Rev., 71, 717 (1947)
9. S.J. Fonash, J. Appl. Phys., 46, 1286 (1975)
10. J.P. Ponpon and P. Stiffert, J. Appl. Phys., 47, 3243 (1976)
11. D.L. Pulfrey and R.F. McOut, Appl. Phys. Lett., 24, 168 (1974)
12. R.F. McOut and D.L. Pulfrey, Proc. 11th IEEE Photo-Voltaic Specialists Conference, p. 371; New York: IEEE, (1975)
13. P.T. Landsberg and C.K. Klimpke, Proc. Royal Soc., Lond., A354, 101 (1977)

14. S. Srivastava, N.K. Swami and H.M. Ghule, Proc. National Solar Energy Convention, Calcutta; p. 107 (1976)

15. S.J. Fonash, Proc. 11th IEEE Photovoltaic Specialists Conference, p. 376; New York: IEEE, (1975)

16. S.J. Fonash,, Proc. 3rd International Conference on Thin Films, Budapest, Hungary,

17. S.J. Fonash, J. Appl. Phys., 47 , 3597 (1976)

18. D.L. Pulfrey, IEEE Trans. Electron Devices, ED-23, 586 (1976)

19. D.R. Lillington and W.G. Townsend, Appl. Phys. Lett., 28 , 97 (1976)

20. B.L. Smith and E. H. Rhoderick, Solid States Electronics, 14 , 71 (1971)

21. R.J. Stirn and Y.C.M. Yeh, Appl. Phys. Lett., 27 , 95 (1975)

22. J.P. Ponpon and P. Stiffert, Extended Abstract, International Solar Energy Congress (ISEC), New Delhi, p. 466, abs. no. 0309, (Jan. 1978)

23. S. Kar, D. Shanker and S.P. Joshi, Ext. Abs., ISEC, p. 469, abs. no. 0322, (Jan. 1978)

24. T. Shewchun, R. Singh and M.A. Green, J. Appl. Phys., 48 , 765 (1977)

25. J.A. St. Pierre, R. Singh, J. Shewchun and J.J. Loferski, Proc. 12th IEEE Photovoltaic Specialists Conference, p. 847, New York: IEEE, (1976)

26. W.A. Anderson, J.K. Kim and A.E. Delahoy, IEEE Trans. Electron Devices, ED-24 , 453 (1977)

27. L.C. Olsen, Proc. 12th IEEE Photovoltaic Specialists Conference, p. 854, New York: IEEE, (1976)

28. L.C. Olsen, Solid State Electronics, 20 , 741 (1977)

29. H.C. Card and E.H. Rhoderick, J. Phys. D, 4 , 1589 (1971)

30. C. Klimpke and P.T. Landsberg, Proc. 12th IEEE Photovoltaic Specialists Conference, p. 868, New York: IEEE, (1976)

*****

Chapter - VI

EFFICIENCY CALCULATIONS ON SCHOTTKY BARRIER SOLAR CELL

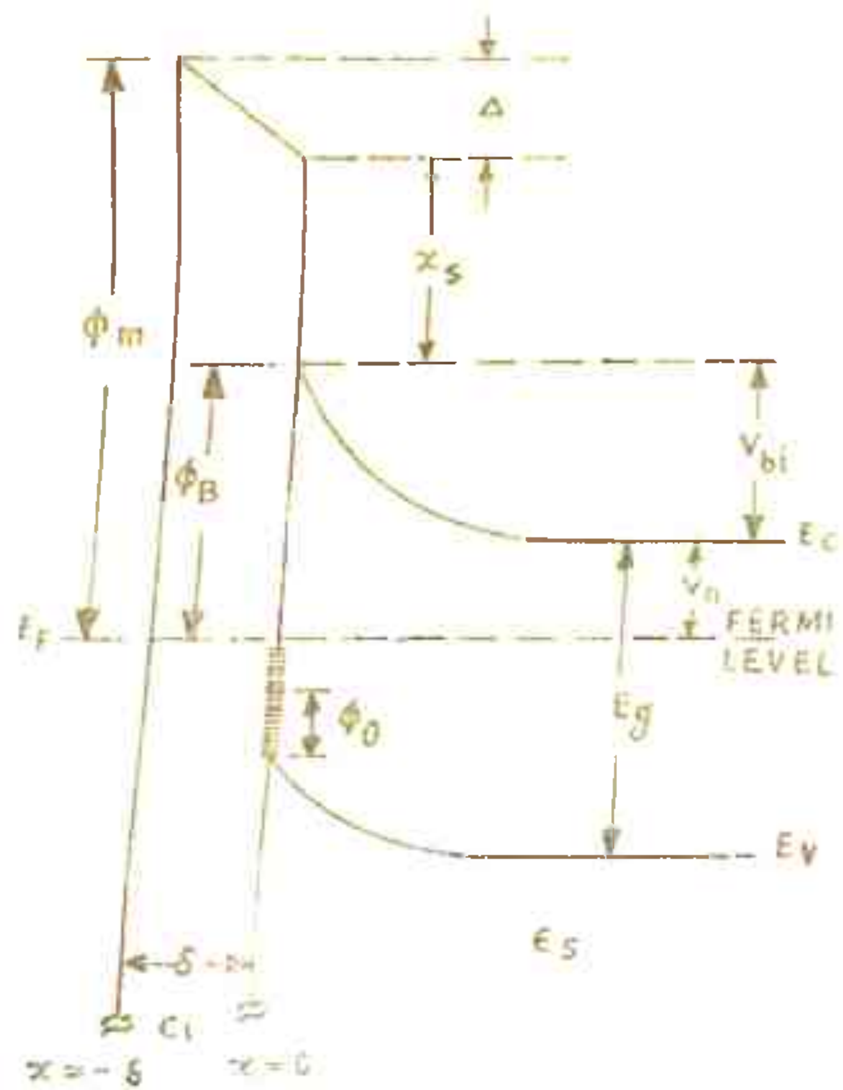
The detailed investigations on Schottky barrier solar cells (SBSC) have been encouraged because of their low cost and ease of fabrication. The Schottky barrier devices to be used as solar cells, could be fabricated to give efficiencies approaching that of the p-n junction solar cells[1]. Fonash[2], later, stressed the importance of surface states in the efficiency determination of SBSC. The SBSC with an interfacial layer is commonly known as MIS (metal-insulator-semiconductor) solar cell or, if oxide is the insulating layer, MOS solar cell. Pompon and Stiffert[3] observed that MOS solar cells could give open circuit voltage upto 0.55 volt against 0.3 volt for metal-semiconductor solar cells. Since then a large number of workers[3-18] have analysed various aspects of these cells. About 14-15% efficiency has been experimentally achieved for GaAs SBSC[9,19] and about 7-8% for silicon SBSC[8,20,21].

In the present chapter, we present a theoretical study on the dependence of efficiency of SBSC on the thickness of interfacial layer between metal and semiconductor. Fonash[2] and Landsberg and Klimpke[14,15] have

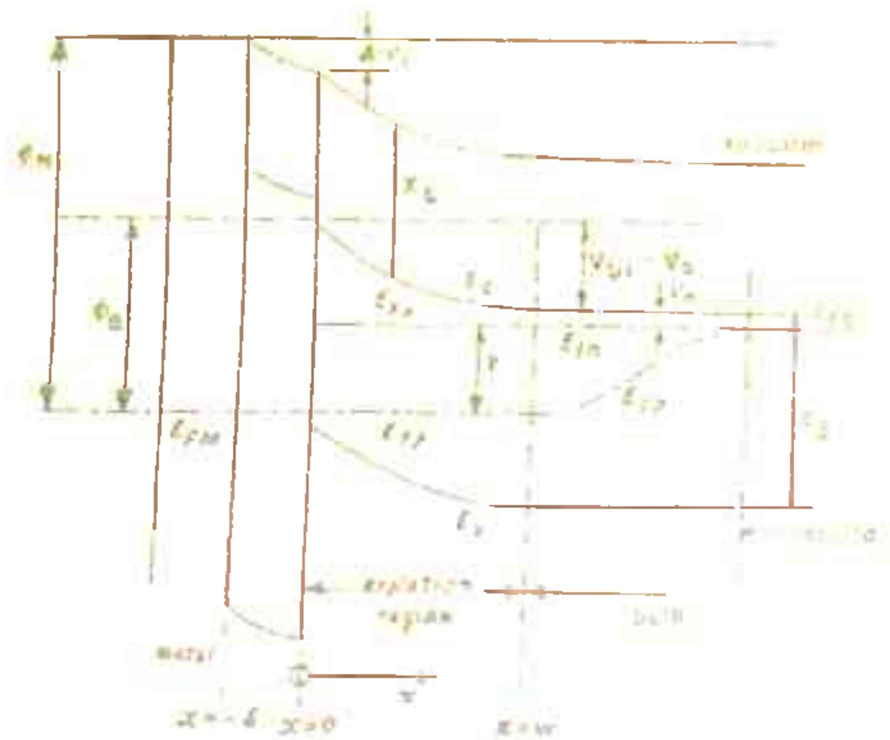
studied the effect of surface states on the performance of SBSC with an interfacial layer. One drawback with their models was that these authors[2,14] took the tunneling probability for electrons across the interfacial layer (commonly known as transmission coefficient) to be unity. In reality, the tunneling probability is a function of the thickness of interfacial layer. The transmission coefficient is, therefore, an important factor, which influences the efficiency of the cell. The present work takes into account this factor; and in addition to this, the effects of surface states, doping density of the semiconductor and the metal work function, on the efficiency of SBSC have also been computed.

6.1 Direct tunneling of charge carriers

In this section we assume that the surface states are not participating as charge transfer centres. Strikha[22] justified this assumption under conditions in which the low energy surface states are immobilized by the electron exchange with the metal, while the high energy surface states are not taken into account, as a first approximation, because influence is small as a result of low concentrations. Here, we consider the charge transport directly between the metal and the semiconductor.



(a) WITHOUT ILLUMINATION



(b) WITH ILLUMINATION

FIG. 6.1 METAL — SEMICONDUCTOR SYSTEM

6.1(a) Theory

The energy band diagram of SBSC with an interfacial layer is shown in Fig. 6.1. It shows the cell in dark (Fig. 6.1a) and also the device under illumination when it develops a voltage V. This voltage V appears partly across the semiconductor depletion region (V_s) and partly across the interfacial layer (V_i), such that

$$V = V_i + V_s . \tag{6.1}$$

Thus, when the cell is illuminated, the net potential drop across the depletion region of width ω is $V_{bi} - V_s$, where V_{bi} is the built-in-potential due to bending of the conduction and valence bands at the surface; and the net potential drop across the interfacial layer of width δ, is $\Delta - V_i$, where Δ is the equilibrium potential drop across the interfacial layer.

The voltage V developed across the cell under illumination, is given by[2]

$$V = V_s + \left(\frac{\delta}{\varepsilon_i}\right) [(2e N_D \varepsilon_s)^{1/2} \{(V_{bi})^{1/2} - (V_{bi} - V_s)^{1/2}\} + e D_{ss} (E_{Fss} - E_g + \varphi_B)] , \tag{6.2}$$

where ε_i and ε_s are the permittivities of interfacial layer and semiconductor respectively, N_D is the donor density,

D_{ss} is the density of surface states, E_g is the band gap of the semiconductor, φ_B is the barrier height, and E_{Fss} is the quasi Fermi level at the surface, measured from the valence band edge.

The quantity ($E_{Fss} - E_g + \varphi_B$) ranges between V_s and $- V_i$, depending on whether the interface states follow the Fermi level of the semiconductor or that of the metal. If the tunneling of electrons between these states and the metal were easily accomplished, E_{Fss} would tend to follow the metal Fermi level. And, if this tunneling were extremely difficult, E_{Fss} would follow the semiconductor Fermi level. When the communication between the metal and interface states is extremely difficult, the voltage V is given by[2]

$$V = \left(1 + \frac{e D_{ss} \delta}{\varepsilon_i} \right) V_s + C \left[(V_{bi})^{1/2} - (V_{bi} - V_s)^{1/2} \right] \qquad (6.3)$$

and in the case of efficient communication between them, it is

$$V = V_s + \frac{C}{1 + \frac{e \delta D_{ss}}{\varepsilon_i}} \left[(V_{bi})^{1/2} - (V_{bi} - V_s)^{1/2} \right], \qquad (6.4)$$

where the constant $C = (2e N_D \varepsilon_s)^{1/2} \left(\frac{\delta}{\varepsilon_i} \right)$. (6.5)

It is found[2] that for difficult communication between metal and interface states (eq. 6.3), V increases

with increasing D_{ss}, whereas for the efficient communication between them (eq. 6.4), V decreases with the increase in D_{ss}.

For $V_s \ll V_{bi}$, eq. (6.3) may be written as

$$V_s \approx \frac{V}{N}, \tag{6.6}$$

$$\text{where } N = 1 + \frac{e\,\delta\,D_{ss}}{\varepsilon_i} + \frac{C}{2\sqrt{V_{bi}}}. \tag{6.7}$$

The potential drop across the interfacial layer, V_i, is obtained using the following boundary condition[22].

$$\varepsilon_s\, E_s^o = \varepsilon_i\, E_i^o = \varepsilon_i \left(\frac{\Delta - V_i}{\delta} \right), \tag{6.8}$$

where E_s^o and E_i^o are the electric fields on the two sides of the boundary between the semiconductor and the interfacial layer. The field E_s^o is obtained by solving the Poisson's equation

$$\vec{\nabla} \cdot \vec{E} = 4\pi\rho, \tag{6.9}$$

which gives

$$E_s^o = \frac{4\,\pi\,e\,N_D\,\omega}{\varepsilon_s} = \frac{4\,\pi\,Q_{sc}}{\varepsilon_s}, \tag{6.10}$$

where Q_{sc} is charge per unit area in the depletion region.

Fig. (6.1a) shows that the equilibrium potential drop across the interfacial layer is

$$\Delta = \varphi_m - \chi_s - \varphi_B , \tag{6.11}$$

where χ_s is the electron affinity of the semiconductor and φ_m is the metal work function.

Substituting eqs. (6.10) and (6.11) in eq. (6.8), the potential drop V_i is obtained as

$$V_i = \frac{\delta}{\epsilon_i} \left(\frac{\epsilon_i \Delta}{\delta} - 4 \pi Q_{sc} \right) . \tag{6.12}$$

Having obtained V_s and V_i, the current flowing through the device may now be determined.

The current density through the device consists of four components. These are the electron current density from metal to semiconductor J^e_{ms} , the electron current density from semiconductor to metal J^e_{sm}, the net hole current density at the edge of the depletion region, towards the junction $J_h(w)$, and the light generated hole current density in the depletion region J^L_h, which is towards the junction.

The components J^e_{ms} and J^e_{sm} may be obtained in the thermionic emission approximation or in the diffusion approximation. The deciding factor for these to be written in one of these approximations, is the electric field E^o_s in the

depletion region of the semiconductor[23]. In the present case, the field is of the order of 10^5 volts/cm. At such high fields, the thermionic emission approximation holds and not the diffusion approximation. Therefore, in thermionic approximation, J_{ms}^{e} and J_{sm}^{e} are written as follows.

$$J_{ms}^{e} = Tr\, A^{*}\, T^{2} \exp(-\beta\, \varphi_{s}) \exp(-\beta V_{1}) \tag{6.13}$$

$$J_{sm}^{e} = Tr\, A^{*}\, T^{2} \exp(-\beta\, \varphi_{s}) \exp(\beta V_{2}) \tag{6.14}$$

where, $\beta = \frac{e}{kT}$ and Tr is the transmission coefficient for the tunneling of electrons, given by[22]

$$Tr = \exp\left[- \frac{4\pi}{3h} \frac{(2m)^{1/2}\, \delta}{(\omega - V_{1})} \{(\chi_{s} + \omega - V_{1})^{3/2} - \chi_{c}^{3/2}\} \right], \tag{6.15}$$

m being the mass of electron.

The hole current densities J_{h}^{L} and $J_{h}(\omega)$ may be obtained in the same way as explained in the previous chapter (section 5.9); and their expressions are given by eqs. (5.27) and (5.30), respectively.

The net current density through the device (taking the directions of its components same as in the last chapter) is given by

$$J = J_{sm}^{e} - J_{ms}^{e} - J_{h}(\omega) - J_{h}^{L}. \tag{6.16}$$

Substituting the expressions for various components,

$$J = T r A^* T^2 \exp(-\beta \phi_B)(e^{\beta V_s} - e^{-\beta V_i}) - \left[\frac{e \alpha L_p \bar{\Phi} \exp(-\alpha \omega)}{1 + \alpha L_p} - \frac{e p_{no} D_p}{L_p}(e^{\beta V} - 1) \right] - e \bar{\Phi}(1 - e^{\alpha \omega}) \qquad (6.17)$$

This equation may be rewritten as

$$J = (J_n + J_h)(e^{\beta V} - 1) - J_{ph},$$

where $J_n = T r A^* T^2 \exp(-\beta \phi_B) \exp(-\beta V_i)$, $\qquad (6.18)$

$$J_h = \frac{e p_{no} D_p}{L_p}, \qquad (6.19)$$

and $J_{ph} = e \bar{\Phi} \left(1 - \frac{e^{-\alpha \omega}}{1 + \alpha L_p}\right)$. $\qquad (6.20)$

$\qquad (6.21)$

Taking into account the diode quality factor $n = \frac{\varepsilon_s \delta}{\varepsilon_i \omega} + 1$, the current density J becomes

$$J = (J_n + J_h)(e^{\beta V/n} - 1) - J_{ph}. \qquad (6.22)$$

This eq. (6.22) gives the current-voltage characteristics of SMSC. The light generated current density J_{ph} is greater than the reverse saturation current density $(J_n + J_h)$, which makes the current density J negative. Thus the device has the potentiality of a power generating device.

The power developed by the device is

$$P_{output} = VI \qquad (6.23)$$

and its conversion efficiency can be obtained as already defined in the last chapter.

6.1(b) Results and discussions

Now we present the results of the efficiency calculations done for the SBSC consisting of gold-silicon dioxide-n silicon system. In this case, the surface states are not supposed to be participating as charge transfer centres and only the tunneling of charge carriers through the interfacial layer is considered. The data used in the calculations are given in Table 6.1.

The conversion efficiency of the device is given by

$$\eta = \frac{P_{output}}{P_{input}} = \frac{V_{mp}\, I_{mp}}{P_{input}} . \qquad (6.24)$$

The maximum power output is obtained by differentiating the expression P = VI with respect to V and equating it to zero (I being the product of the current density J and the area of the device). This gives V_{mp}, the voltage corresponding to maximum power point in the V-I characteristic. The current I_{mp} is obtained by substituting V_{mp} for V in the expression for I. The results of these calculations are presented in Figs. 6.2 and 6.3.

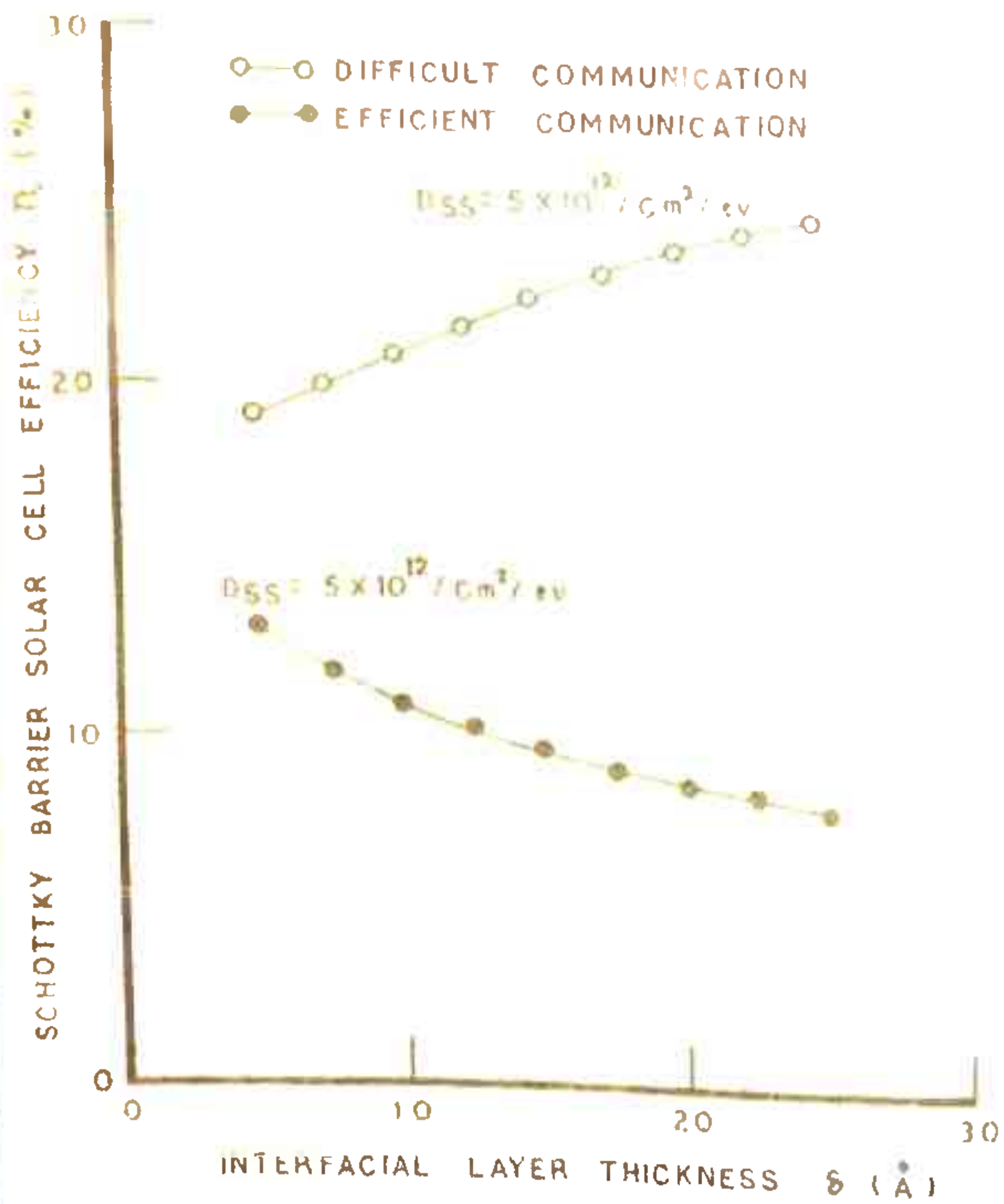


FIG. 6.2 VARIATION OF EFFICIE :Y η WITH INTERFACIAL LAYER THICKNESS δ FOR I ·ICULT AND EFFICIENT COMMUNICATION BETWEEN IN .FACE STATES AND METAL.

Table-6.1

Data used in efficiency calculations, when surface states are not supposed to be participating as recombination centres.

$e = 1.602\times10^{-19}$ Coul	$m = 9.108\times10^{-31}$ Kg
$k = 1.380\times10^{-23}$ Joule/°K	$T = 300$°K
$h = 6.625\times10^{-34}$ Joule-sec.	$\varepsilon_o = 8.854\times10^{-14}$ Farad/cm
$\varepsilon_s = 11.8\ \varepsilon_o$	$\varepsilon_i = 4.0\ \varepsilon_o$
$N_D = 1\times10^{17}$ cm^{-3}	$D_{ss} = 5\times10^{12}$ cm^{-2} eV^{-1}
$\varphi_m = 4.7$ eV	$\varphi_n = 0.8$ eV
$E_g = 1.12$ eV	$\chi_s = 4.05$ eV
$A^* = 120$ Amp.cm^{-2} °K^{-2}	$\alpha = 10^5$ cm^{-1}
$\tau_p = 10^{-5}$ sec.	$D_p = 10$ cm^2/sec
$N_c = 2.8\times10^{19}$ cm^{-3}	$N_v = 1.02\times10^{19}$ cm^{-3}
$N_i = 1.6\times10^{10}$ cm^{-3}	
$p_{no} = N_i^2/N_D = 2560$ cm^{-3}	$L_p = \sqrt{(D_p\ \tau_p)} = 10^{-2}$ cm

$\bar{\Phi}$ (Air Mass zero) = 4×10^{17} cm^{-2} sec^{-1}

P_{input}(AMO) = 135 milliwatts/cm^2.

Fig.6.2 shows the variation of the device efficiency with thickness of the interfacial layer for (i) difficult communication between metal and interface states and (ii) efficient communication between them. The transmission coefficient Tr for tunneling of electrons through the interfacial

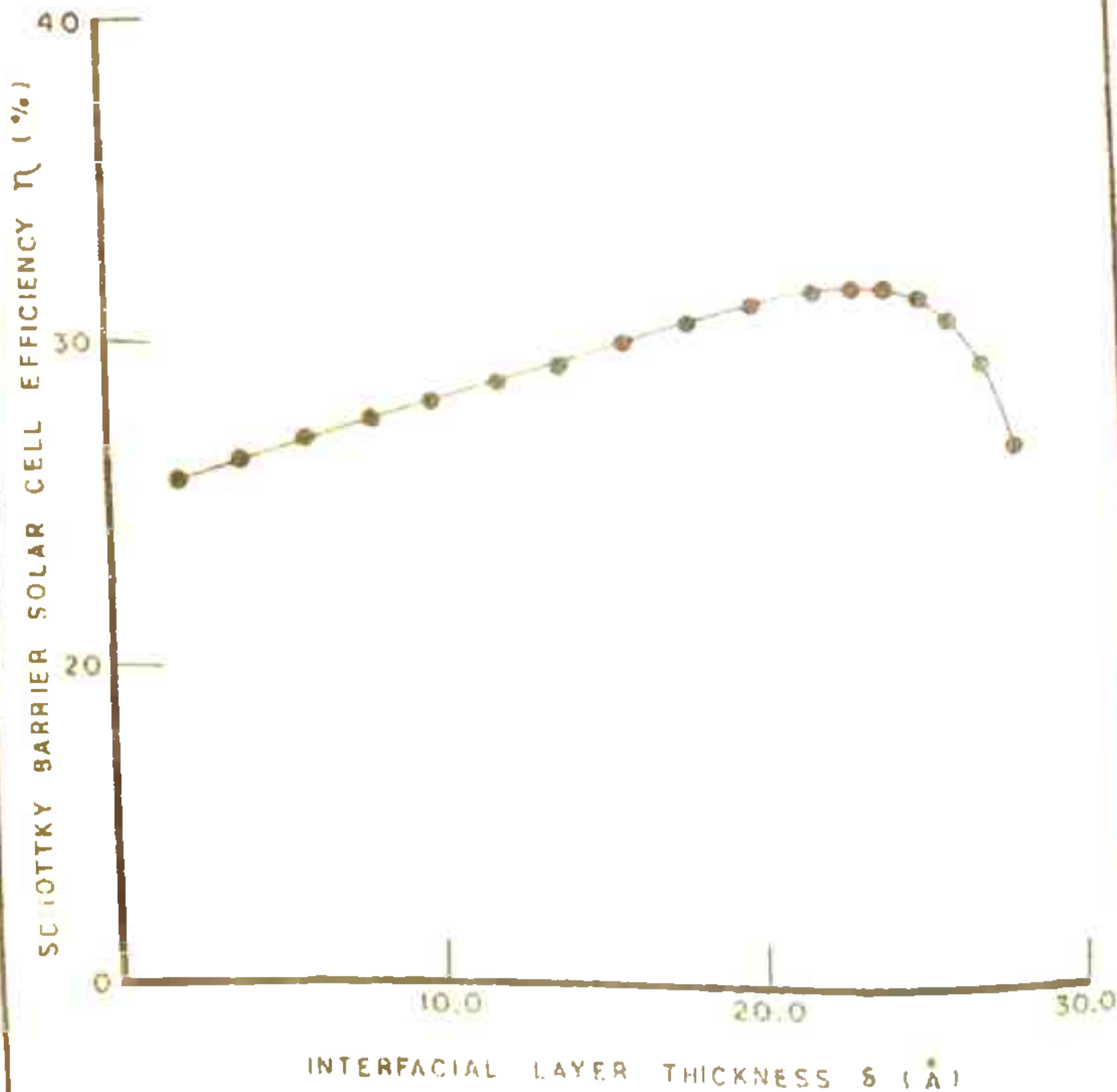


FIG. 6.3 EFFICIENCY η FOR SCHOTTKY BARRIER SOLAR CELL AS A FUNCTION OF INTERFACIAL LAYER THICKNESS δ WITH TRANSMISSION COEFFICIENT Tr.

layer is taken, in the present case, to be unity. Inspite of the fact that δ appears in the equation for voltage developed across the device, Fonash[2] did not consider its effect on the efficiency of the cell. It is obvious from the figure that for case (i), the efficiency increases with the increase in thickness of the interfacial layer, whereas for case (ii), the efficiency decreases with the increase in the interfacial layer thickness.

The effect of δ on efficiency of the cell in the case of difficult communication between metal and interface states (case (i) of Fig. 6.2) is shown in Fig. 6.3. Calculations were done only for this case and not for the other (case (ii) of Fig. 6.2), because in this case, the efficiency is higher and it increases with δ ; and our interest is to obtain maximum efficiency of the device. In these calculations, the non-unity value of the transmission coefficient Tr, as given by eq. (6.15), has been taken into account. Tr was taken to be unity by Fonash[2] and Landsberg and Klimpke[14], but as Fig. 6.2 (and also Fig. 6.8 for $\chi = 0$) whows, the efficiency increases when δ is increased. This, however, can not be unlimited, since it would mean that one could increase the efficiency to any high value by merely increasing the interfacial layer thickness. Moreover, for higher values of δ, the light generated current would also decrease and therefore, the efficiency can not just

go on increasing with δ. Fig. 6.3 shows that by properly taking into account the transmission coefficient , the efficiency first increases with increase in δ and after reaching a certain maximum value, it starts decreasing[24]. The variation of η with δ seems quite logical and it is concluded that there exists an optimum thickness of the interfacial layer, which gives the maximum efficiency of the device.

6.2 Surface states as recombination centres

The surface states act as centres of recombination of charge carriers, as mentioned earlier. The charges which get accomodated in these states, modify the potential and the field at the semiconductor surface. The effect of surface states, acting as recombination centres, on the efficiency of SBSC have been investigated in the present section.

6.2(a) Theory

Let Q_{ss} and Q_{sc} be the charges per unit area, in the surface states and the depletion region, respectively. The electric field $E_i(x)$ at a position x in the interfacial layer, is obtained, using Gauss's theorem, as

$$E_i(x) = \frac{1}{\epsilon_i} [\rho x - (Q_{ss} + Q_{sc})] , \tag{6.25}$$

where ρ is the charge density (charge per unit volume), assumed

to be present in the interfacial layer. Integrating eq. (6.25), the potential drop ($\Delta - V_i$) across the interfacial layer is obtained as

$$\Delta - V_i = -\int_{-\delta}^{0} \mathcal{E}_i(x)\, dx$$

$$\text{or} \quad \frac{\varepsilon_i}{\delta} (\Delta - V_i) = \frac{1}{2} \delta\rho + Q_{ss} + Q_{sc} \,. \qquad (6.26)$$

Under equilibrium condition this equation reduces to

$$\frac{\varepsilon_i}{\delta} \Delta = \frac{1}{2} \delta \rho_o + Q_{sso} + Q_{sco} \,. \qquad (6.27)$$

ρ_o , Q_{sso} and Q_{sco} are the corresponding quantities, when the cell is not illuminated.

V_i is obtained from eqs. (6.26) and (6.27), which give

$$- \frac{\varepsilon_i V_i}{\delta} = \frac{1}{2} \delta(\rho - \rho_o) + (Q_{ss} - Q_{sso}) + (Q_{sc} - Q_{sco}) \qquad (6.28)$$

Thus, knowing ρ , ρ_o , Q_{ss}, Q_{sso}, Q_{sc} and Q_{sco}, the potential drop V_i may be calculated and this gives also the potential drop V_s from eq. (6.1), i.e., $V = V_s + V_i$.

The charge density Q_{sc} in the depletion region is given by

$$Q_{sc} = e N_D w = \{2e \varepsilon_s N_D(V_{bi} - V_s) \}^{1/2}, \qquad (6.29)$$

which gives the charge density Q_{sco} as

$$Q_{sco} = \{ 2e \varepsilon_s N_D V_{bi} \}^{1/2}, \qquad (6.30)$$

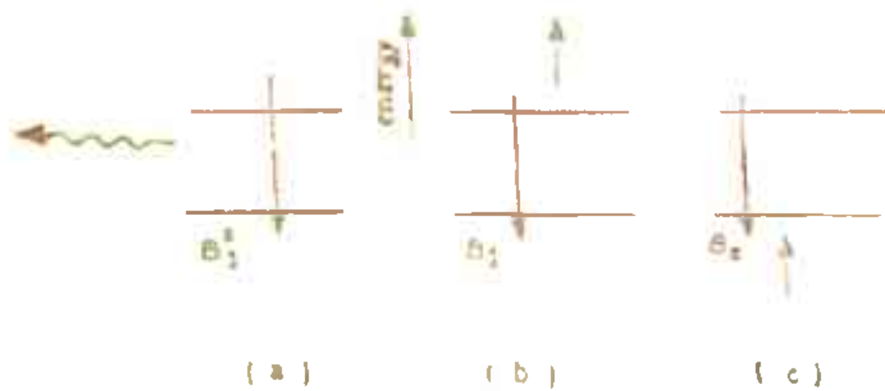


FIG. 6.4. DIAGRAM SHOWING BAND TO BAND UNAVOIDABLE RECOMBINATION OF CHARGE CARRIERS
(a) RADIATIVE RECOMBINATION
(b) ELECTRON EMISSION (c) HOLE EMISSION

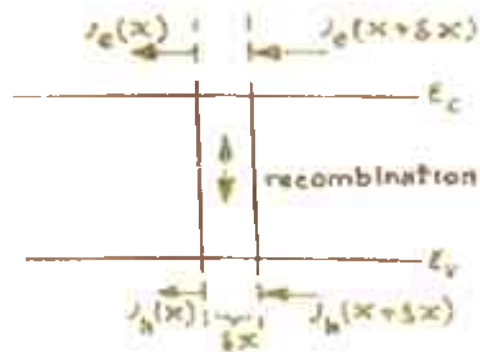


FIG. 6.5 DIAGRAM ILLUSTRATING CHARGE CONSERVATION.

since in equilibrium condition $V = V_i = V_s = 0$.

The charge densities in the surface states under illumination and non-illumination conditions, Q_{ss} and Q_{sso} respectively, are obtained by assuming a continuous distribution of surface states of density D_{ss} (per unit area per electron volt). The detailed evaluation of Q_{ss} and Q_{sso} is given in Appendix-A.

Thus, having obtained the potentials V_i and V_s from eqs. (6.28) and (6.1) respectively, the current flowing ~~the~~ through the device can now be calculated .

The recombination of charge carriers takes place through the surface states. Another cause of recombination is jumping of electrons from conduction band to valence band, which get trapped there. This is known as unavoidable band to band recombination. This takes place by three processes, namely, radiative recombination, electron emission and hole emission, (these processes are explained in Appendix-A for the electrons being trapped in the surface states). These are shown in Fig. 6.4, where B_1^s , B_1 and B_2 are the respective reaction constants for the three processes. The unavoidable recombination rate, as derived by Evans and Landsberg[25], is

$$U_{anav} = \bar{F} (np - n_i^2), \tag{6.31}$$

$$\text{in which } \bar{F} = B_1^s + B_1 n + B_2 p, \tag{6.32}$$

where n, p and n_i are respectively, the electron concentration in the conduction band, hole concentration in the valence band and the intrinsic carrier concentration. If F is the generation rate of electron-hole pairs, then the net recombination rate is (U-F), where U is the total recombination rate (due to both, the unavoidable recombination and the surface states).

Fig. 6.5 shows the electron and hole current densities, $J_e(x)$ and $J_h(x)$ at position x and $J_e(x + \delta x)$ and $J_h(x + \delta x)$ at position $x + \delta x$. The conventional current density has been taken to be positive from semiconductor to metal. The different current densities at the two positions show that the recombination is taking place in the region δx. The number of electrons lost per sec. due to recombination in this region, is

$$(U-F)\ \delta x = -\frac{1}{e}\left[J_e(x+\delta x) - J_e(x) \right] = -\frac{1}{e}\ \frac{dJ_e(x)}{dx}\ \delta x \qquad (6.33)$$

$$\text{or } e\ (U-F) = -\ \frac{dJ_e(x)}{dx}.$$

Similarly, for hole current density $J_h(x)$, we have

$$e\ (U - F) = \frac{dJ_h(x)}{dx}. \qquad (6.34)$$

Adding eqs. (6.33) and (6.34) and integrating, one gets

$$J_e(x) + J_h(x) = J = \text{constant}. \qquad (6.35)$$

This equation (6.35) gives the total current density J through the junction, under illumination, which at $x = 0$, is

$$J = J_e(0) + J_h(0), \tag{6.36}$$

$J_e(0)$ is the electron current density across the barrier and consists of two components J^e_{sm} and J^e_{ms}, which are due to the flow of electrons from semiconductor to metal and from metal to semiconductor, respectively. Therefore, the net electron current density from semiconductor to metal is

$$J_e(0) = J^e_{ms} - J^e_{sm} \tag{6.37}$$

in which J^e_{sm} and J^e_{ms} are the same as those given by eqs. (6.13 and (6.14). Therefore,

$$J_e(0) = -A^* T^2 \, Tr \exp(-\beta\varphi_B) \exp(-\beta V_i)(e^{\beta V} - 1). \tag{6.38}$$

In this equation, (6.38), Tr is the transmission coefficient for tunneling of electrons across the interfacial layer, which was taken to be unity by Fonash[2] and Landsberg and Klimpke[14]. Tr, as given by eq. (6.15), is dependent on δ. However, eq. (6.15 is found to reduce to a simpler form,

$$Tr = \exp\{-\sqrt{\chi_{eff}}\,\delta\}, \tag{6.39}$$

as given by Card and Rhoderick[26]. Here, χ_{eff} is the effective barrier height in eV and δ is the thickness of the interfacial layer in Angstroms.

The net current density J can also be written as

$$J = J_e(0) + J_h(\omega) + \int_0^{\omega} (F - U)\, dx, \tag{6.40}$$

because the hole current density $J_h(0)$, from semiconductor to metal, at $x = 0$, consists of two components: (i) The net hole current density at $x = \omega$, i.e., at the edge of the depletion region in the semiconductor bulk, represented by $J_h(\omega)$; and (ii) the contribution due to generation of holes, under illumination, in the depletion region. If $F(x)$ is the generation rate of charge carriers due to illumination and $U(x)$ is the net recombination rate, at a position x in the depletion region, this component of $J_h(0)$ is $\int_0^{\omega} (F-U)\,dx$. Thus, the total hole current at $x = 0$, is given as

$$J_h(0) = J_h(\omega) + \int_0^{\omega} (F-U)\,dx. \tag{6.41}$$

The net hole current density at $x = \omega$ is given by

$$J_h(\omega) = e\,D_p \left.\frac{dp}{dx}\right|_{x=\omega}, \tag{6.42}$$

where D_p is the diffusion coefficient and p is the hole concentration in the semiconductor valence band at a position x. $J_h(\omega)$ may be obtained by integrating the continuity equation for holes:

$$\frac{d^2p}{dx^2} - \frac{p - p_{no}}{D_p\,\tau_p} + \frac{F}{D_p} = 0, \tag{6.43}$$

where p_{no} is the hole concentration in the semiconductor bulk and τ_p is the life time for holes.

The generation rate $F(x)$, according to Gartner[27], is given by

$$F(x) = \alpha \Phi \exp(-\alpha x), \tag{6.44}$$

where both, the absorption coefficient of the material (silicon in the present case) α and the light flux density incident on the semiconductor, Φ (number of photons of a particular wavelength falling on unit area per second), are dependent on the wavelength of the photons. Therefore, to obtain the total generation rate, eq. (6.44) has to be integrated between the wavelength limits corresponding to 1.1 eV (energy gap of silicon) and 2.4 eV. These two limits define the cut off wavelengths λ_1 and λ_o. The net generation rate is, thus, given by

$$F(x) = \int_{\lambda_o}^{\lambda_1} \alpha \Phi e^{-\alpha x} \, d\lambda \tag{6.45}$$

Now, solving eq. (6.43), after substituting eq. (6.45), one gets the hole current density as

$$J_h(a) = \int_{\lambda_o}^{\lambda_1} \frac{e\alpha L_p \Phi e^{-\alpha a}}{1 + \alpha L_p} \, d\lambda - J_h^o \tag{6.46}$$

where $J_h^o = \dfrac{e p_{no} D_p (e^{\beta V} - 1)}{L_p}$.

The first term in eq. (6.46) represents the generation of holes due to illumination and the second term J_h^o represents the recombination in the bulk.

Now we evaluate the contribution to the current density from the depletion region, by substituting for F(x) from eq.(6.45).

$$e\int_0^{\omega}(F-U)\,dx = \int_{\lambda_0}^{\lambda_1} e\,\bar{\Phi}\,(1-e^{-\alpha\omega})\,d\lambda - e\int_0^{\omega} U\,dx$$

$$= J_{DL} - J_{rec} \qquad (6.47)$$

Here, J_{DL} is the current due to light being absorbed in the depletion region and J_{rec} is the net recombination current density which is due to band to band recombination (J_{unav}) and interfacial recombination (J_{ifr}).

$$J_{rec} = J_{unav} + J_{ifr} \qquad (6.48)$$

Thus, the net current density through the device is

$$J = J_e(0) + J_h(0) = J_e(0) + [\,J_h(\omega) + J_{DL} - J_{rec}\,]$$

$$= J_e(0) + \left[\int_{\lambda_0}^{\lambda_1} \frac{e\alpha L_p \bar{\Phi}\, e^{-\alpha\omega}}{1+\alpha L_p}\,d\lambda - J_h^o + J_{DL} - J_{rec}\right]$$

$$= J_{ph} + [\,J_e(0) - J_h^o - J_{rec}\,],$$

where $$J_{ph} = \int_{\lambda_0}^{\lambda_1} \frac{e\alpha L_p \bar{\Phi}\, e^{-\alpha\omega}}{1+\alpha L_p}\,d\lambda + \int_{\lambda_0}^{\lambda_1} e\,\bar{\Phi}\,(1-e^{-\alpha\omega})\,d\lambda$$

$$= \int_{\lambda_0}^{\lambda_1} e\,\bar{\Phi}\left[1 - \frac{e^{-\alpha\omega}}{1+\alpha L_p}\right]d\lambda. \qquad (6.49)$$

The net current density may be written as

$$J = -\,(J_D - J_{ph}) \qquad (6.50)$$

where J_D represents the dark current of the device and J_{ph} is the total light generated current. The negative sign is coming because the current density J is taken to be positive in the reverse direction. eq.(6.49) shows that the

light generated current is independent of x. However, J_{ph}, being a function of the width ω of the depletion region, depends upon the voltage developed by the cell. The voltage dependence of ω is given by

$$\omega = \left[\frac{2 \varepsilon_s (V_{bi} - V_s)}{eN_I} \right]^{1/2} \tag{6.51}$$

The determination of the recombination current density J_{rec} is explained in Appendix-B.

The power developed by the device is obtained by P= VI, where the current I is equal to the area of the device times the current density J given by eq. (6.50). The conversion efficiency, once again, is calculated in the way explained in the previous chapter.

6.2(c) Results and discussions

The efficiency calculations, in this case also, were done for SBSC consisting of the gold - silicon dioxide - n silicon system. Here, the surface states are taken to be participating as recombination centres for the charge carriers. The data used in these calculations are given in Table 6.2. The conversion efficiency η is finally obtained, using the relation, (eq. 6.24),

$$\eta = \frac{V_{mp} \; I_{mp}}{P_{input}} \quad ;$$

and the maximum power point, $P_{max} = V_{mp} \; I_{mp}$, is determined from the current-voltage plot for the cell.

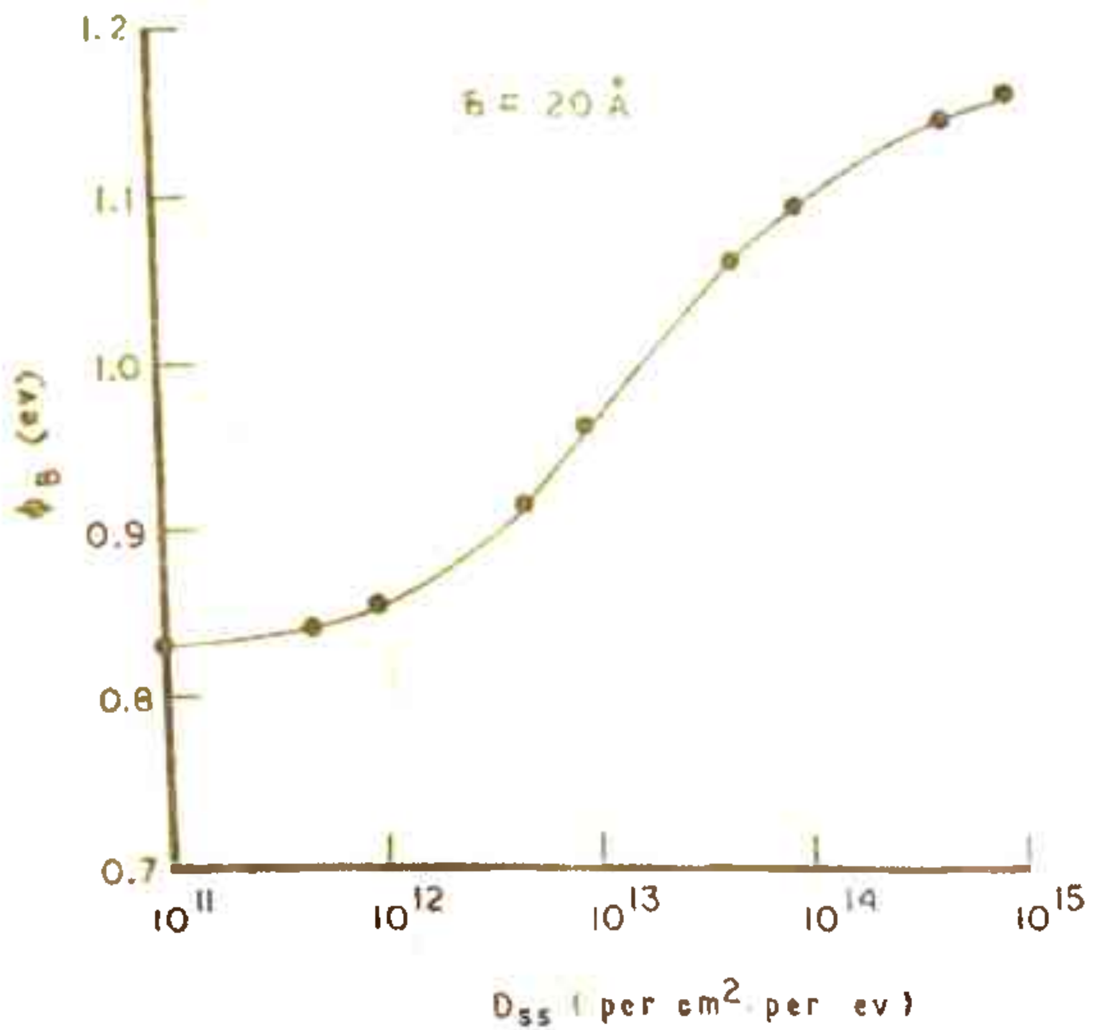


FIG. 6.6 EFFECT OF DENSITY OF SURFACE STATES ON THE BARRIER HEIGHT

Table-6.2

Data used in efficiency calculations, when the surface states are considered to be participating as recombination centres.

$q = 1.602 \times 10^{-19}$ Coul.

$k = 1.380 \times 10^{-23}$ Joule/^{o}K

$\epsilon_s = 11.8\ \epsilon_o$

$N_D = 3 \times 10^{17}$ cm^{-3}

$E_g = 1.12$ eV

$A^{*} = 120$ Amp cm^{-2} ^{o}K^{-2}

$N_c = 2.8 \times 10^{19}$ cm^{-3}

$\tau_p = 3.33 \times 10^{-7}$ sec

$p_{no} = N_i^{2}/N_D = 853$ cm^{-3}

$B_1^{s} = 1 \times 10^{-11}$ cm^3 sec^{-1}

$T_1^{s} = T_2^{s} = 1.12 \times 10^{-8}$ cm^3 sec^{-1}

$T_1 = T_2 = T_3 = T_4 = 3.66 \times 10^{-25}$ cm^6 sec^{-1}

P_{input} (Air Mass 1) = 106 milliwatts cm^{-2}

$\epsilon_o = 8.854 \times 10^{-14}$ Farad/cm

$T = 300^{o}$K

$\epsilon_i = 4.0\ \epsilon_o$

$\phi_m = 4.7$ eV

$\chi_s = 4.05$ eV

$n_i = 1.6 \times 10^{10}$ cm^{-3}

$N_v = 1.02 \times 10^{19}$ cm^{-3}

$D_p = 11$ cm

$L_p = \sqrt{(D_p \tau_p)} = 1.9 \times 10^{-3}$ cm

$B_1 = B_2 = 1.2 \times 10^{-32}$ cm^6 sec^{-1}

Values of α and $\bar{\Phi}$ have been taken from references 23 and 28, respectively; and J_{ph} has been evaluated by numerical integration

Fig. 6.6 shows the effect of density of surface states (D_{ss}) on the barrier height ϕ_B of the SBSC, as obtained by substituting eq. (6.27) in eq. (6.11) for a fixed value of δ. It shows that the barrier height first increases and then becomes

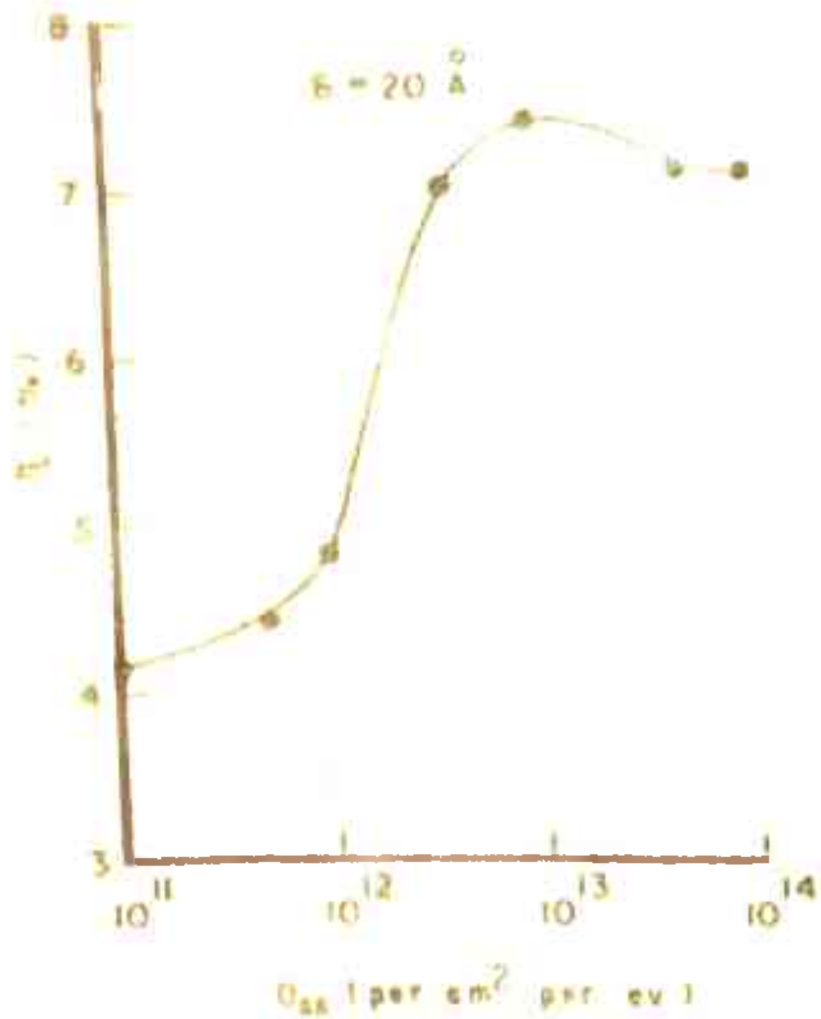


FIG. 6.7 EFFECT OF DENSITY OF SURFACE STATES ON THE EFFICIENCY OF SBSC.

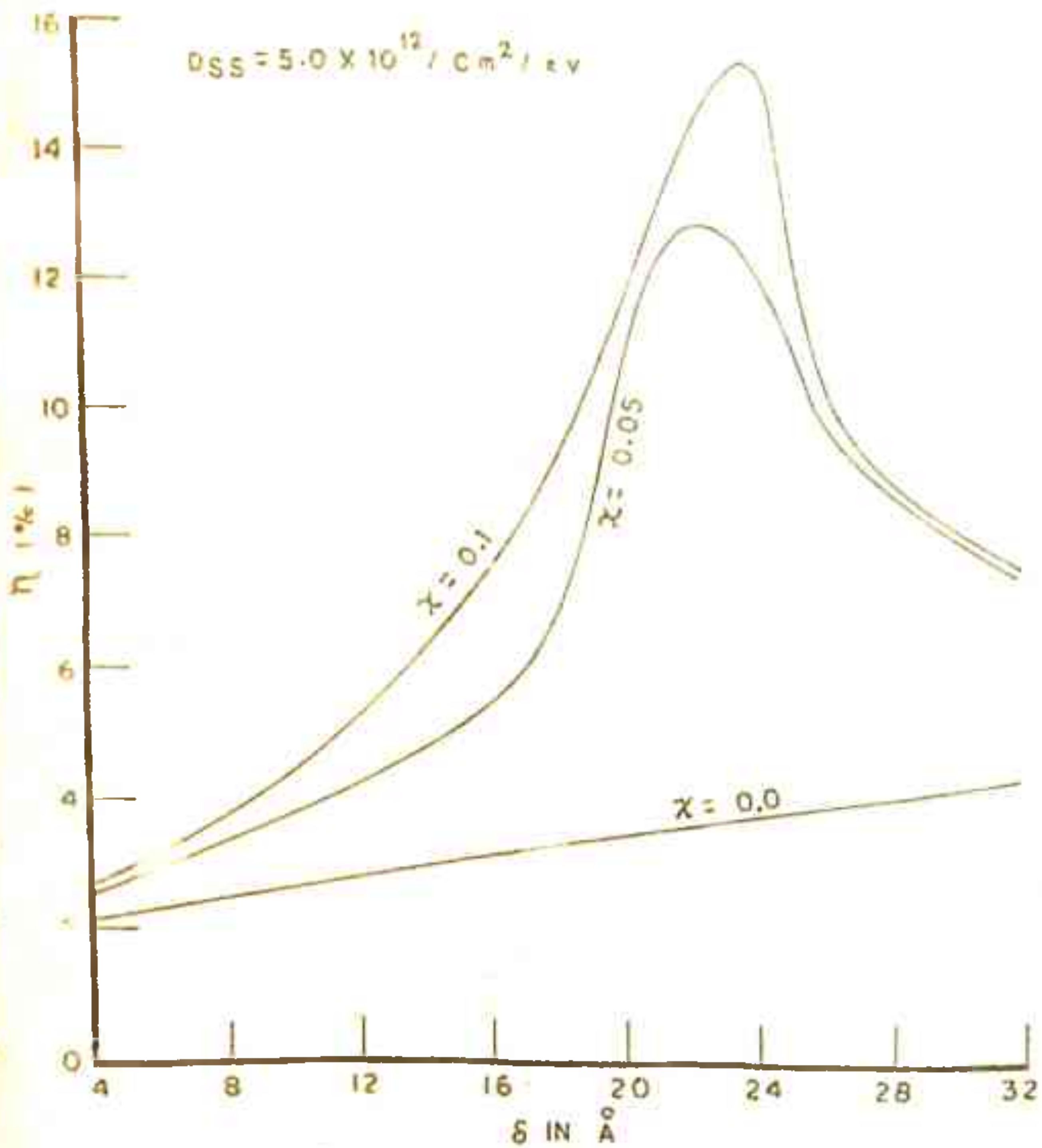


FIG. 6.8 EFFECT OF INTERFACIAL LAYER THICKNESS AND TRANSMISSION COEFFICIENT ON THE EFFICIENCY OF SCHOTTKY BARRIER SOLAR CELL

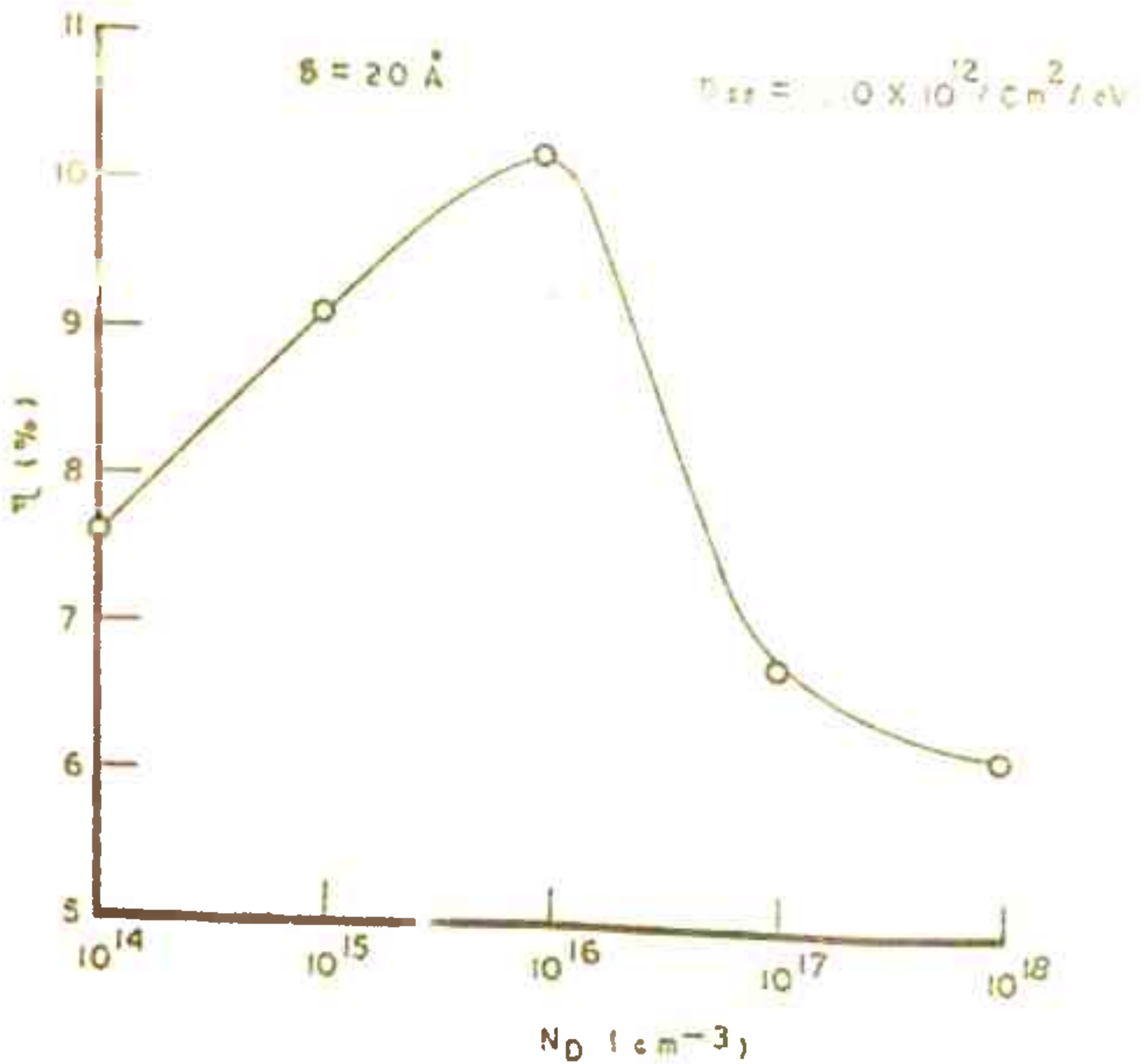


FIG. 6.9 EFFECT OF DONOR CONCENTRATION ON THE EFFICIENCY OF SBSC

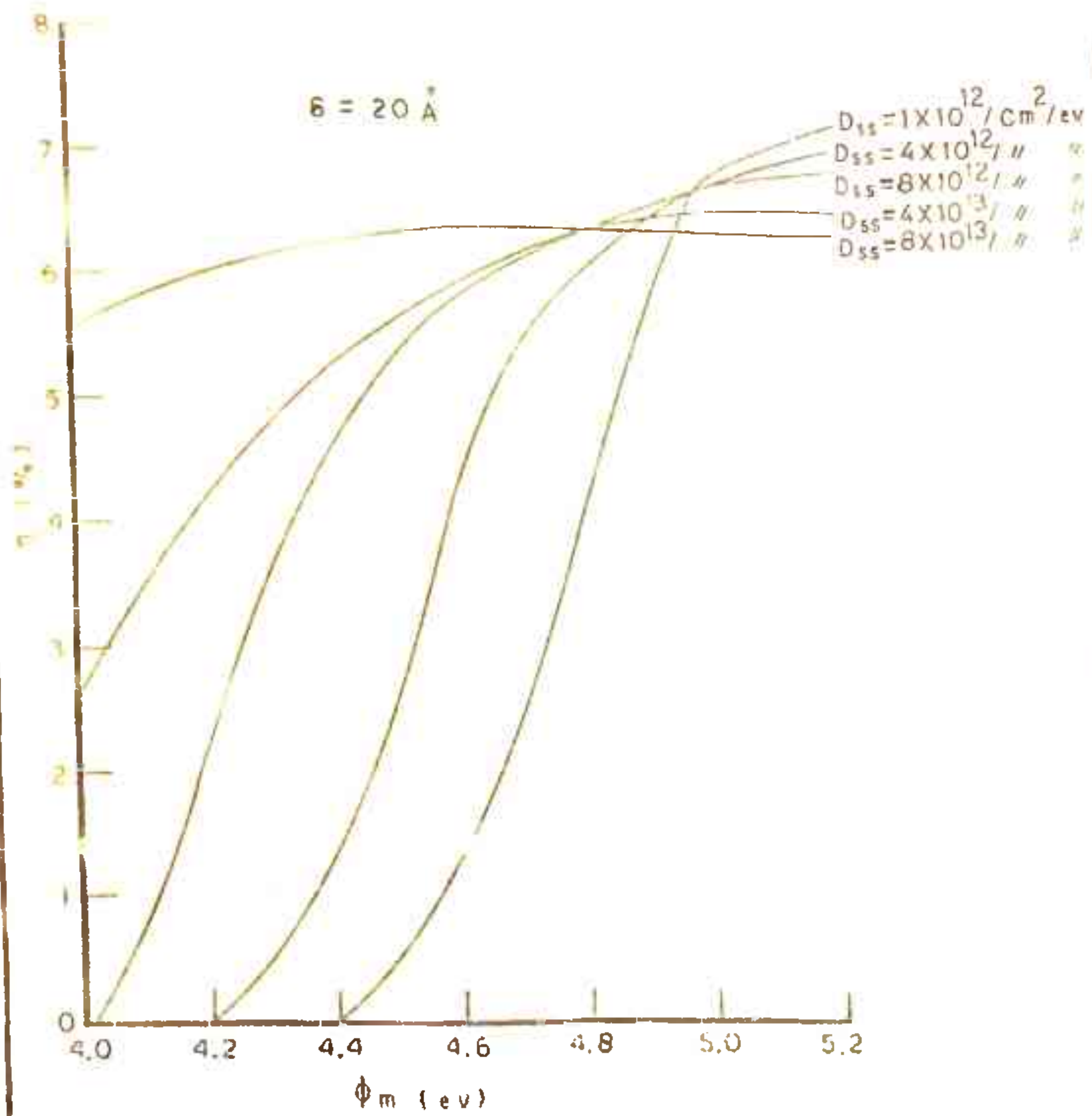


FIG 6.10 EFFECT OF METAL WORK FUNCTION ON THE EFFICIENCY OF SBSC.

constant, if D_{ss} is kept increasing.

The results of the efficiency calculations, for a more realistic case of the surface states actively participating in charge transfer mechanism, are presented in Figs. 6.7 to 6.10. The transmission coefficient Tr (given by eq. 6.39) has properly been taken into account in this study. The effect of density of surface states (D_{ss}) on the efficiency of SBSC is shown in Fig. 6.7. The efficiency of the cell is found to be first increasing with the increase in D_{ss} and then decreasing with further increase in D_{ss}. The increase in efficiency is attributed to the increase in barrier height, (φ_B increases with D_{ss} upto D_{ss} ~10^{14}/ cm^2 per eV; when D_{ss} becomes greater than 10^{15}, φ_B becomes constant) For further increase in D_{ss}, the recombination through surface states also increases which pulls down the efficiency. The results[29] for constant δ are shown in Figs. 6.6 and 6.7.

The effect of interfacial layer thickness δ on the efficiency is shown in Fig. 6.8, for the average barrier heights χ= 0.0, 0.05 and 0.1. The curve for χ = 0.0 (i.e., Tr unity) shows that η increases with increase in δ. The η vs. δ curves for χ = 0.05 and 0.10 show that the thickness of the insulating layer should be optimized to give the maximum efficiency. Consideration of Tr also reduces the dark current density, which is necessary for increasing the power generating current density J (= J_{dark} - $J_{light\ generated}$), because smaller the value of

dark current density (J_{dark}), greater will be the power generating current.

The results of Figs. 6.3 and 6.8 are in agreement with the experimental observation of Lillington and Townsend[8] that an optimum thickness of interfacial layer gives the maximum conversion efficiency[29] of the cell.

The effects of donor density and metal work function are shown in Figs. 6.9 and 6.10, respectively. The efficiency curve of the device for different doping densities also passes through a maximum. The two factors which vary with the doping density or the substrate resistivity, are the diffusion length (through mobility) and the minority carrier lifetime. The efficiency of the cell is found to decrease for the values of $N_D > 10^{17}/cm$, because the minority carrier lifetime becomes very very small for high doping[30] ($\tau_p(N_D) = \tau_{po}/[1+(N_D/N_{Do})]$, where τ_{po} and N_{Do} are constants). Shewchun et al[31] have found an optimum acceptor density around $10^{17}/cm^3$, whereas Fig. 6.9 shows the optimum donor density to be around $10^{16}/cm^3$.

The metal work function φ_m is not found to have much effect on the conversion efficiency η for high values of D_{ss}, whereas for low D_{ss}, η increases as φ_m increases. This may be attributed to the fact that φ_B does not increase much with the increase in φ_m for high values of D_{ss}, but for low D_{ss}, φ_B increases appreciably with φ_m.

REFERENCES

(Chapter - VI)

1. R.J. Stirn and Y.C.M. Yeh, 10th IEEE Photovaltaic Specialists Conf., New York (1973)
2. S.J. Fonash, J. Appl. Phys., 46, 1286 (1975)
3. J.P. Ponpon and P. Stiffert, J. Appl. Phys., 47 ,3248 (1976)
4. S.J. Fonash, 11th IEEE Photovoltaic Specialists Conf., New York, page 376 (1975)
5. S.J. Fonash, Proc. Third Int. Conf. Thin Films at Budapest, Hungary, paper 11-16, Aug. (1975)
6. S.J. Fonash, J. Appl. Phys., 47 , 3597 (1976)
7. D.L. Pulfrey, IEEE Trans. Electron Devices, ED-23 , 588 (1976)
8. D.R. Lillington and W.G. Townsend, Appl. Phys. Lett., 28 , 97 (1976)
9. R.J. Stirn and Y.C.M. Yeh, Appl. Phys. Lett., 27 95 (1975)
10. J.P. Ponpon and P. Stiffert, Extended Abstracts No. 0309, page 466, Int. Solar Energy Congress (ISEC), New Delhi, Jan. (1978)
11. J. Shewchun, R. Singh and M. A. Green, J. Appl. Phys., 48 , 765 (1977)
12. W.A. Anderson, J. K. Kim and A.E. Delahoy, IEEE Trans. Electron Devices, ED-24, 453 (1977)
13. J.A.St. Pierre, R. Singh, J. Shewchun and J.J. Loferski. 12th IEEE Photovoltaic Specialists Conf., New York, page 847 (1976)

14. P.T. Landsberg and C. Klimpke, Proc. Royal Soc. London, A 354 , 101 (1977)

15. C. Klimpke and P.T. Landsberg, 12th IEEE Photovoltaic Specialists Conf., New York, page 868 (1976)

16. L.C. Olsen, Solid State Electronics, 20 , 741 (1977)

17. L.C. Olsen, 12th IEEE Photovoltaic Specialists Conf., New York, page 854 (1976)

18. M.K.V.V. Thampuran, T. Lakshmi Vishwanathan and R.Sharan, Extended Abs. No. 171, page No. 422, Int. Solar Energy Congress, New Delhi, Jan. (1978)

19. Y.C.M. Yeh and R.J. Stirn, 11th IEEE Photovoltaic Specialists Conf., New York, page 391 (1975)

20. J.A. Roger, J. Pivot and C.H.S. Dupuy, Coloque Int. 'Electricite Solaire' (Toul house: C.E.N.E.S. 1976)

21. W.A. Anderson, A.E. Delahoy and R.A. Milano, J. Appl. Phys., 45 , 3913 (1974)

22. V.I. Strikha, Radio Engg. Electronics Phys., 9 ,552 (1964)

23. S.M. Sze, 'Physics of Semiconductor Devices', John Wiley and Sons., Inc., U.S.A. (1969)

24. S. Srivastava, N.K. Swami and H.M. Ghule, Proc. National Solar Energy Convention, Jadavpur, Calcutta, Nov. 29-Dec. 1 (1976)

25. D.A. Evans and P.T. Landsberg, Solid State Electronics, 6 , 169 (1963)

26. H.C. Card and E.H. Rhoderick, J. Phys. D, 4 , 1589(1971)

27. W.W. Gartner, Phys. Rev., 116 , 84 (1959)

28. J.J. Loferski, J. Appl. Phys., 27 , 777 (1956)

29. S. Srivastava, N. K. Swami and H. M. Ghule, to be presented at National Solar Energy Convention, Bhavnagar, Dec. (1978).

30. J.G. Fossum, Solid State Electronics, 19 , 269 (1976)

31. J. Shewchun, R. Singh and M. A. Green, J. Appl. Phys. 48 , 765 (1977)

....

Appendix-A

DETERMINATION OF CHARGES IN THE SURFACE STATES

Assuming a continuous distribution of surface states of density D_{ss} (per unit area per eV), the number of occupied states n_t in the forbidden energy gap, at the interface, x = 0, is given by

$$n_t = \int_{E_v}^{E_c} D_{ss} f_t \, dE_t \, , \tag{A.1}$$

where f_t is the probability for a state of energy E_t to be charged. It follows from eq. (A.1) that the number of occupied states under equilibrium conditions, is given by

$$n_{to} = \int_{E_v}^{E_c} D_{ss} f_{to} \, dE_{to} \, . \tag{A.2}$$

The function $f_{to} = 1/[1 + \exp\{\beta(E_{to} - \mu)\}]$, (A.3)

where $\beta = e/(kT)$ and μ denotes the equilibrium Fermi level.

To calculate the charge per unit area Q_{sso} in the surface states in equilibrium , a level φ_o is introduced such that states below it are donors and those above it are accepto The value of φ_o is measured from the top of the valence band at the surface. As the states below φ_o are donors (donor states are neutral when occupied by electrons and positively charged when empty), the probability for them to be neutral or occupied is ($1 - f_{to}$).

Therefore,

$$Q_{sso} = e \int_{0}^{\varphi_o} (1 - f_{to})\, D_{ss}\, dE_{to} - e \int_{\varphi_o}^{E_g} f_{to}\, D_{ss}\, dE_{to} \tag{A.4}$$

$$= e\, D_{ss}\, \varphi_o - e\, D_{ss} \int_{0}^{E_g} \frac{dE_{to}}{1 + \exp\{\beta(E_{to} - \mu)\}}$$

$$Q_{sso} = e\, D_{ss}\, \varphi_o + D_{ss}\, kT \left[\ln \left\{ \frac{1 + \exp(\beta \varphi_B)}{1 + \exp\{\beta(\varphi_B - E_g)\}} \right\} - \beta E_g \right] \tag{A.5}$$

Similarly, Q_{ss}, the charge per unit area in the surface states when the device is illuminated, can be written

as $$Q_{ss} = e\, D_{ss}\, \varphi_o - e n_t , \tag{A.6}$$

where $$n_t = \int_{E_v}^{E_c} D_{ss}\, f_t\, dE_t . \tag{A.7}$$

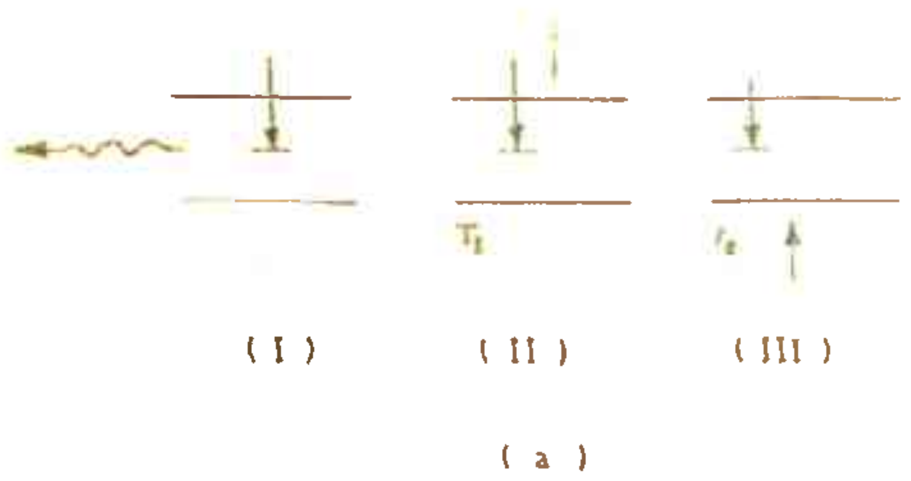
The occupation function f_t (reference 25 of chapter VI) is given by

$$f_t = \frac{G(0)\, n(0) + H(0)\, p_1(0)}{G(0)\{n(0) + n_1(0)\} + H(0)\{p(0) + p_1(0)\}} \tag{A.8}$$

In eq. (A.8), $n(0)$ and $p(0)$ are the electron and hole concen-trations in the conduction band and the valence band, respectively, under illumination and $n_1(0)$ and $p_1(0)$ are the respective concen-trations when the Fermi level is at the trap energy in thermo-dynamic equilibrium. The function $G(0)$ and $H(0)$ are the following.

$$G(0) = T_1^S + T_1\, n(0) + T_2\, p(0) \tag{A.9}$$

$$H(0) = T_2^S + T_3\, n(0) + T_4\, p(0) \tag{A.10}$$



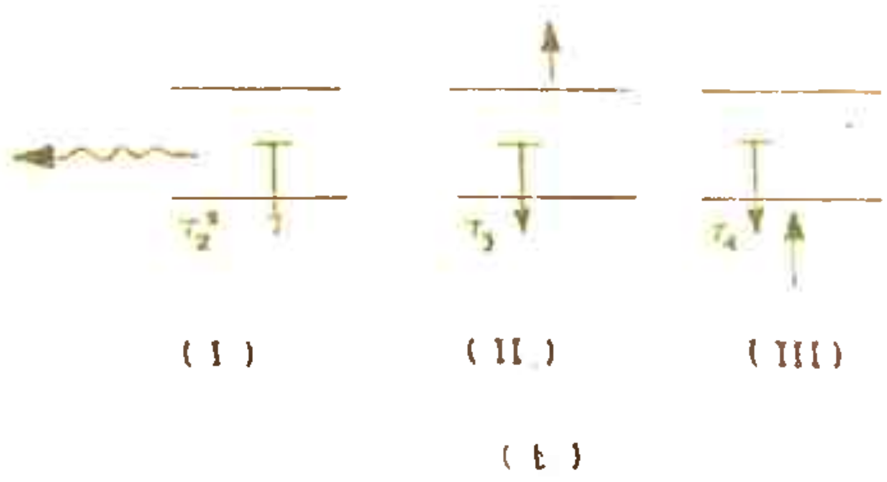


FIG. A.1 DIAGRAM SHOWING RECOMBINATION OF CHARGE CARRIERS DUE TO SURFACE STATES.

(a) ELECTRON CAPTURE

(b) HOLE CAPTURE

(I) RADIATIVE RECOMBINATION (II) ELECTRON EMISSION (III) HOLE EMISSION

T_1^s, T_1, T_2, T_2^s, T_3 and T_4 are the reaction constant described below.

The functions G and H correspond to the electron capture and hole capture, respectively. The electron and hole capture processes due to the presence of surface states in the forbidden energy gap, are shown in Fig. A.1a and A.1b, respectively. Fig. A.1a(i) shows that an electron from the conduction band is captured by the surface state acting as a trap and the energy lost by the electron goes out as a photon. This is known as 'radiative recombination'. Fig. A.1a (ii) shows the emission of an electron by Auger process. The energy released by the captured electron is taken away by an electron in the conduction band which goes to a higher energy level. The energy released by the captured electron can also be taken away by hole in the valence band which would also go to a higher energy state. Fig. A.1a(iii) shows the equivalence of this with the electron energy, where the motion of hole in the downward direction is equivalent to the motion of electron in the upward direction. T_1^s, T_1 and T_2 are the reaction constants for the above three electron capture processes, respectively.

The hole capture process is shown in Fig. A.1b, which also takes place in three ways. Figs. A.1b(i), (ii) and (iii) show the hole capture by radiative recombination, electron emission and hole emission processes, respectively. The third one

shows the equivalent electron motion, in place of the hole motion. T_2^E, T_3 and T_4 are the reaction constants for these three hole capture processes, respectively.

The eq. (A.7), when integrated and substituted in eq. (A.6), gives the charge per unit area in the interface states Q_{ss} under illumination conditions.

$$Q_{ss} = e D_{ss} \varphi_o + \frac{D_{ss} kT}{2} \ln \frac{M_1}{M_2} - \frac{G(0)n(0) - H(0)\,p(0)}{(A-B)\,G(0)\,n_o(0)} \ln \frac{N_1}{N_2} \qquad (A.11)$$

$$M_1 = H(0)\,p_o(0) \exp(-2\beta\varphi_B) + \exp(-\beta\varphi_B)[G(0)n(0) + H(0)p(0)] + G(0)\,n_o(0) \qquad (A.12)$$

$$M_2 = H(0)p_o(0) \exp[2\beta(E_g-\varphi_B)] + \exp[\beta(E_g-\varphi_B)]\{G(0)n(0) \qquad (A.13)$$

$$+ H(0)p(0)\} + G(0)\,n_o(0) \qquad (A.14)$$

$$N_1 = [\exp(\beta\varphi_B) - A][\exp\{\beta(\varphi_B - E_g)\} - B] \qquad (A.15)$$

$$N_2 = [\exp(\beta\varphi_B) - B][\exp\{\beta(\varphi_B - E_g)\} - A]$$

$$\left.\begin{matrix} A \\ B \end{matrix}\right\} = - \frac{\{G(0)\,n(0) + H(0)\,p(0)\}}{2G(0)\,n_o(0)} \pm \left[\left[\frac{G(0)n(0) + H(0)\,p(0)}{2G(0)\,n_o(0)}\right]^2 - \frac{H(0)p_o(0)}{G(0)n_o(0)}\right]^{1/2} \qquad (A.16)$$

***

Appendix-B

DETERMINATION OF RECOMBINATION CURRENTS

There are two types of recombination currents, as explained in chapter VI. One is the recombination current due to electrons jumping from conduction band to valence band and recombining there with holes. This constitutes the unavoidable recombination current density J_{unav}. The other type of recombination takes place through the surface states and J_{ifr} denotes the current density due to recombination in the interface states.

Determination of J_{unav}

The unavoidable recombination rate U_{unav}, given by eq. (6.31), is

$$U_{unav} = (B_1^s + B_1 n + B_2 p)(np - n_i^2) \quad (B.1)$$

Therefore, the unavoidable recombination current density J_{unav} can be written as

$$J_{unav} = e \int_0^w U_{unav} \, dx \quad (B.2)$$

The electron and hole concentrations in the conduction and valence bands, respectively, are

$$n = N_c \exp [\beta (E_{Fn} - E_c)] \quad (B.3)$$

$$\text{and } p = N_v \exp [\beta (E_v - E_{Fp})], \quad (B.4)$$

where N_c and N_v are the density of states in the conduction

and valence bands, respectively, and E_{Fn} and E_{Fp} are the quasi Fermi levels for electrons and holes, respectively, such that $E_{Fn} - E_{Fp} = V$, where $0 < x \leq \omega$, and $E_{Fn} = E_{Fp}$ when $x >> \omega$ (i.e., in the bulk).

Solving the Poisson's equation,

$$\nabla^2 \varphi_s(x) = - \frac{\text{charge in depletion region}}{\epsilon_s},$$

the potential function $\varphi_s(x)$ in the depletion region is obtained as

$$\varphi_s(x) = \text{constant} - \frac{eN_D}{2\epsilon_s} (x - \omega)^2. \qquad (B.5)$$

$$\qquad (B.6)$$

The constant in eq. (B.6) is obtained from Fig. 6.1b, by applying the condition that at $x = \omega$, $E_{Fn} - E_c = -V_n$. This gives the value of the constant in eq. (B.6) as $-V_n$ and therefore,

$$E_{Fn} - E_c = - \{ V_n + \frac{eN_D(x - \omega)^2}{2\epsilon_s} \} . \qquad (B.7)$$

To evaluate the potential difference ($E_v - E_{Fp}$) the boundary condition to be taken is that at $x = \omega$, $E_{Fp} - E_v = E_g - V - V_n$. This gives the constant in eq. (B.6) for this case as $E_g - V_n - V$. Therefore,

$$E_{Fp} - E_v = (E_g - V_n - V) - \frac{eN_D}{2\epsilon_s} (x - \omega)^2. \qquad (B.8)$$

Substituting eqs. (B.7) and (B.8) in eqs. (B.3) and (B.4), respectively, the electron and hole concentrations in the depletion region are found to be

$$n(x, V) = N_c \exp[-\beta (V_n + \frac{e N_D}{2\varepsilon_s}(x-\omega)^2)] \quad (B.9)$$

$$p(x, V) = N_v \exp[\beta \{\frac{e N_D}{2\varepsilon_s}(x-\omega)^2 + V_n + V - E_g\}]. \quad (B.10)$$

Eqs. (B.9) and (B.10) give the equilibrium concentrations of electrons and holes in the depletion region, when the $x = \omega$ and $V = 0$ are put in them.

$$n_{no} = N_c \exp(-\beta V_n) \quad (B.11)$$

$$p_{no} = N_v \exp\{\beta(V_n - E_g)\} \quad (B.12)$$

Thus, n_i is given by

$$n_i^2 = n_{no}\, p_{no} = N_c N_v \exp(-\beta E_g). \quad (B.13)$$

Substitution of eqs. (B.9), (B.10) and (B.13) in equation (B.2), gives the unavoidable recombination current density as

$$J_{unav} = e N_c N_v (e^{\eta} - 1) e^{-\eta_g} [\omega B_1^s + B_1 N_c e^{-\varphi_n} I_1 \quad (B.14)$$

$$+ B_2 I_2 N_v \exp(\varphi_n + \eta - \eta_g)], \quad (B.15)$$

where $\varphi_n = \beta V_n$, $\eta_g = \beta E_g$, $\eta = \beta V$,

$$I_1 = \int_0^{w} \exp\left[-\lambda(x-w)^2 \right] dx \qquad (B.16)$$

$$I_2 = \int_0^{w} \exp\left[\lambda(x-w)^2 \right] dx$$

$$\text{and} \quad \lambda = \frac{e^2 N_D}{2kT\epsilon_s} \, . \qquad (B.17)$$

Thus by evaluating the integrals in eq. (B.16) and substituting them in eq. (B.14), one gets the current density J_{unav}.

Determination of J_{ifr}

Landsberg and Klimpke (ref. 14 of chapter VI) genera-
lized the results of Evans and Landsberg(ref. 25 of chapter VI),
which were given for the discrete trapping level, to a conti-
nuous distribution of surface states in the forbidden energy gap
at the surface (located at x = 0) and found that the recombi-
nation rate R through these states is given by

$$R = \left[n(0)\,p(0) - n_i^2 \right] . \; G(0)\,H(0)\,D_{ss}\,I \, , \qquad (B.18)$$

where $I = \int_{E_v}^{E_c} \left[G(0)\left[n(0)+n_1(0)\right] + H(0)\left[p(0)+p_1(0)\right] \right]^{-1} dE_t .$

Eq. (B.18), after the evaluation of I, gives the recombination
rate due to interface states as

$$R = \left[n(0)\,p(0) - n_i^2 \right] \frac{H(0)\, D_{ss}\, kT}{n_o(0)\, e(A-B)} \ln \frac{K_1}{K_2} \, , \qquad (B.19)$$

where

$$K_1 = \{ \exp(\beta\varphi_B) - A \} [\exp \{ \beta(\varphi_B - E_g)\} - A] \quad (B.20)$$

$$K_2 = \{ \exp(\beta\varphi_B) - B\} [\exp \{\beta(\varphi_B - E_g)\} - B] . \quad (B.21)$$

A and B are defined by eq. (A.16) of Appendix-A.

Thus, eq. (B.19) gives the interface state recombination current density as

$$J_{ifr} = e R . \quad (B.22)$$

...