Chapter 3

Design and Simulation of UPQC-DG

3.1 Preamble

UPQC-DG configuration has certain advantages over combination of separate UPQC and DG (solar) inverter. In UPQC-DG shunt APF feeds power available from solar PV to load eliminating additional solar inverter (which is costly). Also filter capacitor at the output of boost converter is not required as there is already a large capacitor connected at DC link of UPQC-DG. Careful design and simulation of such complex power electronics systems as UPQC-DG is necessary for its desirable performance.

In this work, solar PV is selected as DG source due to its renewable and environment friendly nature. PV array is connected at DC link of UPQC-DG via a boost DC-DC converter as shown in Fig. 3.1. This configuration of UPQC-DG is based upon three phase three wire supply system, which is most common configuration of UPQC [1]. This configuration has three major components or Power Electronic Converters: shunt APF, series APF and DC-DC boost Converter. Both series and shunt APFs are IGBT based three phase three leg bridge inverters sharing a common DC link. Single phase series injection transformers are used in each phase to inject voltage produced by series APF. Interfacing inductors are used at the output of each APF.

High pass RC filters are used at the output of series and shunt APFs to filter out high frequency components in voltage or current, generated by PWM switching of these APFs. RC time constant of these filters is kept small so that high frequency components will pass through them.

In this chapter, conventional approach of design of UPQC-DG and its MATLAB simulation have been presented, which is also serve as basis for chapters that follow,

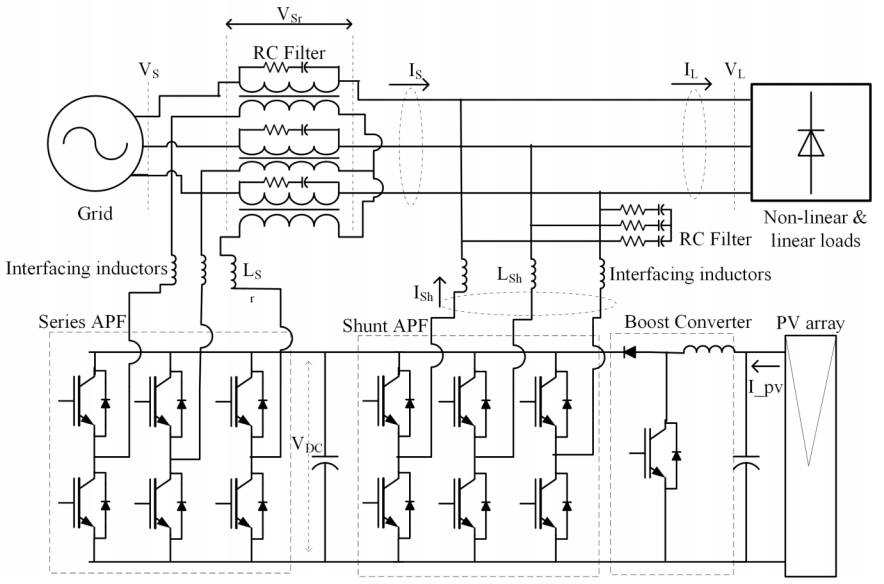

Figure 3.1: Configuration of UPQC-DG with solar PV connected to DC link via a boost converter

which incorporate new control techniques developed in present thesis. In section 3.2, design of UPQC-DG is described, and in section 3.3, MATLAB simulation is presented for a case study system.

3.2 Design Procedure of UPQC-DG

Design of UPQC or UPQC-DG consists of two steps: (1) Sizing of series APF, shunt APF and series transformer, (2) Design of passive filter elements used at output of converters [2–5]. In present configuration of UPQC-DG, design of DC-DC converter is additional [6, 7]. Both the sizes of converters and values of passive filters depend on specifications of load, DG, & grid and compensation requirements. In case study system of present work, a three-phase, three-wire distribution system has been considered. solar PV array has been considered as DG, since it has major scope in Indian scenario. Load has been taken as mix of non-linear and linear reactive (R-L) loads. The specifications of case study system have been shown in Table. 3.1.Design procedure for UPQC-DG has been explained in following subsections:

3.2.1 Design of DC link

The minimum value of DC link voltage of VSC is twice the peak of output phase voltage, and it is computed using Eq. 3.1, where V_{LL} is rms value of line-to-line voltage and m is modulation index.

$$V_{DC,min} = 2\sqrt{2}V_{LL}/\sqrt{3}m \tag{3.1}$$

Keeping V_{LL} as 415 V, and m as 1.0, the minimum value of DC link voltage is found to be 677.7 V and nominal (reference) DC link voltage is selected as 700 V.

DC link capacitor should be large enough to supply instantaneous energy to shunt/series converters during transients. Using the principle of energy conservation, Eq. 3.2 is obtained, where C_{DC} is DC link capacitance, V_{DC} is nominal DC link voltage, k_1 is per unit variation in energy during transients, a is overloading factor, V is rated phase voltage, I is rated phase current of shunt APF, and t is the time in which DC link voltage is to be restored [2].

$$\frac{1}{2}C_{DC}(V_{DC}^2 - V_{DC,min}^2) = 3k_1aVIt \tag{3.2}$$

From Eq. 3.2, using $V_{DC} = 700$ V, $V_{DC,min} = 677.7$ V, $k_1 = 0.1$, $a = 1.15$, $V = 239.6$ V,$I = 50.2$ A (shunt APF current considering reactive power compensation and PV power injection), $t = 20$ ms, the value of C_{DC} is obtained as 5560 μF and it is selected as 5500 μF.

Table 3.1: Parameters of system

3-phase supply	415 V, 50 Hz, R_S = .08 Ω, L_S = 0.24 mH
Load-1	3-phase rectifier (R_{DC} = 26 Ω, P_{DC} = 12 kW)
Load-2	3-phase R-L load (20 kW, 0.707 p.f. lagging)
Load-3	3-phase R-L load (10 kW, 0.707 p.f. lagging)
PV array	P_{MPP} = 15.3 kW, V_{MPP} = 545 V

3.2.2 Design of Shunt APF

Interfacing AC inductance of shunt APF is related to m, V_{DC}, a, switching frequency (f_S), and current ripple ($I_{cr,pp}$) as given by Eq. 3.3 [4]:

$$L_{sh} = \sqrt{3} m V_{DC} / 12 a f_S I_{cr,pp} \tag{3.3}$$

Using $m = 1.0$, $V_{DC} = 700$ V, $a = 1.15$, $f_S = 12$ kHz, $I_{cr,pp} = 10\%$ of 50.2 A, Value of L_{Sh} is computed as 1.46 mH and it is selected as 1.5 mH.

Per phase current rating of shunt APF is 50.2 A and rated phase voltage is equal to load voltage, which is maintained constant by series APF. So, three phase VA rating of shunt APF is found to be 41.5 kVA.

RC filter is selected based on following criteria [2]:

1. The time constant of filter should be much less than the fundamental time period.

2. Filter should offer low impedance at high frequency and high impedance at fundamental frequency.

So, R & C values of filter are selected as 5 Ω, and 10 μF leading to time constant of 50 μs and impedance of 318 Ω at 50 Hz, & 5.93 Ω at 5 kHz.

Voltage and current ratings of switches (IGBTs) are computed using Eq. 3.4, & 3.5 as 770 V, 95.1 A respectively. Practically available switches of ratings higher than computed values are selected for realization of shunt APF.

$$V_{sw} = V_{DC} + V_{d,peak} \tag{3.4}$$

$$I_{sw} = 1.25(I_{cr,pp} + I_{peak}) \tag{3.5}$$

3.2.3 Design of Series APF

Series APF is connected in series with supply using injection transformers. Output voltage of the transformer depends on sag/swell compensation requirements. For 40% sag/swell compensation, rated series output voltage equals to $239.6 \times 0.4 = 95.8$ V, so maximum turns ratio of transformer is given by Eq.3.6, and it is taken as 1.0 in present work.

$$n_{T,max} = V_{VSC} / V_{Sr} = 415 / (95.8 \times \sqrt{3}) = 2.5 \tag{3.6}$$

During sag, source voltage reduces, so source current increases to supply same amount of load power. Source current is also the secondary or output current of series injection transformer, so its current rating depends on source current during sag, which is computed:

$$I_{S,sag} = P_L/3(V_S - V_{Sr}) \tag{3.7}$$

For total load of Tab. 6.1, active power (P_L) is 42 kW, Nominal source voltage per phase (V_S) is 239.6 V, and series voltage during 40% sag is 95.8 V. Using these values, $I_{S,sag}$ is found to be 97.4 A. Correspondingly, the VA rating of series transformer (including all three phases) is found to be 28 kVA. Since all the power flowing through injection transformer also flows through series APF, the rating of series APF is assumed to be equal to that of injection transformer.

Interfacing inductance of series APF depends on source current during swell, which is computed using Eq. 3.8 as 41.7 A.

$$I_{S,swell} = P_L/3(V_S + V_{Sr}) \tag{3.8}$$

Eventually the AC interfacing inductance is calculated using Eq. 3.9, in which $m = 1.0$, $V_DC = 700$ V, injection transformer turns ratio (n_T)=1.0, $a = 1.15$, $f_S = 10$ kHz, $I_{cr,pp}$ is 5% of $I_{S,swell}$. Value of L_{Sr} is calculated as 4.0 mH and it is taken as 4.5 mH.

$$L_{Sr} = \sqrt{3}mV_{DC}n_T/12af_SI_{cr,pp} \tag{3.9}$$

RC filter of series APF is selected based on same criteria of shunt APF, but lower resistance and higher capacitance is chosen for series APF for effective elimination of ripples from output voltage of series APF which has less magnitude in comparison to terminal voltage of shunt APF. R & C values of filter are chosen as 2 Ω and 20 μF respectively. Resultant time constant, impedance at 50 Hz, and impedance at 5 kHz are 40 μs, 159.2 Ω, and 2.6 Ω respectively.

Voltage rating of switches of series APF is same as that of shunt APF since DC link is common. RMS current rating of series APF devices is given by current handled by it during sag, which is 97.4 A.

3.2.4 Design of Solar PV array

Solar PV array is chosen so that it would supply one third of total load power at maximum power point. SunPower SPR-305E-WHT-D PV module is selected in this

work for constructing PV array and its manufacturer's specifications are shown in Table. 3.2. Ten such PV modules are connected in series to form a string and five such strings are connected in parallel to form complete PV array. Parameters of solar

Table 3.2: Specifications of solar PV module

Maximum Power	305.2 W
Number of cells per module	96
Open circuit voltage	64.2 V
Short circuit current	5.96 A
Voltage at MPP	54.7 V
Current at MPP	5.58 A

PV array at standard test conditions (1000 W/m^2, 25°) are shown in Table. 3.3.

Table 3.3: Parameters of solar PV array

Maximum Power	15.3 kW
Open circuit voltage	642 V
Short circuit current	30.3 A
Voltage at MPP	547 V
Current at MPP	27.9 A

3.2.5 Design of DC-DC converter

DC-DC converter input rated input voltage is 545 V, which is maximum power point at standard environmental conditions. Output voltage of converter is DC link which is 700 V, so the converter is designed to be a boost converter. Range of input voltage is taken as 500-575 V to support variations in PV output. For stable CCM mode of operation the inductance of boost converter is found using Eq. 3.10 [6]:

$$L_B = V_{PV}(V_{DC} - V_{PV})/\Delta I_L f_S V_{DC} \tag{3.10}$$

In Eq. 3.10, $V_{PV} = 545$ V, $V_{DC} = 700$ V, $\Delta I_L = 2.0$ A, $f_S = 15$ kHz, which yield $L_B = 4.02$ mH, and it is selected as 5 mH.

Considering maximum input current and voltage of boost converter, its VA rating is estimated to be 16.1 kW. As discussed in previous section, the output capacitive filter of boost converter is not needed since there is large DC link capacitor already present at output.

3.3 Modeling and Simulation of UPQC-DG

In this section, modeling and simulation of conventional UPQC-DG using MATLAB/Simulink is presented. In following chapters real-time simulation results for proposed control techniques have been presented, which have been performed in Opal-RT. Since the simulations of Opal-RT are implemented in the real time simulator using MATLAB/Simulink, these simulations form basis for it. So, MATLAB/Simulink simulations of UPQC-DG have been presented in here.

3.3.1 Modeling of UPQC-DG in MATLAB/Simulink

MATLAB model of UPQC-DG shown in Fig. 3.1, is implemented using 'Sim-power-sytems' block sets of Simulink library. Main Simulink file containing all major components of MATLAB model are shown in Fig. 3.2. A three phase grid (source) is modeled using a programmable three phase source block, which can be used to simulate disturbances such as voltage sag, swell or harmonics. Solar PV model with boost converter and MPPT control is shown in Fig. 3.3. Three phase loads including non-linear and linear loads are shown in Fig. 3.4. Simulation time step is kept as 10 μs.

Parameters of MATLAB model are calculated using procedure followed in 3.2, and their selected values are shown in Table 3.4. A three phase supply of 415 V, 50 Hz with source resistance R_S and inductance L_S is selected. Load-1, a non-linear load, consists of a three phase diode bridge rectifier with DC side connected to series combination of R and L. Load-2 is linear constant power load. For this system dc link voltage V_{DC}, and capacitor C_{DC} is selected. n_T and S_T are turns ratio and kVA rating of each series injection transformer. L_{Sh}, and L_{Sr} are AC interfacing inductors used for connecting shunt and series APFs. L_b is value of inductor used in boost converter.

SunPower SPR-305E-WHT-D, PV module is selected in this work for simulating PV array. Ten such PV modules are connected in series to form a string and fifteen

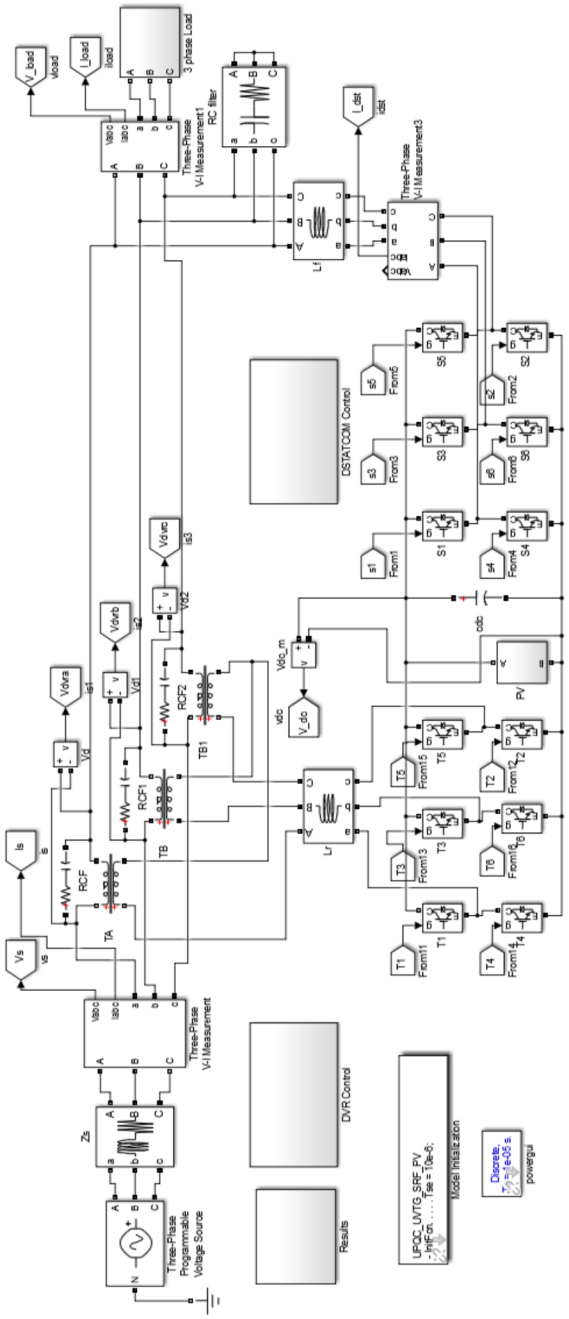

Figure 3.2: MATLAB/Simulink model of PV based UPQC-DG

such strings are connected in parallel to form complete PV array. For solar PV array modeling predefined model of MATLAB (SimPowerSystems toolbox) is used. This

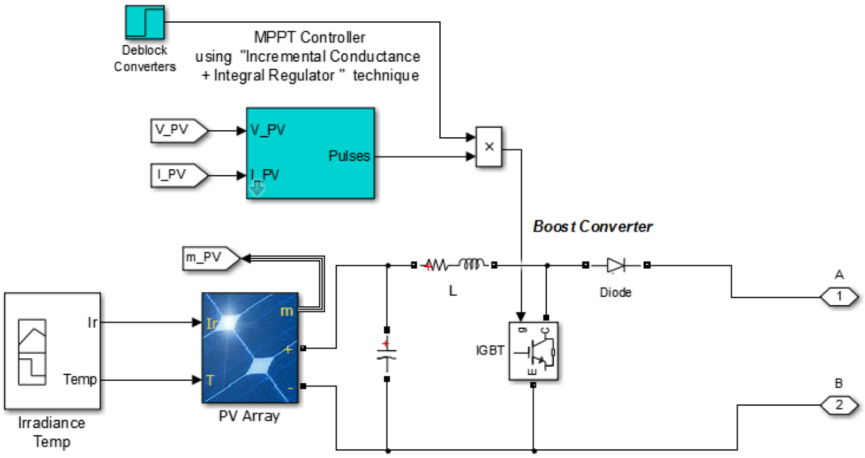

Figure 3.3: MATLAB Simulink model of Solar PV array

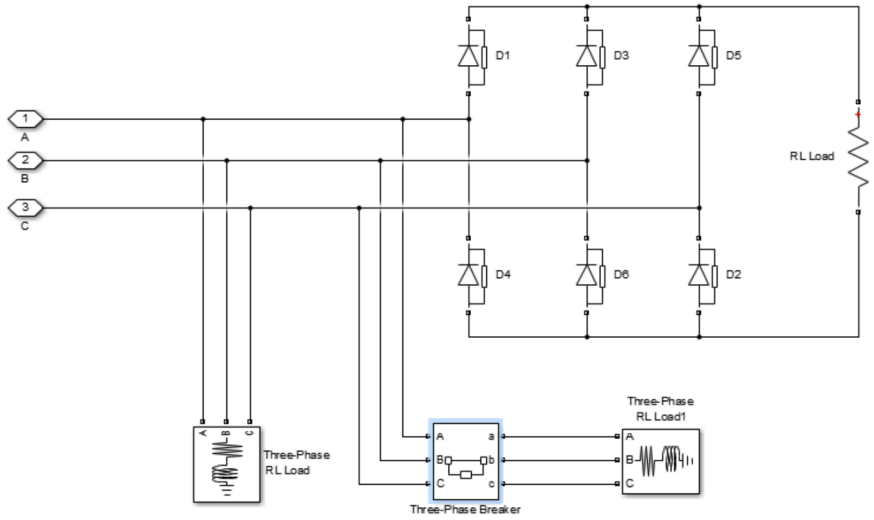

Figure 3.4: MATLAB Simulink model of three phase load

predefined model is based on equivalent circuit of solar PV using a controlled current source with diode in parallel, series and shunt resistances. This model of solar PV is best suited for power electronics circuit analysis and simulation [8]. Parameters of equivalent circuit of PV array are calculated internally by MATLAB. Parameters of solar PV array at standard test conditions (1000 W/m^2, 25°) are shown in Table. 3.3. Because voltage at MPP is below the DC link voltage, a boost converter is necessary.

Table 3.4: Parameters of UPQC-DG

3 Phase supply	415 V, 50 Hz, R_S = .05 Ω, L_S = 0.25 mH
DC link	V_{DC} = 700 V, C_{DC} = 5500 μF
Shunt APF	42 kVA, L_{Sh} = 1.5 mH
Series APF	29 kVA, L_{Sr} = 4.5 mH, n_T = 1, S_T = 29 kVA
Series transformer	10 kVA (each phase), n_T = 1 (240/240 V)
Boost Converter	V_I = 500-550 V, V_O = 700 V, L_b = 5 mH
Load-1	thyristor bridge rectifier (R = 26 Ω)
Load-2	3-phase R-L load (20 kW, 0.707 p.f. lagging)
Load-3	3-phase R-L load (10 kW, 0.707 p.f. lagging)

3.3.2 Control of UPQC-DG

In conventional UPQC, shunt APF compensates for current based power quality issues by injecting appropriate current into system and series APF compensates for voltage based power quality issues by injecting suitable series voltage. Shunt APF also takes care of DC link voltage regulation. In UPQC-DG configuration, shunt APF has to perform additional task of supplying DG power to load and/or grid. DC-DC converter gives required change in voltage for connecting DG to DC link and provides duty ratio control to track maximum power generated by DG in case of solar PV and wind. It is to be noted that in this section only UPQC-P control strategy (in which series APF compensates only for transient disturbances and injects voltage in phase with source current, as discussed in previous chapter) has been shown. Power angle control will be demonstrated from next chapter. Details of control of each of three converters are described as follows.

SRFT is used for control of Shunt APF (Fig. 3.5). SRFT is based on extraction and manipulation of currents, so making it simpler to incorporate the current fed by solar PV directly in the control block. Measurements of three phase source voltages, three phase load currents, DC link voltage and three phase source currents are used in this control scheme. Fundamental component of load current is extracted using abc-dq0 (Park's) transformation using Eq. 3.11 and ωt signal required for this

transformation is generated by three phase PLL applied on source (grid) voltages.

$$\begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{L0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} sin\omega t & sin(\omega t - \frac{2\pi}{3}) & sin(\omega t + \frac{2\pi}{3}) \\ cos\omega t & cos(\omega t - \frac{2\pi}{3}) & cos(\omega t + \frac{2\pi}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} \tag{3.11}$$

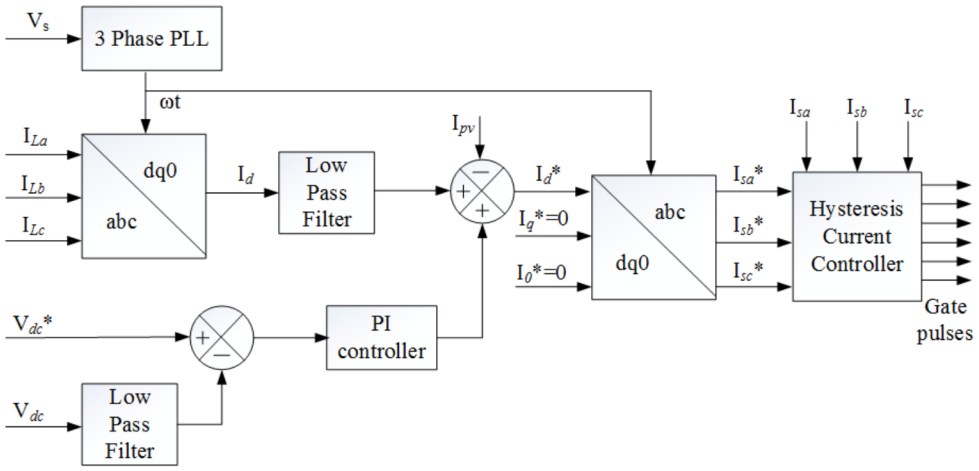

Figure 3.5: Control of shunt APF

This transformation converts fundamental components to dc quantity which is easily extracted using a low pass filter. As shown in Fig. 3.5, output current of PV array is subtracted from the d-axis (fundamental) component of load current (I_{Ld}) because the difference of two needs to be supplied by grid. Current required for maintaining voltage of DC link is estimated by a PI controller and added to I_{Ld} to form reference d-axis current ($I_d{}^*$). The q-axis components and zero axis components are assumed to be zero to get three phase balanced reference source currents from $I_d{}^*$ using dq0 to abc (inverse Park's) transform.

Series APF is controlled using Unit Vector Template Generation (UVTG) technique [9]. It is simple and reduces the computation burden on the system. In this technique no PI controller is used as envisaged from its block diagram shown in Fig. 3.6. Thus, PI tuning is also not required. A three phase PLL is used to generate *wt* corresponding to phase A (reference phase) fundamental component of source voltage, which then is utilized to generate three phase balanced unit vectors using

(2).

$$\begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} = \begin{bmatrix} sin\omega t \\ sin(\omega t - 2\pi/3) \\ sin(\omega t + 2\pi/3) \end{bmatrix} \tag{3.12}$$

The desired (reference) magnitude of load voltage is multiplied to these vectors to get reference load voltage signals. Sensed load voltage signals and reference load voltage signals are then fed to voltage PWM controller of series APF.

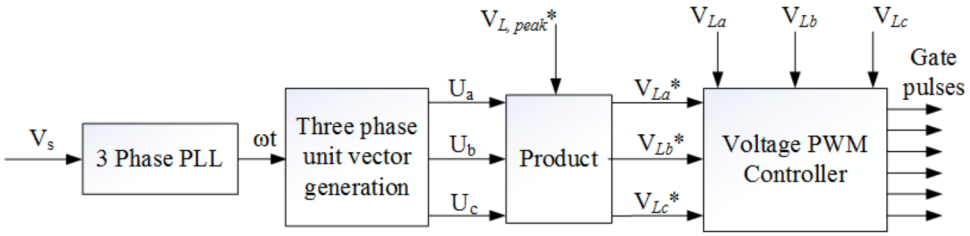

Figure 3.6: Control of series APF

A boost DC-DC converter is used to step up the voltage at DG terminal to DC link voltage, and to extract maximum available power from DG using Maximum Power Point Tracking (MPPT) control. There are various MPPT algorithms available for solar PV such as Perturb and Observe algorithm and Incremental Conductance algorithm. In this work Incremental Conductance algorithm with integral regulator is used [10]. From P-V curve of solar PV $dP/dV = 0$, at Maximum Power Point (MPP). This yields:

$$\frac{dI}{dV} = -\frac{I}{V} \tag{3.13}$$

Integral regulator minimizes the error $(dI/dV + I/V)$ and gives correction in duty cycle in order to track MPP.

3.3.3 Simulation Results and Discussion

Designed UPQC-DG system is simulated in MATLAB/Simulink for steady state, variation in solar irradiation, voltage sag, swell, harmonics, and change in load. These cases are described as follows:

In steady state shunt APF compensates for load current based power quality issues namely harmonics and reactive power. Due to shunt compensation, source current (I_S) is kept sinusoidal and in-phase with source voltage (V_S) Fig. 3.7. DC link voltage is held constant and series APF doesn't inject any voltages in steady state

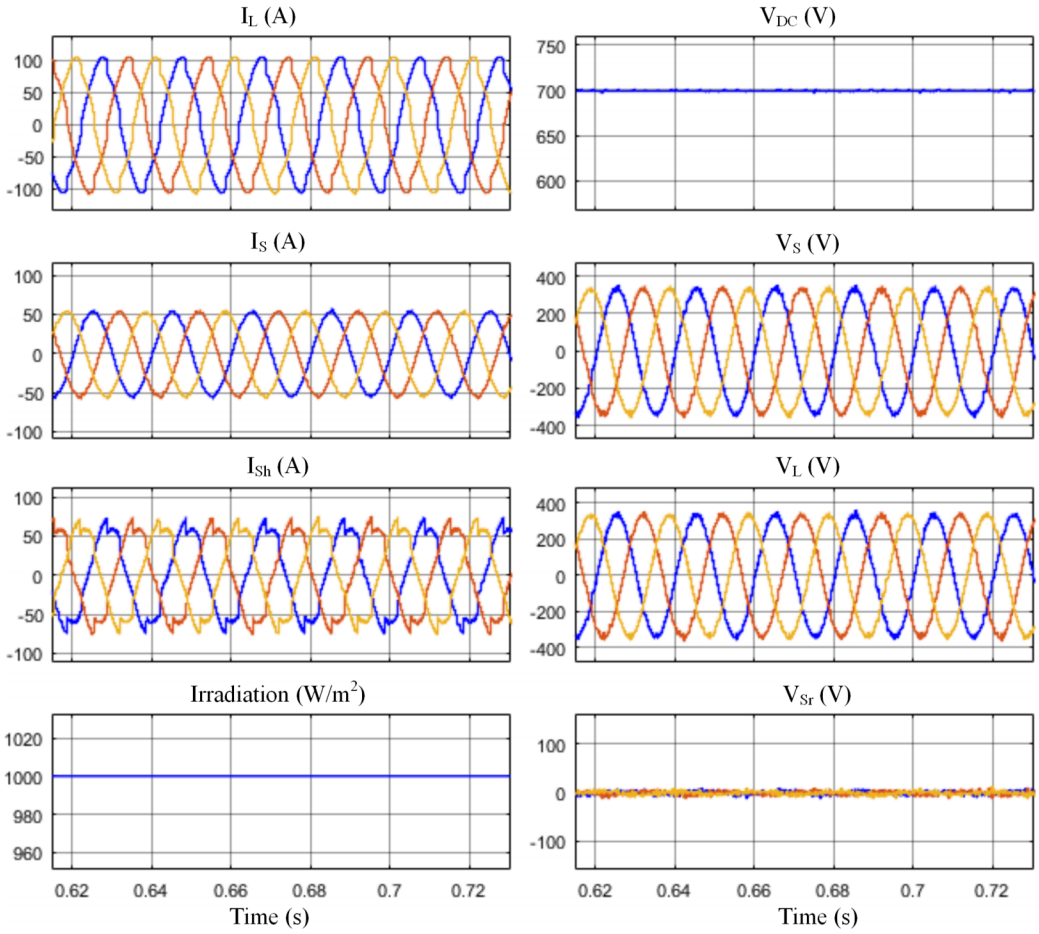

Figure 3.7: MATLAB Simulation results for steady state

(in UPQC-P control strategy). Harmonic analysis results of source and load currents are shown in Fig. 3.12. THD of load current is 9.59% and that of source current is 2.09%. Fundamental components in Fig. 3.12, marked with red top, are not fully shown for enabling relative view of low magnitude, higher order frequency terms. Solar irradiation is kept as 1000 W/m^2 in steady state and PV array supplies its rated power output.

Solar irradiation is changed from 1000 W/m^2 to 600 W/m^2 linearly at 0.85 s and results are shown in Fig. 3.8. As solar irradiation reduces, grid current increases to keep supplying the constant load power but maintains its THD value well within limit of 5% imposed by IEEE Standard 519. DC link voltage is also maintained at its reference value (700 V) during variation in solar irradiation.

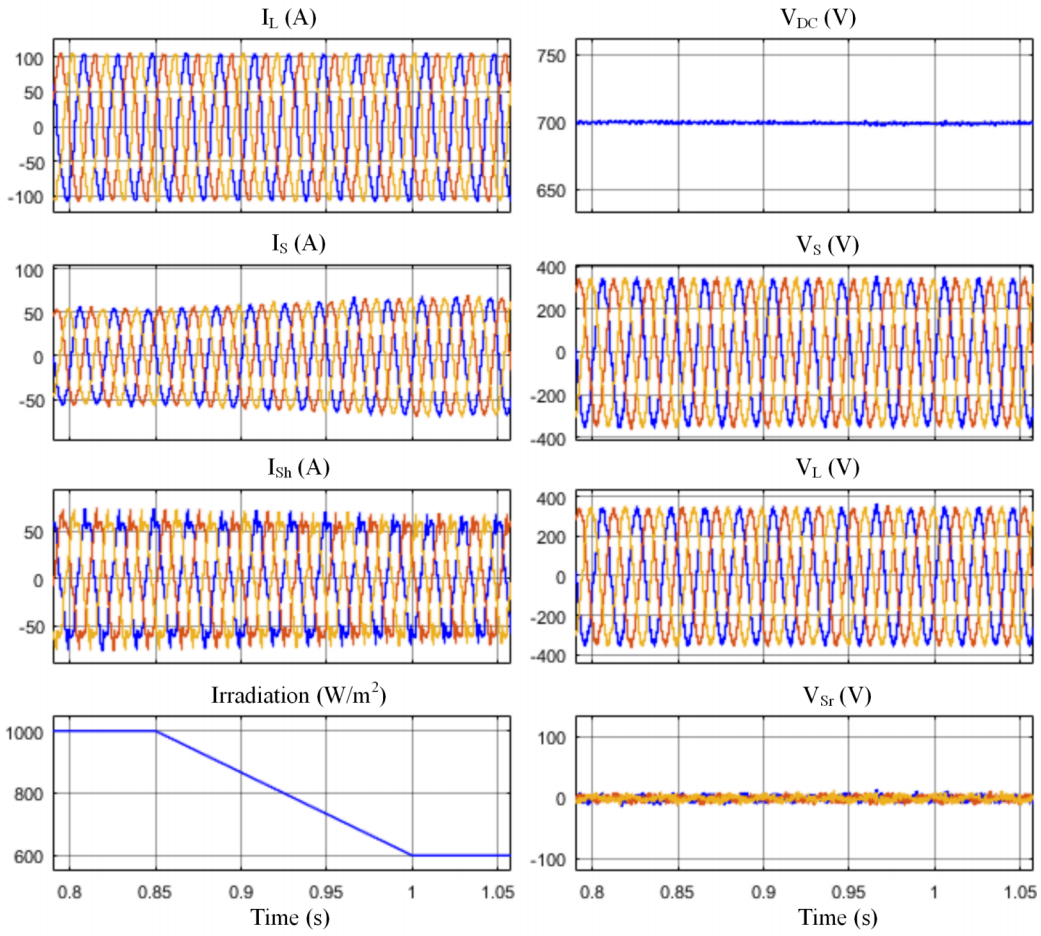

Figure 3.8: MATLAB Simulation results during variation in solar irradiation

Performance of UPQC-DG is tested during voltage sag, which occurs at 1.1 s for duration of 0.1 s. During this sag, voltage at load terminals is maintained constant (Fig. 3.9) through injection of difference voltage by series APF. Source current increases to supply same amount of load power at reduced voltage. On occurrence of sag, DC ling voltage experiences undershoot of 20.5 V (3% of steady state value) but settles to 700 V within 0.08 s. In conventional UPQC series APF injects real power and thus DC link voltage falls down, large amount and duration of voltage sag can cause considerable decrease in DC link voltage. In case of UPQC-DG such a risk is eliminated since PV power is fed to DC link acts as feed-forward control.

Performance during distortion in source voltage and swell is shown in Fig. 3.10.

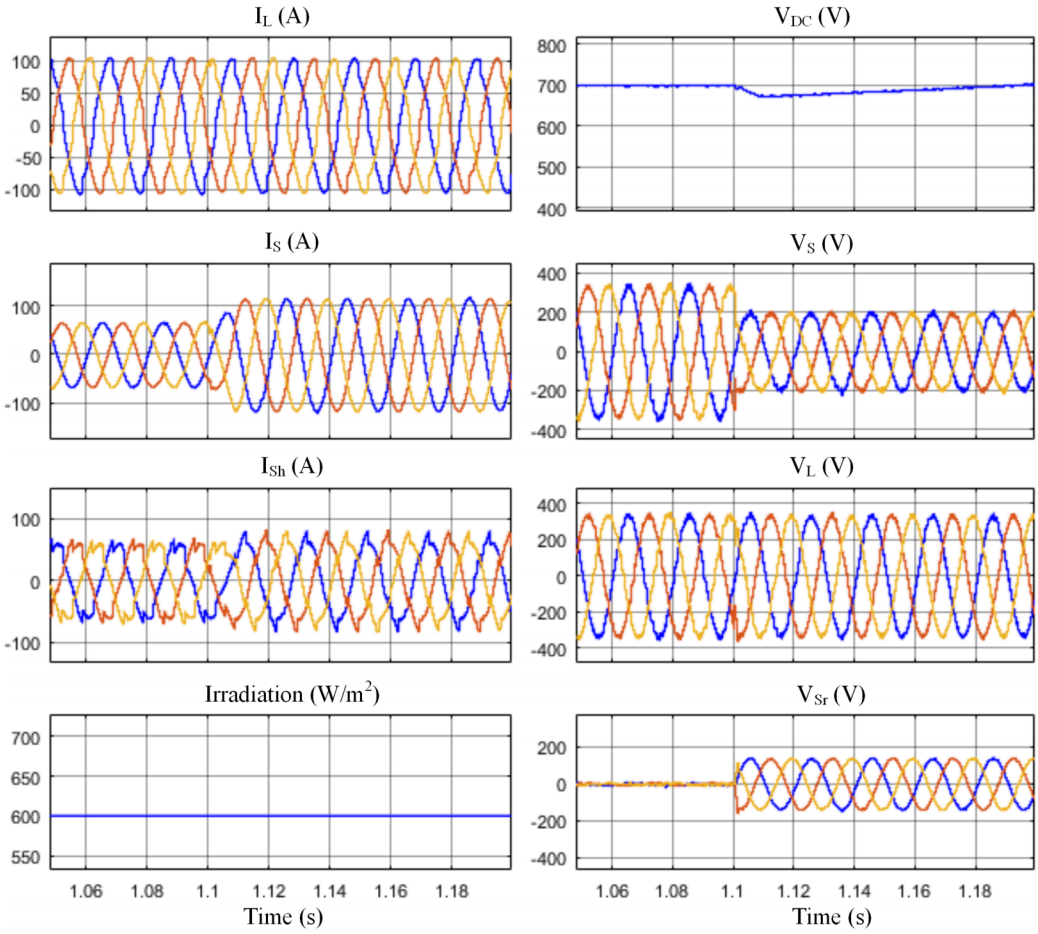

Figure 3.9: Matlab Simulation results during voltage sag

During distorted grid voltage, load terminal voltage is maintained free from distortion. Harmonic spectrum of source and load voltages is shown in Fig 3.13. THD of source voltage is 7.55% and THD of load voltage is maintained within 2.1%. During swell, load voltage is held constant. At the moment of voltage swell, DC link experiences a small overshoot of 1.7% but settles to steady state within 0.02 s.

These results also verify fault ride through operation of solar PV connected using UPQC-DG. Without UPQC-DG, solar PV connected through normal inverter requires ideal supply voltage at inverter terminal and any variation is supply voltage leads to disconnection of solar PV from grid. But here solar PV remains connected and continues to supply power to load and grid during such variations in supply voltage as sag and swell of predetermined magnitude.

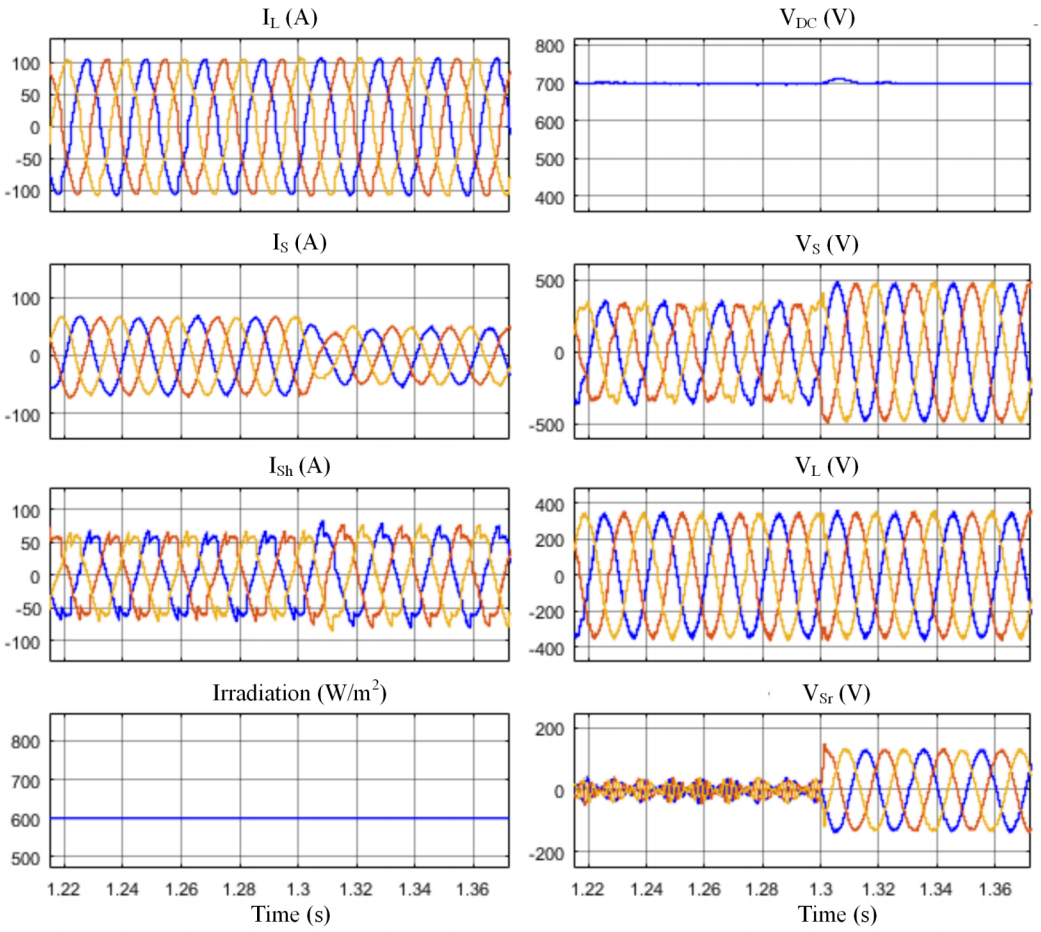

Figure 3.10: Matlab Simulation results for voltage distortion and swell

A linear load (load-3) is disconnected at 1.7 s, making total load a mixture of non-linear and linear complex load. As shown in Fig. 3.11, current from grid reduces when load-2 is switched off because power demand of load reduces. Shunt current decreases since reactive power demand of load also reduces. DC voltage experience slight fluctuations but settles to steady state. Load and source voltages are not affected by change in load.

3.4 Summary

UPQC-DG is designed based on load data, compensation requirements of series and shunt APFs and power output of PV. Design methodology is based on mathematical

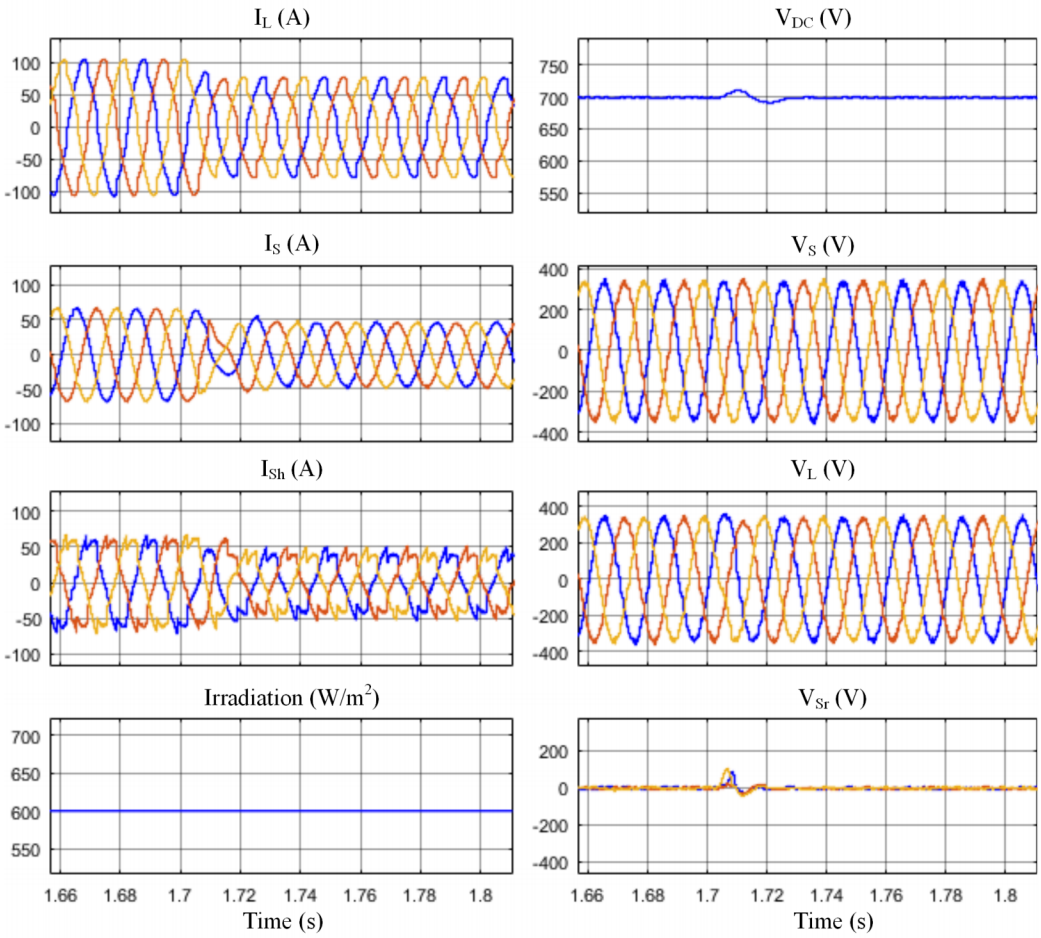

Figure 3.11: Simulation results during change in load

and empirical techniques proposed in existing literature of UPQC. UPQC design focuses on selection of values of circuit parameters like inductance, filter capacitor and resistance. Design of UPQC-DG is presented for a case study system and the system thus designed is simulated in MATLAB/Simulink using conventional control strategy, in which series APF compensates only for transient grid disturbances, and not for load reactive power. Simulation studies are carried out for steady state as well as transient performance and the results have been found as desired. In further chapters, power angle control is introduced which incorporates power sharing between series and shunt APFs of UPQC-DG.

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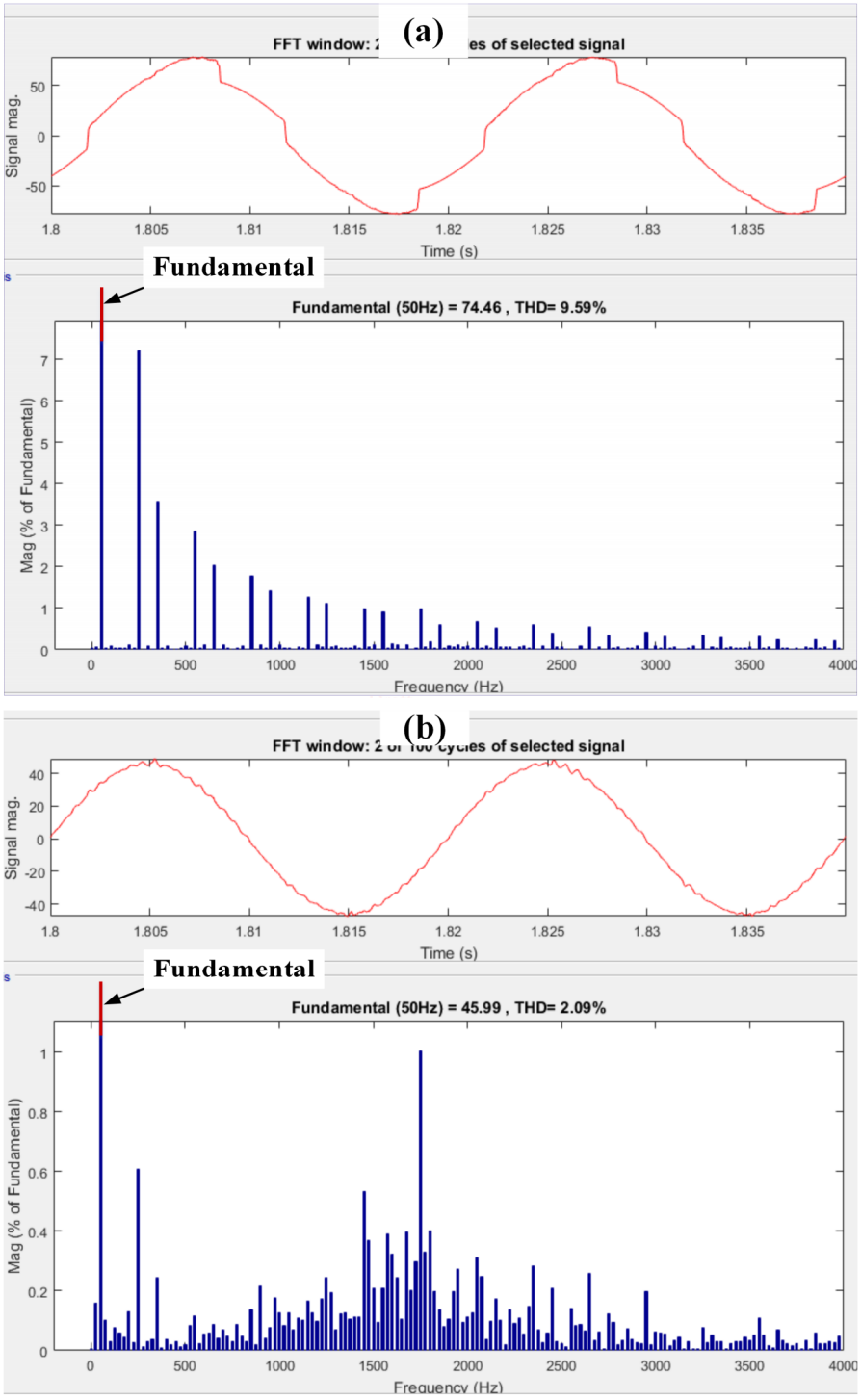

Figure 3.12: FFT analysis of (a) load current and (b) source current

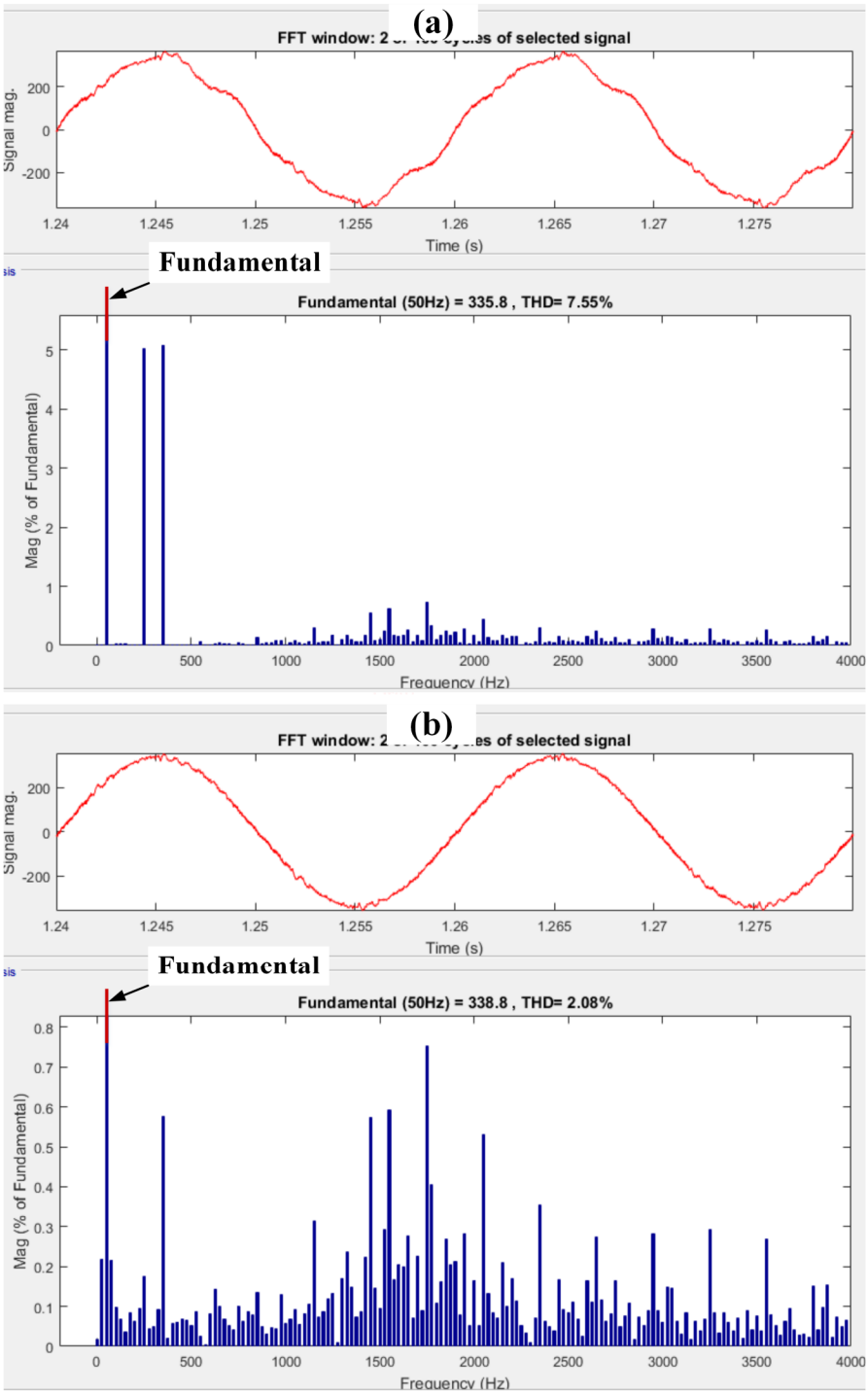

Figure 3.13: FFT analysis of (a) source voltage and (b) load voltage